AN7291SC, AN7291FBP

FM—IF, Detection, Noise Canceller, MPX Demodulation IC

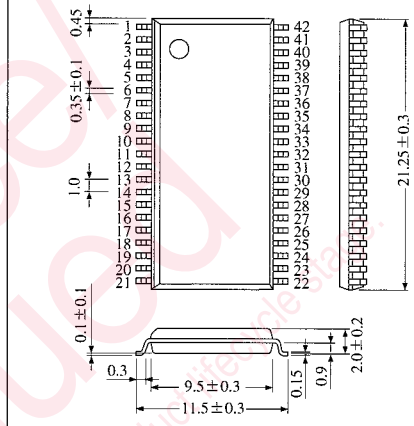
■ Overview

The AN7291SC, AN7291FBP are IC integrated FM—IF/Det., PNL, MPX into a single chip. PNL, MPX is basicaly the same confi guration as previous AN7465S, but VCO is adjustment-free by using ceramic lock.

■ Features

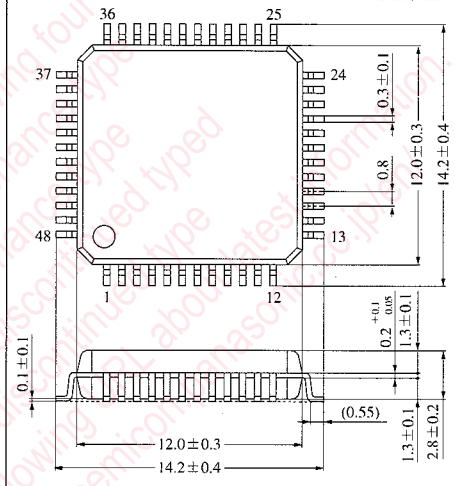
- Integration previous 2-chip (IF/Det., PNL/MPX) into a single chip
- High IF sensitivity
- With IF counter output, SEEK sensitivity adjustment
- Adjustment-free VCO (ceramic lock 912kHz)
- Fewer external parts (Fewer large capacitance capacitor)
- Good control voltage linearity, wide adjusting range
- Multipath detection amp. built-in

AN7291SC Unit : mm



42-Lead SOP Package (SSOP042-P-0450)

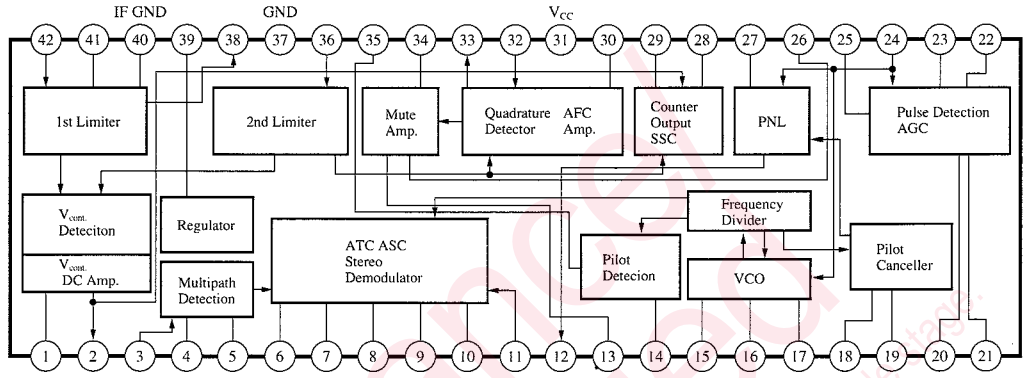
AN7291FBP Unit : mm



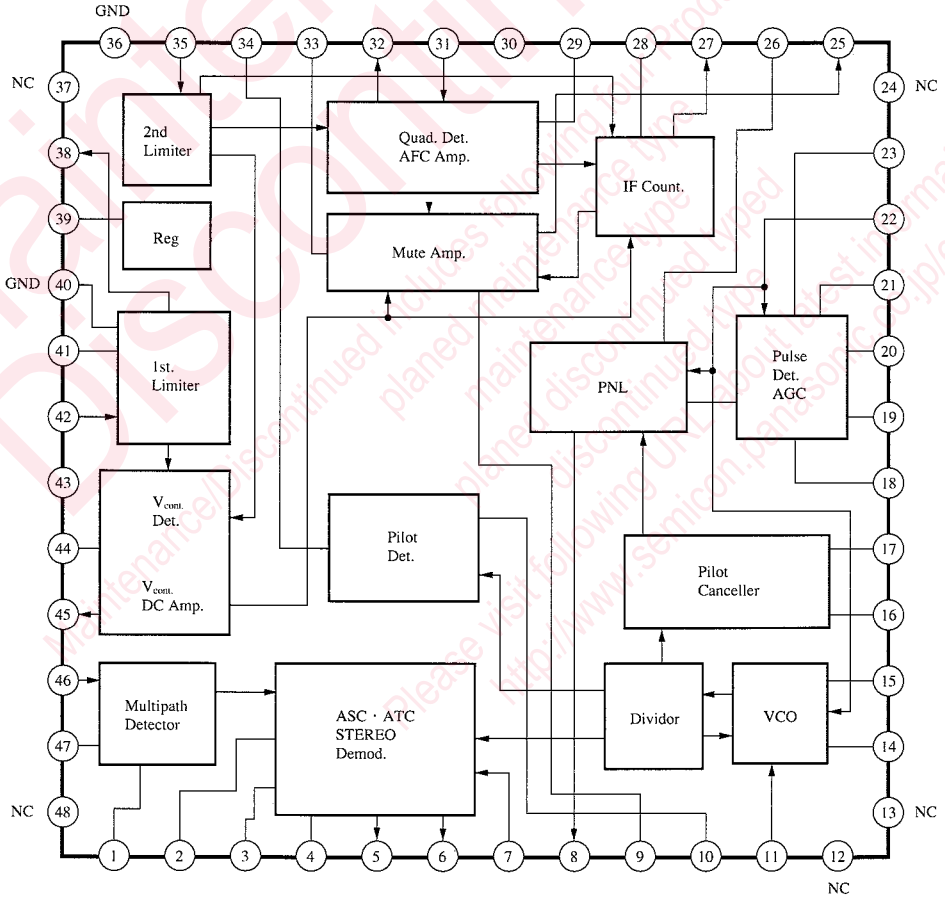
48-Lead QFH Package (QFH048-P-1212)

Block Diagram

AN7291SC



AN7291FBP



■ Absolute Maximum Ratings (Ta=25℃)

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	9.6	V
Supply Current	I_{CC}	43	mA
Power Dissipation (Ta=75℃)	P_D	787 Note1)/670 Note2)	mW
Operating Ambient Temperature	T_{opr}	−30～+80	℃
Storage Temperature	T_{stg}	−55～+125	℃

Note 1) AN7291SC Note 2) AN7291FBP

■ Recommended Operating Range (Ta=25℃)

Parameter	Symbol	Range
Operating Supply Voltage Range	V_{CC}	7.2V～9.6V

∗ The AN7291SC pin numbers are used below. For the AN7291FBP, refer to Pin No. Correspondence Table.

■ Electrical Characteristics (V_{CC}=8V, f_{in}=10.7MHz, $f_{Mod.}$=1kHz 30%FM, Ta=25℃)

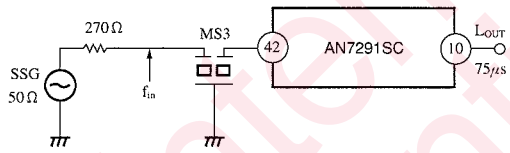
Parameter	Symbol	Condition	min.	typ.	max.	Unit
Control Voltage (1)	V_{C1}	No input Pin②DC voltage	0.1	0.5	0.9	V
Control Voltage (2)	V_{C2}	V_{in}=40dBμ, Pin②DC voltage	1.25	1.55	1.85	V
Control Voltage (3)	V_{C3}	V_{in}=70dBμ, Pin②DC voltage	2.8	3.3	3.8	V
Control Voltage (4)	V_{C4}	V_{in}=100dBμ, Pin②DC voltage	4.5	5.15	5.7	V
Control Voltage (5)	V_{C5}	$V_{C5}=V_{C3}-V_{C2}$	1.5	1.7	1.9	V
Control Voltage (6)	V_{C6}	$V_{C6}=V_{C4}-V_{C3}$	1.6	1.8	2	V
AFC Offset Voltage	V_{AFC}	No signal input DC voltage between Pin㉚ and ㊴	−0.2	0	0.2	V
Output Level L	V_{OL}	V_{in}=70dBμ, Pin⑩AC voltage	125	145	165	mVrms
Output Level R	V_{OR}	V_{in}=70dBμ, Pin⑨AC voltage	125	145	165	mVrms
Channel Balance	CB	CB=20log (V_{OL}/V_{OR})	−1	0	1	dB
Limiting Sensitivity	V_{lim}	V_{OL}= 0dB, Input Pin⑩AC voltage decreases by 3dB	21	24	27	dBμV
Residual Pilot Voltage	V_{PC}	V_{in}=70dBμ pilot signal 10% modulation Pin⑫AC voltage	—	7	14	mVrms
Stereo Lamp ON Level	$Lamp_{(ON)}$	Modulation only by pilot signal. Pin㉟ DC voltage=less than 2V	2.6	4.7	6.3	%
Stereo Lamp OFF Level	$Lamp_{(OFF)}$	Modulation only by pilot signal. Stereo lamp ON/OFF level ratio	2	4.5	7	dB
Separation Lch	Sep. L	V_{in}=70dBμ, L+R=90% Pilot 10%	22	35	—	dB
Separation Rch	Sep. R	V_{in}=70dBμ, L+R=90% Pilot 10%	22	35	—	dB
Capture Range	CR	V_{in}=70dBμ , pilot signal 8% modulation	+0.6 −0.45	±1	—	%
Counter Output Level (1)	V_{IF1}	V_{in}=70dBμ, Pin㉙=0V, Pin㉘10.7MHz output voltage	0	1	10	mVrms
Counter Output Level (2)	V_{IF2}	V_{in}=70dBμ, Pin㉙=V_{CC}, Pin㉘AC output voltage	80	100	120	mVrms
Supply Current	I_{tot}	No input, Pin⑮=0V	28	35	40	mA
Monaural THD (Lch)	THDL	Monaural input 400mV, 1kHz Lch distortion rate	—	0.15	0.3	%
Monaural THD (Rch)	THDR	Monaural input 400mV, 1kHz Rch distortion rate	—	0.15	0.3	%

Electrical Characteristics (Cont.) (V_{CC}=8V, f_{in}=10.7MHz, $f_{Mod.}$=1kHz 30%FM, Ta=25℃)

Parameter	Symbol	Condition	min.	typ.	max.	Unit
Stereo THD (Lch)	THD SL	Stereo, L+R=360mV, V_P=40mV, Lch distortion rate	—	0.15	0.3	%
Stereo THD (Rch)	THD SR	Stereo, L+R=360mV, V_P=40mV, Rch distortion rate	—	0.15	0.3	%
AGC Voltage (1)	V_{AGC1}	Input=0mVrms, R_S=600Ω, Pin㉓DC voltage	—	0	0.4	V
AGC Voltage (2)	V_{AGC2}	Input V_{in2}=2mVrms, 150kHz, Pin㉓DC voltage	1.3	1.48	1.65	V
Noise Detection Voltage	$V_{Det.}$	V_{in2}=100mVrms, 150kHz, Pin㉒DC voltage	—	0	0.3	V
Gate Pulse Width	PW	V_{in2}=0.3V_{P-P}, tw=1μs f=1kHz, Pin⑫ output	19	24	29	μs
Residual Noise Voltage	V_{NR}	V_{in2}=1V_{P-P}, tw=10μs, f=1kHz, Input through LPF. Lch output	—	0	0.7	mVrms

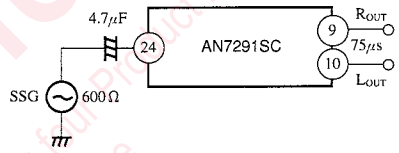
Characteristics Curve

①Measuring Condition at IF Input



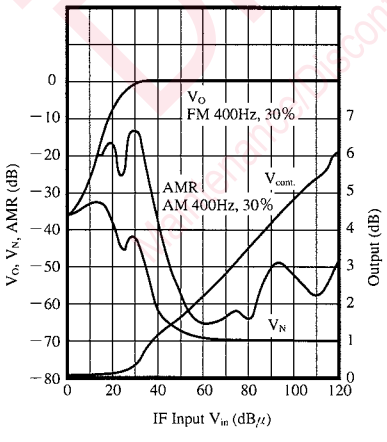
Unless otherwise specified, V_{CC}=8V, f_{in}=10.7MHz
FM Modulation 30%, 400Hz,
V_{in}=70dBμ

②Measuring Condition at NC Input

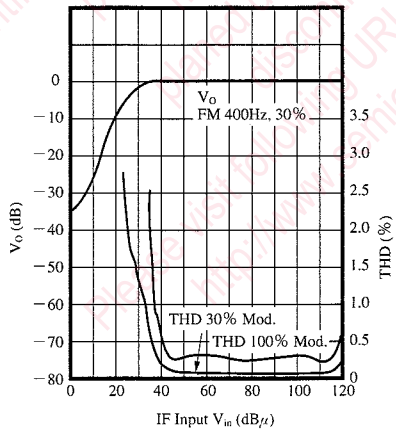


Unless otherwise specified, V_{CC}=8V, f_{in}=1kHz,
V_{in}=400mV (Monaural)
L+R=360mV (Stereo)
V_P=40mV (Stereo)

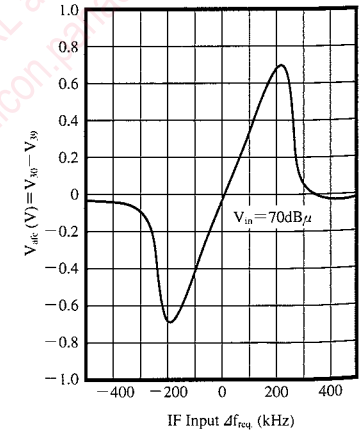
V_O, V_N, AMR, $V_{cont.}$—V_{in}



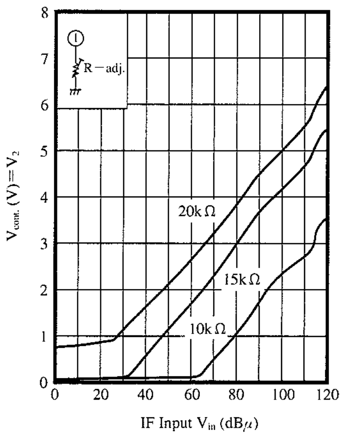
V_O, THD—V_{in}



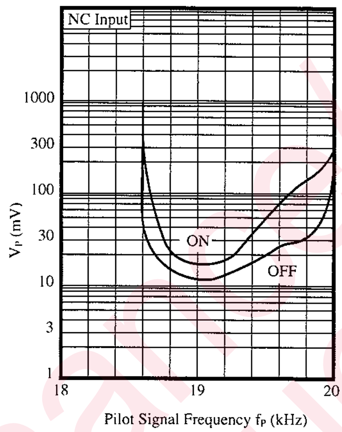
V_{afc}—$\Delta f_{req.}$



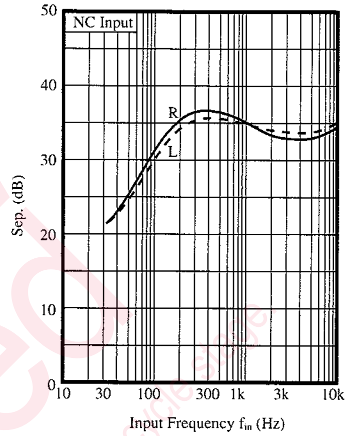
Control Voltage
Control Example



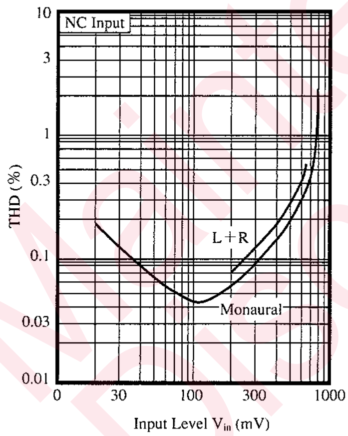
Lamp ON/OFF—f_P



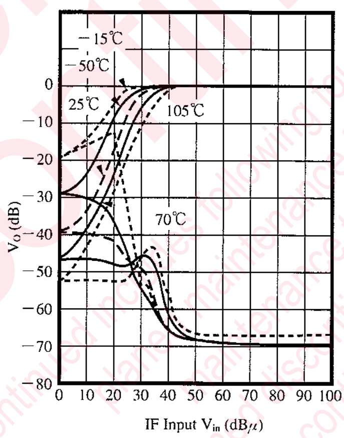
Sep.—f_{in}



THD—V_{in}

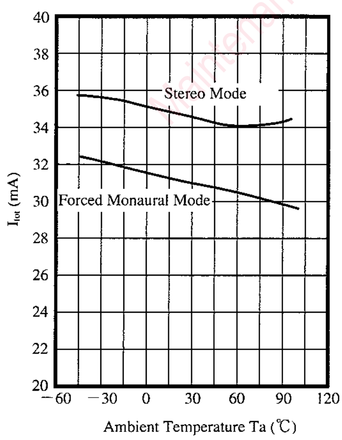


Input/Output Characteristics

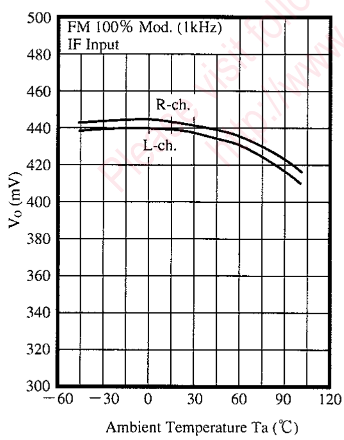


ICs for Tuner

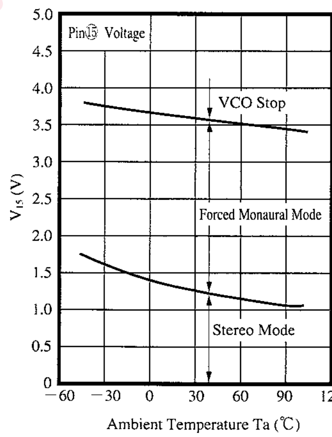
I_{tot}— Ta



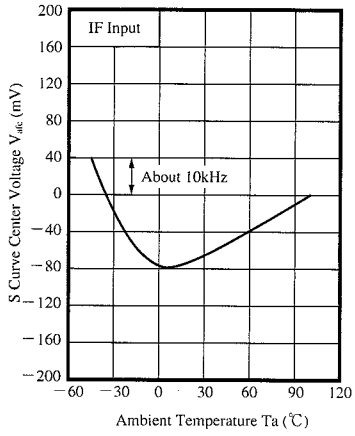
V_O— Ta



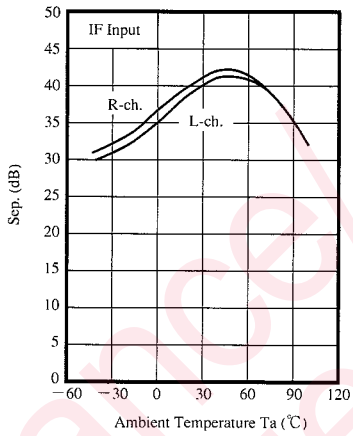
Forced Monaural
Operation Voltage—Ta



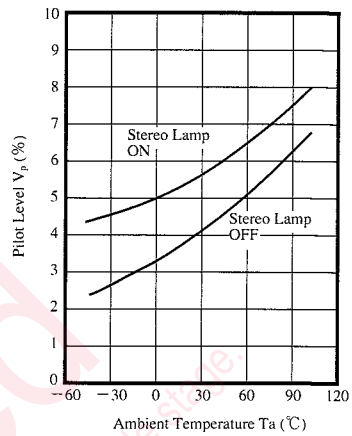
V_{afc}—Ta



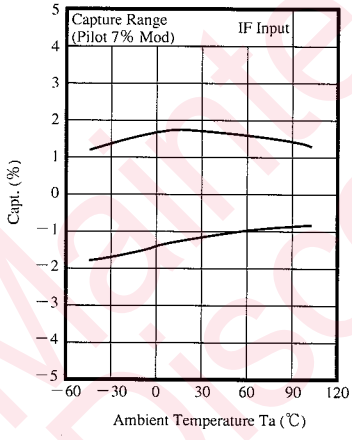
Sep.—Ta



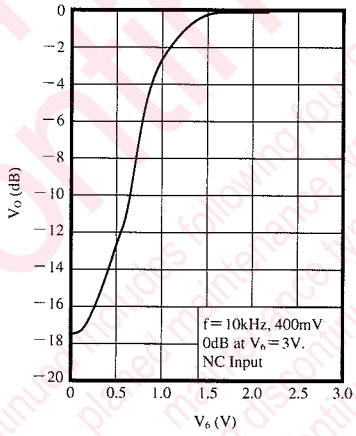
Stereo Lamp ON/OFF—Ta



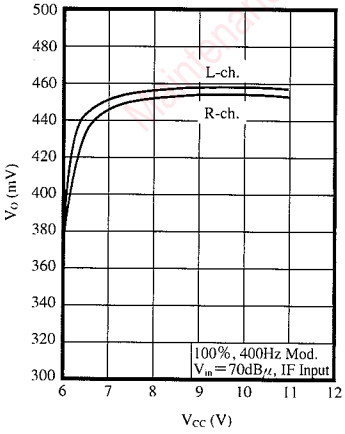
Capt.—Ta



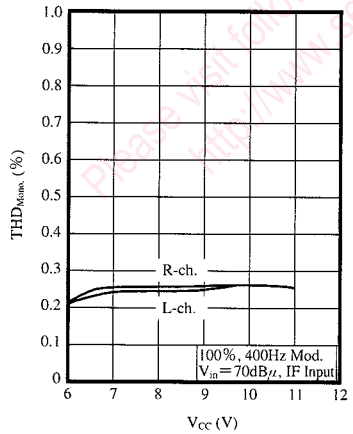
ATC Characteristics



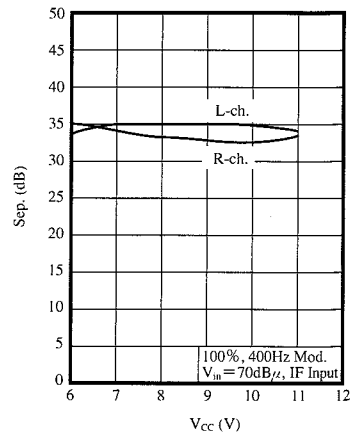
V_O—V_{CC}



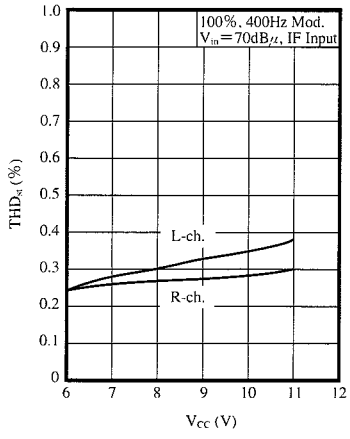
$THD_{Mono.}$—V_{CC}



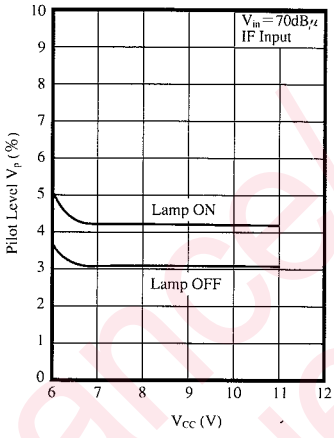
Sep.—V_{CC}



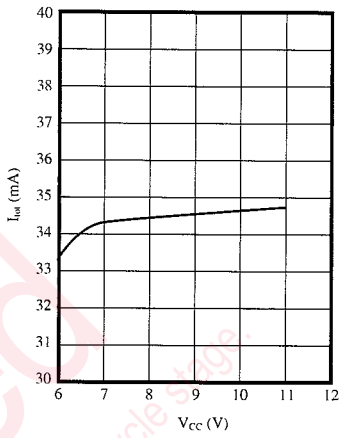
THD$_{st}$—V$_{CC}$



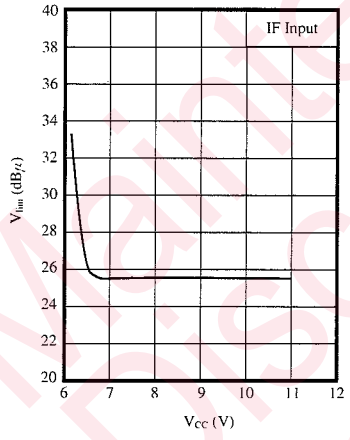
Pilot ON/OFF—V$_{CC}$



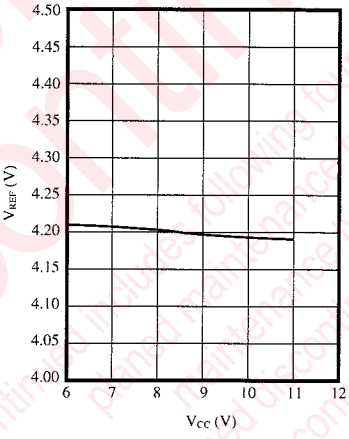
I$_{tot}$—V$_{CC}$



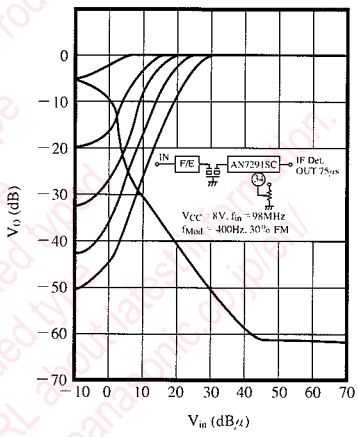
V$_{lim}$—V$_{CC}$



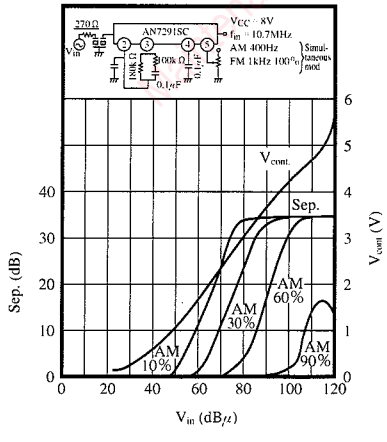
V$_{REF}$—V$_{CC}$



Soft Mute Example V$_O$—V$_{in}$

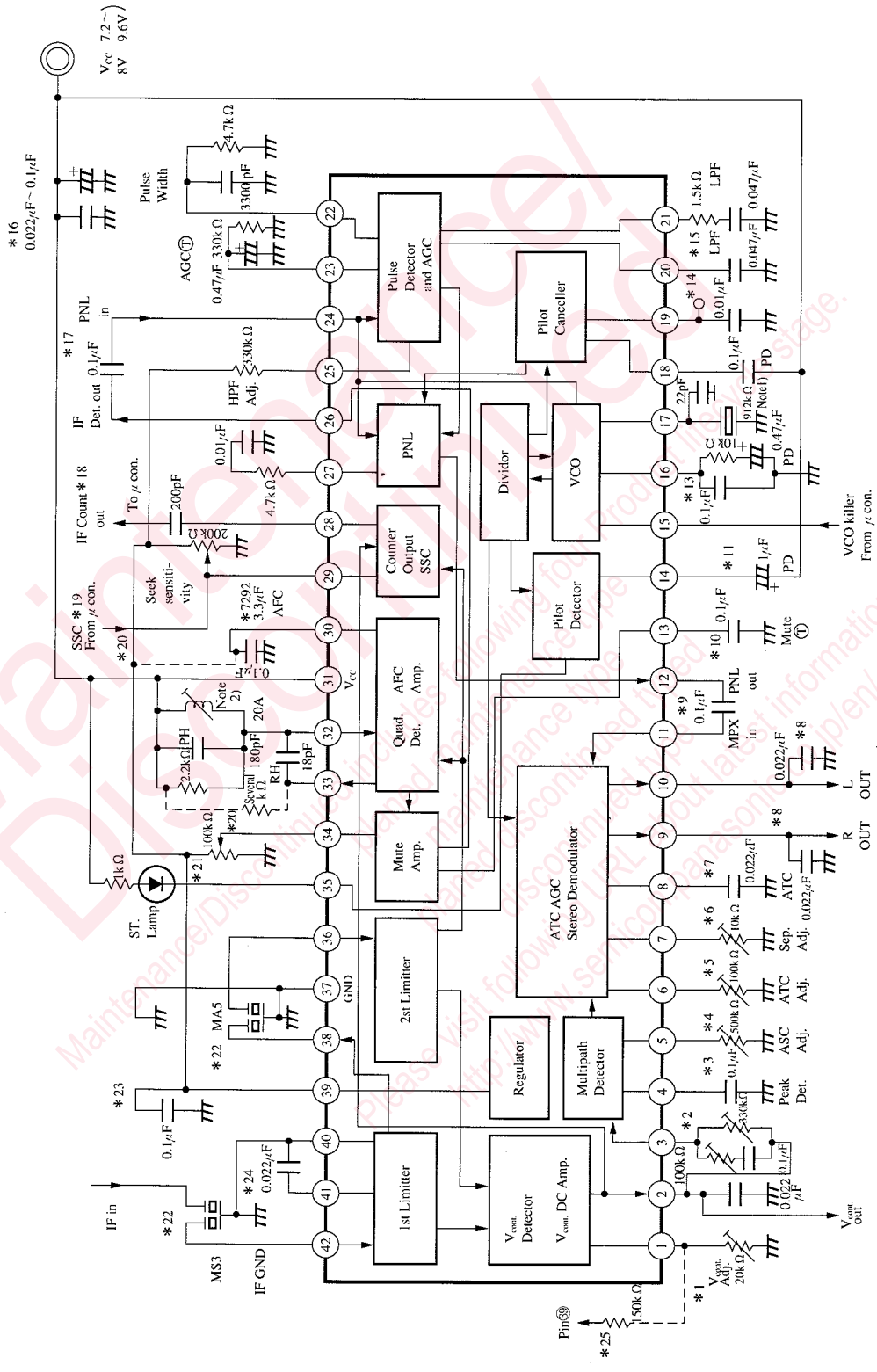


Sep. V$_{cont.}$—V$_{in}$



ICs for Tuner

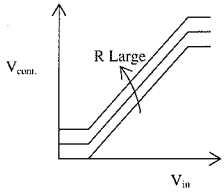
■ Application Circuit (Example of AN7291SC)



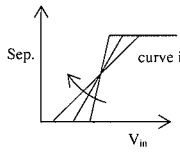
Note1) Ceramic lock CSB912JF101 (by Murata Manufacturing Co., Ltd.), Note2) IFT ZIF−5EB020A (by Matsushita)

■ Description on Pins Shown in Application Circuit Diagram

＊1
Control voltage adj.

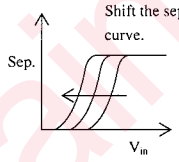


＊2

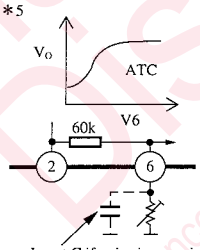


＊3 At multipath detection
Capacitor for
Detection : up to 1μF

＊4



＊5



Insert C if noise is conspicuous.

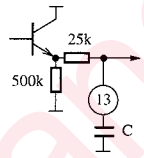
＊6 Adjust the separation max. value.

＊7 Capacitor of 0.01 to 0.022μF
for determining ATCF time

＊8 0.022μ is C. for de-emphasis.
Inside 3.3kΩ

＊9 Pin⑪ input impedance is 400kΩ.
At 0.1μF, high frequency band Sep.
is lowered, but can be used.
The larger the better. 0.1μ is min.

＊10 Vary the soft mute time constant.

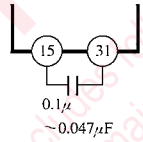


Voltage : Strong Weak
$\tau_1 = 25k \times C$
Weak Strong
$\tau_2 = 525k \times C$

＊11 Pilot Detection
Phase Detection Filter
Small···Lamp malfunction due to noise
Large···Lamp ON speed high

＊12 VCO stop $3.9 < V_{15} < V_{CC}$
Forced monaural $1.7 < V_{15} < 3.2$
Stereo mode $0 < V_{15} < 1.0$

・When Pin⑮ is not used, preferably
insert C between V_{CC}.



＊13 VOC For phase detection
Lag lead filter

＊14 For pilot canceller Pseudo sine wave
output : Capacitance = 0.0068μ ~0.015μ

＊15 PNL noise amp. Path control

＊16 (Put it at the possible nearest position to IC pin.)

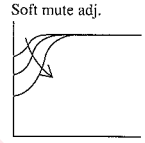
＊17 Pin㉔ input impedance is 500kΩ.
0.1μF is min. value.
The larger the better.

＊18 IF counter output Take care for routing.
(Keep it away from input)

＊19 SSC
V29 > 1V··· Counter OUT
V29 ≈ 0V···IF counter OFF

＊20 THD improved

＊21
Soft mute adj.



＊22 For domestic use, vary the
frequency band according
to applications.

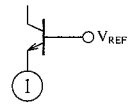
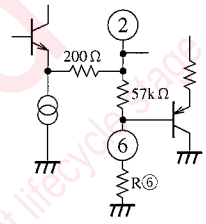
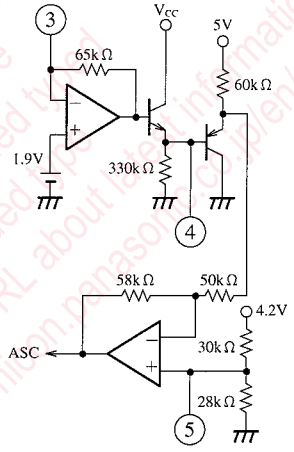
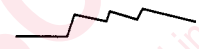
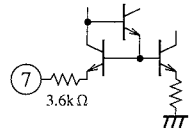
＊23 Regulator by-passTake
care for GND location.

＊24 1st limiter path control

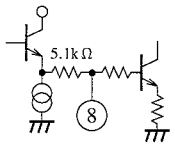
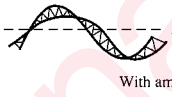
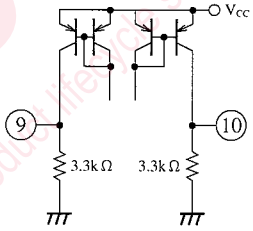
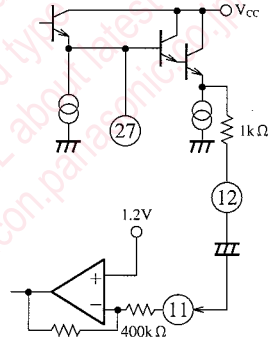
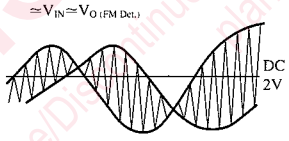
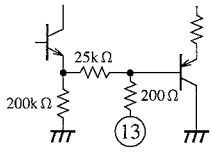
＊25 S-meter in hot condition improved

ICs for Tuner

■ Pin Descriptions (Example of AN7291SC)

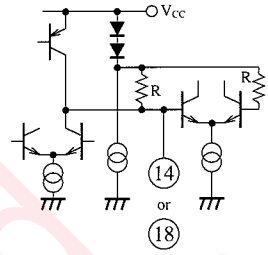
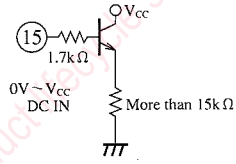
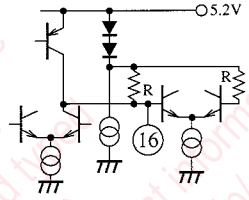
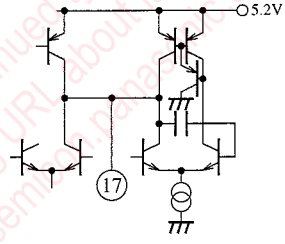
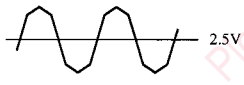
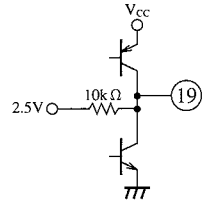
Pin No.	Pin Name	Pin Waveform, Voltage	I/O Impedance	Equivalent Circuit
1	$V_{CONT.}$ Adj.	DC≃3.5V	Low	
2	$V_{CONT.}$ OUT (Level Meter)		200Ω	
6	ATC Adj.	$V_{⑥} = \frac{R_{⑥}}{57k\Omega + R_{⑥}} V_{②}$	57kΩ	
3	AMDC IN	DC about 1.9V	Low	
4	AMDC Peak Det.		Rise Low Fall 330kΩ	
5	AMDC Adj.	DC about 2.3V	14.5kΩ	
	Note) AMDC: Automatic Multi Path Distortion Canceller			
7	Separation Adj.	DC (max.) ≃1.2V AC=0~$V_{⑪}$	2kΩ	

■ Pin Descriptions (Example of AN7291SC) (Cont.)

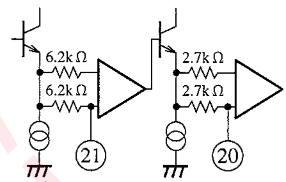
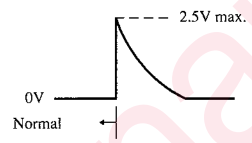
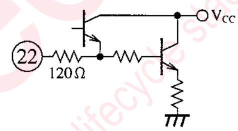
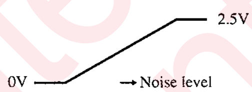
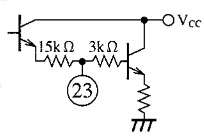
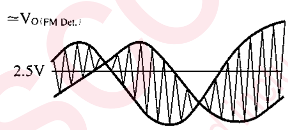
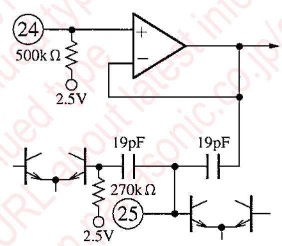
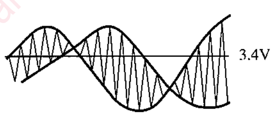
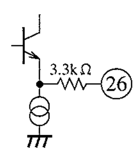
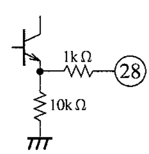
Pin No.	Pin Name	Pin Waveform, Voltage	I/O Impedance	Equivalent Circuit
8	ATC L. P. F	Same as V⑪, level higher than external capacitor down.	5.1kΩ	
9	L-ch. OUT	AC varies with input condition.  With amplitude	3.3kΩ	
10	R-ch. OUT	AC varies with input condition.  With amplitude	3.3kΩ	
11	MPX. IN	AC=Same as Pin⑫. DC=1.3V	400kΩ	
12	NC. OUT		1kΩ	
27	NC. Hold	V(AC)≃V⑫ V(DC)≃3.3V	1.5kΩ	
13	Soft Mute Time Const.	DC≃0V～4.1V	25kΩ	

ICs for Tuner

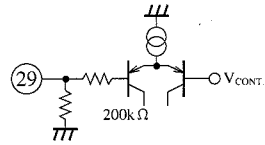
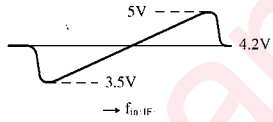
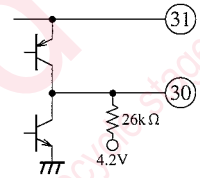
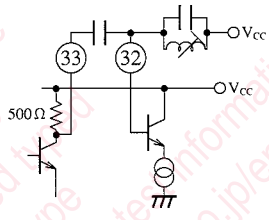
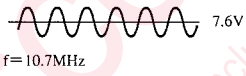
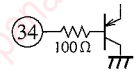
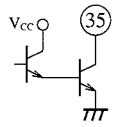
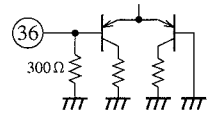
■ Pin Descriptions (Example of AN7291SC) (Cont.)

Pin No.	Pin Name	Pin Waveform, Voltage	I/O Impedance	Equivalent Circuit
14	Pilot Det. L. P. F	DC≃V_{CC}−1.4V	R=36kΩ	
18	Pi. Can. Control L. P. F	DC≃V_{CC}−1.4V	R=68kΩ	
15	ST/Mono. Control	Pin Voltage / Demo-dulation / LED / Pilot Can. / VCO 0V~1V: ○ ○ ○ ○ 1.7V~3.2V: × × ○ ○ 3.9V~V_{CC}: × × × ×	High	
16	PLL L. P. F	DC≃4.3V	R=66kΩ	
17	VCO (Ceramic Lock Pin)	 f=912kHz AC≃3V_{P-P}	High	
19	Pi. Can. Quasi−sin	 f=19kHz AC≃100mV_{P-P}	—	

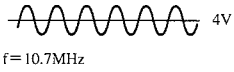
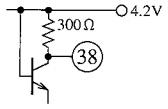
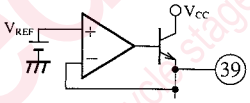
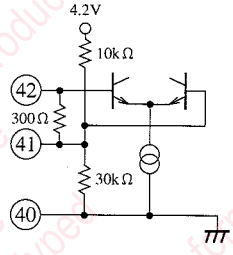
Pin Descriptions (Example of AN7291SC) (Cont.)

Pin No.	Pin Name	Pin Waveform, Voltage	I/O Impedance	Equivalent Circuit
20	AGC Amp. L. P. F	DC≃3.5V AC is noise	6.2kΩ	
21	Pulse Amp. L. P. F	DC≃4.2V AC is noise	2.7kΩ	
22	Gate Time Adj.		Usually High Low at Operation	
23	Noise Amp. AGC		Rise 15kΩ Fall High	
24	NC IN		500kΩ	
25	NC H. P. F	Level lower than Pin㉔ waveform down. DC is determined by external voltage (4.2V).	High	
26	IF Det. OUT	 (Vary with input condition)	3.3kΩ	
28	IF Count Out	DC≃4V AC≃80mVrms (Nomal AC is OFF)	1kΩ	

■ Pin Descriptions (Example of AN7291SC) (Cont.)

Pin No.	Pin Name	Pin Waveform, Voltage	I/O Impedance	Equivalent Circuit
29	SCC [Seek Sence. Adj.]	Apply bias voltage from outside.	200kΩ	
30	AFC OUT		26kΩ	
31	V_{CC}	8V	Low	———
32	Quad. IN	DC=8V (Determined by outside.) <90° phase shift	High	
33	Limitter OUT		500Ω	
34	Soft Mute Adj.	Voltage input from outside 0V~V_{REF} (4.2V)	High	
35	LED Driver	At stereo DC=0V~0.5V	Low	
		At monaural Determined by external voltage.	High	
36	2nd IF IN	≃0V	300Ω	

■ Pin Descriptions (Example of AN7291SC) (Cont.)

Pin No.	Pin Name	Pin Waveform, Voltage	I/O Impedance	Equivalent Circuit
37	System GND	0V	Low	———
38	IF1 Limitter OUT	 4V f=10.7MHz	300Ω	
39	V_{REF}	4.2V constant voltage	Low	
40	IF GND	———	Low	
41	IF Amp. Bypass	DC=3.1V	7.5kΩ	
42	IF IN	DC=3.1V AC=$V_{in\ (IF)}$	300Ω	

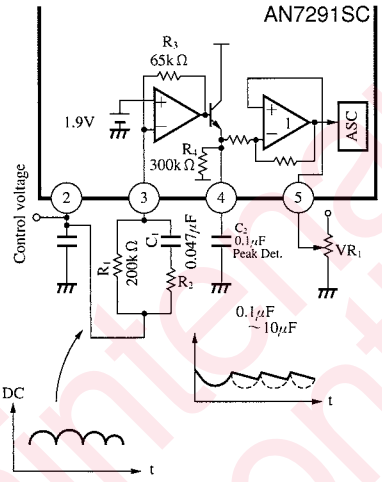
■ Supplementary Explanation

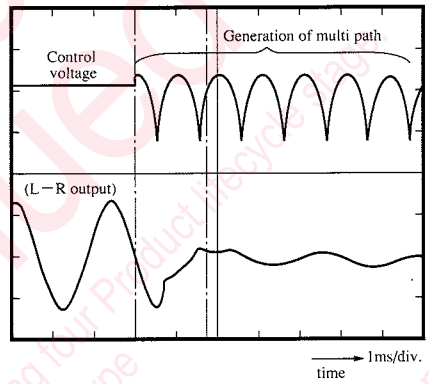
(1) On Multi path Distortion Preventive Circuit (AN7291SC pin numbers are used in the following explanation.)

1. Principle

Multi path distortion is apt to increase especially in the stereo receiving mode. In consideration of this phenomenon, the AN7291SC has been designed so as to suppress the feeling of physical disorder incidental to multi path noise by degrading the separation against multi path distortion.

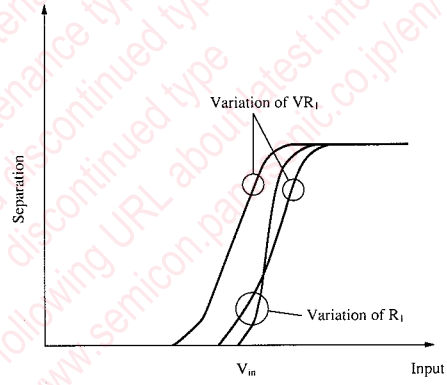
Detection method···Detection of AM components included in control voltage (level meter) output
Separation control···Operation of conventional ASC circuit by conversion of detected AM components into DC voltage





(1) Operation in a state free from multi path (Operation as ASC)

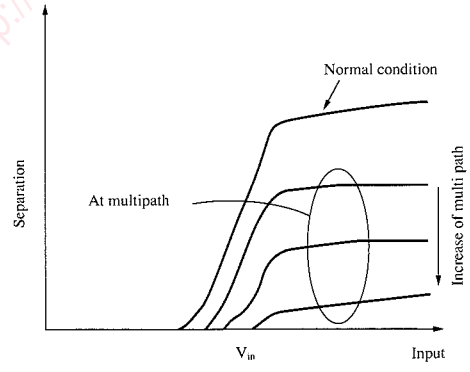
The control voltage of ② is sent to the ASC through the two operational amplifiers. The gradient of the characteristics curve can be set by R_3/R_1, and the start point can be set by VR_1.



(2) Operation in a state exposed to multi path

The variation to appear in the control voltage on account of multi path distortion is put to AM detection, and the DC voltage to the ASC is suitably lowered to degrade the separation.

The frequency characteristics of the AM components are adjusted through C_1 shown in the sketch, and the AM components are put to peak value detection by R_4 and C_2.

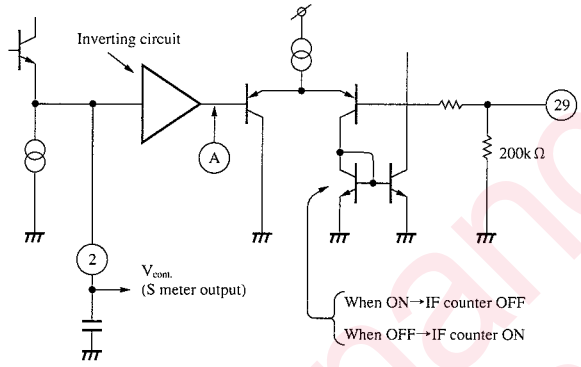


(2) On SSC Pin (AN7291SC pin numbers are used in the following explanation.)

1. What is SSC?

SSC is the acronym of Search Stop Clear, and it usually denotes the search stop clear control. In AN7291SC, the IF count output is obtained on the SSC pin only in the search mode.

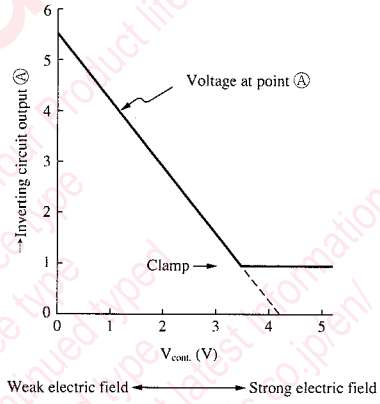
2. Internal Equivalent Circuit of SSC Pin㉙



3. Operational Description

The inverting circuit has the gain of about 1.3 times, and its input-output characteristics changes as shown in the right sketch. (Calculated values)

This inverting circuit generates the IF count output only when the voltage at point Ⓐ is lower than the set voltage of Pin㉙.



[3] Selection Standard of Noise Canceler Resistance Value (AN7291SC pin numbers are used in the following explanation.)

AN7291SC

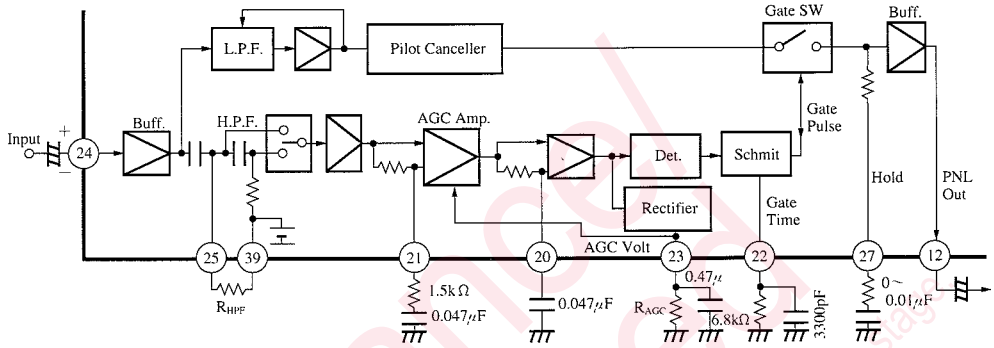


Fig.1 Pulse Noise Limiter (PNL) Block Diagram

(1) Relation to field strength

1. In weak electric field

In a weak electric field where noise is apt to increase, the AGC effectively controls the PNL operation.

a) In case operation error is frequently caused by white noise, Suitably increase the value of Pin㉓ R_{AGC} (220kΩ to 1MΩ).

b) In case operation error is frequently caused by overmodulation. Suitably increase the value of R_{HPF} between Pin㉕ and Pin㊴ (47kΩ to 470kΩ).

2. In medium to strong electric field

In a medium to strong electric field relatively free from noise generation, the AGC becomes less effective and noise is detected almost at the maximum sensitivity.

a) In case the detection sensitivity is too high, suitably decrease the value of R_{HPF} between Pin㉕ and Pin㊴ (10kΩ to 47kΩ)

3. In every electric field

a) In case the detection sensitivity is excellent but the PNL effect deteriorated due to holding level fluctuation by noise, suitably increase the resistance value of the resistor connected in series with the Pin㉗ holding capacitor (10kΩ to 4.7kΩ).

b) In case the noise of the gate pulse itself is conspicuous, suitably narrow the gate pulse width by decreasing the resistance value of the Pin㉒ resistor (3kΩ to 6.8kΩ).

(2) Selection of AGC Resistor R_{AGC} Pin㉓

Pin㉓ is the AGC LPF, and enables AGC effective level adjustment. The equivalent circuit in the vicinity of this pin has been so constituted as shown in Fig.2, and the output impedance at the charging time is 15kΩ while the input impedance at the discharging time is about 1MΩ.

The standard value of R_{AGC} is 330kΩ, but in case operation error is frequently caused in a weak electric field by white noise, selectively increase the value of R_{AGC} to a suitable level between 200kΩ and 1MΩ. So long as the value of R_{AGC} was properly increased, the AGC voltage proportionally becomes higher to prolong the discharging time constant, and the rate of operation error sharply drops with decrease of the gain of the AGC Amp. (Though Pin㉓, the noise components are put to peak (envelope) detection. Even if the value of R_{AGC} was increased, the charging time and voltage remain almost unchanged because Z_O=15kΩ).

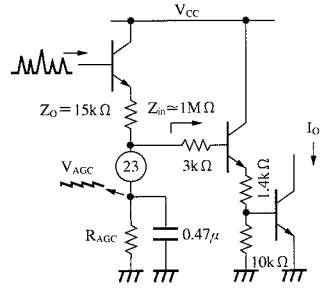
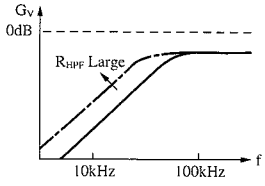


Fig.2

(3) Selection of HPF Resistor R_{HPF} Pin㉕

When the resistance value R_{HP} of the resistor between Pin㉕ and ㊴ was increased, the cut-off frequency of the HPF proportionally becomes lower.

The standard value of R_{HPF} is 330kΩ, but in case the operation error is frequently caused in a weak electric field by white noise at the modulation time or non-modulation time, selectively increase this R_{HPF} to a suitable value not exceeding 470kΩ.



[4] Cautions on Use of PLN (AN7291SC pin numbers are used in the following explanation.)

Care should be taken to use the PNL, because under the following conditions, in the PNL circuit of this IC, the output wave form may be distorted due to the oscillation of the PNL circuit.

1. Oscillation conditions

When the PNL is used under the conditions described in the following items (1) to (3) and the PNL−AGC voltage (Pin㉓ voltage) becomes 2.3 V or more, oscillation may occur.

(1) The PNL input frequency is 15 kHz or more and 500 mVrms is exceeded.

(2) The voltage of AGC pin (Pin㉓) is forced to exceed the above voltage.

(3) The voltage AC or DC of +/− several ten mV or more is directly applied to the PNL filter pins (Pin⑳ and Pin㉑).

The oscillation occurrence depends on V_{CC}.

The oscillation can not be stopped unless V_{CC} is much increased, if it occurs.

The above three conditions are not given under the normal operation, and therefore oscillation problems are not suffered in practical use. In the review stage, keep in mind that oscillation may occur when the above conditions are given.

2. Effect by external components

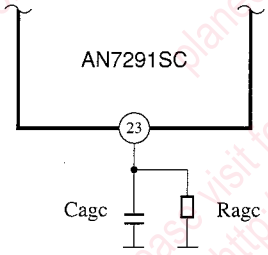
The PNL circuit oscillation depends on an external resistor and capacitor of AGC pin.

(1) C_{agc} is currently set to 0.47μF. The larger it is, the less frequently oscillation occurs.

(2) R_{agc} is 330kΩ. The smaller it is, the less frequently oscillation occurs.

When the above values are changed, take particular consideration for setting characteristics.

Also, when the use under the special conditions is expected, review the countermeasures against oscillation.



ICs for Tuner

■ Pin No. Correspondence Table

AN7291SC	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
AN7291FBP	44	45	46	47	1	2	3	4	5	6	7	8	9	10	11	14	15	16	17	18	19
AN7291SC	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42
AN7291FBP	20	21	22	23	25	26	27	28	29	30	31	32	33	34	35	36	38	39	40	41	42

* Pins 12, 13, 24, 37, 43 and 48 for the AN7291FBP are NC.

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