Integrated Circuit Systems, Inc.

AV9170-07

Clock Multiplier

General Description

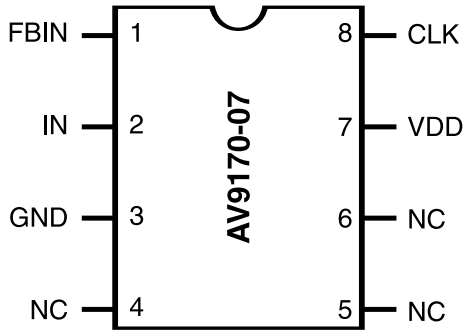
The **AV9170-07** is a PLL (Phase-Locked Loop) based frequency multiplier designed for use on Media Vision sound boards. This clock output is 4X the input clock, it is restricted to the output divider and the VCO range. The output frequency range is 1 to 12.5MHz, with an input range of 0.64 to 0.768MHz for IN and 0.256 to 3.072MHz for FBIN. By integrating the sensitive analog sections of the PLL, such as the phase comparator, loop filter and VCO, jitter is minimized and external part count is reduced.

The **AV9170-07** is a derivative of the AV9170 available from Integrated Circuit Systems, Inc. For additional information on the **AV9170-07**, please refer to the AV9170 Application Note.

Features

- Single chip clock multiplier
- On-chip Phase-Locked Loop
- Low output jitter
- 5 volt only power supply
- Low power CMOS technology
- Small 8-pin DIP or SOIC package
- On-chip loop filter

Pin Configuration

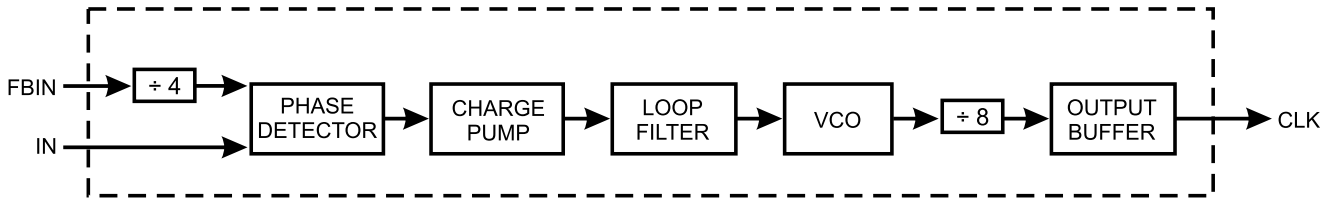


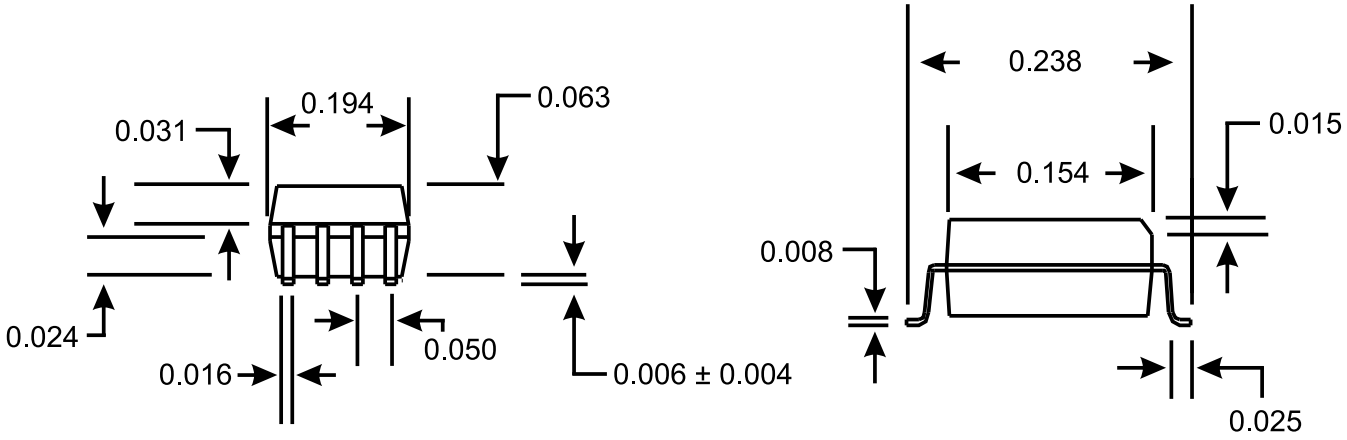
8-Pin DIP or SOIC J-3, J-6

Pin Descriptions

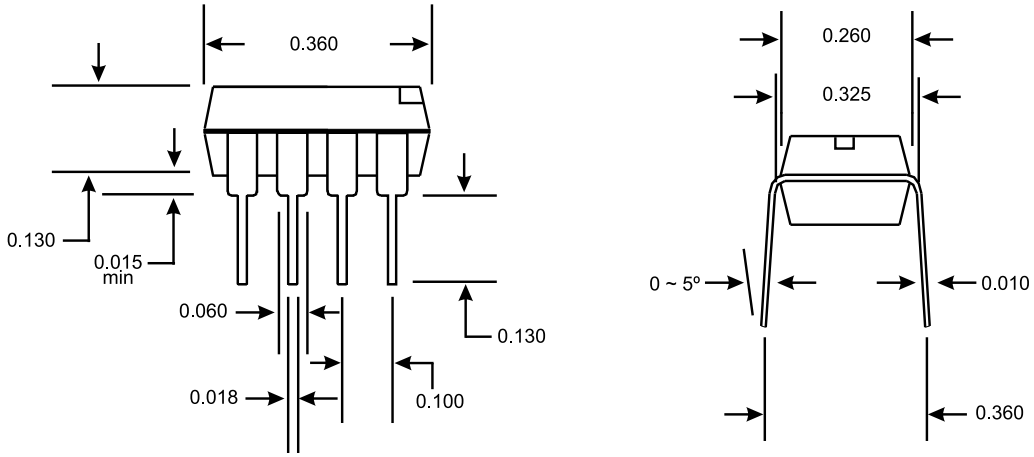
PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	FBIN	Input	FEEDBACK INPUT for Phase-Locked Loop.
2	IN	Input	INPUT for reference clock.
3	GND	-	GROUND.
4	NC	-	No Connection.
5	NC	-	No Connection.
6	NC	-	No Connection.
7	VDD	-	Power Supply (+5V).
8	CLK	Output	CLOCK output.

Block Diagram





8 - Pin SOIC



8 - Pin DIP

Ordering Information

AV9170-07CN08 (8 Lead Plastic DIP)
AV9170-07CS08 (8 Lead SOIC)

Example:

ICS XXXX-PPP M X#W

Lead Count & Package Width
Lead Count=1, 2 or 3 digits
W=.3" SOIC or .6" DIP; None=Standard Width

Package Type
N=DIP (Plastic)
S=SOIC

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS=Standard Device; GSP=Genlock Device; AV=ICS (West Coast)