
**Description of UFDFPN5, UFDFPN8 and WFDFPN8
for STMicroelectronics EEPROMs and recommendations for use**

Introduction

This document describes the following Dual Flat No-Lead Package (DFN) 5 and 8 leads used for STMicroelectronics EEPROM products, and provides recommendation on how to use them:

- UFDFPN5
- UFDFPN8
- WFDFPN8

During recent years ST conducted research on next-generation Chip-Size Packaging (CSP). The DFN is a near CSP plastic encapsulated package using conventional copper lead frame technology. This construction benefits from being a cost effective advanced packaging solution which helps to maximize board space with improved electrical and thermal performance over traditional leaded packages.

Such a package is a leadless package, with low profile (less than 1.0 mm), where electrical contact to the PCB is made by soldering the lands on the bottom surface of the package to the PCB, instead of the conventional formed leads. The DFNs are molded in one solid array. Individual units are singulated using a saw.

Warning: This technical note is widely distributed and the list of applicable products is constantly evolving. Please verify the product under consideration does include at least one of the packages described herein before assuming this document applies.

Contents

Contents **2**

1 Overview **4**

2 Mechanical data **5**

3 Device marking **9**

4 Packing specifications and labeling description **10**

 4.1 Carrier tape 10

 4.2 Cover tape 10

 4.3 Reels 11

 4.4 Final packing 12

 4.5 Labeling 12

 4.6 Storage and shipping recommendations 12

5 Surface mount considerations for DFN package **14**

6 PCB design guidelines **15**

 6.1 Perimeter pads design 15

 6.2 PCB central pad guidelines 15

7 Stencil design for perimeter pads **16**

8 Stencil thickness and solder paste **17**

9 Solder joint standoff height and fillet formation **18**

10 Reflow soldering **19**

11 Inspections **20**

12 X-Ray inspections **21**

13 Package changes **22**

14	Package quality	23
	14.1 Electrical inspection	23
	14.2 Visual inspection	23
15	Conclusion	24
16	Revision history	25

1 Overview

The DFN is available in 3 formats.

The smallest being the UFDFPN5 (5 leads) with body size of 1.7x1.4 mm and body thickness is 0.55 mm.

The consumer one UFDFPN8 (8 leads) with body size of 2.0x3.0 mm and body thickness is 0.55 mm.

The automotive one WFDFPN8 (8 leads) with body size of 2.0x3.0 mm and body thickness is 0.75 mm.

UFDFPN8/WFDFPN8 comply with Jedec Outline MO-229.

The DFN family has been designed to fulfill the same quality levels and same reliability performance as standard semiconductor plastic packages. As a consequence these DFN can be considered as standard surface mount devices which are assembled on a printed circuit board (PCB) without any special or additional process steps.

Only Lead-free RoHS / Halogen Free compliant DFN are available in mass production.

Figure 1. UFDFPN5

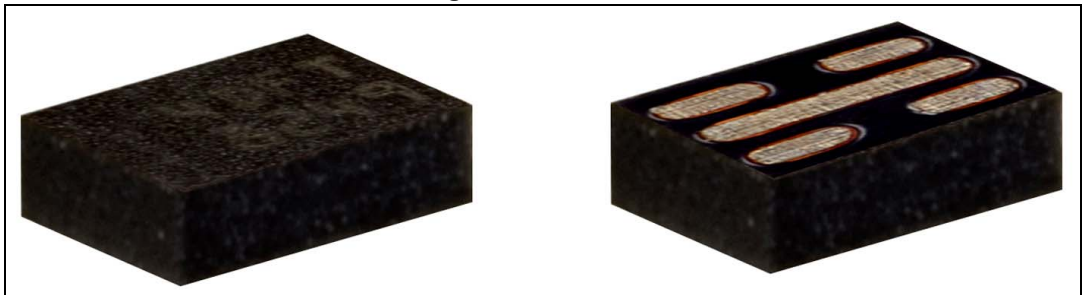
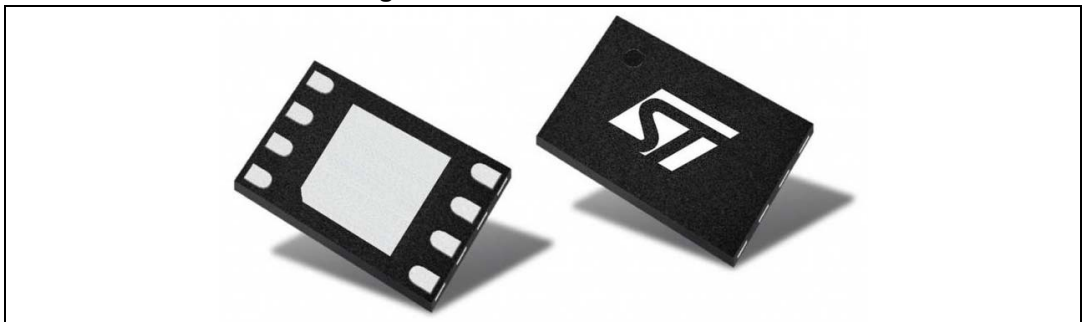


Figure 2. UFDFPN8/WFDFPN8



2 Mechanical data

Figure 3. UDFPN5 1.7x1.4x0.55 5L Pitch 0.4 package outline

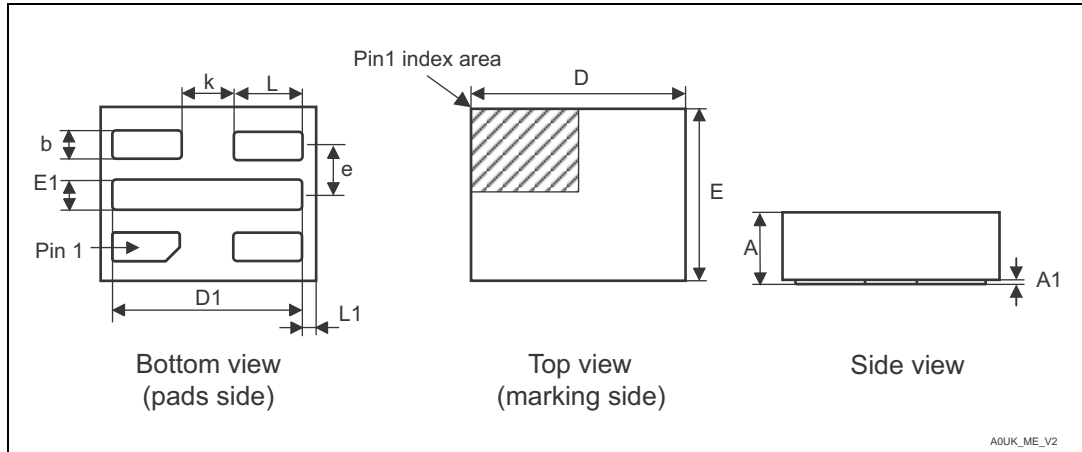


Table 1. UDFPN5 1.7x1.4x0.55 5L Pitch 0.4 mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	0.5	0.55	0.6	0.0197	0.0217	0.0236
A1	0	-	0.05	0	-	0.002
b ⁽²⁾	0.18	0.22	0.26	0.0071	0.0087	0.0102
D	1.6	1.7	1.8	0.063	0.0669	0.0709
E	1.3	1.4	1.5	0.0512	0.0551	0.0591
D1	1.4	1.5	1.6	0.0551	0.0591	0.063
E1	0.18	0.22	0.26	0.0071	0.0087	0.0102
e	-	0.4	-	-	0.0157	-
L	0.5	0.55	0.6	0.0197	0.0217	0.0236
L1	-	0.1	-	-	0.0039	-
k	-	0.4	-	-	0.0157	-

1. Values in inches are converted from mm and rounded to four decimal digits.

2. Dimension b applies to plated terminal and is measured between 0.15 and 0.30 mm from the terminal tip.

Figure 4. UFDFPN8 8-lead Ultra thin Fine pitch Dual Flat Package No lead 2x3 mm package outline

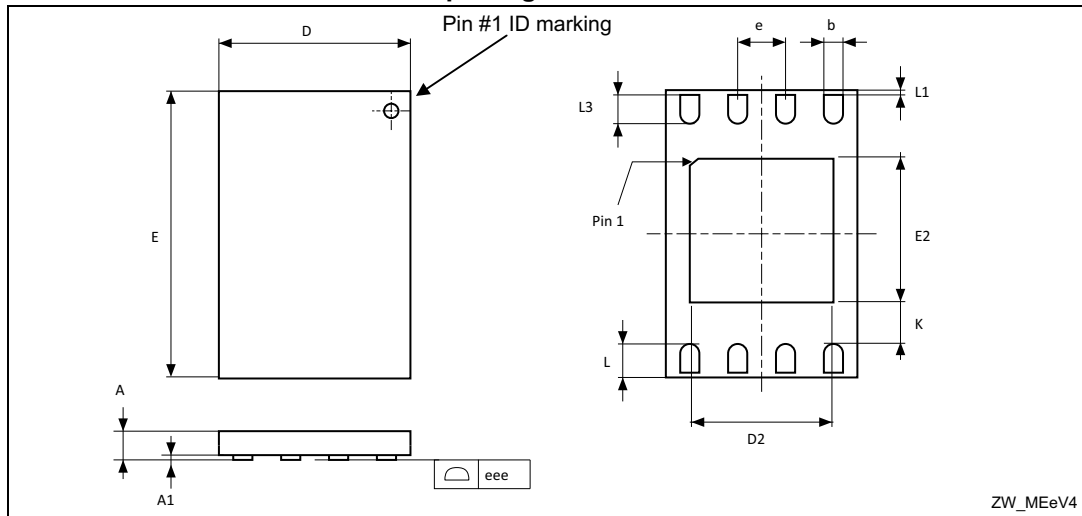
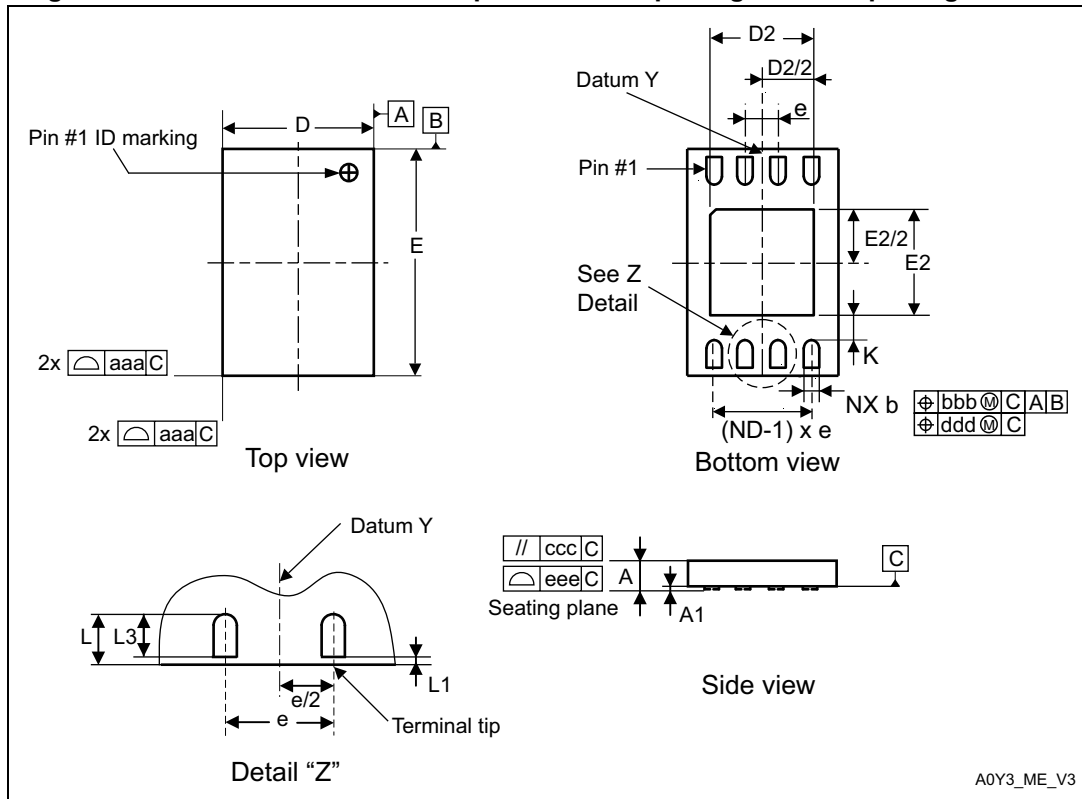


Table 2. UFDFPN8 8-lead Ultra thin Fine pitch Dual Flat Package No lead 2x3 mm mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	0.45	0.55	0.6	0.0177	0.0217	0.0236
A1	0	0.02	0.05	0	0.0008	0.002
b	0.2	0.25	0.3	0.0079	0.0098	0.0118
D	1.9	2	2.1	0.0748	0.0787	0.0827
D2	1.2	-	1.6	0.0472	-	0.063
E	2.9	3	3.1	0.1142	0.1181	0.122
E2	1.2	-	1.6	0.0472	-	0.063
e	-	0.5	-	-	0.0197	-
K	0.3	-	-	0.0118	-	-
L	0.3	-	0.5	0.0118	-	0.0197
L1	-	-	0.15	-	-	0.0059
L3	0.3	-	-	0.0118	-	-
eee ⁽²⁾	-	0.08		-	0.0031	

1. Values in inches are converted from mm and rounded to four decimal digits.
2. Applied for exposed die paddle and terminals. Excludes embedding part of exposed die paddle from measuring.

Figure 5. WFDFPN8 8-lead thin fine pitch dual flat package no lead package outline



A0Y3_ME_V3

Table 3. WFDFPN8 8-lead thin fine pitch dual flat package no lead mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	0.7	0.75	0.8	0.0276	0.0295	0.0315
A1	0.025	0.045	0.065	0.001	0.0018	0.0026
b	0.2	0.25	0.3	0.0079	0.0098	0.0118
D	1.9	2	2.1	0.0748	0.0787	0.0827
E	2.9	3	3.1	0.1142	0.1181	0.122
e	-	0.5	-	-	0.0197	-
L1	-	-	0.15	-	-	0.0059
L3	0.3	-	-	0.0118	-	-
NX ⁽²⁾	8			8		
ND ⁽³⁾	4			4		
aaa	0.15	-	-	0.0059	-	-
bbb	0.1	-	-	0.0039	-	-
ccc	0.1	-	-	0.0039	-	-
ddd	0.05	-	-	0.002	-	-

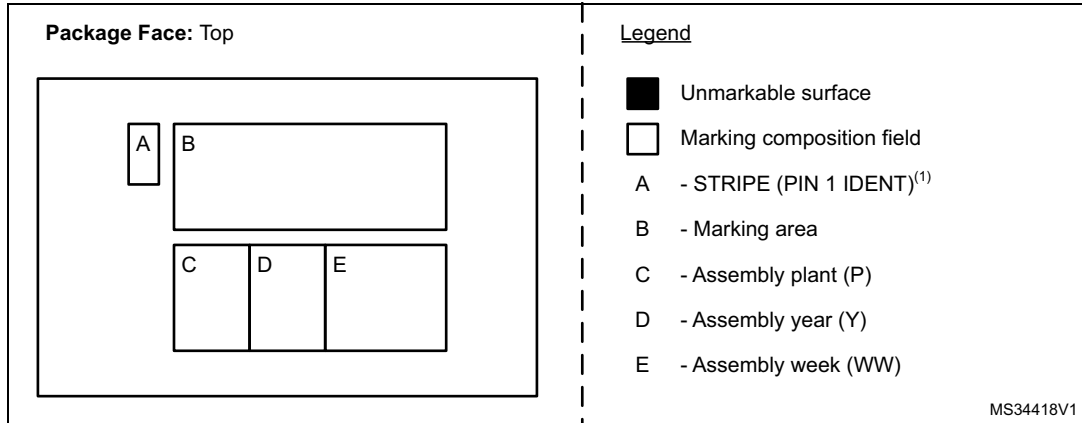
Table 3. WFDFPN8 8-lead thin fine pitch dual flat package no lead mechanical data (continued)

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
eee ⁽⁴⁾	0.08	-	-	0.0031	-	-
D2	1.05	-	1.65	0.0413	-	0.065
E2	1.05	-	1.45	0.0413	-	0.0571
K	0.45	-	-	0.0177	-	-
L	0.3	-	0.5	0.0118	-	0.0197

1. Values in inches are converted from mm and rounded to four decimal digits.
2. NX is the number of terminals.
3. ND is the number of terminals on "D" sides.
4. Applied for exposed die paddle and terminals. Excluding embedding part of exposed die paddle from measuring.

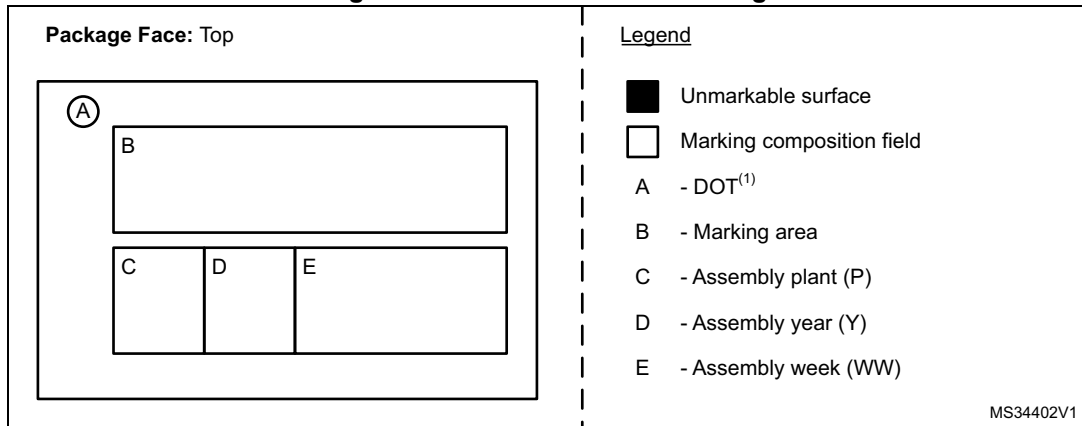
3 Device marking

Figure 6. UDFPN5 device marking



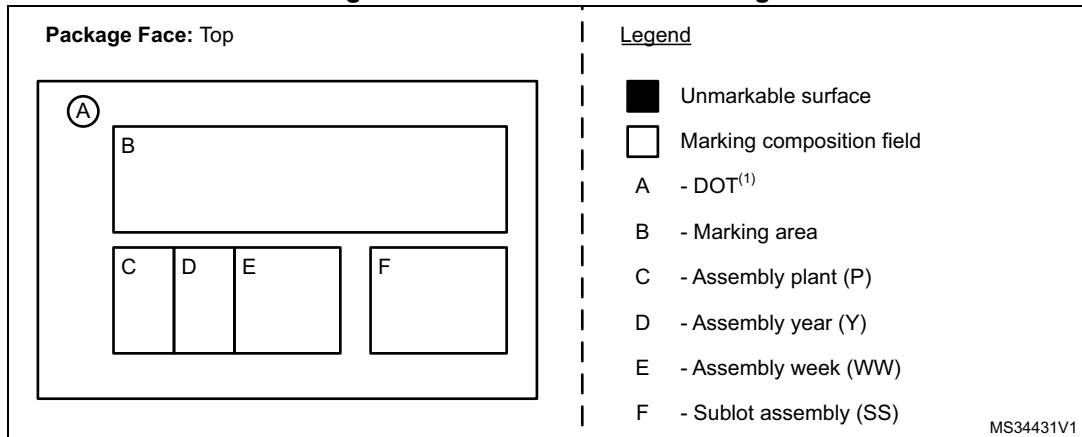
1. Pin 1 identification

Figure 7. UDFPN8 device marking



1. Pin 1 identification

Figure 8. WFDFPN8 device marking



1. Pin 1 identification

4 Packing specifications and labeling description

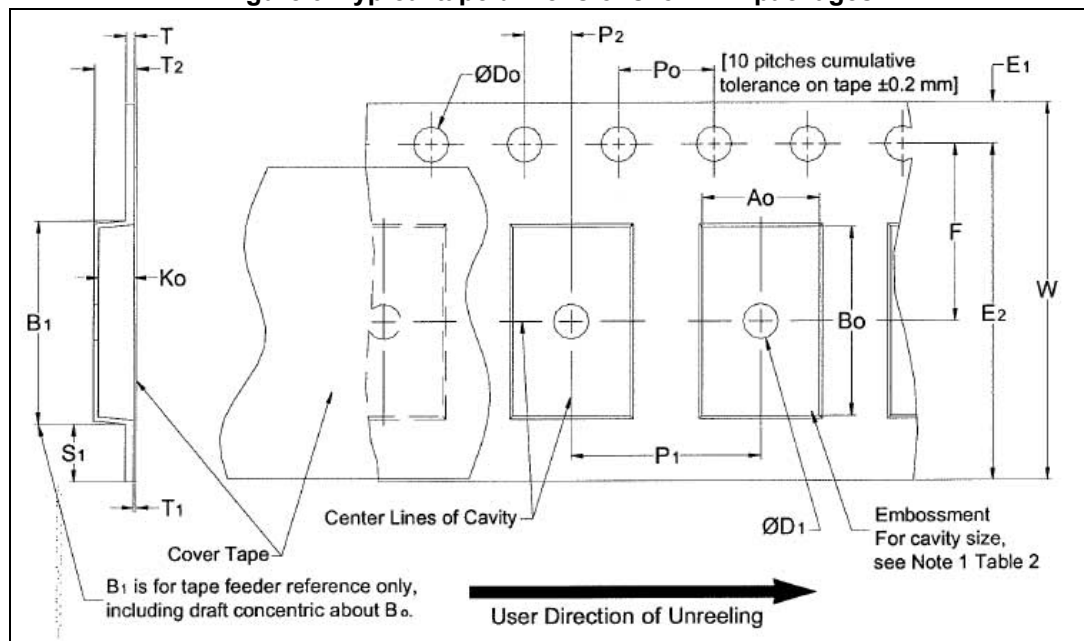
DFN devices are delivered in tape and reel to be fully compatible with standard high volume SMD components. All tape and reel characteristics are compliant with EIA-481-C and IEC 60286-3 standards and EIA 763 (783).

4.1 Carrier tape

The DFN are placed in carrier tapes with their leads side facing the bottom of the cavity so that the devices can be picked up by their flat side. The devices are positioned in the carrier tape with pin 1 on the sprocket hole side.

An example of carrier tape mechanical dimensions is shown in *Figure 9*. The standard tape width is 12 mm.

Figure 9. Typical tape dimensions for DFN packages



No hole is present in the cavity to avoid any external contamination.

The embossed carrier tape is in a black conductive material (surface resistivity within 10^4 and $10^8 \Omega/\text{sq}$). Using this material prevents the component from being damaged by electrostatic discharge and ensures the total discharge of the component prior to the placement on the PCB. Conductivity is guaranteed to be constant and is not affected by shelf life or humidity. The material does not break when bent and does not have any powder or flake residue that rubs off.

4.2 Cover tape

The carrier tape is sealed with a transparent antistatic (surface resistivity ranging from $10^5 \Omega/\text{sq}$ to $10^{12} \Omega/\text{sq}$) polyester film cover tape using a heat activated adhesive. The cover tape tensile strength is higher than 10 N.

The peeling force of the cover tape ranging from 0.1 N to 0.7 N in accordance with the testing method EIA-481-C and IEC 60286-3. Cover tape is peeled back in the direction opposite to the carrier tape travel. The angle between the cover tape and the carrier tape is between 165 and 180 °, and the test is performed at a speed of 120 ± 10 % mm/min.

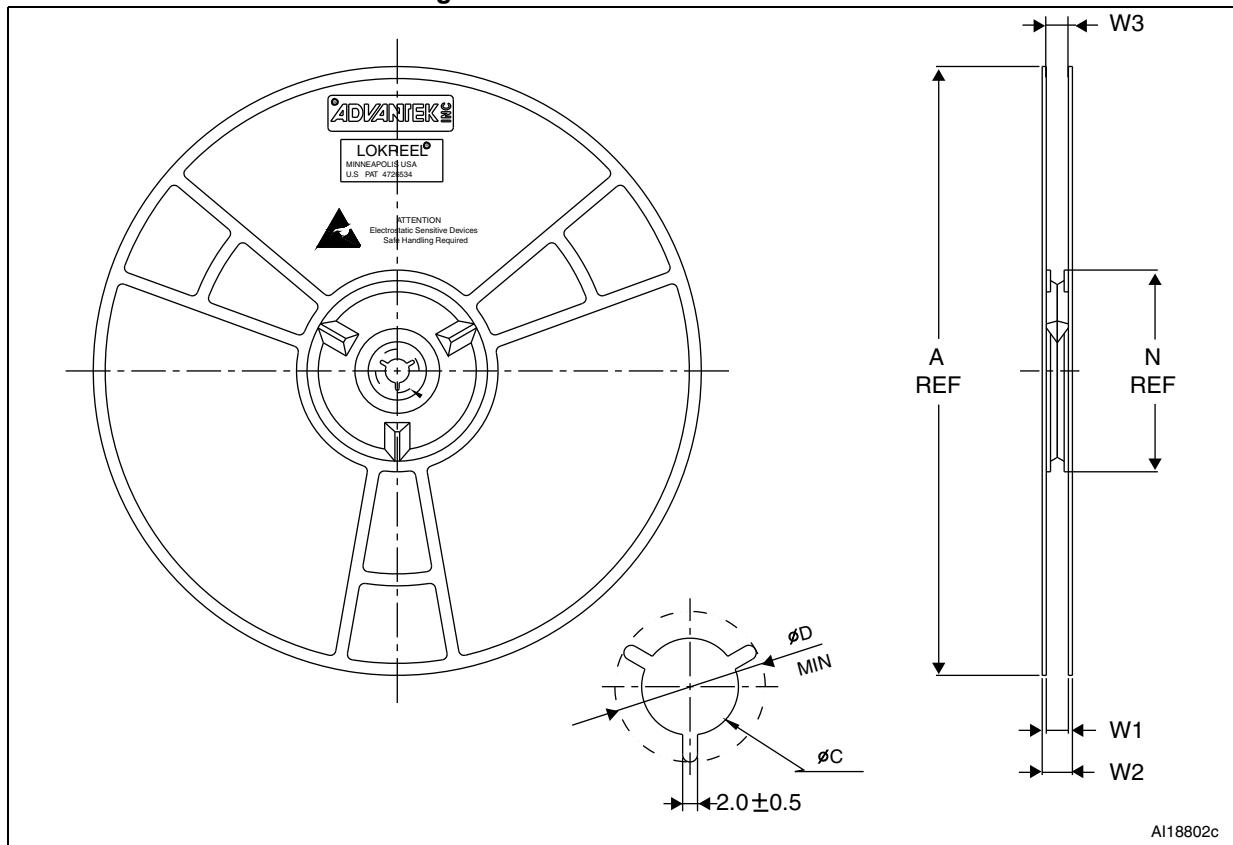
4.3 Reels

The sealed carrier tape containing the DFN is reeled on 7-inch reels (see [Figure 10](#) and [Table 4](#) for reel mechanical dimensions). These reels are compliant with EIA-481-C standard. In particular, they are made of an antistatic polystyrene material. The reel color may vary depending on supplier.

Dice quantity per reel is 2500. A reel may contain devices coming from 2 different wafer lots.

The reels have a minimum leader of 600 mm and a minimum trailer of 160 mm (in compliance with EIA-481-C and IEC 60286-3 standards). The leader makes up a portion of carrier tape with empty cavities and sealed by cover tape at the beginning of the reel (external side). It is affixed to the last turn of the carrier tape by using adhesive tape. The trailer is located at the end of the reel and consists of empty sealed cavities.

Figure 10. 7-inch reel schematics



AI18802c

Table 4. 7-inch reel dimensions

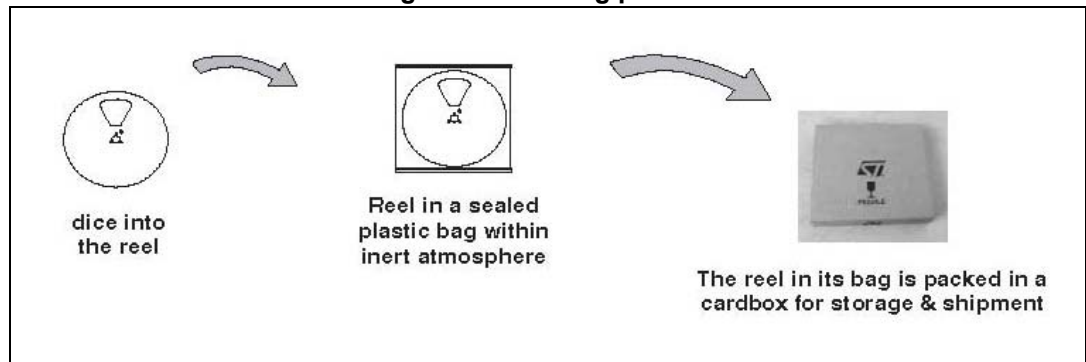
Reel	W1 (mm) ⁽¹⁾⁽²⁾	W2 (mm) ⁽²⁾	W3 (mm)	A (mm)	C (mm)	D (mm)	N (mm)
7"	12.8 (typ)	18.2 (max)	12	177.8 (typ.)	13.0 ⁽³⁾	20.2 (min)	100.0 (typ)
	16.8 (typ)	22.2 (max)	16				
	24.8 (typ)	30.2 (max)	24				
	32.8 (typ)	38.2 (max)	32				
	44.8 (typ)	50.2 (max)	44				

1. +0.6 mm, -0.4 mm.
2. Measured at the hub.
3. +0.5 mm, -0.2 mm.

4.4 Final packing

Each reel is heat-sealed under inert atmosphere in a transparent recyclable antistatic polyethylene bag (minimum of 4 mils material thickness). Reels are then packed in cardboard boxes. A full description of the packing process is shown in [Figure 11](#).

Figure 11. Packing process



4.5 Labeling

To trace each production lot and shipment lot, the 7-inch reels and the cardboard box are identified by labels that mention the device part number, the shipped quantity and traceability information.

The trace code printed on the labels ensures backward traceability from the lot received by the customer to each step of the process. It includes in/ out dates, as well as quantities during diffusion, assembly, test phase, and in the final storage. Likewise, forward traceability is able to trace a lot history from the wafer fab to the customer location.

4.6 Storage and shipping recommendations

DFN reels are packed under inert N2 atmosphere in a sealed bag. For shipment and handling, reels are packed in a cardboard box.

ST consequently recommends the following shipping and storage conditions:

- Relative humidity between 15 and 70 %
- Temperature ranging from -55 to +150 °C.
- Components in a non opened sealed bag can be stored for 6 months after shipment.
- Components in tape and reel must be protected from exposure to direct sunlight.

5 Surface mount considerations for DFN package

In order to perform at peak, special considerations are needed to properly design the motherboard and to mount the package. For enhanced thermal, electrical, and board level performance, we recommend the exposed pad on the package to be soldered to the board using a corresponding pad on the board. The PCB footprint design needs to be considered from dimensional tolerances due to package, PCB, and assembly.

A number of factors may have a significant effect on mounting DFN package on the board and the quality of solder joints. Some of these factors include: amount of solder paste coverage in thermal pad region, stencil design for peripheral and thermal pad region, type of vias, board thickness, lead finish on the package, surface finish on the board, type of solder paste, and reflow profile. This information note proposes some guidelines for this purpose. It should be emphasized that this is just a guideline to help the user in developing the proper motherboard design and surface mount process.

6 PCB design guidelines

As the lands on the package bottom side are rectangular in shape with rounded edge and since the package does not have any solder balls, the electrical connection between the package and the motherboard is made by printing the solder paste on the motherboard and reflowing it after component placement. In order to form reliable solder joints, special attention is needed in designing the motherboard pad pattern and solder paste printing.

6.1 Perimeter pads design

We recommend the PCB pad pattern to be designed based on industry standards such as IPC-SM-782. However, we recommend development of proper design using some experimental trials. For the purpose of this document, IPC's methodology is used here for designing PCB pad pattern.

There are two approaches in PCB pad designs, namely Non-solder Mask Defined pad (NSMD) and Solder Masked Defined pad (SMD).

The NSMD has an opening that is larger than the copper pad. The PCB pad area is controlled by the size of the copper pad. Since the copper pad etching process is rather capable and stable, a smaller size copper pad can be defined accurately. As DFN are fine pitch and small outline packages, it is recommended to use the NSMD method to define the perimeter pad on the PCB.

6.2 PCB central pad guidelines

The DFN package, with its exposed die pad soldered to the PCB has a good mechanical attach to the board. The mechanical performance of the package is greatly influenced by the PCB design. The PCB should be Solder Mask Defined (SMD). The pad area is controlled by the size of the solder mask opening. The size of the central pad land pattern should be equal to the exposed pad of the package. Finally, the solder mask opening should overlap the edges of the PCB thermal pad land by at least 0.065 mm on all four sides.

Board Mounting Guidelines

Because of the small lead surface area and the sole reliance on printed solder paste on the PCB surface, care must be taken to form reliable solder joints for DFN packages. This is further complicated by the large thermal pad underneath the package and its proximity to the inner edges of the leads. Special considerations are needed in stencil design and paste printing for both perimeter and central pads. Since surface mount process varies from company to company, careful process development is recommended. The following provides some guidelines for stencil design.

7 Stencil design for perimeter pads

The optimum and reliable solder joints on the perimeter pads should have about 50 to 75 microns (2 to 3 mils) standoff height and good side fillet on the outside. A joint with good standoff height but no or low fillet will have reduced life but may meet application requirement. The first step in achieving good standoff is the solder paste stencil design for perimeter pads. The stencil aperture opening should be so designed that maximum paste release is achieved. This is typically accomplished by considering the following two ratios:

For rectangular aperture openings, as required for this package, these ratios are given as

Area Ratio = $LW/2T(L+W)$, and

Aspect Ratio = W/T

Where L and W are the aperture length and width, and T is stencil thickness. For optimum paste release the area and aspect ratios should be greater than 0.66 and 1.5 respectively.

It is recommended that the stencil aperture should be 1:1 to PCB pad sizes as both area and aspect ratio targets are easily achieved by this aperture. The stencil should be laser cut and electro polished. The polishing helps in smoothing the stencil walls which results in better paste release. It is also recommended that the stencil aperture tolerances should be tightly controlled, especially for 0.4 and 0.5 mm pitch devices, as these tolerances can effectively reduce the aperture size.

8 Stencil thickness and solder paste

The stencil thickness of 0.100 mm is recommended for 0.4 and 0.5 mm pitch parts. A laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release.

Since not enough space is available underneath the part after reflow, it is recommended that "No Clean", Type 3 paste be used for mounting DFN packages. Nitrogen purge is also recommended during reflow.

9 Solder joint standoff height and fillet formation

The solder joint standoff is a direct function of amount of paste coverage. The standoff height is also affected by the type and reactivity of solder paste used during assembly; PCB thickness and surface finish, and reflow profile.

The peripheral solder joint fillets formation is also driven by multiple factors. It should be realized that only bottom surface of the leads are plated with solder and not the ends and the bare Cu on the side of the leads may oxidize if the packages are stored in uncontrolled environment. It is, however, possible that a solder fillet will be formed depending on the solder paste (flux) used and the level of oxidation.

The fillet formation is also a function of PCB land size, printed solder volume, and the package standoff height. Since there is only limited solder available, higher standoff - controlled by paste coverage on the thermal pad – may not leave enough solder for fillet formation. Conversely, if the standoff is too low, large convex shape fillets may form.

Since center pad coverage has the greatest impact on standoff height the volume of solder necessary to create optimum fillet varies. Package standoff height and PCB pads size will establish the required volume.

10 Reflow soldering

The purpose of the reflow process is to melt the solder particles, wet the surfaces to be joined, and solidify the solder into a stronger metallurgical bond.

Temperature profile is the most important control in reflow soldering and it must be fine-tuned to establish a robust process. DFN components probably would be among the smallest devices on any PCB. In such cases, place thermocouples under the heaviest thermal mass device on the PCB to monitor the reflow profile. Generally, when the heaviest thermal mass device reaches reflow temperatures, all other components on the PCB will reach reflow temperatures as well.

For all devices on the PCB, the solder paste needs to be taken into account for the reflow profile. Every paste has a flux, and the flux dominates the reflow profile for steps like soak time, soak temperature, and ramp rates. Peak reflow temperature is the melting temperature of the metals in the paste, plus a "safety" margin to ensure that all solder paste on the PCB reflows.

The reflow profile should follow the paste supplier's "recommended" profile.

Since solder joints are not fully exposed in the case of DFN, any retouch is limited to the side fillet. For defects underneath the package, the whole package has to be removed. Rework of DFN packages can be a challenge due to their small size and is not recommended. In most applications, DFN will be mounted on smaller, thinner, and denser PCBs that introduce further challenges due to handling and heating issues. Since reflow of adjacent parts is not desirable during rework, the proximity of other components may further complicate this process.

11 Inspections

Unlike traditional leaded components, the solder joints of DFN are formed underneath the package. The conventional visual inspection technique to check the quality of the solder joint is time consuming. Whenever possible, optical inspection and X-ray inspection are recommended to verify any open or short circuit after reflow soldering.

12 X-Ray inspections

X-ray is one way to detect solder shorts underneath the DFN package. X-rays transmitted from the X-ray tube are absorbed by the components in proportion to their density. In this case, a solder joint having a higher density absorbs most of the X-rays, and the resultant X-ray intensity is detected and interpreted in a gray scale image. The X-ray image is also a good instrument to view solder voids in the exposed pad region.

13 Package changes

STMicroelectronics reserves the right to implement minor changes of geometry and manufacturing processes without prior notice. Such changes will not affect electrical characteristics. However for confirmed orders, no variation with respect to the datasheet will be made without prior customer's approval.

14 Package quality

14.1 Electrical inspection

All the critical parameters defined in the DFN device datasheet are 100 % electrically characterized. The other parameters are guaranteed by technology, design rules or by continuous monitoring systems.

14.2 Visual inspection

A visual control is performed on all manufacturing lots according to JESD22_B101B specification.

15 Conclusion

Lead-free DFN have been developed by STMicroelectronics for electronic applications where integration and performance are designer's main concerns.

STMicroelectronics DFN key features are:

- Remarkable board space saving: package size near die size and total height less than 800 μm .
- Enhanced electrical performance: minimized parasitic inductance due to very short electrical paths.

DFN are delivered in tape and reel and are fully compatible with other high volume SMD components (standard plastic packages or CSP/BGA packages) in regards to existing pick-and-place equipment, standard solder reflow assembly equipment and standard PCB techniques.

16 Revision history

Table 5. Document revision history

Date	Revision	Changes
25-Mar-2014	1	Initial release.
07-Apr-2014	2	Removed table on cover page. Updated <i>Figure 5: WFDFPN8 8-lead thin fine pitch dual flat package no lead package outline.</i>
25-Nov-2014	3	Updated stencil thickness in <i>Section 8: Stencil thickness and solder paste.</i>

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