TAT2814A1L

DOCSIS 3.0 / Edge QAM Variable Gain Amplifier

Applications

- Integrated DOCSIS 3.0 / Edge QAM Amplifier Chain
- Forward Path Variable Gain Amplifier

Product Features

- Meets DOCSIS 3.0 With +4 dB Typical Performance Margin
- < 5 Watt Nominal Power Consumption
- 45 – 1003 MHz Bandwidth
- Low-Reflection Differential Input / Output Stages
- 18 dB Typical Return Loss Across Gain Range
- Variable Gain Attenuator: 18 dB Typical Range
- 30 dB Typical Max Gain
- +49 dBm Typical OIP3
- 2.7 dB Typical Noise Figure
- Typical Input Stage Bias: +5 V, 290 mA
- Typical Output Stage Bias: +8 V, 415 mA

General Description

The TAT2814A1L is an RFIC for DOCSIS 3.0 Output Sections, such as CMTS and Edge QAM. It combines a low-reflection differential input stage, a variable gain attenuator and an efficient output amplifier to provide significant reduction in power consumption and PC board space. It replaces circuitry requiring up to 10x the board space and 2x the power.

The TAT2814A1L meets the stringent DOCSIS 3.0 output linearity specifications with extra margin to overcome additional losses before the output connector.

The TAT2814A1L is packaged in an industry standard 7 x 7 mm 48-pin leadless SMT package and consumes 5 W between a +5 V input amplifier supply and an +8 V output amplifier supply. The TAT2814A1L utilizes proven GaAs pHEMT to optimize performance and cost. It allows the designer to optimize output stage voltage to significantly reduce power consumption in Edge QAM applications.

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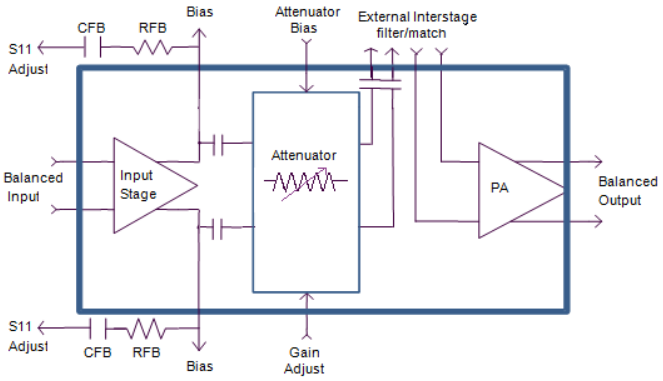
48-pin 7x7mm leadless SMT Package

Functional Block Diagram



Ordering Information

Part No.	Description
TAT2814A1L	DOCSIS 3.0 Edge QAM Variable Gain Amplifier
TAT2814A1L-EB	Evaluation Board

Standard T / R size = 1000 pieces on a 7” reel

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−40 to +100 °C
Device Voltage (V_{DD})	+10 V
RF Input Power (single tone)	+10 dBm

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V_{DD} - Stage 1		+5		V
V_{PA} - Stage 2		+8		V
Operating Ambient Temp.	−40		+85	°C
Tj (for >10^6 hours MTTF)			150	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

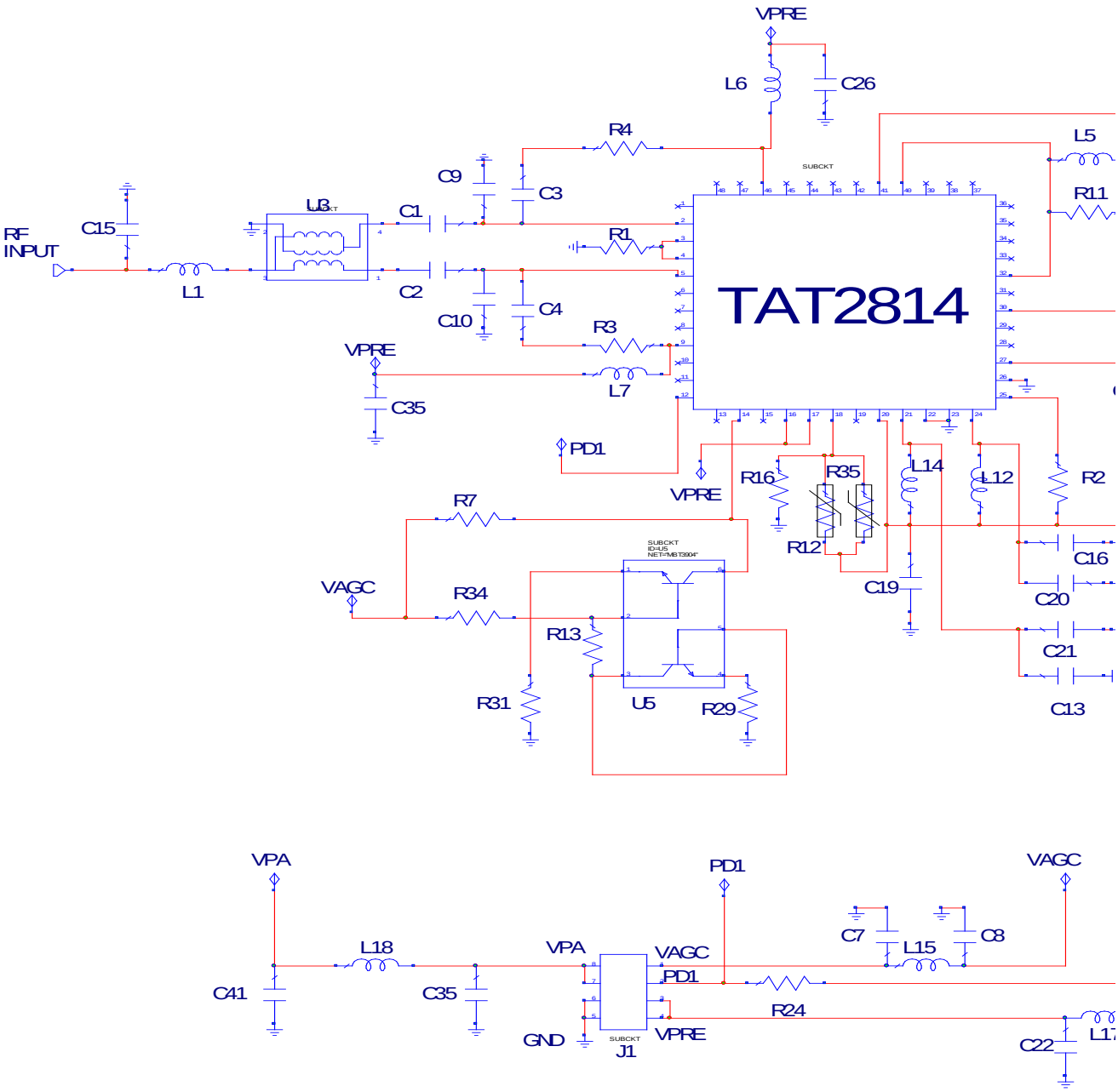
Electrical Specifications

Test conditions unless otherwise noted: V_{DD} = +5 V, V_{PA} = +8 V, $T_{AMBIENT}$ = +25 °C, Includes input and output balun losses

Parameter	Conditions		Min	Typ	Max	Units
Operational Frequency Range			45		1003	MHz
Gain	I_{AGC}= 1 mA, f= 1003 MHz		27.5	30	32	dB
Gain Variation over Temp (1)	Maximum gain deviation within passband within temp. range of −40 °C to +85 °C relative to +25 °C.			1.0		dB
Gain Flatness	Peak deviation from straight line across full band.			±0.25	±0.5	dB
Gain Slope	Max slope of best fit straight line over all attenuator		−1.4	−1.0		dB
Attenuator Range	Max Gain - Min Gain			18		dB
Input Return Loss	I_{AGC}= 1 mA			18		dB
Output Return Loss	I_{AGC}= 1 mA			20		dB
EQAM V_{OUT}	Four Channel ACPR on a Single Port	Adjacent (1, 2)	+55	+56		dBmV / chan.
		Next-adjacent channel (1, 3)				
		Third-adjacent channel (1, 4)				
EQAM Vout (1, 5)	Single Channel Harmonics		+63	+64		dBmV
Output P1dB				+28		dBm
Output IP3	Pout=+8 dBm/tone, 6 MHz tone spacing			+49		dBm
Noise Figure				2.7		dB
1st Stage Current	V_{DD}=+5 V			290	330	mA
2nd Stage Current	V_{PA}=+5 V			415	450	mA
Power Down DC Control Pin 12)		Input High Voltage	1.8			V
		Input Low Voltage			0.5	
		Input High Current			300	uA
		Input Low Current			−-50	
AGC Input Current (Pin 14)			−40		−1	mA
Thermal Resistance, θjc (6)				11.8		°C/W

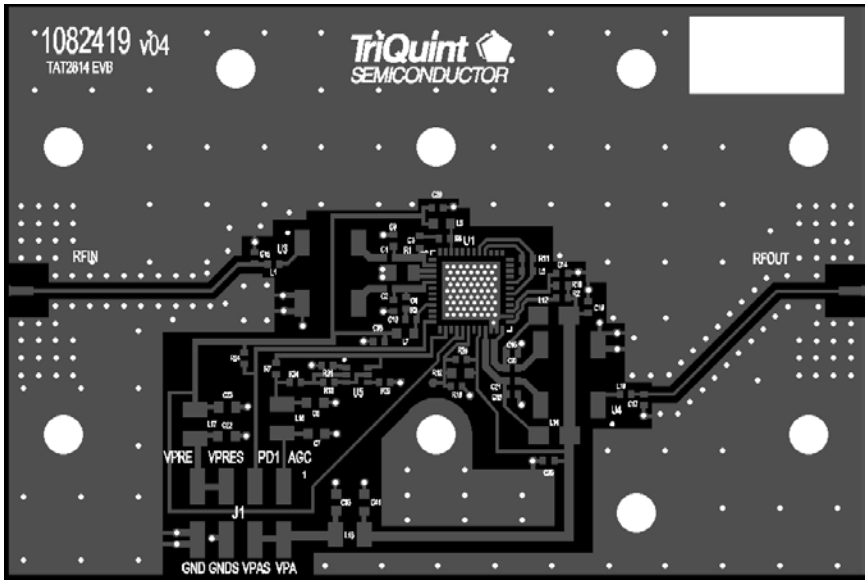
Notes:
1. Production tested at 66 and 990 MHz.
2. Adjacent channel (750 kHz from channel block edge to 6 MHz from channel block edge) better than −60 dBc.
3. Next-adjacent channel (6 MHz from channel block edge to 12 MHz from channel block edge) better than −63 dBc.
4. Third-adjacent channel (12 MHz from channel block edge to 18 MHz from channel block edge) better than −65 dBc.
5. In each of 2N contiguous 6 MHz channels or in each of 3N contiguous 6 MHz channels coinciding with 2nd harmonic and with 3rd harmonic components, respectively (up to 1002 MHz) better than −63 dBc..
6. $\Theta_{jb} = (Tj_{max} - T_{groundslug})/P_{diss}$, where P_{diss} = power dissipated in the 2nd stage amplifier (power amplifier)

TAT2814A1L-EB Schematic



Note: R3 and R4 required for matching and stability of input amplifi

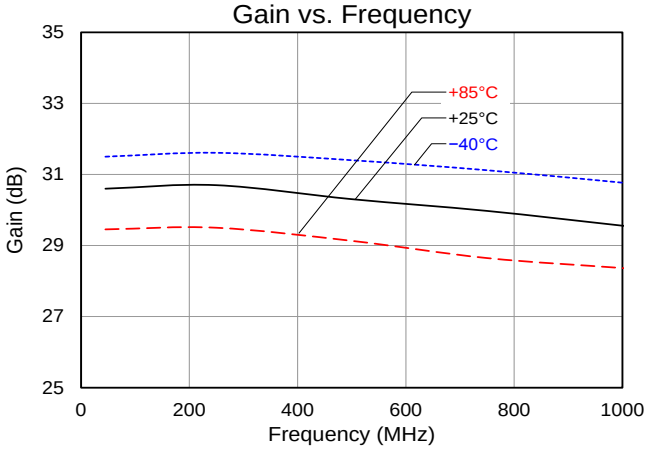
Bill of Material – TAT2814A1L-EB



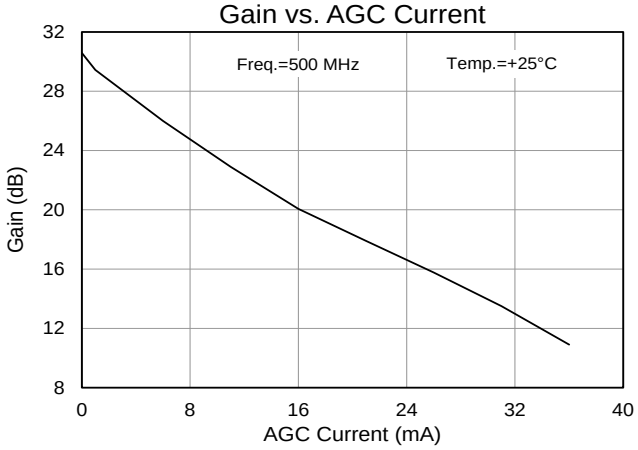
Reference Des.	Value	Description	Manuf.	Part Number
U1		Variable Gain Amplifier, QFN 7 x 7	TriQuint	TAT2814A
C1, C2, C20, C21	0.01 µF	Ceramic Cap, 0402, X7R, 16 V, 10%	Various	
C3, C4, C19, C26, C35	1000 pF	Ceramic Cap, 0402, 5%	Various	
C7, C8, C22, C23, C35, C41	0.01 µF	Ceramic Cap, 0603, X7R, 50 V,5%	Various	
C9, C10, C13, C14, C15, C16, C17, C36, R7, R10	DNP	No Load Parts		
L1	1.8 nH	Ind, wirewound, 0402, 5%	Various	
L16, R2, R13	0 Ω	Res, thin film, 0402	Various	
L5	420 nH	Ind, wirewound, 0402, 5%	Coilcraft	0402AF-421XJLU
L6, L7	560 nH	Ind, wirewound, 0603, 5%	Coilcraft	0603AF-561XJRU
L12, L14	500 nH	Ind, wirewound, 1206, 5%	Murata	LQH31HNR50K
L15, L17, L18	0.9 µH	Ind, Ferrite, 1008, 10%	Various	
R1	1.8 Ω	Res, thin film, 0805, 1/4 W 5%	Various	
R3, R4	2.5 kΩ	Res, thin film, 0402, 5%	Various	
R11	560 Ω	Res, thin film, 0402, 5%	Various	
R12	1 kΩ	Thermistor, PTC, 0603, 5%	Panasonic	ERAV33J102V
R16	680 Ω	Res, thin film, 0402, 1%	Various	
R29	36 Ω	Res, thin film, 0402, 1%	Various	
R31	1.0 Ω	Res, thin film, 0402, 1%	Various	
R34	1.27 kΩ	Res, thin film, 0402, 5%	Various	
R35	150 kΩ	Thermistor, NTC, 0402, 5%	Panasonic	ERTJOEV154J
U3, U4	1:1	Transformer, 50 – 1200 MHz	M/A-COM	MABA-009210-CT1760
U5	NPN	Trans, dual NPN, SOT363	Various	

Typical Performance – TAT2814A1L-EB

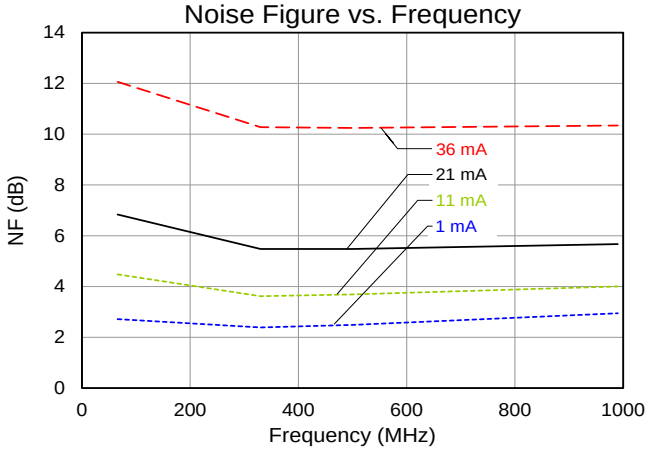
Gain vs. Frequency



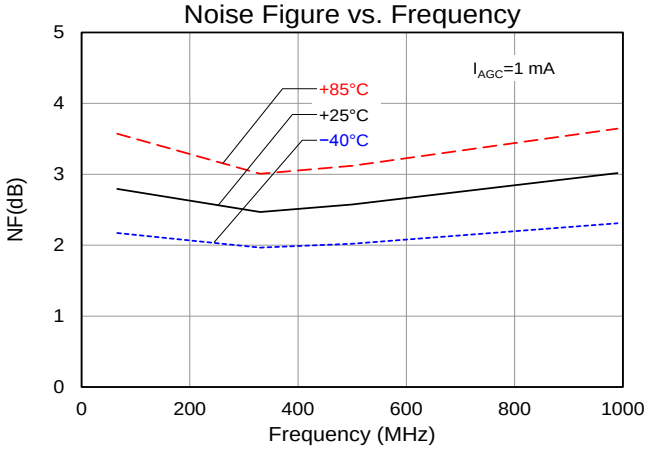
Gain vs. AGC Current



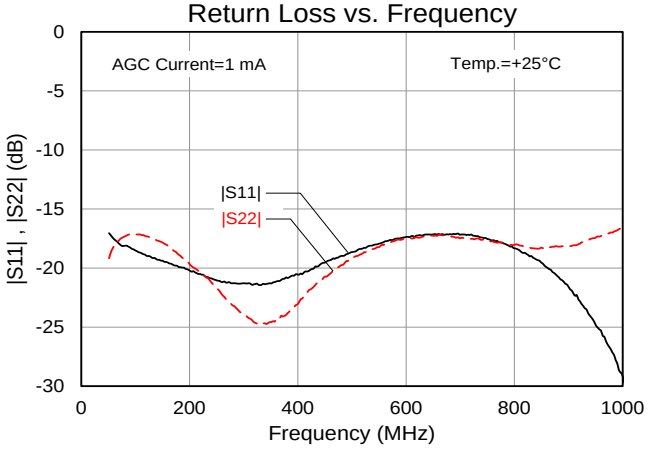
Noise Figure vs. Frequency



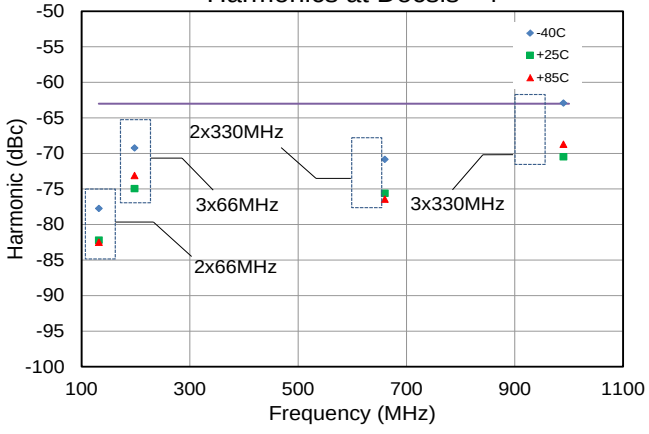
Noise Figure vs. Frequency



Return Loss vs. Frequency

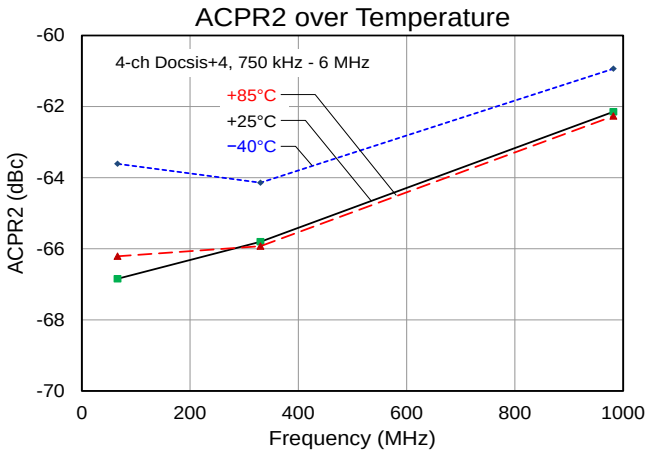


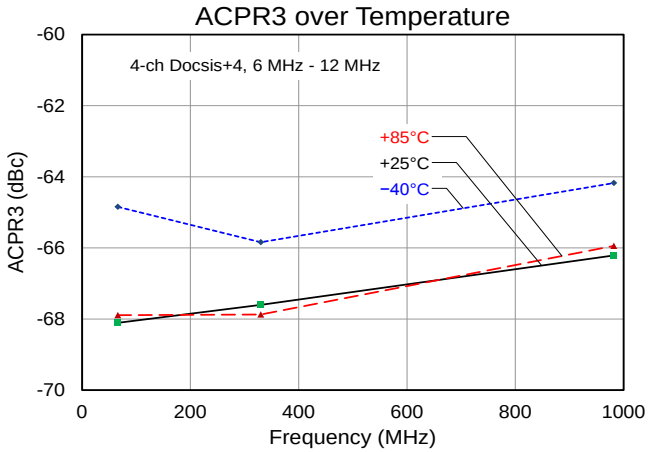
Harmonics at Docsis +4

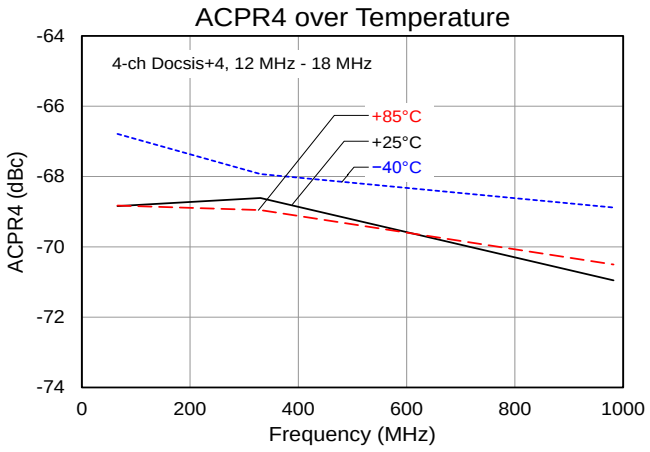


Typical Performance – TAT2814A1L-EB

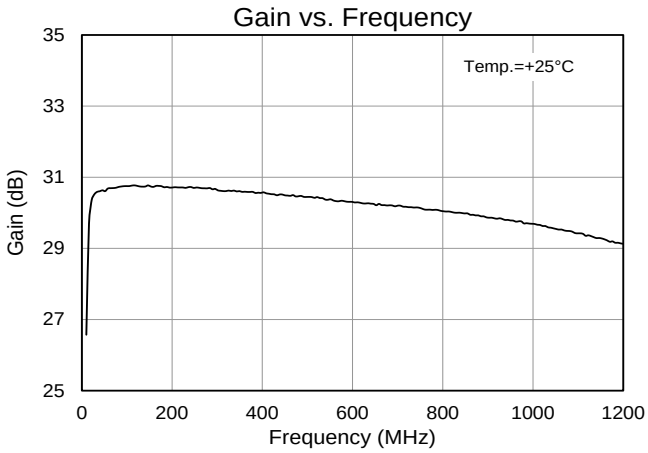
Measurements at 990 MHz taken using a high pass filter to minimize contributions from the source

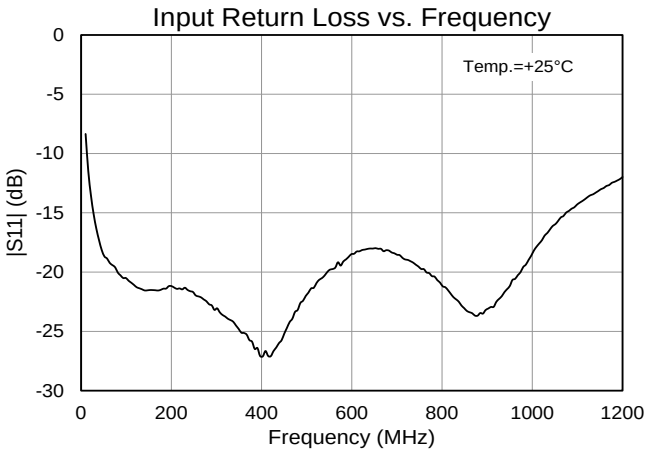


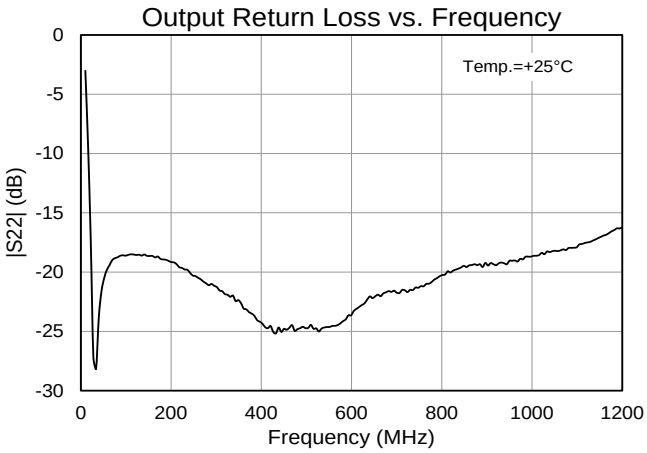


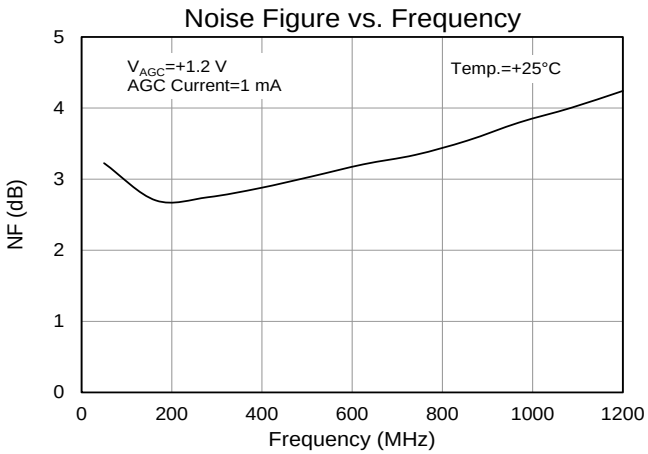


1200 MHz Performance – TAT2814A1L-EB









Detailed Device Description

Balance
The TAT2814A1L is designed for excellent differential-mode performance throughout the chain. Unlike many commercially available push-pull amplifiers built with 2 discrete die, both stages of the TAT2814A1L are single-chip designs utilizing a differential pair topology for best common-mode performance. Provision is made for using external bias inductors to increase tail impedances in the input differential pairs, improving further the signal balance and 2nd order performance through the chain. The RF output of the first stage is connected internally to the differential attenuator and brought out to external pins for applying stage bias and enabling RF feedback to the input. The attenuator outputs are brought out to a single side of the TAT2814A1L for customers desiring to perform inter-stage filtering or signal processing. The differential inputs to the output stage are located on an adjacent side of the die, spaced to minimize package coupling so as to not limit the performance of off-stage filtering.

Input Matching
The input stage uses external feedback to achieve 75 Ω differential input impedance. The bias current of the input stage may be adjusted with an external resistor to ground.

Pre-Amp Powerdown
The preamp stage of the TAT2814A1L can be powered down by setting PD pin to Logic LOW. V_{DD} pins should be set to 5 V in both power-down and operating modes.

Gain Adjustment
A fully differential gain control function is implemented with a low distortion analog diode-based attenuator. The attenuator provides for monotonic gain adjustment over a full 18 dB attenuation range. The excellent RF match characteristics ensure excellent gain flatness and return loss over the full attenuation range. Control is provided by a single current controlled line. Attenuation is monotonic and linear with control current.

Output Stage
A differential output stage has excellent output linearity performance at very low power. The differential outputs of the second stage may be combined with a commercially available balun to provide for single-ended drive signals. The bias current of the output stage may be placed in active bias control. This is implemented by sensing the voltage at pin 19 and providing a feedback voltage bias to pin 27. Please contact TriQuint for further details.

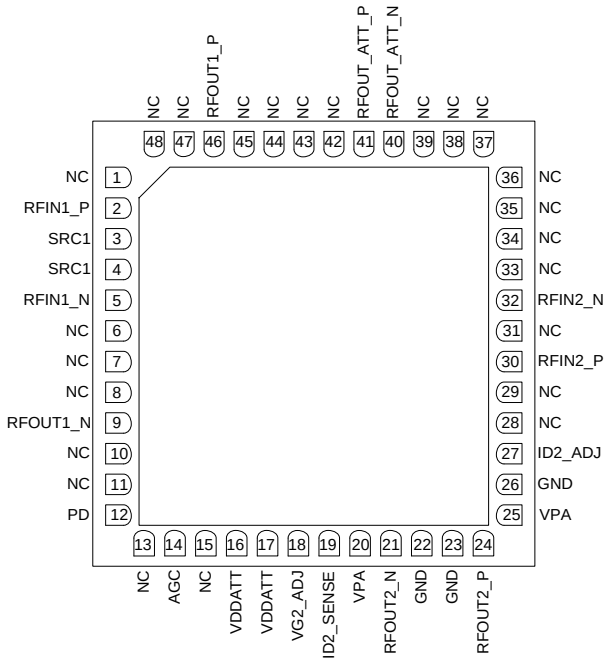
Thermal Management
Total maximum power consumption of the TAT2814A1L is 5.25 Watts. Care must be taken in the layout to provide adequate thermal path with multiple vias under the TAT2814A1L. A heat sink should also be used to carry heat away from the backside PCB. See section on Mechanical Information for recommended mounting pattern for the part.

Technology
The TAT2814A1L utilizes proven pHEMT device technology that has yielded over 200 million RFICs to date. For detailed qualification and reliability reports on other products fabricated in this process, please consult TriQuint. Key RFICs that will be used in the TAT2814A1L have already exceeded industry qualification requirements in other packages.

Bias Current Set
Bias current to each amplification stage is set by external circuitry to allow trade-off of power consumption and distortion performance.

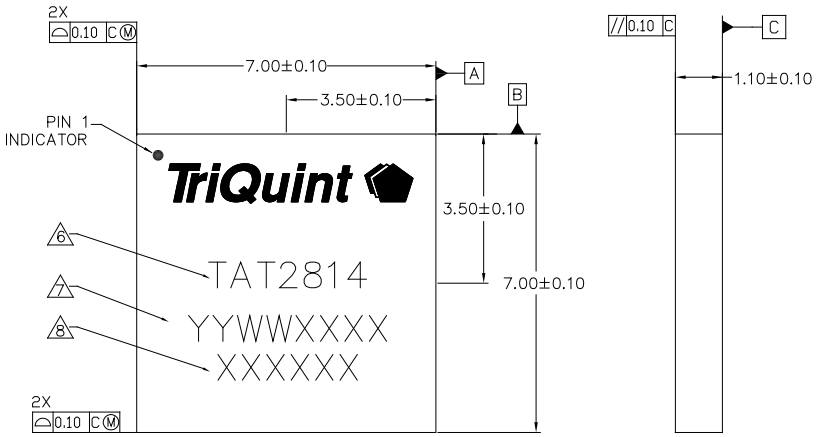
Separate Bias Voltage for each stage
Preamplifier, interstage attenuator, and driver amplifier have independent voltage supply pins.

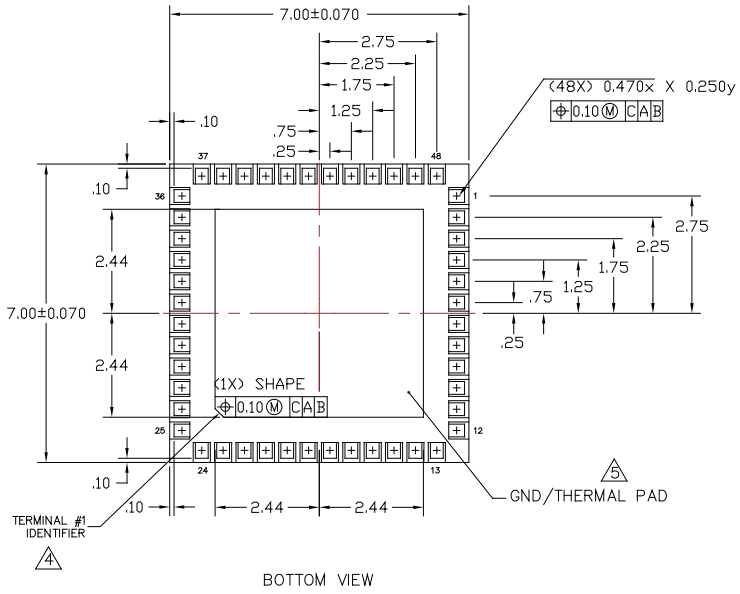
Pin Configuration and Description



Pin No.	Label	Description
1, 6 – 8, 10, 11, 13, 15, 28, 29, 31, 33 – 39, 42 – 45, 47, 48	NC	No Connect
2	RFIN1_P	PreAmp RF Input, Positive
3, 4	SRC1	PreAmp RF Source
5	RFIN1_N	PreAmp RF Input, Negative
9	RFOUT1_N	PreAmp RF Output, Negative
12	PD	Power Down Control
14	AGC	Current Based Attenuator Control
16, 17	VDDATT	Attenuator Bias
18	VG2_ADJ	Power Amplifier VG2 Bias Adjust
19	ID2_SENSE	Power Amplifier Current Sense
20, 25	VPA	Power Amplifier Supply
21	RFOUT2_N	Power Amplifier RF Output, Negative
22, 23, 26	GND	Ground Pin
24	RFOUT2_P	Power Amplifier RF Output, Positive
27	ID2_ADJ	Power Amplifier Bias Current Adjust (Optional)
30	RFIN2_P	Power Amplifier RF Input, Positive
32	RFIN2_N	Power Amplifier RF Input, Negative
40	RFOUT_ATT_N	Attenuator RF Output, Negative
41	RFOUT_ATT_P	Attenuator RF Output, Positive
46	RFOUT1_P	PreAmp RF Output, Positive
Backside Pad	GND	Backside Ground Slug

Package Marking and Dimensions





This package is lead-free/RoHS-compliant. The plating material on the leads is 100 % Matte Tin. It is compatible with both lead-free (maximum 260 °C reflow temperature) and lead (maximum 245 °C reflow temperature) soldering processes.

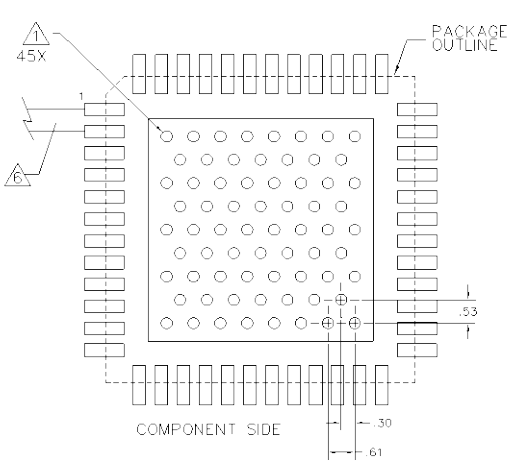
The TAT2814A will be marked with a “TAT2814A” designator and an 8 digit alphanumeric lot code (YYWWCCCC). The first four digits are a date code consisting of the year and work week (YYWW) of assembly. The last four digits are the lot code (XXXX).

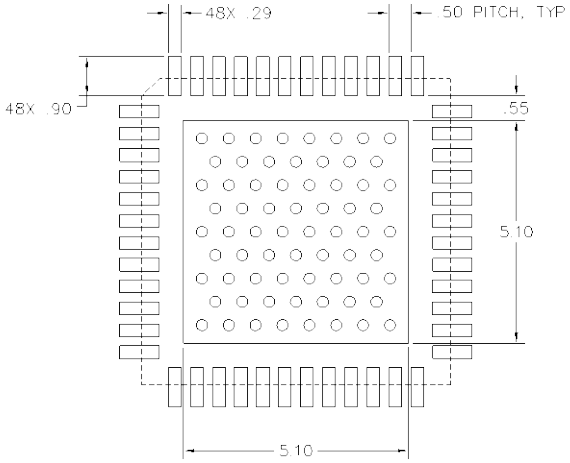
NOTES:

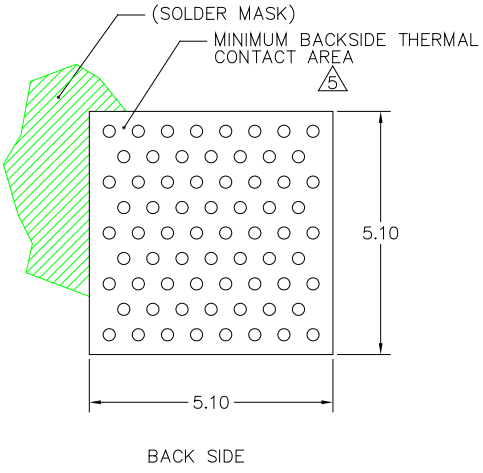
1. EXCEPT WHERE NOTED, THIS PART OUTLINE CONFORMS TO JEDEC STANDARD MO–220, ISSUE E (VARIATION VJJC) FOR THERMALLY ENHANCED PLASTIC VERY THIN FINE PITCH QUAD FLAT NO LEAD PACKAGE (QFN).
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.4M–1994.
3. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.

4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION CONFORM TO JESD 95–1 SPP–012.
5. COPLANARITY APPLIES TO THE EXPOSED GROUND/THERMAL PAD AS WELL AS THE TERMINALS.
6. PRODUCT CODE.
7. ALPHA–NUMERIC LOT CODE.
8. VENDOR CODE AND TRIQUINT LOT NUMBER

PCB Mounting Pattern







BACK SIDE

NOTES:

1. GROUND/THERMAL VIAS ARE CRITICAL FOR THE PROPER PERFORMANCE OF THIS DEVICE. VIAS SHOULD USE A .35mm (#80/.0135") DIAMETER DRILL AND HAVE A FINAL, PLATED THRU DIAMETER OF .25mm (.010").
2. ADD AS MUCH COPPER AS POSSIBLE TO INNER AND OUTER LAYERS NEAR THE PART TO ENSURE OPTIMAL THERMAL PERFORMANCE.
3. TO ENSURE RELIABLE OPERATION, DEVICE GROUND PADDLE–TO–GROUND PAD SOLDER JOINT IS CRITICAL.
4. ADD MOUNTING SCREWS NEAR THE PART TO FASTEN THE BOARD TO A HEATSINK. ENSURE THAT THE GROUND/THERMAL VIA REGION CONTACTS THE HEATSINK.
5. DO NOT PUT SOLDER MASK ON THE BACK SIDE OF THE PC BOARD IN THE REGION WHERE THE BOARD CONTACTS THE HEATSINK.
6. RF TRACE WIDTH DEPENDS UPON THE PC BOARD MATERIAL AND CONSTRUCTION.
7. USE 1 OZ. COPPER MINIMUM.
8. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.

Product Compliance Information

ESD Sensitivity Ratings

Caution! ESD-Sensitive Device

ESD Rating: Class 1A
Value: ≥ 250 V to < 500 V
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

ESD Rating: Class C2
Value: ≥ 500 V to < 1000 V
Test: Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101

MSL Rating

MSL Rating: Level 3
Test: 260°C convection reflow
Standard: JEDEC Standard IPC/JEDEC J-STD-020

Solderability

Compatible with J-STD-020, Lead free solder, (260° maximum reflow temperature) and tin/lead (245°C maximum reflow temperature) soldering processes.

Contact plating: NiPdAu

RoHs Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

Web: **www.triquint.com** **Tel:** **+1.503.615.9000**
Email: **info-sales@triquint.com** **Fax:** **+1.503.615.8902**

For technical questions and application information:

Email: **sjcapplications.engineering@triquint.com**

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