AN4213
Application note

High-frequency ballast 2x58 W (T8 fluorescent tubes) based on a PowerFLAT™ 5x6 package

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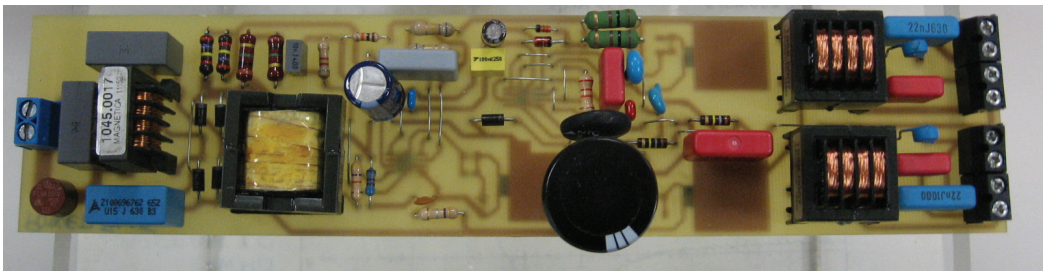
Introduction

Fluorescent lamps are increasingly driven by electronic rather than electromagnetic ballasts mainly because fluorescent lamps can produce around 20% more light for the same input power when driven above 20 kHz instead of 50/60 Hz. Operation at high frequency also eliminates both light flickering and audible noise.

This application note describes the design calculations and test results of the STEVAL-ILB010V1demonstration board able to drive 2x58 W linear T8 fluorescent tubes. The electronic ballast consists of two sections: a power factor correction pre-regulator (PFC), using the L6562A, and the lamp ballast stage with the L6569. The main purpose of this application note is to evaluate the electrical features of the new PowerFLAT™ 5x6 package and to compare its thermal results with that of the DPAK package. The PowerFLAT™5x6 package is used in the STEVAL-ILB010V1 demonstration board shown below.

Figure 1. STEVAL-ILB010V1



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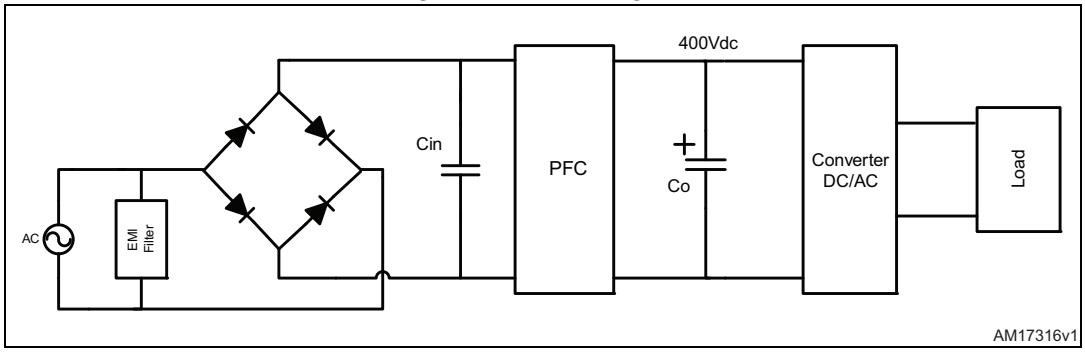


The electronic ballast consists of two sections: a power factor correction pre-regulator (PFC), using the L6562A, and the lamp ballast stage with the L6569.

The power factor correction section is based on the L6562A. This is a current-mode PFC controller operating in transition mode (TM). It is especially designed for electronic lamp ballast applications (to better understand the L6562A characteristics, refer to AN2761).

The lamp ballast stage is based on the L6569 which is a high-voltage half-bridge driver with a built-in oscillator. The load consists of an L-C series resonant circuit with the lamps connected across the capacitors. This topology allows operating in zero-voltage switching, to reduce the transistor switching losses and the electromagnetic interference generated by the output wiring of the lamp.

2 PFC section

The power factor correction circuit reshapes the distorted input current waveform to approximate a sinusoidal current that is in phase with the input voltage. It is an index which measures the efficiency of the energy transfer from an AC source to a generic load.

The input power factor (PF) is defined as the ratio of the real power (transferred to the output) over apparent power (see *Equation 1*).

Equation 1

$$PF = \frac{\mathrm{Re}alPower}{ApparentPower} = \frac{I_{rms}V_{rms}\cos\phi}{I_{rms}V_{rms}} * \frac{I_{rms_1}}{I_{rms_T}} = K_d \cos\phi$$

where:

$$K_d = \frac{I_{rms1}}{I_{rms}}$$

is a distortion factor and cos∅ is the phase angle between input ac voltage and the fundamental current.

Two typical techniques used to achieve a sinusoidal input current waveform with low distortion are passive correction and active correction. Passive PFC techniques shape the input current waveform by using a passive input filter consisting of inductors and capacitors. Because it operates at the line frequency, 50 or 60 Hz passive filters require relatively large fixed-value inductors and capacitors to reduce the low-frequency harmonic currents. It is difficult to achieve near unity power factor with passive filters. Also, very large currents may circulate in the filter. However the passive filter is an effective PFC solution where the line frequency line voltage and load are relatively constant.

An active PFC performs very well and is significantly smaller and lighter than the passive PFC circuit. The active PFC circuits operate at a higher switching frequency than the line frequency to allow a large reduction in the size and cost of passive filter elements.

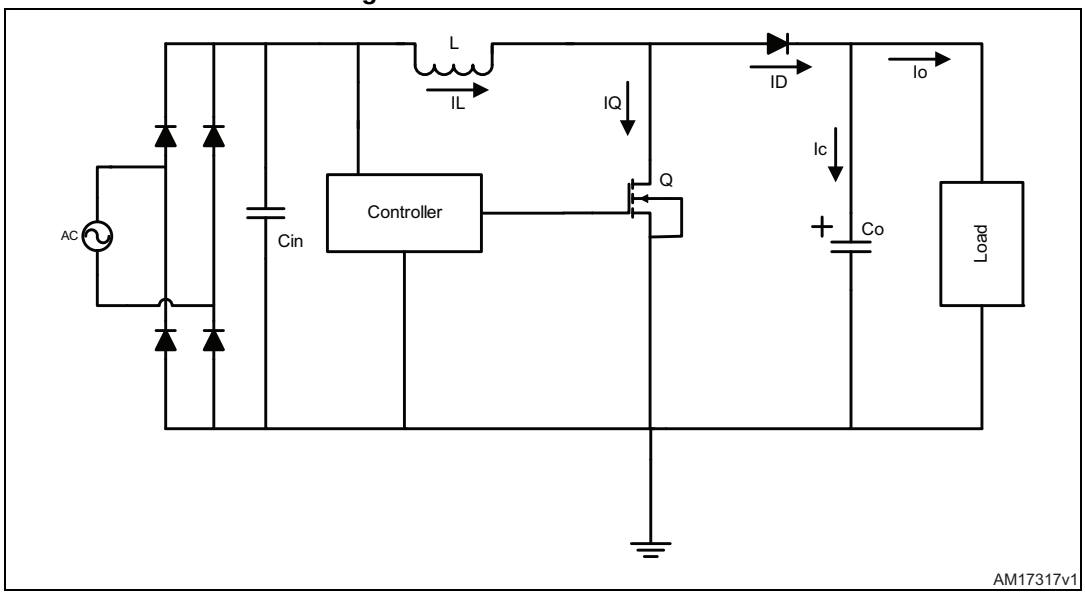
A typical active PFC circuit using switching techniques, located between the rectifier bridge and the filter capacitor, allows drawing a quasi-sinusoidal current from the mains, in phase with the line voltage.

The boost circuit-based PFC topology is the most popular. The boost PFC circuit is a cheap solution to comply with the regulations. It can be implemented with a boost inductor, a controlled power switch, a catch diode, an output capacitor and, obviously, a control circuitry. (See *Figure 3*).

The boost inductor in the boost PFC circuit is in series with the AC power line. Therefore the input current does not pulsate, minimizing conducted EMI at the line. This allows the size of the EMI filter and the conductors in the input circuit to be reduced. This topology accepts a wide input voltage range without an input voltage selector switch.

The output voltage of a boost PFC circuit should be higher than the peak value of the maximum input voltage.

Figure 3. Boost converter circuit



The boost converter can operate in two modes: discontinuous conduction mode (DCM) and continuous conduction mode (CCM).

Discontinuous conduction mode is when the Power MOSFET of the boost converter is turned on when the inductor current reaches zero after a dead time and turned off when the inductor current meets the input reference voltage. In this way, the input current waveform follows the input voltage one, therefore obtaining a power factor close to 1. DCM is suitable for power levels of 300 W or less. DCM uses larger cores and has higher I^2R and skin-effect losses due to the larger inductor current swing. With the increased swing a larger input filter is also required. On the positive side, since in the discontinuous mode the Power MOSFET switches on when the inductor current is at zero, there is no reverse-recovery current (IRR) specification required on the boost diode. This means that less expensive diodes can be used.

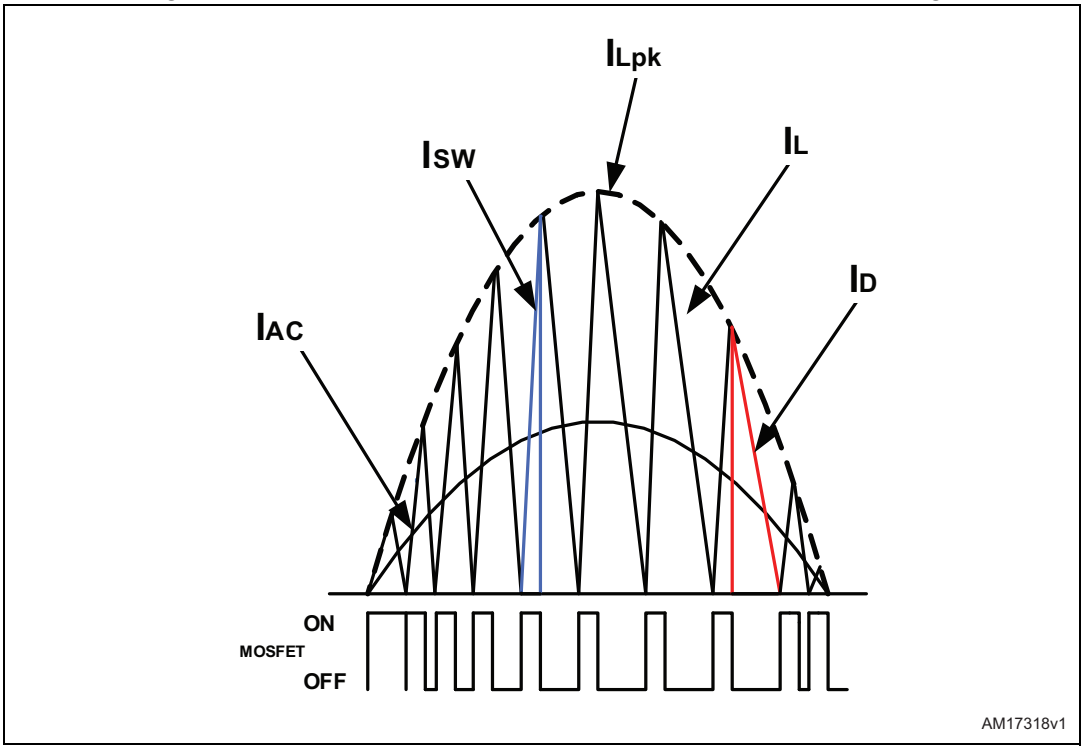
Continuous conduction mode (CCM) is when the current in the energy transfer inductor never reaches zero during the switching cycle. The Power MOSFET starts conducting when the current through itself is not zero. Continuous conduction mode (CCM) is suitable for high power ratings (>300 W). The voltage swing is less than in DCM resulting in lower I^2R losses and the lower ripple current results in lower inductor core losses. Less voltage swing also reduces EMI and allows for a smaller input filter to be used. Unfortunately, since the Power MOSFET is not being turned on when the current of the inductor is at zero, a very fast reverse-recovery diode is required to keep losses to a minimum.

Transition conduction mode which is typically used in lighting applications represents a good cost-benefit compromise. In the transition mode approach, the switch-on time is held constant during the line cycle and the switch is turned on when the inductor current falls to zero, so that the converter operates at the boundary between continuous and discontinuous conduction mode. In this way, the freewheeling diode is turned off softly (no recovery losses) and the switch is turned on at zero current, so the commutation losses are reduced. Besides the simplicity and the few external parts required, this system minimizes the inductor size due to the low inductance value needed. On the other hand, the high current ripple on the inductor involves high RMS current and high noise on the rectified main bus, which needs a heavier EMI filter to be rejected. These drawbacks limit the use of the TM PFC in a lower power range (typically below 200 W).

The principle scheme is shown in *Figure 4*. The instantaneous input current is constituted by a sequence of triangles whose peaks are proportional to the line voltage. Thus, the average input current becomes proportional to the line voltage without duty-cycle modulation during the line cycle.

In this application note boost topology working in transition mode is considered.

Figure 4. Inductor current waveform and Power MOSFET timing



3 Designing a TM PFC

3.1 Input specification

The first consideration for designing a new boost PFC converter is a detailed specification of the operating conditions of the circuit that is needed for the calculation.

In this example a 116 W, single-input range mains PFC circuit has been considered.

Table 1. Specified parameters

Converter specification data and fixed parameters		
Symbol	**Description**	**Values**
$V_{AC(min)}$	Mains voltage range	185 V_{AC}
$V_{AC(max)}$		265 V_{AC}
fl	Minimum mains frequency	47 Hz
P_{OUT}	Rated output power	116 W
V_{OUT}	Regulated DC output voltage	400 V
$\eta=P_{OUT}/P_{IN}$	Expected efficiency	90%
PF	Expected power factor	0.99

The L6562A integrates an OVP in order to prevent excessive output voltage that can overstress the output components and the load.

- Maximum output overvoltage:

$$\Delta V_{OVP} = 40V$$

The PFC minimum switching frequency is one of the main parameters used to dimension the boost inductor. The switching frequency at low mains on the top of the sinusoid and at full load conditions has been considered. It must be higher than the audio bandwidth in order to avoid audible noise and it must not interfere with the L6562A minimum internal starter period. On the other hand, if the minimum frequency is set too high, the circuit shows excessive losses at a higher input voltage. The typical minimum frequency range is 20 - 50 kHz.

- Minimum switching frequency (kHz):

$$f_{SW\,\min} = 35kHz$$

In order to properly select the power components of the PFC, the maximum operating ambient temperature around the PFC circuitry must be known. The designer must take into consideration that it is the temperature at which the PFC components are working and not the maximum external operating temperature of the entire equipment.

- Maximum ambient temperature (°C):

$$T_{ambx} = 50°C$$

3.2 Operating conditions

The first step is to define the main parameters of the circuit as follows:

- Rated DC output current:

Equation 2

$$I_{OUT} = \frac{P_{OUT}}{V_{OUT}} = \frac{116}{400} = 0.29A$$

- Maximum input power:

Equation 3

$$P_{IN} = \frac{P_{OUT}}{\eta} = \frac{116}{0.9} = 129W$$

- RMS input current:

Equation 4

$$I_{IN} = \frac{P_{IN}}{V_{AC\,\min} * PF} = \frac{129}{185 * 0.99} = 0.7A$$

- Peak inductor current:

Equation 5

$$I_{Lpk} = 2\sqrt{2} * I_{IN} = 1.97A$$

- RMS inductor current:

Equation 6

$$I_{LRMS} = \frac{2}{\sqrt{3}} * I_{IN} = 0.8A$$

- AC inductor current:

Equation 7

$$I_{LAC} = \sqrt{I_{LRMS}^2 - I_{IN}^2} = 0.38A$$

The current flowing into the inductor can be divided in two parts depending on the instant of conduction. During the on time, it increases from zero up to its peak value and flows in the switch, otherwise during the off time the current decreases from its peak down to zero and it flows into the diode. Therefore, in order to calculate the losses of these two elements, it is useful to know the RMS current which flows into the switch and into the diode.

- RMS switch current:

Equation 8

$$I_{SWRMS} = I_{Lpk}\sqrt{\frac{1}{6} - \frac{4\sqrt{2}}{9\pi} * \frac{V_{AC\,\min}}{V_{OUT}}} = 0.51A$$

- RMS diode current:

Equation 9

$$I_{DRMS} = I_{Lpk}\sqrt{\frac{4\sqrt{2}}{9\pi} * \frac{V_{AC\min}}{V_{OUT}}} = 0.59A$$

3.3 Power section design

3.3.1 Bridge rectifier

The input rectifier bridge can use standard, slow-recovery, low-cost devices. Typically a 600 V device is selected in order to have a good margin against mains surges.

Equation 10

$$\overline{I_{INRMS}} = \frac{\sqrt{2} * I_{IN}}{2} = 0.49A$$

Equation 11

$$\overline{I_{IN-avg}} = \frac{\sqrt{2} * I_{IN}}{\pi} = 0.31A$$

The power dissipated on the bridge is calculated using *Equation 12*:

Equation 12

$$P_{BRIDGE} = 4 * R_{DIODE} * \overline{I_{INRMS}^2} + 4 * V_{TH} * \overline{I_{IN-avg}}$$

where R_{DIODE} and V_{th} are given in the technical datasheet.

3.3.2 Input capacitor

The input capacitor has to attenuate the switching noise due to the high-frequency inductor current ripple. The worst condition happens on the peak of the minimum rated input voltage (V_{INmin}=185 V).

The maximum high-frequency voltage ripple across C_{IN} is usually imposed between 5% and 20% of the minimum rated input voltage.

This is expressed by a coefficient r (from 0.05 to 0.2) as an input design parameter.

- Ripple voltage coefficient (%):

r = 0.2

Taking into account a minimum half-bridge switching frequency of 35 kHz and an output power of 116 W, the input capacitor can be determined by the following equation.

Equation 13

$$C_{IN} = \frac{I_{IN}}{2\pi * f_{SW\min} * r * V_{AC\min}} \qquad C_{IN} = \frac{0.7}{2 * 3.14 * 35 * 0.2 * 185} = 0.086\mu F$$

C_{IN} has been selected equal to 150 nF.

Of course a bigger capacitor provides a benefit in terms of EMI, but on the other hand worsens the THD, mainly at high mains voltage. For this reason the right trade-off is needed in order to have the best performance. A good quality film capacitor must be selected in order to provide good filtering effectiveness.

3.3.3 Output capacitor

The selection of the output bulk capacitor C_{OUT} depends on the DC output voltage, the allowable overvoltage and the converter output power. With these values, the output capacitor can be calculated using the following equation:

Equation 14

$$C_{OUT} \geq \frac{P_{OUT}}{4\pi f_{main} * V_{OUT} * \Delta V_{OUT}} = \frac{116}{4\pi * 47 * 400 * 10} \geq 49\mu F$$

To obtain the smallest possible ripple and good reliability, a commercial capacitor of 56μF, 450 V has been selected.

3.3.4 Boost inductor

In the transition mode control, the inductor value needs to be calculated to start the next switching cycle at zero current. The boost inductor determines the operating frequency of the converter. First, the inductance value must be defined. The inductance (L) is usually determined so that the minimum switching frequency is greater than the maximum frequency of the L6562A internal starter, in order to ensure correct TM operation.

Assuming unity PF, it is possible to write:

Equation 15

$$t_{on}(V_{AC}, \vartheta) = \frac{L * I_{Lpk} * \sin\vartheta}{\sqrt{2} * V_{AC} * \sin\vartheta} = \frac{L * I_{Lpk}}{\sqrt{2} * V_{AC}}$$

Equation 16

$$t_{off}(V_{AC}, \vartheta) = \frac{L * I_{Lpk} * \sin\vartheta}{V_{OUT} - \sqrt{2} * V_{AC} * \sin\vartheta}$$

T_{on} and T_{off} are, respectively, the ON-time and the OFF-time of the Power MOSFET, I_{Lpk} is the maximum peak inductor current in a line cycle and θ is the instantaneous line phase in the interval (0, π).

The instantaneous switching frequency in a line cycle is given by *Equation 17*:

Equation 17

$$f_{SW}(V_{AC}, \vartheta) = \frac{1}{t_{on} + t_{off}} = \frac{1}{2L * P_{IN}} * \frac{V_{AC}^2 * \left(V_{OUT} - \sqrt{2} * V_{AC} * \sin\vartheta\right)}{V_{OUT}}$$

The switching frequency is minimum at the top of the sinusoid

$$\left(\vartheta = \frac{\pi}{2} \Rightarrow \sin\vartheta = 1\right)$$

and it is maximum at the zero-crossing of the line voltage (ϑ=0,π = sinϑ=0) where t_{off} = 0 μs.

The absolute minimum frequency f_{SWmin} can occur at either the maximum V_{ACmax} or the minimum mains voltage V_{ACmin}, so the inductor value is calculated by the formula:

Equation 18

$$L(V_{AC}) = \frac{V_{AC}^2 * \left(V_{OUT} - \sqrt{2} * V_{AC}\right)}{2}$$

where V_{AC} can be either V_{ACmin} or V_{ACmax}, whichever gives the lower value for L.

The values of the inductor at low mains and at high mains, respectively $L(V_{ACmax})$ and $L(V_{ACmin})$ are given by following equations:

Equation 19

$$L(V_{AC\,max}) = \frac{V_{AC\,min}^2 * \left(V_{OUT} - \sqrt{2} * V_{AC\,min}\right)}{2 * f_{SW\,min} * P_{IN} * V_{OUT}} \Rightarrow L(V_{AC\,max}) = \frac{185^2 * \left(400 - \sqrt{2} * 185\right)}{2 * 35 * 10^3 * 129 * 400} = 1.36mH$$

Equation 20

$$L(V_{AC\,min}) = \frac{V_{AC\,max}^2 * \left(V_{OUT} - \sqrt{2} * V_{AC\,max}\right)}{2 * f_{SW\,min} * P_{IN} * V_{OUT}} \Rightarrow L(V_{AC\,max}) = \frac{265^2 * \left(400 - \sqrt{2} * 265\right)}{2 * 35 * 10^3 * 129 * 400} = 0.51mH$$

At this point the minimum value has to be taken into account. It becomes the maximum inductance value for PFC dimensioning.

For this application a 0.5 mH boost inductance has been selected.

3.3.5 Power MOSFET selection

The main switch selection is driven by the amount of allowable power dissipation. It is important to choose a device that minimizes gate charge and capacitance and minimizes the sum of switching and conduction losses at a given frequency.

The breakdown voltage is fixed just by the output voltage, plus the allowable overvoltage and a safety margin.

The conduction losses are given by:

Equation 21

$$P_{COND} = R_{DSon} * \left(I_{SWrms}(V_{AC})\right)^2$$

where, as given in *Equation 8*:

$$I_{SWrms} = I_{Lpk}\sqrt{\frac{1}{6} - \frac{4\sqrt{2}}{9\pi} * \frac{V_{AC\min}}{V_{OUT}}}$$

The switching losses in the Power MOSFET occur only at turn-off because of TM operation and can be expressed by:

Equation 22

$$P_{switch}(V_{AC}) = \frac{Q_{gd} * V_{OUT} * I_{Lrms}}{2I_g} f_{SW}(I_{Lrms})$$

This equation represents the crossing between the Power MOSFET current that decreases linearly during the fall time and the voltage on the Power MOSFET drain that increases. In fact during the fall time the current of the boost inductor flows into the parasitic capacitance of the Power MOSFET, charging it. For this reason switching losses depend on the total drain capacitance.

At turn-on the losses are due to the discharge of the total drain capacitance inside the Power MOSFET itself.

The capacitive losses are given by:

Equation 23

$$P_{CAP}(V_{AC}) = \frac{1}{2} C_d * V_{MOS}^2 * f_{SW}(V_{AC})$$

Where C_d is the total drain capacitance and V_{MOS} is the drain voltage at Power MOSFET turn-on.

Based on the above considerations, the Power MOSFET device selected is the STL13N60M2. This device is an N-channel Power MOSFET developed using a new generation of MDmesh II Plus™ low Q_g. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. This choice is confirmed by the good electrical performance and thermal behavior.

3.3.6 Boost diode selection

A fast-recovery boost diode is used. The value of its DC and RMS current (see *Equation 9*), useful for the calculation of the losses, are both:

Equation 24

$$I_D = I_{OUT} = 0.29A$$

The conduction losses can be estimated as follows:

Equation 25

$$P_{DON} = V_{th} * I_D + R_d * I_{DRMS}^2$$

Where, V_{th} (threshold voltage) and R_d (differential resistance) are parameters of the diode.

The breakdown voltage is fixed by the same criterion as the Power MOSFET. A minimum breakdown voltage of 1.2*(V_{OUT} - ΔV_{OVP}) and a current rating higher than 3*I_{OUT}, can be chosen for a rough initial selection of the rectifier.

In this 116 W application an STTH1L06 (600 V, 1 A) has been selected.

From the STTH1L06 datasheet, V_{th} is 0.89V and R_d is 0.165 Ω, therefore substituting these values in *Equation 25*, we have:

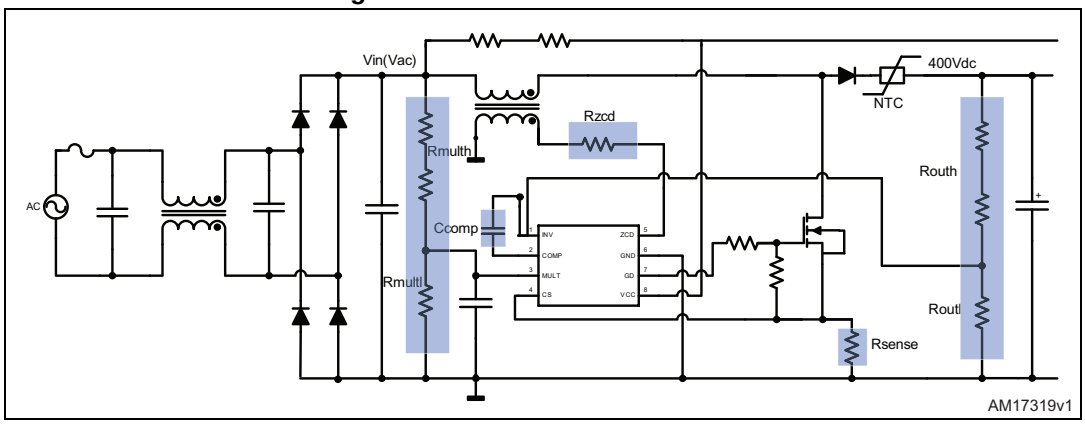
$$P_{DON} = 0.89V * 0.29A + 0.165\Omega * (0.59A)^2 = 0.315W$$

3.4 L6562A biasing circuitry (pin by pin)

This section explains the dimensioning of the biasing circuitry pin-by-pin.

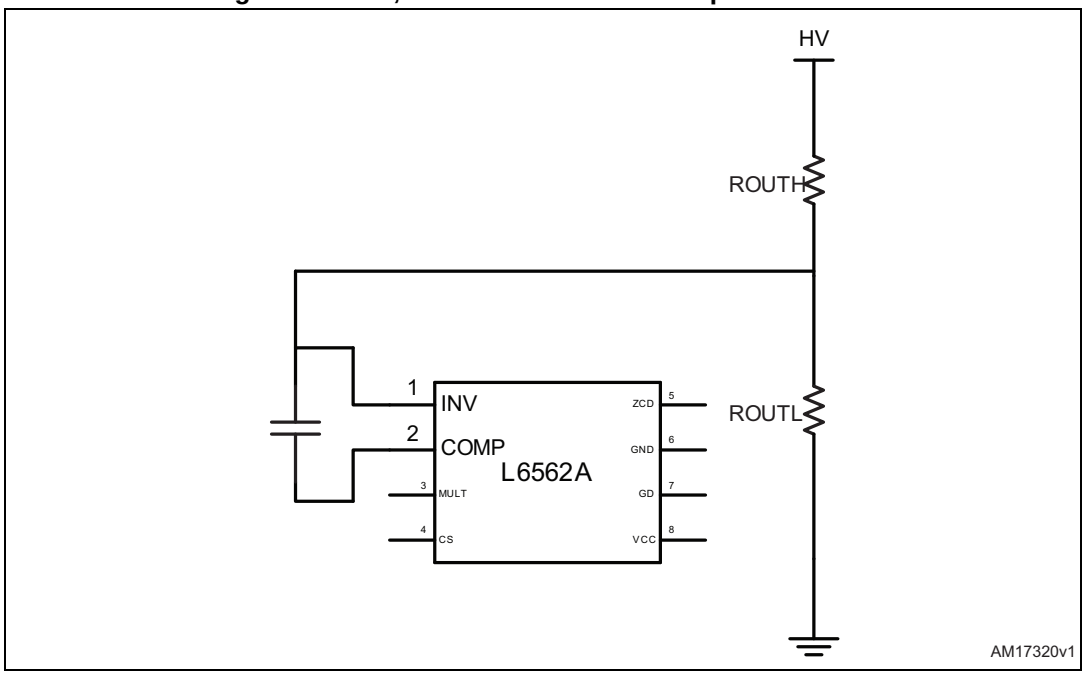
For reference, the relevant components have been highlighted in the figure below.

Figure 5. PFC electrical schematic



Pin 1, 2: feedback network implementation

Figure 6. Pin 1, 2: Feedback network implementation



Pin 1 (INV): Inverting input of the error amplifier. The information on the output voltage of the PFC pre-regulator is fed into this pin through a resistor divider (R_{OUTH} and R_{OUTL}). The internal reference on the non-inverting input is 2.5 V (typ), while the DIS intervention threshold is 27 μA. R_{OUTH} and R_{OUTL} are then selected as follows:

Equation 26

$$R_{OUTH} = \frac{\Delta V_{OVP}}{27\mu A} = 1480k\Omega$$

Equation 27

$$\frac{R_{OUTH}}{R_{OUTL}} = \frac{V_{OUT}}{2.5V} - 1 = 159 \Rightarrow R_{OUTL} = \frac{R_{OUTH}}{159} = 9.3k\Omega$$

The commercial selected values are two resistors in series each 680 kΩ for R_{OUTH} and R_{OUTL} equal to 8.2 kΩ.

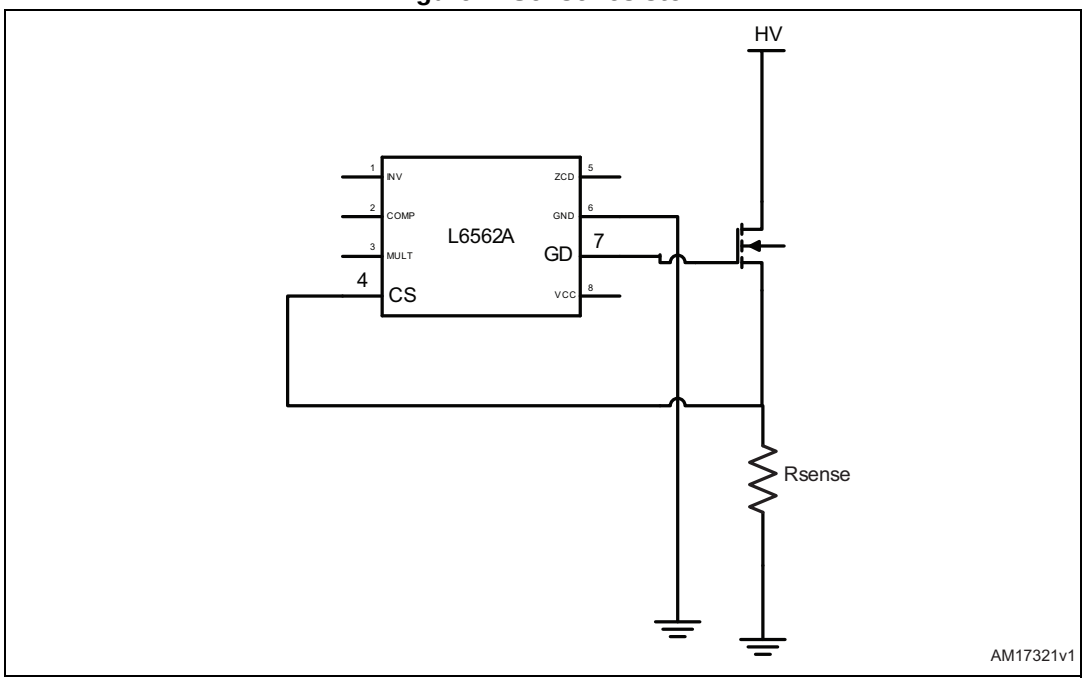
Pin 2 (COMP): Output of the error amplifier. A compensation network is placed between this pin and INV (pin 1) in order to achieve stability of the voltage control loop and ensure high power factor and low THD. It has to be designed with a narrow bandwidth in order to avoid that the system rejects the output voltage ripple that would bring high distortion of the input current waveform. Setting a bandwidth (BW) from 20 to 30 Hz, C_{COMP} (as shown in *Figure 6*) can be calculated as follows:

Equation 28

$$C_{COMP} = \frac{1}{2\pi\left(R_{OUTH} IIR_{OUTL}\right) * BW} \cong 1\mu F$$

Pin 4 (CS): input to the PWM comparator

Figure 7. Sense resistor



The current flowing in the Power MOSFET is sensed through a resistor, the resulting voltage is applied to this pin and compared with an internal sinusoidal-shaped reference, generated by the multiplier, to determine Power MOSFET turn-off. The Power MOSFET stays in the OFF-state until the PWM latch is reset by the ZCD signal.

The sense resistor value can be calculated as follows:

Equation 29

$$R_S \leq \frac{V_{CS\,\min}}{I_{Lpk}} \leq 0.502\Omega$$

Where:

- I_{Lpk} is the maximum peak current in the inductor, equal to 1.99 A
- V_{CSmin} = 1 V is the minimum voltage allowed on the L6562A current sense (given in the datasheet).

For this project the selected commercial value for R_S is 0.47Ω.

Using this value and considering the maximum voltage V_{CSmax} = 1.16 V allowed on the L6562A (as given in the datasheet), the maximum peak of the inductor current can be calculated as follows:

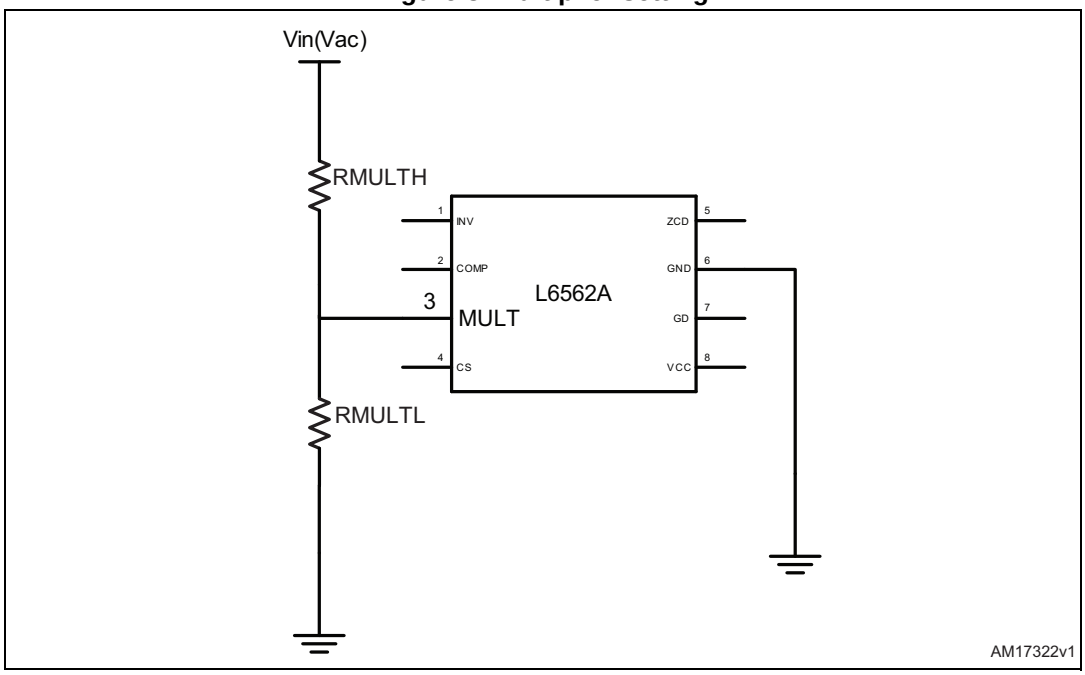
Equation 30

$$I_{Lpkx} = \frac{V_{CS\,\max}}{R_S} = 2.5A$$

The calculated I_{Lpkx} is the saturation inductor current and it is used for calculating the winding number of the inductor and its air gap.

Pin 3 (MULT): main input to the multiplier.

Figure 8. Multiplier setting



This pin is connected to the rectified mains voltage via a resistor divider and provides the sinusoidal reference to the current loop.

The multiplier can be described by the relationship:

Equation 31

$$V_{CS} = K(V_{COMP} - 2.5V) * V_{MULT}$$

Where:

- V_{CS} (multiplier output) is the reference for the current sense
- K = 0.38 (typ) is the multiplier gain
- V_{COMP} is the voltage on pin 2
- V_{MULT} is the voltage on pin 3

First, the maximum peak value for V_{MULT}max is selected. This value has to be selected in the range from 0 up to 3 V. Typically, it should be less than 3 V in case of single mains

Equation 32

$$V_{MULTpk\,\max} = \frac{I_{Lpk} * R_S}{1.1} * \frac{V_{AC\,\max}}{V_{AC\,\min}} = \frac{1.99 * 0.47}{1.1} * \frac{265}{185} = 1.21V$$

where 1.1 V is the multiplier maximum slope which is given in the datasheet.

In this way, the resistor divider will be such that

Equation 33

$$k_p = \frac{R_{MULTL}}{R_{MULTL} + R_{MULTH}} = \frac{V_{MULT\,max}}{\sqrt{2}V_{AC\,max}} = \frac{1.21}{1.41 * 265} = 3.24 * 10^{-3}$$

supposing a 200 μA current flowing into the multiplier divider, R_{MULTL} is calculated as follows:

Equation 34

$$R_{MULTL} = \frac{V_{MULT}}{200\mu A} = \frac{1.21}{200 * 10^{-6}} = 6.2k\Omega$$

Taking into account this value and from *Equation 33*:

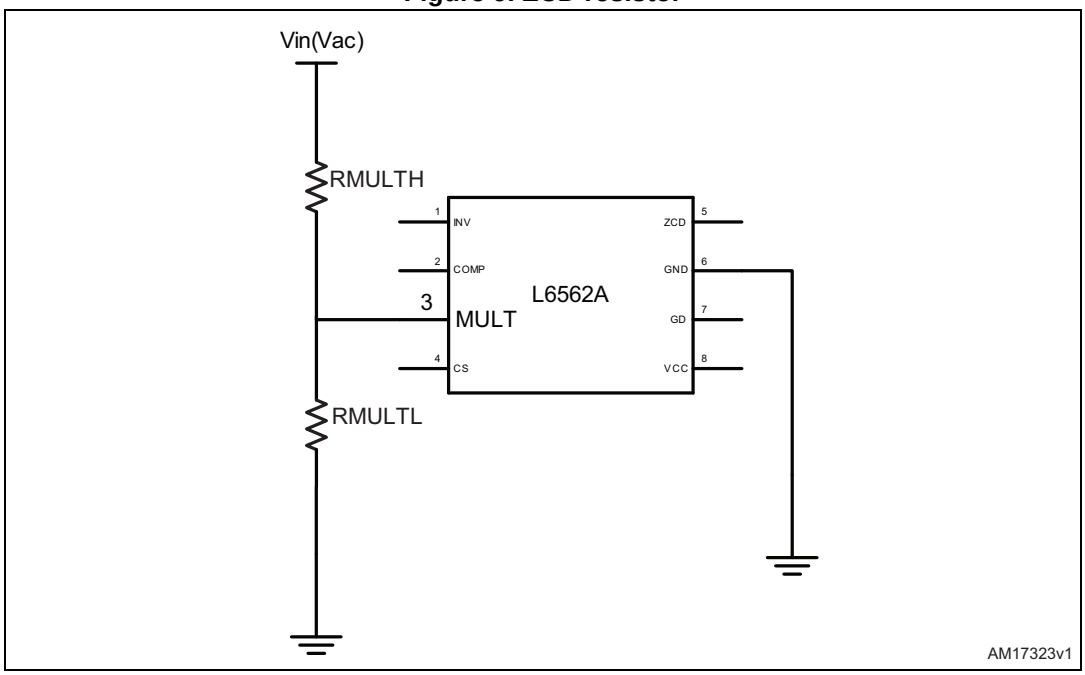
Equation 35

$$R_{MULTH} = \frac{1 - K_P}{K_P} R_{MULTL} = 1.9M\Omega$$

The selected values are R_{MULTL} = 8.2 kΩ and R_{MULTH} = 2 MΩ

Pin 5 (ZCD): zero-current detection

Figure 9. ZCD resistor



The zero-current detection (ZCD) block switches the external Power MOSFET on as the voltage across the boost inductor reverses, just after the current through the boost inductor has gone to zero. This feature allows transition mode operation. The ZCD pin is connected to the auxiliary winding of the inductor boost through a limiting resistor.

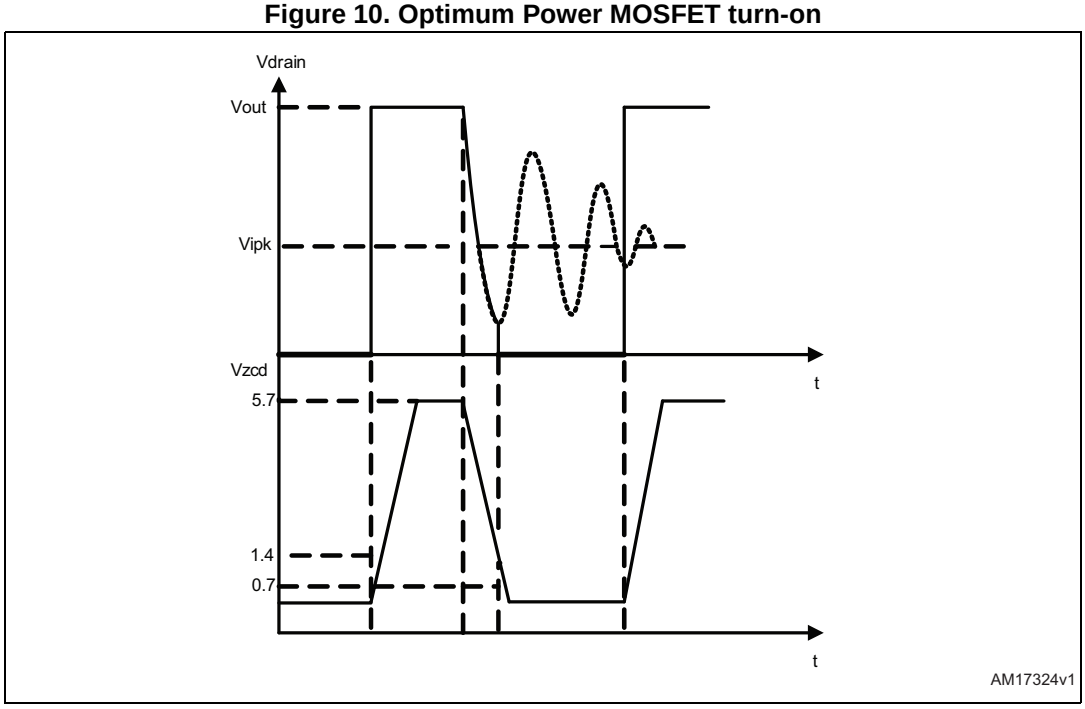
The maximum main-auxiliary winding turn ratio, nmax, has to ensure that the voltage delivered to the pin during the OFF-time of the Power MOSFET is sufficient to arm the ZCD circuit.

Equation 36

$$n \le \frac{n_{primary}}{n_{secondary}} \le \frac{V_{OUT} - \sqrt{2}V_{AC\,max}}{1.4 * 1.15} \Rightarrow n \le 15.7$$

The minimum value of the limiting resistor can be found assuming 0.8 mA current through the pin and considering the maximum voltage across the auxiliary winding with a selected turn ratio n = 10. The actual value can be fine-tuned in order to make the turn-on of the Power MOSFET occur exactly on the valley of the drain voltage oscillation (the boost inductor, completely discharged, is ringing with the drain capacitance, as shown in the figure below). This will minimize the power dissipation at turn-on.

Figure 10. Optimum Power MOSFET turn-on



Equation 37

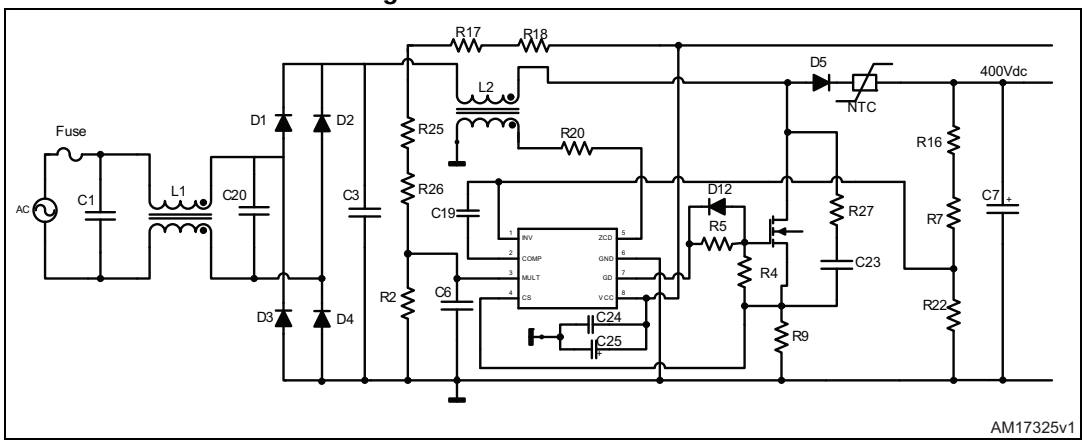
$$R_1 = \frac{\frac{V_{out}}{n} - V_{ZCDH}}{0.8mA} = \frac{\frac{400}{10} - 5.7}{0.8mA} = 42.9k\Omega$$

Equation 38

$$R_2 = \frac{\frac{\sqrt{2}V_{AC\,max}}{n} - V_{ZCDL}}{0.8mA} = \frac{\frac{\sqrt{2} * 265}{10} - 0}{0.8mA} = 46.8k\Omega$$

where V_{ZCDH} = 5.7 V (typ) and V_{ZCDL} = 0 (typ) are given in the datasheet. We consider the highest value, for this reason the selected limiting resistor is R_{ZCD} = 47 kΩ. The complete boost PFC schematic is given in the following figure.

Figure 11. Boost PFC section

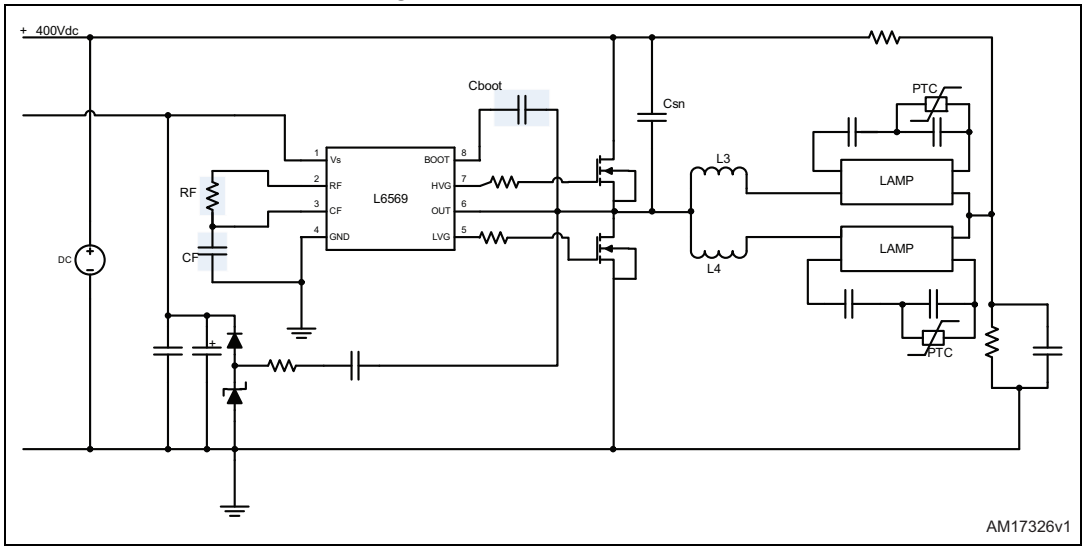


4 DC/AC converter and lamp

The DC/AC converter uses a half-bridge voltage-fed topology with two Power MOSFETs driven by the L6569 driver. It is a high-voltage half-bridge driver with an oscillator inside.

Here below is the complete electrical schematic of DC/AC inverter in half-bridge topology:

Figure 12. DC/AC converter



Voltage-fed series resonant half-bridge inverters are currently used for fluorescent lamps. This topology makes easy to operate in zero-voltage switching (ZVS) resonant mode, dramatically reducing transistor switching losses and the electromagnetic interference. This type of inverter can operate up to 150 kHz in ZVS mode. For this project, the frequency has been selected between 50 and 100 kHz, specifically $f_{run} \approx 57$ kHz.

The frequency of the internal oscillator can be programmed using an external circuitry composed of a resistor R_F and a capacitor C_F. The nominal oscillator frequency can be calculated using the following *Equation 39*:

Equation 39

$$f_{OSC} = \frac{1}{2 * R_F * C_F \ln 2} = \frac{1}{1.3863 * R_F * C_F} = 57kHz$$

From the above equation, imposing C_F=560 pF, R_F will be equal to 22 kΩ.

4.1 Bootstrap circuit

The bootstrap block is needed to supply the high-voltage section. This function is normally accomplished by a high-voltage fast-recovery diode. The L6569 has an internal bootstrap circuit that replaces the external diode. The bootstrap capacitor (C_{BOOT}) is charged every time the low-side driver is on and the output pin is below the supply voltage (V_{DD}) of the gate driver. The bootstrap capacitor is discharged only when the high-side switch is turned on. This bootstrap capacitor is the supply voltage (V_{BS}) for the high circuit section.

The first parameter to take into account is the maximum voltage drop that we have to guarantee when the high-side switch is in the on state. The maximum allowable voltage drop (V_{BOOT}) depends on the minimum gate drive voltage (for the high-side switch) to maintain. If V_{GSMIN} is the minimum gate-source voltage, the capacitor drop must be:

Equation 40

$$\Delta V_{BOOT} = V_{DD} - V_F - V_{GSMIN}$$

where:

- V_{DD} is supply voltage of the gate driver [V];
- V_F is the bootstrap diode forward-voltage drop [V].

The value of the bootstrap capacitor is calculated by:

Equation 41

$$C_{BOOT} = \frac{Q_{TOTAL}}{\Delta V_{BOOT}}$$

Where, Q_{TOTAL} is the total amount of the charge supplied by the capacitor. The total charge supplied by the bootstrap capacitor is calculated using *Equation 42*:

Equation 42

$$Q_{TOTAL} = Q_{GATE} + \left(I_{LKCAP} + I_{LKGS} + I_{QBS} + I_{LK} + I_{LKDIODE}\right) * t_{ON} + Q_{LS}$$

Where:

- Q_{GATE} is the total gate charge
- I_{LKCAP} is the bootstrap capacitor leakage current
- I_{LKGS} is the switch gate-source leakage current
- I_{QBS} is the bootstrap circuit quiescent current
- I_{LK} is the bootstrap circuit leakage current
- $I_{LKDIODE}$ is the bootstrap diode leakage current
- T_{ON} is the high-side switch-on time
- Q_{LS} is the charge required by the internal level shifter, which is set to 3 nC for all HV gate drivers.

The capacitor leakage current is important only if an electrolytic capacitor is used, otherwise this can be neglected. Recommended values for the bootstrap capacitor are within the range of 100 nF~570 nF, but the right value must be selected according to the application in which the device is used. When the capacitor value is too large, the bootstrap charging time slows and the low-side on-time might be not long enough to reach the bootstrap voltage. For this project the selected value is 100 nF/400 V. The output drivers drive an external N-channel Power MOSFET. The internal logic ensures a deadtime (typ 1.25 μs) to avoid cross-conduction of the power devices. The selected power device is STL13N60M2.

4.2 Lamp requirements

4.2.1 Output inductor design

The output inductor should be designed to allow a sufficient peak ignition current without saturating. This is important as the ballast will be unable to ignite if it cannot deliver sufficient voltage to the lamp.

The ignition current depends on the type of the lamp being used and must be kept to a minimum by ensuring that the cathodes are sufficiently preheated. To minimize eddy current losses in the inductor, multi-stranded wire for the windings should be used. It is important to have a large enough air gap to produce the highest available peak current before allowing the inductor to saturate. When the cores are hot, the saturation point and hence the peak current for the inductor will be lower, therefore a poorly designed inductor may result in the ballast failing to ignite the lamp during an attempted hot re-strike. The value of the output inductor is given by following equation:

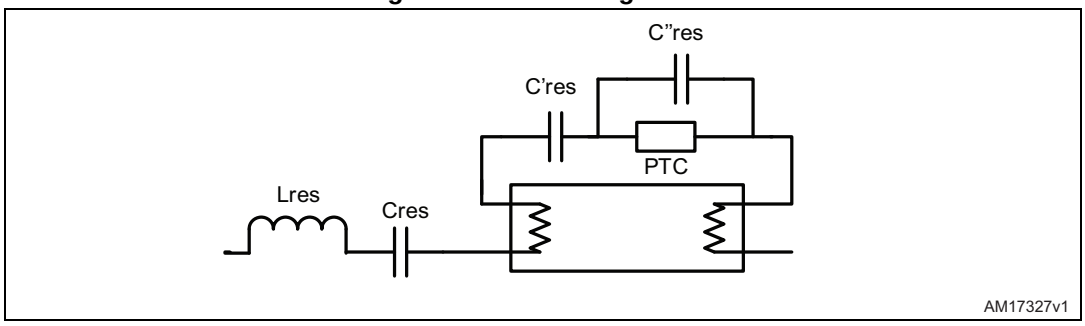
Equation 43

$$L = \frac{V_{in}^2 \eta}{f_{run}\sqrt{2}\pi^2 P_{run}}$$

4.2.2 Lamp preheating

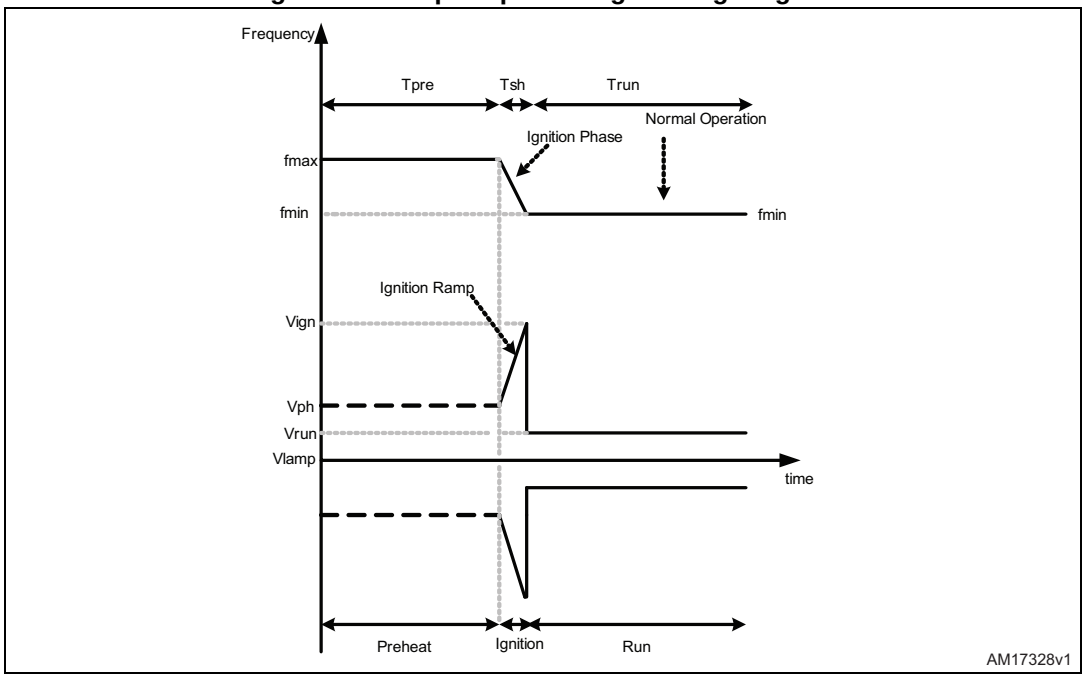
It is essential that the lamp be sufficiently preheated before ignited. In order to achieve the maximum possible lamp life, it is necessary to heat the cathodes to the correct temperature before ignition. Accelerated deterioration occurs if lamps are ignited when the cathodes are either not sufficiently heated or overheated. The preheating of the cathodes allows an easy strike of the lamp, reducing ignition voltage. During preheating time the lamp is characterized by high impedance and the current flows through the filament. Its resistance value is strictly dependent on the lamp model. Typically these filaments show an initially low value (a few ohms) that will increase by 5 times during the preheating. One method to obtain the preheating cathodes is to adopt a PTC resistor. *Figure 13* shows its typical connection.

Figure 13. Preheating circuit



At startup when the PTC is cold, it can be considered as a short-circuit, the circuit operating frequency is determined by C'res and Lres (we can neglect Cres). During the preheating the current flows through the PTC and C'res heats both the cathodes and the PTC at the same time. The value of C'res must be chosen in order to avoid high voltage on the lamp and consequent switch-on. When the PTC is hot (end of preheating) its resistance increases until it can be considered as an open circuit. In this case the current flows through the series formed by C''res and C'res. Therefore the equivalent capacitance across the lamp becomes lower than the initial value, increasing the capacitive reactance and allowing the tube ignition. We can summarize the turn-on sequence in three phases: preheating, ignition and normal lamp operation. The preheating of the lamp filaments is achieved by a high switching frequency f_{PRE}, to ensure that a current flows in the filaments without lamp ignition. In fact the initial voltage applied across the lamp is below the strike potential. The duration of the preheating period t_{PRE} is set by the capacitor C'res together with Lres. The choice of this time is strictly dependent on the lamp type. The ignition sequence begins after t_{PRE}. During the ignition phase, the frequency shifts from f_{MAX} to f_{MIN} (that is the normal operation frequency) in a period TSH. The voltage across the lamp increases causing the ignition. At the end of the ignition time the frequency reaches the normal operation value, f_{MIN}, and the lamp is in run mode (as shown in *Figure 14*).

Figure 14. Lamp output voltage timing diagram



The following figures indicate the preheating, ignition and run mode phases, respectively.

Figure 15. Lamp output voltage during preheating phase

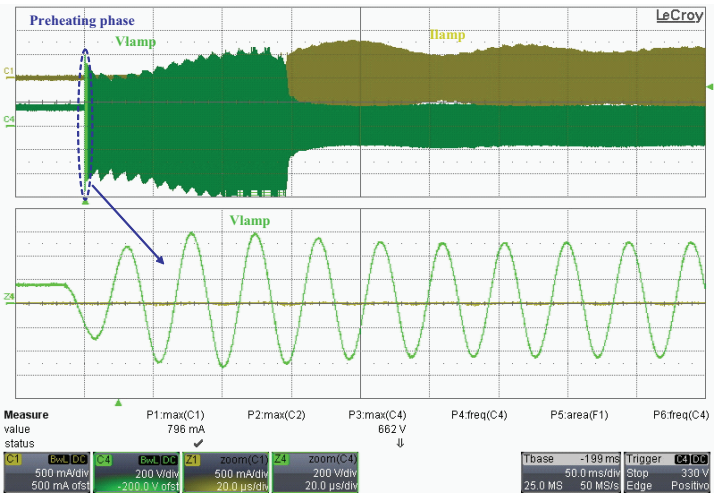


Figure 16. Lamp output voltage during ignition phase

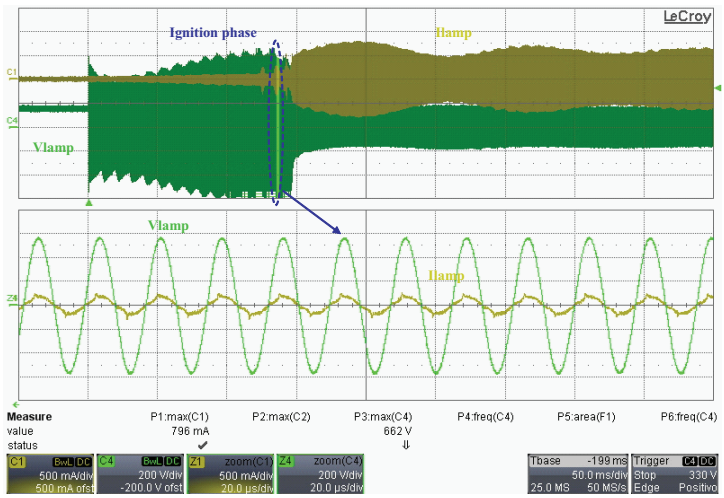
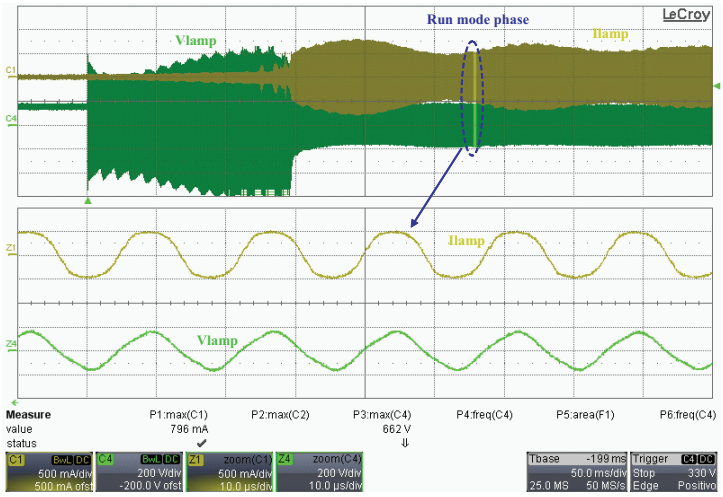


Figure 17. Lamp output voltage during run-mode phase



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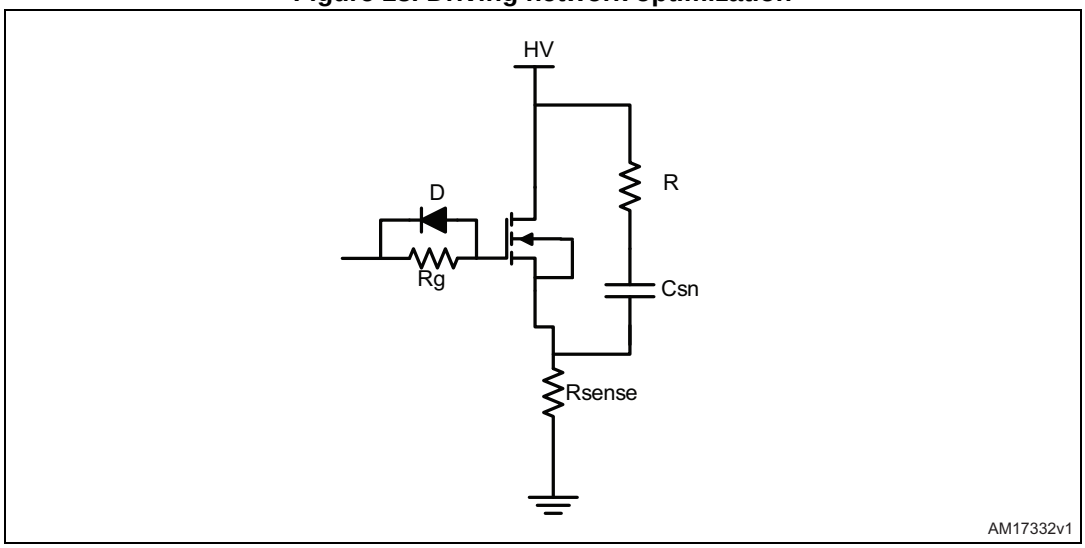
5 Driving optimization

A driving network optimization has been performed with the main purpose to have thermal and dynamic behavior of the devices compliant to the features of the system.

5.1 Power MOSFET circuit optimization

Here below is the electrical schematic concerning the driving circuit of the Power MOSFET.

Figure 18. Driving network optimization



An RC snubber network, R = 180 Ω and C_{sn}=47 pF, has been inserted in order to avoid a voltage spike and voltage oscillation across the Power MOSFET during its turn-off.

Furthermore, limiting the rise slope of the Power MOSFET voltage, $\Delta V_{DS}/\Delta T$, the cross between voltage and current is also reduced resulting in less switching losses during turn-off. On the other hand, a too high value involves a peak on the current during turn-on. So a right trade-off has to be found in order to balance the switching losses during turn-off and turn-on and to have the best performance of the device.

The driving circuit, R_g = 220 Ω and the diode D, allows the Power MOSFET to not have turn-on too quickly, reducing the discharge of snubber capacitor and consequently guaranteeing negligible switch-on losses and thanks to the diode, it allows the fastest discharge of parasitic capacitance of the Power MOSFET and therefore speeds up the switch-off.

A comparison has been performed between two different driving networks in order to find the best solution. The following figures show the waveforms of various conditions.

Figure 19. Turn-off detail with R_g=220 Ω, speed off diode and C_{sn}= 47 pF @ 230 V_{AC}

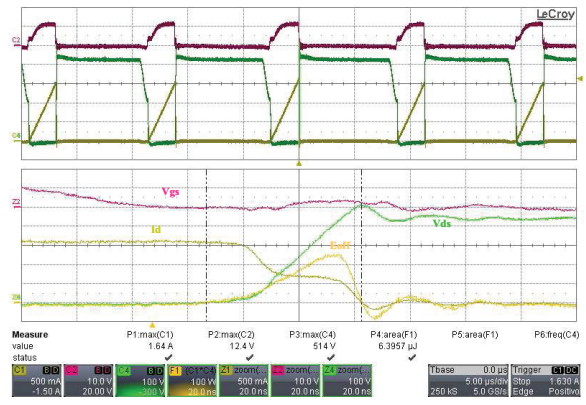


Figure 20. Turn-off detail with R_g=220 Ω, speed off diode and C_{sn}=100 pF @ 230 V_{AC}

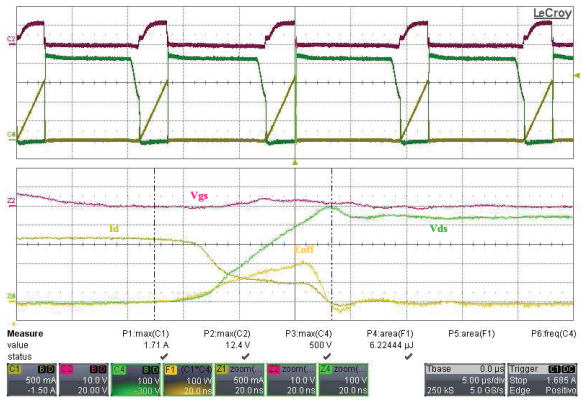


Figure 21. Turn-on detail with R_g= 220 Ω, speed off diode and C_{sn} = 47 pF @ 230 V_{AC}

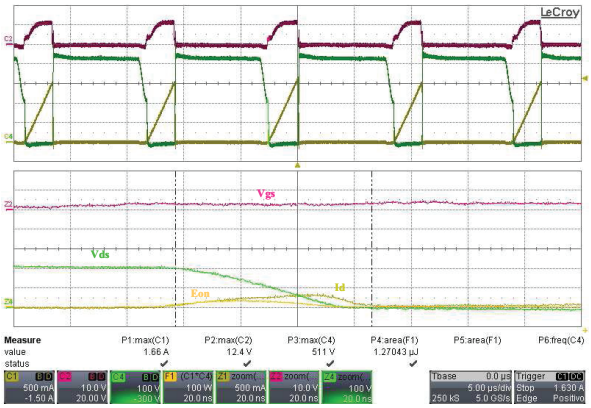


Figure 22. Turn-on detail with R_g= 220 Ω, speed off diode and C_{sn}= 100 pF @ 230 V_{AC}

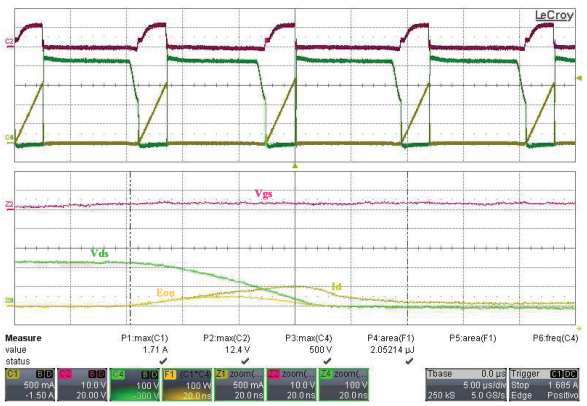


Figure 23. Turn-off detail with R_g =47 Ω, no speed off diode and C_{sn} = 47 pF @ 230 V_{AC}

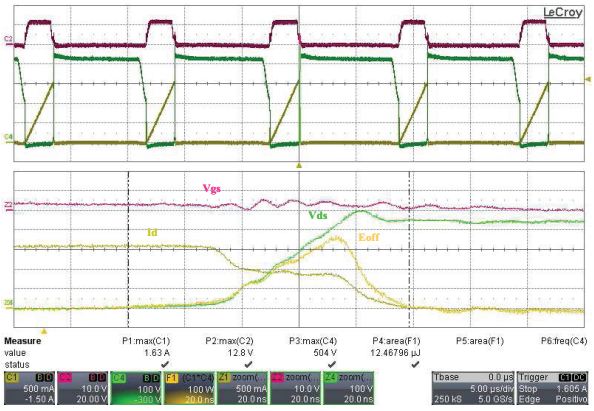


Figure 24. Turn-off detail with R_g = 47 Ω, no speed off diode and C_{sn} = 100 pF @ 230 V_{AC}

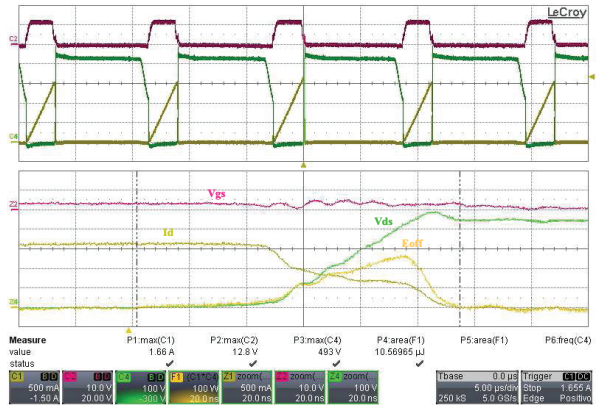


Figure 25. Turn-on detail with R_g = 47 Ω, no speed off diode and C_{sn} = 47 pF @ 230 V_{AC}

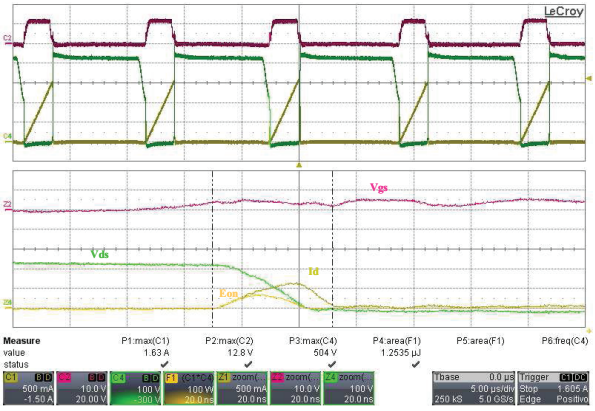
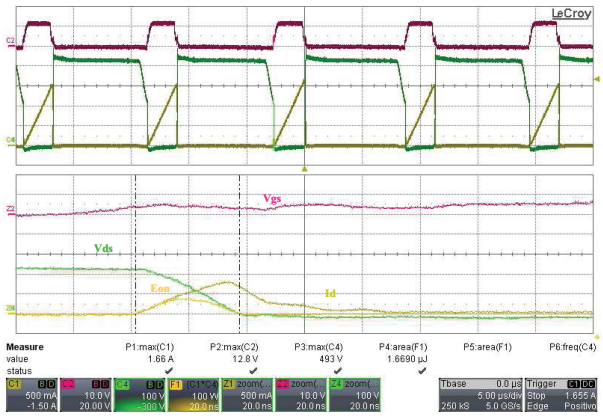


Figure 26. Turn-on detail with R_g = 47 Ω, no speed off diode and C_{sn} = 100 pF @ 230 V_{AC}



Here below is the summary table, in terms of dissipated energy during both turn-on and turn-off detail.

Table 2. Summary table of dissipation energy

Driving conditions	E_{on} (µJ)	E_{off} (µJ)	E_{tot} (µJ)
R_g=220 Ω, speed off diode, C_{sn}= 47 pF	1.27	6.39	7.66
R_g=220 Ω, speed off diode, C_{sn}= 100 pF	2.05	6.22	8.72
R_g=220 Ω, no speed off diode, C_{sn}= 47 pF	1.25	12.46	13.71
R_g=220 Ω, no speed off diode, C_{sn}= 100 pF	1.66	10.56	12.22

As *Table 2* shows, the best compromise in terms of switching losses, is to have a smaller snubber capacitor, C_{sn} = 47 pF, in order to reduce the peak on the drain current during turn-on (as shown in *Figure 21*) and R_g = 220 Ω with speed off diode in order to speed up the device turn-off (as shown in *Figure 19*.). In fact a greater R_g provides a slower switch-on of the Power MOSFET, reduces the snubber capacitor discharge, guaranteeing negligible power losses during turn-on.

6 DC/AC converter waveforms

The figures below depict the waveforms during steady-state operation and turn-off and turn-on detail related to the DC/AC converter stage which adopts a half-bridge voltage-fed topology. The device is STL13N60M2 which works at ~57 kHz.

Figure 27. STL13N60M2 during steady-state operation in half-bridge section @ 230 V_{AC}

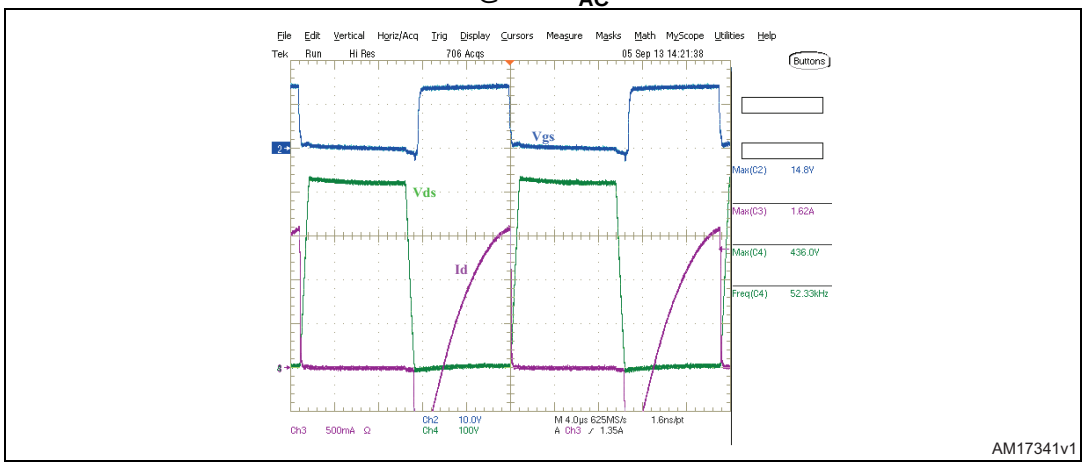


Figure 28. STL13N60M2 during turn-off in half-bridge section @230V_{AC} (detail)

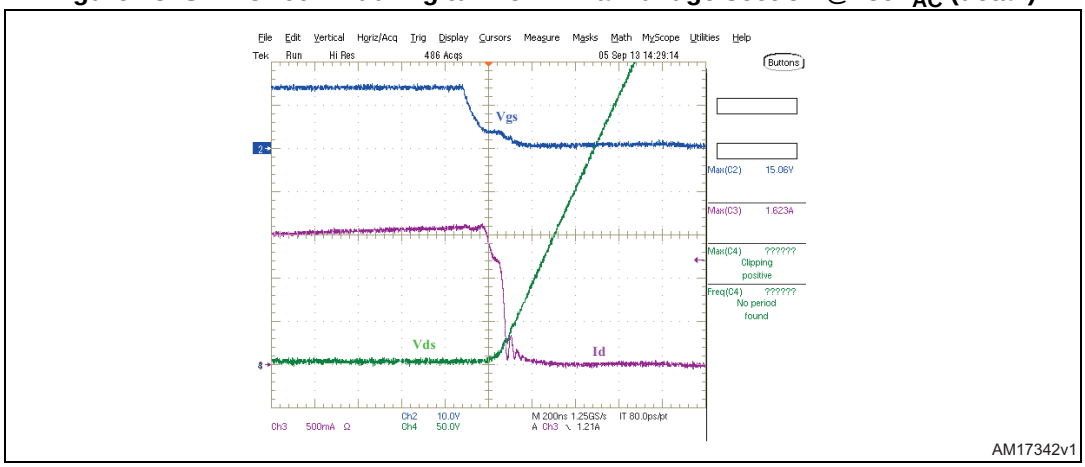
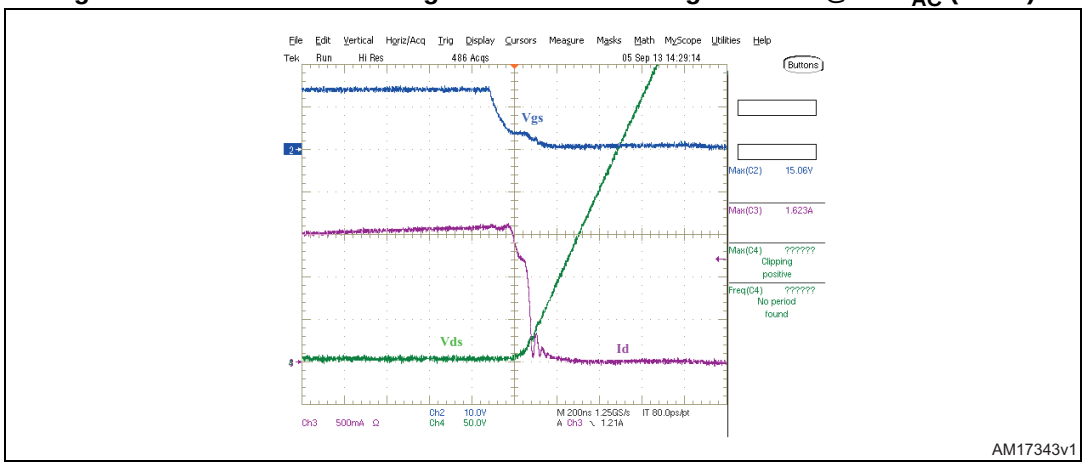


Figure 29. STL13N60M2 during turn-on in half-bridge section @230V$_{AC}$ (detail)



It's clear that the device has good performance in the half-bridge section. In fact, the cross during turn-off (see *Figure 28*) is very low, resulting in low power dissipation.

7 Experimental results

The experimental results have been measured with different input voltages and leaving the board exposed to room temperature (25 °C). The devices have been kept soldered on the PCB. Temperature has been detected using an infrared thermal camera pointed on the package of the devices. The test equipment used is provided below as well as the test conditions:

- Input voltage: 185 V_{AC} - 230 V_{AC} - 265 V_{AC}
- Test equipment:
  - Agilent AC power source/analyzer 6813B
  - Flir system thermal camera
  - LeCroy 64Xi-A oscilloscope
  - LeCroy active current probe CP030
  - LeCroy active differential voltage probe ADP305
- Ambient temperature: 25°C.

The table below shows electrical and thermal results obtained with both packages, DPAK and PowerFLAT™ 5x6, at different input voltages.

Table 3. Main electrical and thermal results @ 25 °C ambient temperature

Device	V_{IN}(V)	I_{in}(A)	Power factor	THD (%)	Pin (W)	T_{HB} (°C)	T_{PFC} (°C)
STD13N60M2 (DPAK)	185	0.576	0.997	~ 7.5	106	70	64.2
STL13N60M2 (PowerFLAT™ 5x6)		0.569	0.997	~ 7.2	104.9	71.9	67
STD13N60M2 (DPAK)	230	0.465	0.995	~ 8.1	106.4	71	66.5
STL13N60M2 (PowerFLAT™ 5x6)		0.456	0.994	~ 8	104.4	72	69
STD13N60M2 (DPAK)	265	0.404	0.991	~ 9	106.3	71.8	70.4
STL13N60M2 (PowerFLAT™ 5x6)		0.395	0.99	~ 8.5	103.9	72.2	73

Changing input voltage, the main electrical parameters of the PFC and THD suggest that the application performances are very good. The temperatures of the two packages are not so different and the devices work within safety conditions.

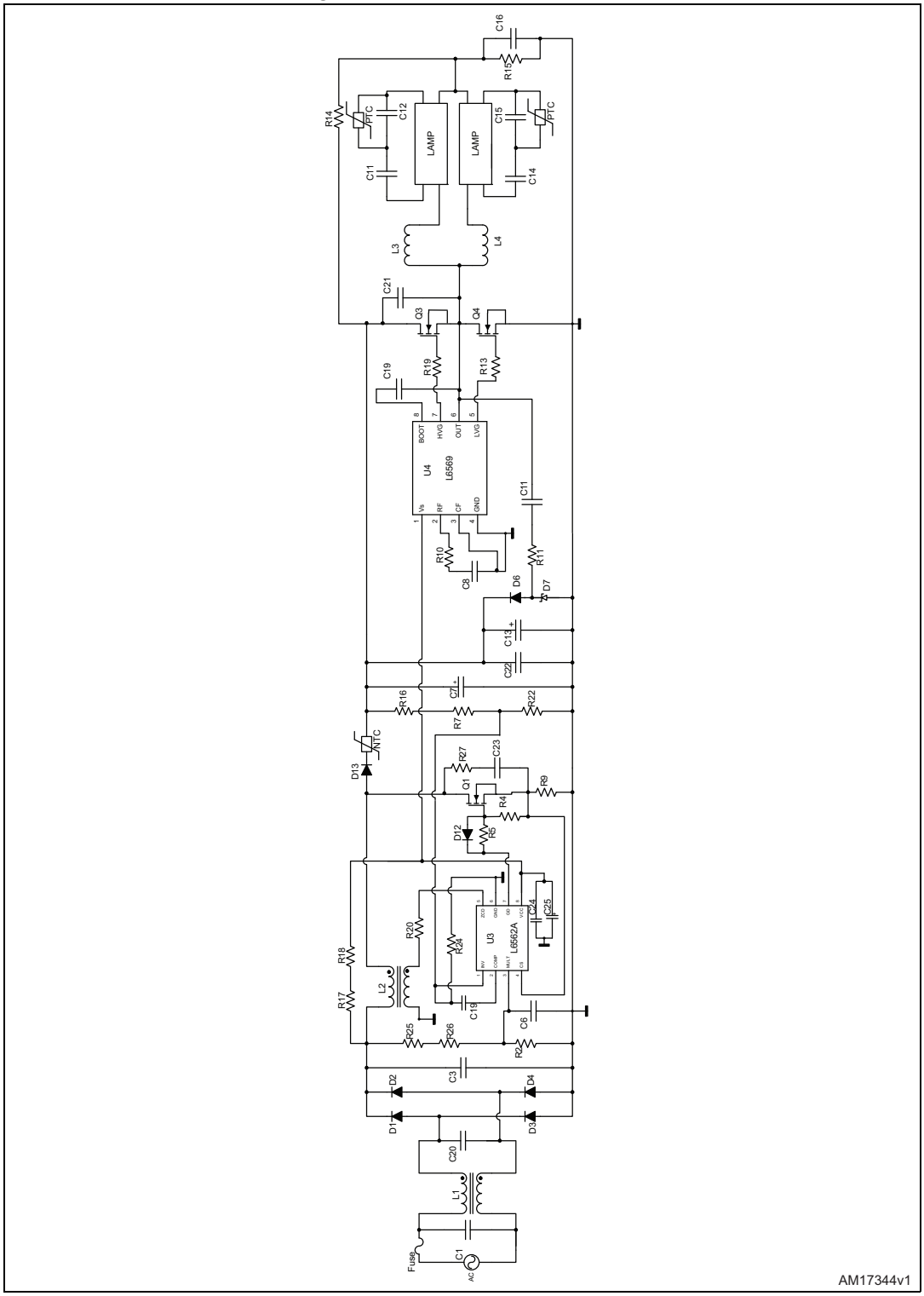
8 Conclusion

The proposed design of the electronic ballast has shown the capability of the demonstration board to drive 2x58 W fluorescent lamps with very good electrical and thermal performance. The choice of components and the optimization of the power devices guarantee the highest PF and lowest THD.

The main purpose of this exercise was to evaluate the electrical and thermal features of the PowerFLAT™ 5x6 compared to the DPAK package. The PowerFLAT™ 5x6 package showed comparable thermal results. For both package options the temperature is fully compliant with the absolute maximum rating limit in the datasheet specification.

Appendix A Board description

Figure 30. Electrical schematic



Appendix B Bill of material

Table 4. Board bill of material

Reference	Qty	Value/part number	Description
R2/R22	2	8.2 kΩ/0.25 W	RC07
R4	1	56 kΩ	SMD 1206
R20	1	47 kΩ/0.25 W	RC07
R5	1	220 kΩ	SMD 1206
R7/R16	2	680 kΩ/0.25 W	RC07
R9	1	0.47 kΩ/0.5 W	RC07
R10	1	22 kΩ/0.25 W	RC07
R11/R28	2	100 kΩ/2 W	RC07
R13/R19	2	47 kΩ	SMD 1206
R17/R18	2	270 kΩ/0.25 W	RC07
R24	1	10 kΩ/0.25 W	RC07
R25/R26	2	1 MΩ/0.5 W	RC07
R27	1	180 kΩ/0.25 W	RC07
C1/C20	2	220 nF/305 V_{AC}	X2 Metallized polypropylene capacitor
C3	1	150 nF/630 V_{DC}	Plastic capacitor
C6	1	10 nF/100 V_{DC}	Metallized polyester capacitor
C7	1	56 µF/450 V	Electrolytic capacitor
C8	1	560 pF/50 V	Ceramic capacitor
C9	1	100 nF/400 V_{DC}	Polyester capacitor
C16	1	100 nF/630 V_{DC}	Polyester capacitor
C10	1	560 pF/500 V_{DC}	Ceramic capacitor
C11/C14	2	15 nF/630 V_{DC}	Metallized polypropylene capacitor
C12/C15	2	22 nF/630 V_{DC}	PHE450 film capacitor
C13	1	22 µF/50 V	Electrolytic capacitor
C19	1	1 µF/100 V	Polyester capacitor
C21	1	2.2 nF/1000 V	Ceramic capacitor
C22	1	100 nF/100 V_{DC}	Polyester capacitor
C23	1	47 nF/500 V_{DC}	Ceramic capacitor
C24	1	220 nF/100 V	Metallized polyester capacitor
C25	1	10 µF/>25 V	Electrolytic capacitor
D1/D2/D3/D4	4	1N4007	DO-41
D13	1	SWTTH1RL06	ST DO-41

Table 4. Board bill of material (continued)

Reference	Qty	Value/part number	Description
D6	1	1N4148	DO-35
D8/D9	2	Omitted	
D12	1	LL4148	SMD 1406
D7	1	Zener 16 V	DO-41
PTC	2	600 Ω/120 °C	TDK/EPC B59884C0120A070
NTC	1	2.5 Ω	TDK/EPC B57236S0259M0
FUSE	1	1.6 A/250 V	Serie TR5
L1	1	2x10mH/1A	Magnetica: common mode inductor code: 02106 class code:1045.0017
L2	1	500 µH/0.81A	Magnetica: PFC inductor code: 06535 class code:2216.0001
L3/L4	2	1.5 mH/0.6A/2A pk	Magnetica: Ballast inductor code: 07056 class code:1956.0007
Q1/Q2/Q3	3	STL13N60M2	N-channel 600 V, 0.39 Ω typ., 7 A MDmesh II Plus™ low Qg Power MOSFET in a PowerFLAT™ 5x6 HV package
U3	1	L6562A	ST PFC driver SO-8
U4	1	L6569	ST HB driver SO-8

Appendix C Layout layers

Figure 31. Bottom layout layer

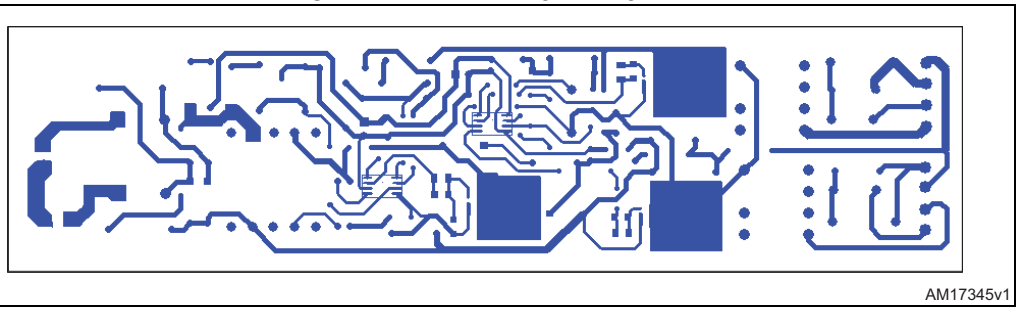


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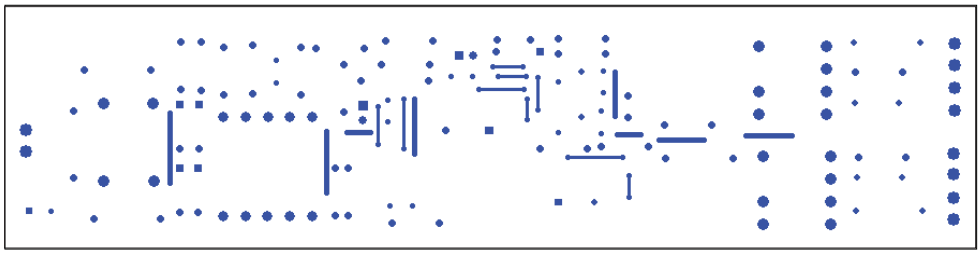
Figure 32. Top layout layer



AM17346v1

Figure 33. Silkscreen top

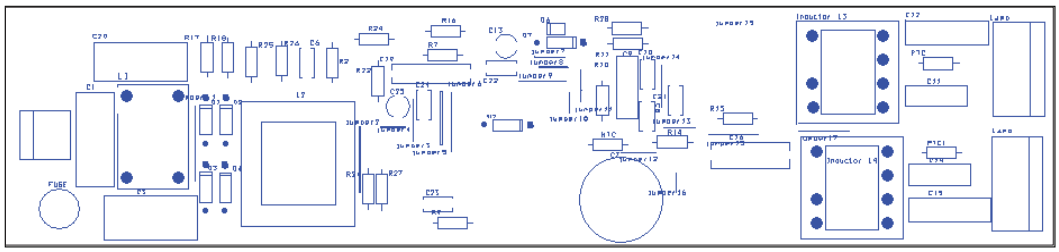


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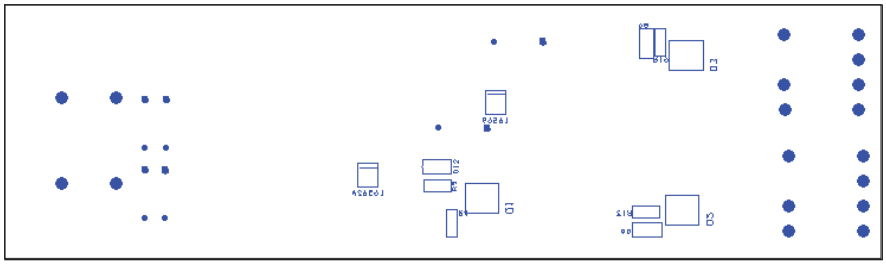
Figure 34. Silkscreen bottom



AM17348v1

9 Reference

1. AN2761 application note

10 Revision history

Table 5. Document revision history

Date	Revision	Changes
31-Jul-2013	1	Initial release.
12-May-2014	2	– Updated: *Section 6* – Updated: *Figure 27*, *28*, *29* and *Table 3* – Updated: *Table 4* – Minor text changes