NSM4002MR6

Dual NPN Transistors for Driving LEDs

NSM4002MR6 contains a single two NPN transistors. The base of the Q2 NPN transistor is internally connected to the collector of the Q1 NPN transistor. This device is designed to replace a discrete solution that is common for providing a constant current by integrating these two components into a single device. NSM4002MR6 is housed in a SC−74 package which is ideal for surface mount applications in space constrained applications.

Features

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- LED Lighting
- Driver Circuits

MAXIMUM RATINGS Q_1 (T_A = 25°C)

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	40	Vdc
Collector−Base Voltage	V_{CBO}	60	Vdc
Emitter−Base Voltage	V_{EBO}	6.0	Vdc
Collector Current − Continuous	I_C	200	mAdc

MAXIMUM RATINGS Q_2 (T_A = 25°C)

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	45	Vdc
Collector−Base Voltage	V_{CBO}	50	Vdc
Emitter−Base Voltage	V_{EBO}	5.0	Vdc
Collector Current − Continuous	I_C	500	mAdc

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Rating	Symbol	Max	Unit
Total Device Dissipation T_A = 25°C Derate above 25°C	P_D (Note 1)	 260 2.08	 mW mW/°C
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$ (Note 1)	480	°C/W
Total Device Dissipation T_A = 25°C Derate above 25°C	P_D (Note 2)	 300 2.4	 mW mW/°C
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$ (Note 2)	416	°C/W
Junction and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C

1. FR−4, 100 mm², 2 oz. Cu.
2. FR−4, 500 mm², 2 oz. Cu.

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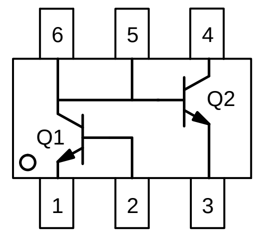
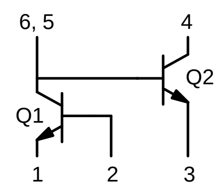
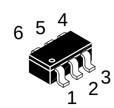
Dual NPN Transistors for Driving LEDs

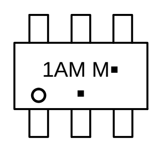






SC−74
CASE 318F

MARKING DIAGRAM



1AM = Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping†
NSM4002MR6T1G	SC−74 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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Table 1. ELECTRICAL CHARACTERISTICS Q_1 (T_A = 25°C, unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	40	−	Vdc
Collector−Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)	$V_{(BR)CBO}$	60	−	Vdc
Emitter−Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	$V_{(BR)EBO}$	6.0	−	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, $V_{EB(OFF)}$ = 3.0 Vdc)	I_{CEX}	−	50	nAdc
Base Cutoff Current (V_{CE} = 30 Vdc, $V_{EB(OFF)}$ = 3.0 Vdc)	I_{BL}	−	50	nAdc
ON CHARACTERISTICS				
DC Current Gain (Note 3) (I_C = 100 μA, V_{CE} = 1.0 V) (I_C = 1.0 mA, V_{CE} = 1.0 V) (I_C = 10 mA, V_{CE} = 1.0 V) (I_C = 50 mA, V_{CE} = 1.0 V) (I_C = 100 mA, V_{CE} = 1.0 V)	h_{FE}	 40 70 100 60 30	 − − 300 − −	
Collector−Emitter Saturation Voltage (Note 3) (I_C = 10 mA, I_B = 1.0 mA) (I_C = 50 mA, I_B = 5.0 mA)	$V_{CE(sat)}$	 − −	 0.20 0.30	V
Base−Emitter Saturation Voltage (Note 3) (I_C = 10 mA, I_B = 1.0 mA) (I_C = 50 mA, I_B = 5.0 mA)	$V_{BE(sat)}$	 0.65 −	 0.85 0.95	V
Cutoff Frequency (I_C = 10 mA, V_{CE} = 20 V, f = 100 MHz)	f_T	300	−	MHz
Output Capacitance (V_{CB} = 5.0 V, f = 1.0 MHz)	C_{obo}	−	4.0	pF
Input Capacitance (V_{EB} = 0.5 V, f = 1.0 MHz)	C_{obo}	−	8.0	pF

Table 2. ELECTRICAL CHARACTERISTICS Q_2 (T_A = 25°C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Breakdown Voltage (I_C = 10 mAdc, I_B = 0)	$V_{(BR)CEO}$	45	−	−	Vdc
Collector−Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)	$V_{(BR)CBO}$	50	−	−	Vdc
Emitter−Base Breakdown Voltage (I_E = 1.0 μAdc, I_C = 0)	$V_{(BR)EBO}$	5.0	−	−	Vdc
Collector Cutoff Current (V_{CB} = 20 Vdc, I_E = 0)	I_{CBO}	−	−	0.1	μAdc
ON CHARACTERISTICS					
DC Current Gain (Note 3) (I_C = 100 mA, V_{CE} = 1.0 V) (I_C = 500 mA, V_{CE} = 1.0 V)	h_{FE}	 250 40	 − −	 600 −	
Collector – Emitter Saturation Voltage (Note 3) (I_C = 500 mA, I_B = 50 mA)	$V_{CE(sat)}$	−	−	0.7	V
Base – Emitter Turn−on Voltage (Note 3) (I_C = 500 mA, V_{CE} = 1.0 V)	$V_{BE(on)}$	−	−	1.2	V
Cutoff Frequency (I_C = 10 mA, V_{CE} = 5.0 V, f = 100 MHz	f_T	100	−	−	MHz
Output Capacitance (V_{CB} = 10 V, f = 1.0 MHz	C_{obo}	−	10	−	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulsed Condition: Pulse Width = 300 msec, Duty Cycle ≤ 2%.

Application Section

Introduction

The NSM4002MR6 is designed to be used as a constant current driver for LEDs. The two resistors in Figure 1 are external from the NSM4002MR6 to allow for customization. R_{set} controls the current through the load, and R_1 controls the bias current.

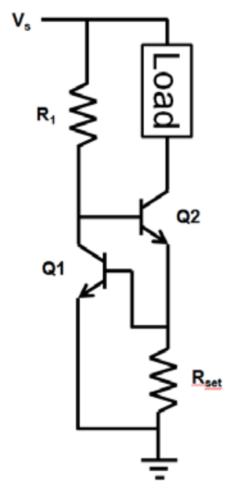


Figure 1. Typical Application Schematic

Selecting R_{set}

The R_{set} resistor is used to set the driving current of the load. It is connected across the Base−Emitter junction of Q1. This V_{BE} voltage is what sets up the constant voltage across the R_{set} resistor. Figure 5 gives the typical values of V_{BE} based on the biasing current. To determine the R_{set} value simply divide the V_{BE} voltage by the desired driving current.

Selecting R_1

The R_1 resistor is used to set the biasing current. The biasing current is split between the base of Q2 and the collector of Q1. When desiring the lowest overhead voltage R_1 should be set as high as possible. It is important to ensure it is not set too high so that Q2 falls out of saturation. However, a lower R_1 value will drive more current through Q1. This will reduce the change in the driving current as temperature is increased. It will also allow a higher driving current to be achieved while maintaining good current regulation. The side affect of a lower R_1 value is that it reduces the overall efficiency because more power is being used in the driving circuit.

Input Votlage, V_s

The maximum input voltage, V_s, is determined by the load. No more than 45 V can be applied across Q2. This leads to:

$$V_{s(max)} = V_{Load} + 45\ V \qquad \text{(eq. 1)}$$

Overhead Voltage

The overhead voltage of this device to reach full current regulation is the combination of the V_{BE} voltages of the two transistors. Under typical conditions this overhead voltage will typically be 1.4 V.

TYPICAL CHARACTERISTICS − Q1

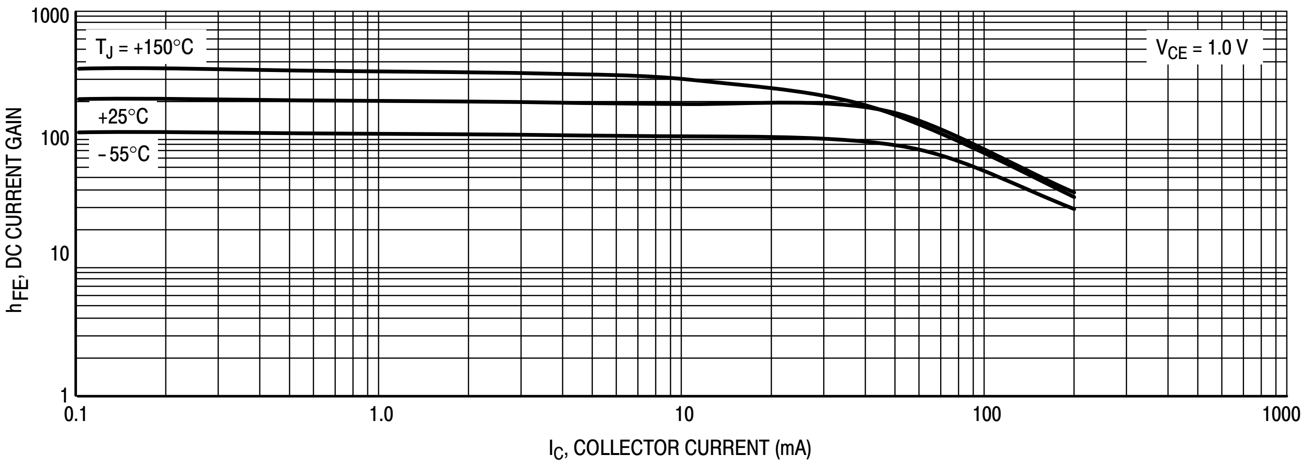


Figure 2. DC Current Gain

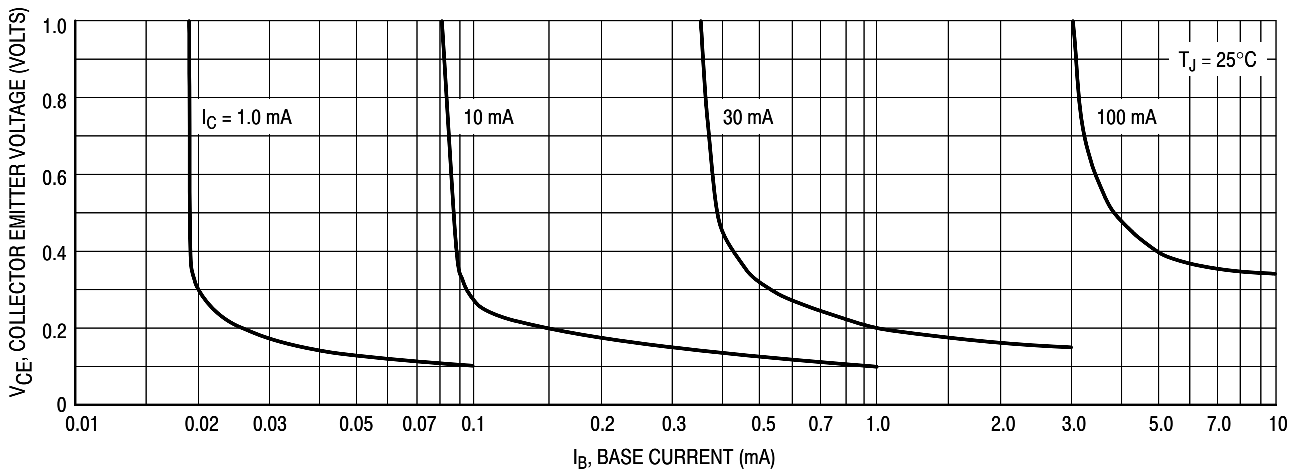


Figure 3. Collector Saturation Region

TYPICAL CHARACTERISTICS − Q1

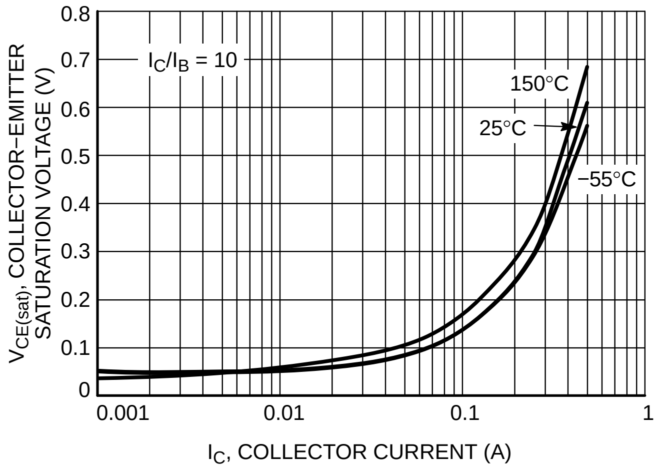


Figure 4. Collector Emitter Saturation Voltage vs. Collector Current

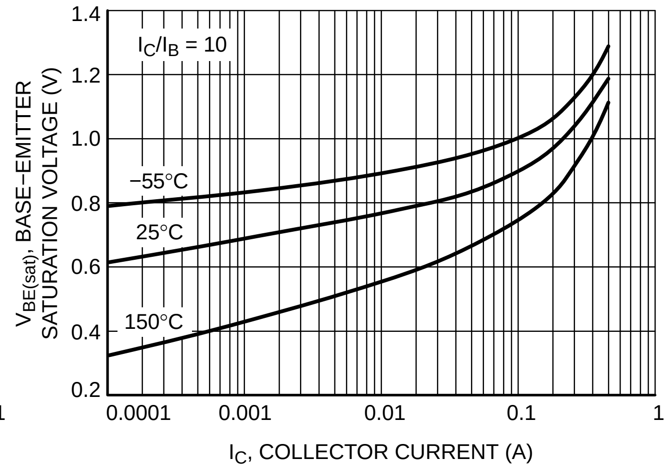


Figure 5. Base Emitter Saturation Voltage vs. Collector Current

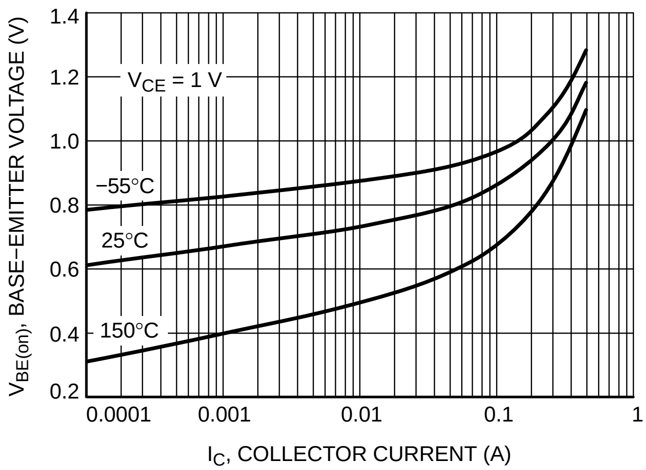


Figure 6. Base Emitter Voltage vs. Collector Current

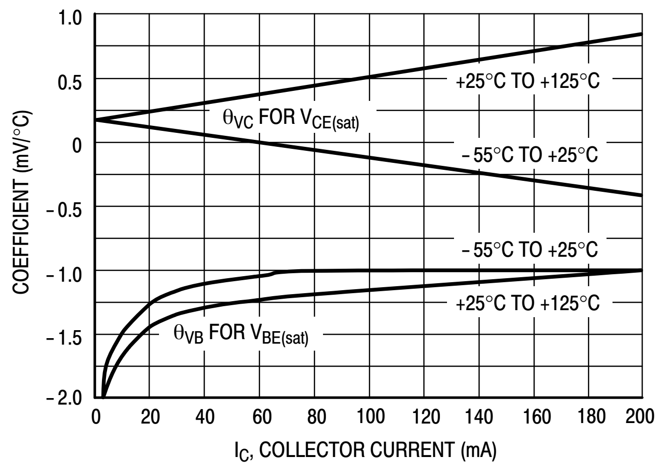


Figure 7. Temperature Coefficients

TYPICAL CHARACTERISTICS − Q2

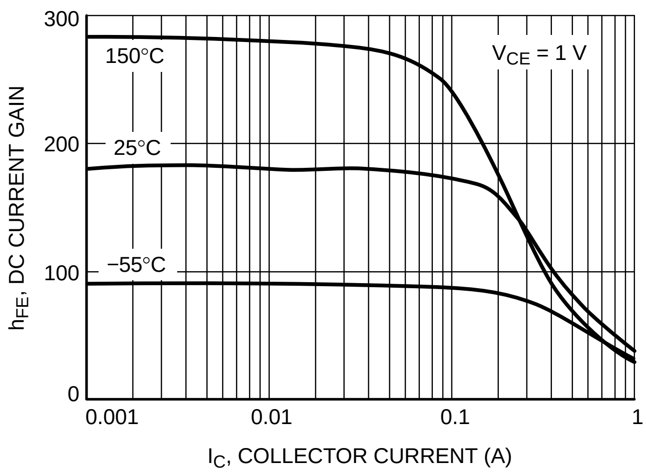


Figure 8. DC Current Gain vs. Collector Current

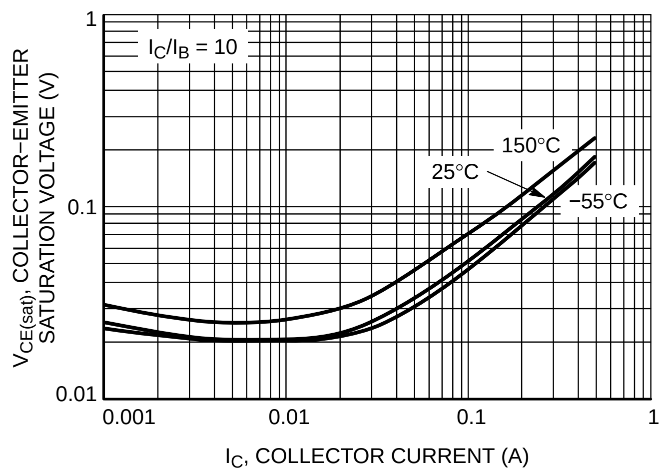


Figure 9. Collector Emitter Saturation Voltage vs. Collector Current

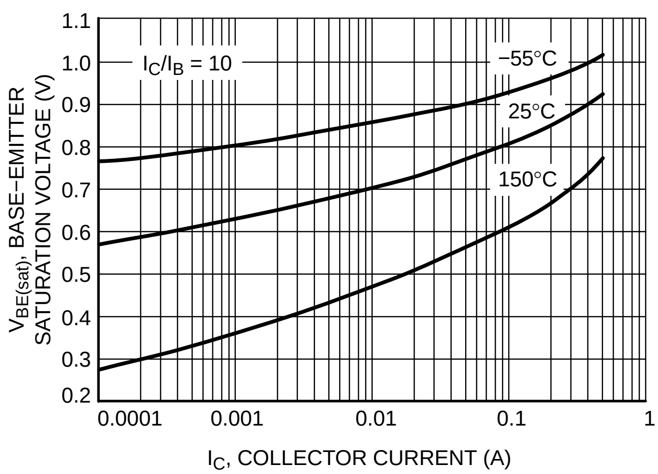


Figure 10. Base Emitter Saturation Voltage vs. Collector Current

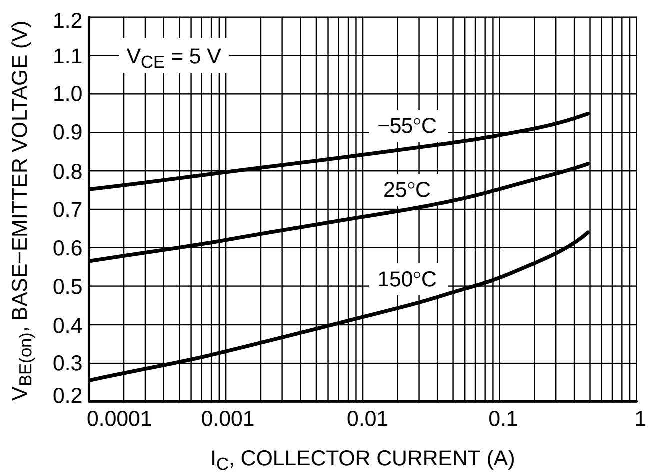


Figure 11. Base Emitter Voltage vs. Collector Current

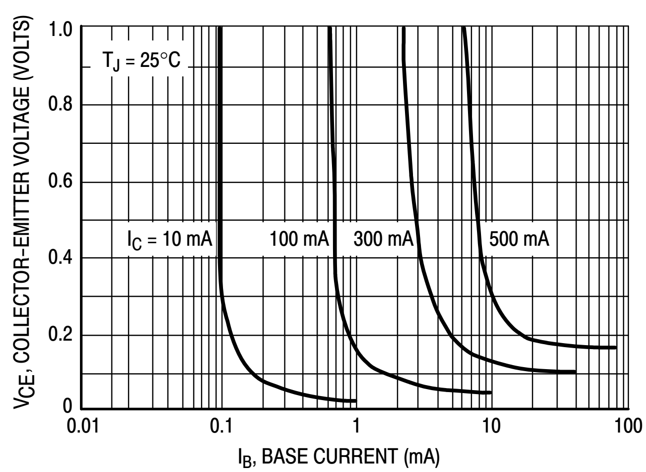
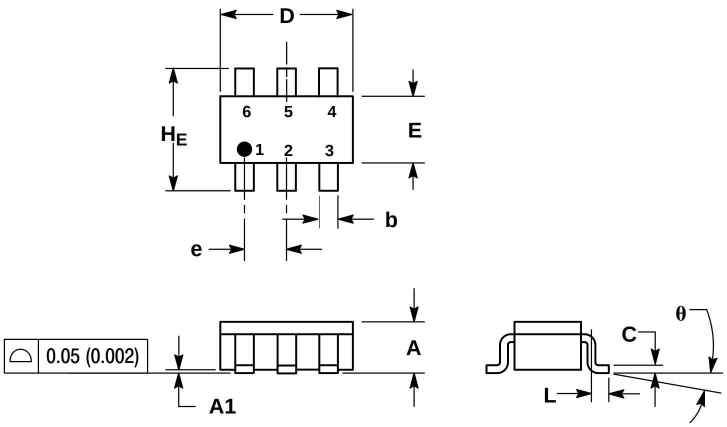


Figure 12. Saturation Region

PACKAGE DIMENSIONS

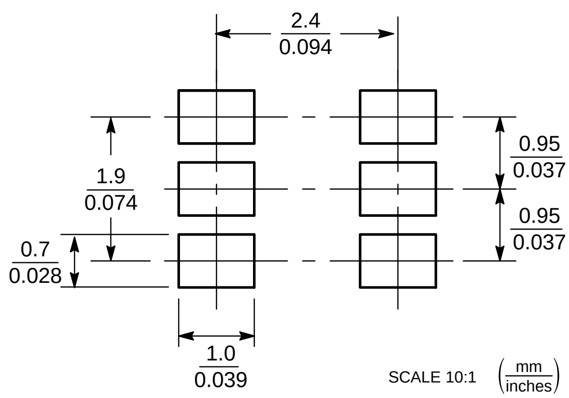
SC−74
CASE 318F−05
ISSUE N



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318F−01, −02, −03 OBSOLETE. NEW STANDARD 318F−04.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.25	0.37	0.50	0.010	0.015	0.020
c	0.10	0.18	0.26	0.004	0.007	0.010
D	2.90	3.00	3.10	0.114	0.118	0.122
E	1.30	1.50	1.70	0.051	0.059	0.067
e	0.85	0.95	1.05	0.034	0.037	0.041
L	0.20	0.40	0.60	0.008	0.016	0.024
H_E	2.50	2.75	3.00	0.099	0.108	0.118
θ	0°	−	10°	0°	−	10°

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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