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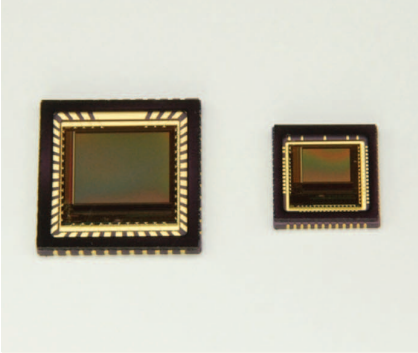
CMOS area image sensors



S11661 S11662

APS (active pixel sensor) type with high near infrared sensitivity

The S11661 and S11662 are APS type CMOS area image sensors with a high sensitivity in the near infrared region. The S11661 is SXGA format type (1280 x 1024 pixels), and the S11662 is VGA format type (640 x 480 pixels). Both types include a timing generator, a bias generator and an A/D converter, and offer digital input/output for easy handling.

Features

- **S11661: 1280 × 1024 pixels**
  S11662: 640 × 480 pixels
- **Pixel size: 7.4 × 7.4 µm**
- **Rolling/global shutter readout**
- **3.3 V single power supply operation**
- **High-speed partial readout function**

Applications

- **Security (infrared camera, palm vein certification)**
- **Position and shape recognition of infrared spot light**

Structure

Parameter	S11661	S11662	Unit
Image size (H × V)	9.472 × 7.578	4.736 × 3.552	mm
Pixel size	7.4 × 7.4		µm
Pixel pitch	7.4		µm
Number of total pixels (H × V)	1320 × 1064	680 × 520	pixels
Number of effective pixels (H × V)	1280 × 1024	640 × 480	pixels
Number of light-shielded lines	Upper and left parts: 8 each Lower and right parts: 32 each		lines
Fill factor	33		%
Package	Ceramic		-
Window material*1 *2	Borosilicate glass (without anti-reflective coating)		-

*1: Resin sealing
*2: Reflactive index=1.523

Absolute maximum ratings

Parameter	Symbol	Condition	Value	Unit
Supply voltage	Vdd(A), Vdd(D)	Ta=25 °C	-0.3 to +4.2	V
Input voltage*3	Vi	Ta=25 °C	-0.3 to +4.2	V
Vcp_out terminal voltage	Vcp_out	Ta=25 °C	-0.3 to +6.5	V
Operating temperature*4	Topr		-10 to +65	°C
Storage temperature*4	Tstg		-10 to +85	°C
Reflow soldering conditions*5	Tsol		Peak temperature 260 °C, 3 times (see P.8)	-

*3: SPI_data, SPI_clk, SPI_enable, MCLK, Vref1 to 9, Vr, Vcp_in, All_reset, MST, SPI_reset
*4: No dew condensation
When there is a temperature difference between a product and the surrounding area in high humidity environment, dew condensation may occur on the product surface. Dew condensation on the product may cause deterioration in characteristics and reliability.
*5: JEDEC level 3 (S11661), JEDEC level 2a (S11662)
Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

Recommended terminal voltage (Ta=25 °C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Supply voltage		Vdd(A), Vr	3.0	3.3	3.6	V
I/O supply voltage		Vdd(D), Vcp_in	3.0	Vdd(A)	3.6	V
Digital input terminal voltage	High level	Vsigi(H)	Vdd(D) - 0.25	Vdd(D)	Vdd(D) + 0.25	V
	Low level	Vsigi(L)	0	-	0.4	

Electrical characterisitics [Ta=25 °C, Vdd(A)=Vdd(D)=3.3 V]

Parameter		Symbol	Min.	Typ.	Max.	Unit
Master clock pulse frequency		f(MCLK)	1 M	-	25 M	Hz
Video data rate		VR		1/2 × f(MCLK)		Hz
Digital output voltage	High level	Vsigo(H)	Vdd(D) - 0.25	Vdd(D)	-	V
	Low level	Vsigo(L)	-	0	0.25	
Current consumption*6	Analog terminal*7	I1	-	47	55	mA
	Digital terminal*8	I2	-	25 (S11661) 19 (S11662)	45 (S11661) 35 (S11662)	

*6: Master clock pulse frequency: 25 MHz, frame rate: 8 frames/s (S11661), 30 frames/s (S11662), load capacitance of each output terminal: 5 pF
*7: Sum of Vdd(A) and Vr terminals
*8: Sum of Vdd(D) and Vcp_in terminals

Electrical and optical characterisitics [Ta=25 °C, Vdd(A)=Vdd(D)=3.3 V, Gain=1 times]

Parameter			Symbol	Min.	Typ.	Max.	Unit
Spectral response range			λ		400 to 1000		nm
Peak sensitivity wavelength			λp	-	760	-	nm
Photosensitivity*9			Sw	10	13	-	V/lx·s
Photoresponse nonuniformity*10			PRNU	-	-	4	%
Dark output*11 *12			Vdark	-	60	180	mV/s
Saturation output voltage			Vsat	1.4	1.6	-	V
Saturation exposure			Lsat	0.1	0.12	-	lx·s
Linearity			LR	-	-	±10	%
Image lag			Lag	-	-	0.1	%
Random noise*12	Rolling shutter mode		RN(RS)	-	1000	1500	μV rms
	Global shutter mode		RN(GS)	-	1500	2250	μV rms
Dynamic range	Rolling shutter mode		DR(RS)	59	64	-	dB
	Global shutter mode		DR(GS)	55	60	-	dB
Blemish	Point defect*13	White spots	WS	-	-	10	pixels
		Black spots	BS	-	-	10	pixels
	Cluster defect*14		ClsD	-	-	0	pieces
Line defect*15			DL	-	-	0	lines

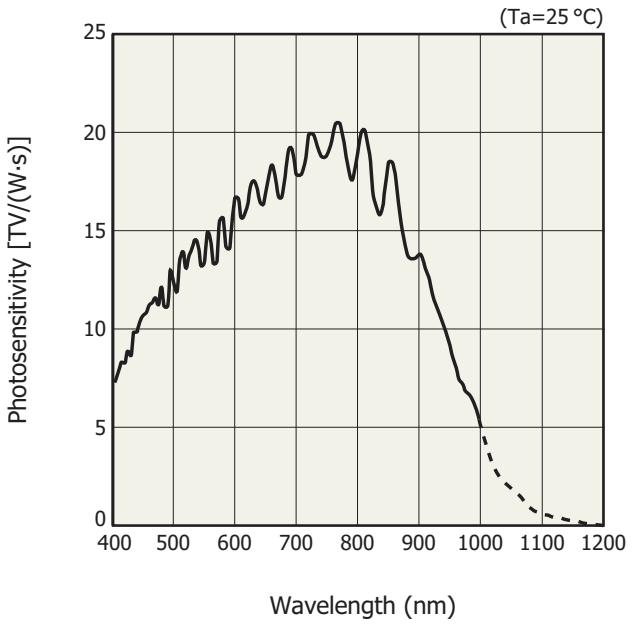
*9: White light 2856 K
*10: Photoresponse nonuniformity (PRNU) is the output nonuniformity that occurs when the photosensitive area is uniformly illuminated by white light which is approx. 50% of the saturation level. PRNU is calculated using the pixels excluding the pixels of the 10 outermost lines and defective pixels, and is defined as follows:
PRNU= ΔX/X × 100 (%)
X: average output of all pixels, ΔX: standard deviation of pixel output
*11: Average value of all effective pixels (excluding defective pixels). Rolling shutter mode
*12: Analog video output value
The final output from the image sensor is a 12-bit digital signal. When the gain is set to 1, the conversion voltage range (0 to 2 V) is A/D converted into 4096 gradation steps. So, 1 DN (digital number) is equal to 0.488 mV (=2000 mV/4096 DN).
*13: White spot=Pixels whose dark output exceeds 1800 mV/s
Black spot=Pixels whose sensitivity is less than 50% of the average sensitivity of adjacent pixels when the image sensor is illuminated with uniform white light that is approximately 50% of the saturation (excluding the outermost 10 lines in the effective pixel area)
*14: A defect consisting of two or more contiguous defective pixels
*15: Column defect and row defect
Column defect=A defect consisting of 10 or more contiguous defective pixels in one column
Row defect=A defect consisting of 10 or more contiguous defective pixels in one row

Electrical and optical characterisitics [A/D converter, Ta=25 °C, Vdd(A)=Vdd(D)=3.3 V]

Parameter	Symbol	Value	Unit
Resolution	RESO	12	bits
Conversion time	tCON	2/f(MCLK)	s
Conversion voltage range*16	-	0 to 2	V

*16: Gain=1

Spectral response (typical example)



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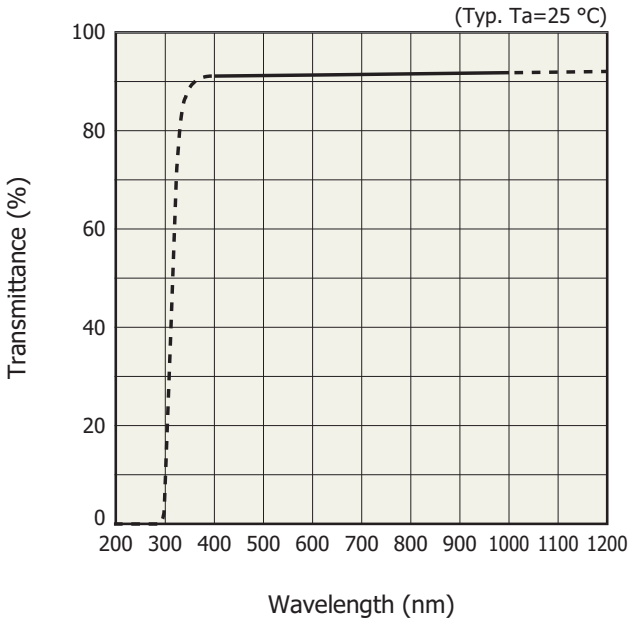
Spectral transmittance characteristics of window material



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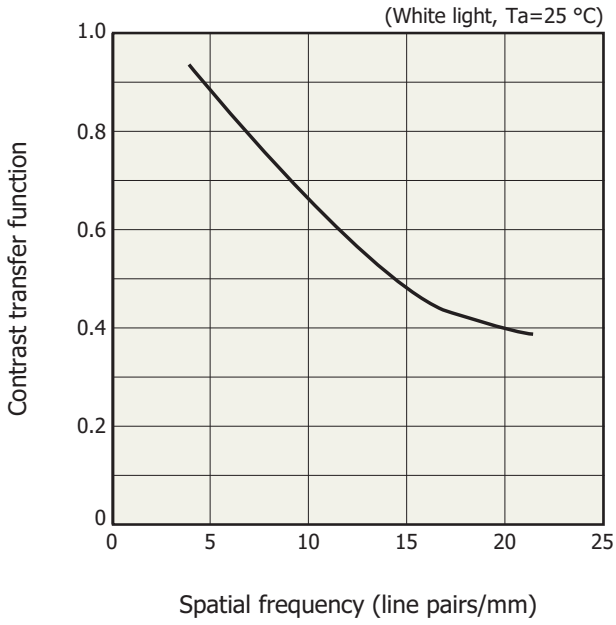
Contrast transfer function vs. spatial frequency (typical example)



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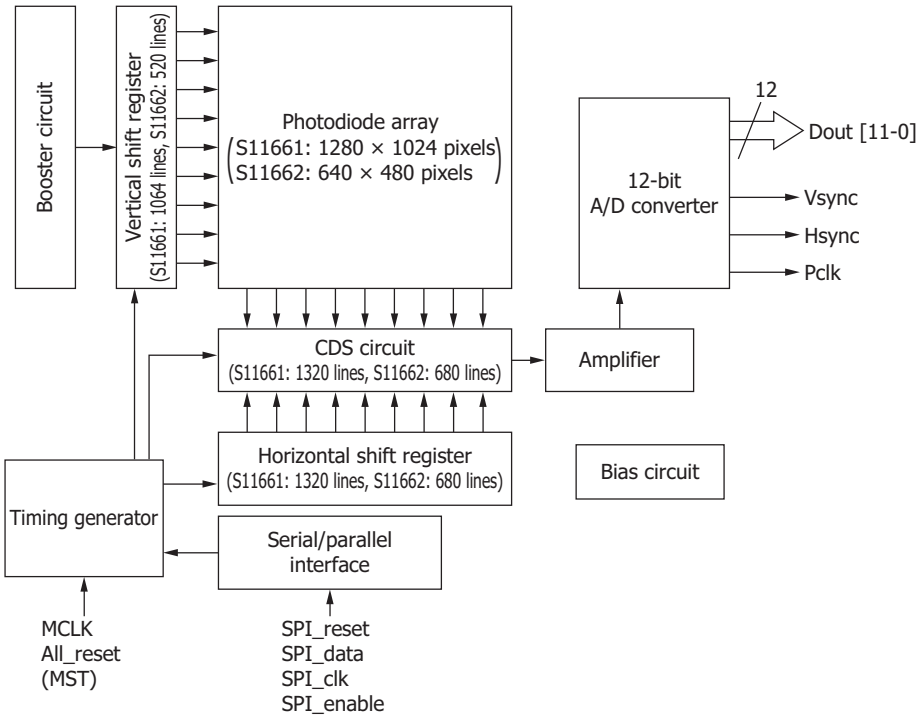
Block diagram



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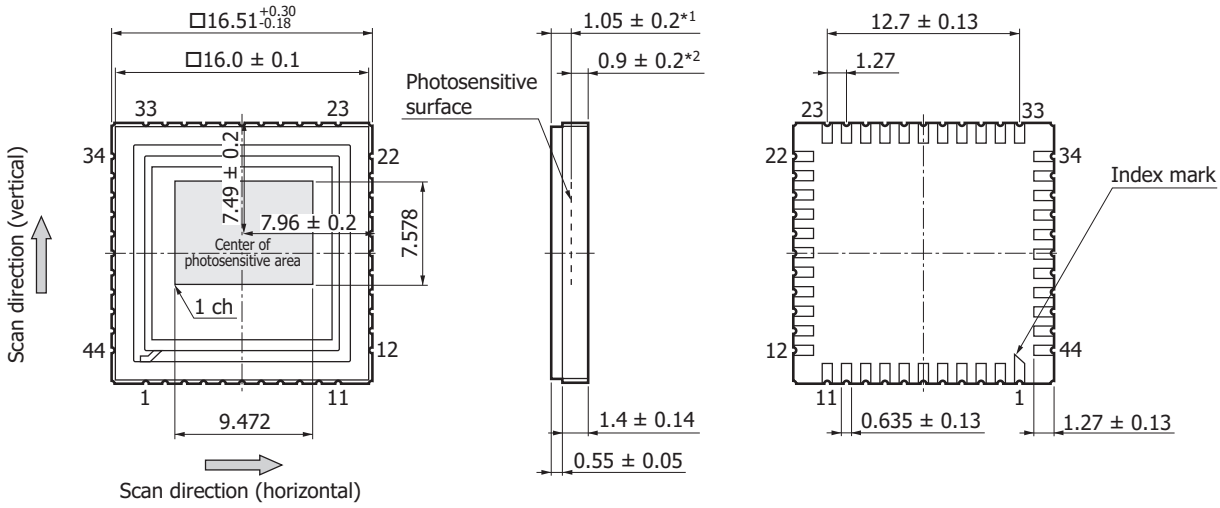
Dimensional outlines (unit: mm)

S11661



Angle accuracy of effective pixels: ±2.4°
Weight: 1.4 g
*1: Distance from upper surface of window to photosensitive surface
*2: Distance from package bottom to photosensitive surface

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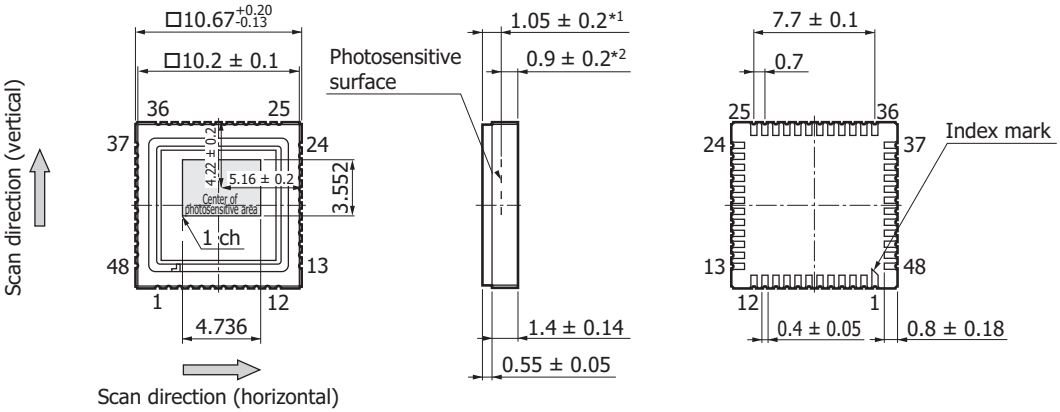
S11662



Angle accuracy of effective pixels: ±3.15 °
Weight: 0.5 g
*1: Distance from upper surface of window to photosensitive surface
*2: Distance from package bottom to photosensitive surface

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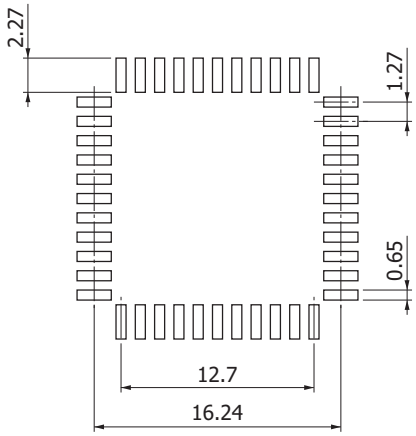
Land pattern examples (unit: mm)

S11661



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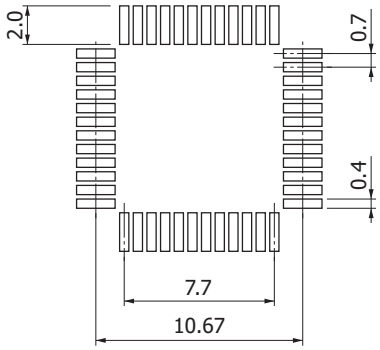
S11662



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Pin connections

S11661

Pin no.	Symbol	Description	I/O
1	GND	Ground	I
2	SPI_data	Data signal for serial/parallel interface	I
3	SPI_clk	Clock signal for serial/parallel interface	I
4	SPI_enable	Enable signal for serial/parallel interface	I
5	MCLK	Master clock signal	I
6	Vdd(A)	Supply voltage (3.3 V)	I
7	Dout11	Video output signal (MSB)	O
8	Dout10	Video output signal	O
9	Dout9	Video output signal	O
10	Dout8	Video output signal	O
11	Dout7	Video output signal	O
12	Vdd(D)	Supply voltage (3.3 V)	I
13	Dout6	Video output signal	O
14	Dout5	Video output signal	O
15	Dout4	Video output signal	O
16	Dout3	Video output signal	O
17	Dout2	Video output signal	O
18	Dout1	Video output signal	O
19	Dout0	Video output signal (LSB)	O
20	Vref1	Bias voltage for A/D converter*17	I
21	Vref2	Bias voltage for A/D converter*17	I
22	Vref3	Bias voltage for A/D converter*17	I
23	Vref4	Bias voltage for A/D converter*17	I
24	Vref5	Bias voltage for A/D converter*17	I
25	Vr	Supply voltage (3.3 V)*18 *19	I
26	GND	Ground	I
27	Vcp_in	Supply voltage (3.3 V)*18 *20	I
28	Vdd(A)	Supply voltage (3.3 V)	I
29	Vcp_out	Bias voltage for booster circuit*21	I
30	Vr	Supply voltage (3.3 V)*18 *19	I
31	Vref6	Bias voltage for CDS circuit*17	I
32	NC	No connection	-
33	Vref7	Bias voltage for CDS circuit*17	I
34	Vref8	Bias voltage for amplifier*17	I
35	Vref9	Bias voltage for amplifier*17	I
36	All_reset	All reset pulse signal	I
37	MST	Master start signal	I
38	Pclk	Pixel output synchronization signal	O
39	Hsync	Line synchronization signal	O
40	Vsync	Frame synchronization signal	O
41	Vdd(D)	Supply voltage (3.3 V)	I
42	Vdd(A)	Supply voltage (3.3 V)	I
43	NC	No connection	-
44	SPI_reset	Reset signal for serial/parallel interface	I

*17: Terminal for monitoring the bias voltage generated in the chip. To reduce noise, insert a capacitor of about 1 µF between the ground and each terminal.
*18: To reduce noise, insert a capacitor of about 0.1 µF and an electrolytic capacitor of about 22 µF/25 V between the ground and each terminal.
*19: Connect this terminal to Vdd(A).
*20: Connect this terminal to Vdd(D).
*21: Voltage of approx. 5.5 V, which was boosted by the chip's internal booster circuit, appears at the terminal. To maintain the voltage, insert a capacitor of about 1 µF between the ground and Vcp_out.

S11662

Pin no.	Symbol	Description	I/O
1	SPI_enable	Enable signal for serial/parallel interface	I
2	NC	No connection	-
3	Dout11	Video output signal (MSB)	O
4	Dout10	Video output signal	O
5	Dout9	Video output signal	O
6	Dout8	Video output signal	O
7	Dout7	Video output signal	O
8	Dout6	Video output signal	O
9	Dout5	Video output signal	O
10	Dout4	Video output signal	O
11	Dout3	Video output signal	O
12	Vdd(D)	Supply voltage (3.3 V)	I
13	Vdd(A)	Supply voltage (3.3 V)	I
14	Dout2	Video output signal	O
15	Dout1	Video output signal	O
16	Dout0	Video output signal (LSB)	O
17	Vref1	Bias voltage for A/D converter*22	I
18	Vref2	Bias voltage for A/D converter*22	I
19	Vref3	Bias voltage for A/D converter*22	I
20	Vref4	Bias voltage for A/D converter*22	I
21	Vref5	Bias voltage for A/D converter*22	I
22	GND	Ground	I
23	Vref6	Bias voltage for CDS circuit*22	I
24	Vref7	Bias voltage for CDS circuit*22	I
25	Vref8	Bias voltage for amplifier*22	I
26	NC	No connection	-
27	Vcp_in	Supply voltage (3.3 V)*23 *24	I
28	Vr	Supply voltage (3.3 V)*23 *25	I
29	NC	No connection	-
30	NC	No connection	-
31	NC	No connection	-
32	NC	No connection	-
33	GND	Ground	I
34	Vr	Supply voltage (3.3 V)*23 *25	I
35	Vcp_out	Bias voltage for booster circuit*26	I
36	All_reset	All reset pulse signal	I
37	MCLK	Master clock signal	I
38	MST	Master start signal	I
39	Pclk	Pixel output synchronization signal	O
40	Hsync	Line synchronization signal	O
41	Vsync	Frame synchronization signal	O
42	Vref9	Bias voltage for amplifier*22	I
43	Vdd(A)	Supply voltage (3.3 V)	I
44	Vdd(D)	Supply voltage (3.3 V)	I
45	GND	Ground	I
46	SPI_reset	Reset signal for serial/parallel interface	I
47	SPI_data	Data signal for serial/parallel interface	I
48	SPI_clk	Clock signal for serial/parallel interface	I

*22: Terminal for monitoring the bias voltage generated in the chip. To reduce noise, insert a capacitor of about 1 µF between the ground and each terminal.
*23: To reduce noise, insert a capacitor of about 0.1 µF and an electrolytic capacitor of about 22 µF/25 V between the ground and each terminal.
*24: Connect the terminal to Vdd(D).
*25: Connect the terminal to Vdd(A).
*26: Voltage of approx. 5.5 V, which was boosted by the chip's internal booster circuit, appears at the terminal. To maintain the voltage, insert a capacitor of about 1 µF between the ground and Vcp_out.

Precautions

(1) Electrostatic countermeasures
This device has a built-in protection circuit against static electrical charges. However, to prevent destroying the device with electrostatic charges, take countermeasures such as grounding yourself, the workbench and tools to prevent static discharges.
Also protect this device from surge voltages which might be caused by peripheral equipment.

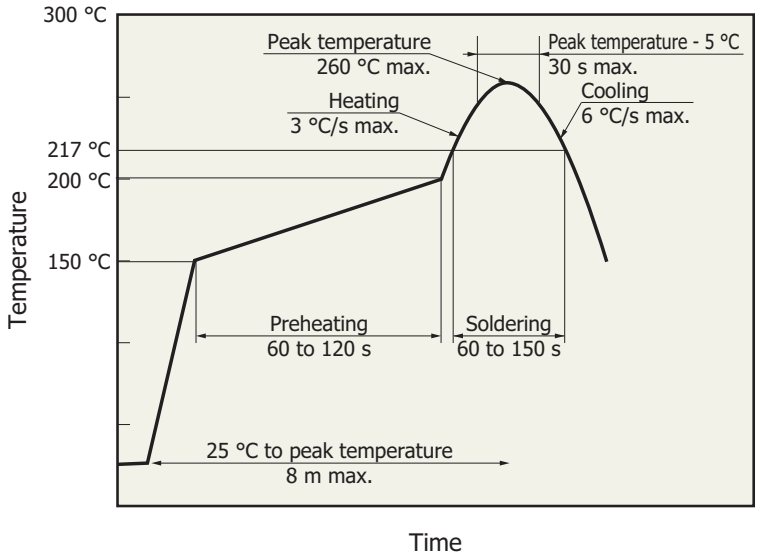
(2) Incident window
If dust or dirt gets on the light incident window, it will show up as black blemishes on the image. When cleaning, avoid rubbing the window surface with dry cloth or dry cotton swab, since doing so may generate static electricity. Use soft cloth, paper or a cotton swab moistened with alcohol to wipe dust and dirt off the window surface. Then blow compressed air onto the window surface so that no spot or stain remains.

(3) Soldering by hand
To prevent damaging the device during soldering, take precautions to prevent excessive soldering temperatures and times.
Soldering should be performed within 5 seconds at a soldering temperature below 260 °C.

(4) Reflow soldering
Soldering conditions may differ depending on the board size, reflow furnace, etc. Check the conditions before soldering. A sudden temperature rise and cooling may be the cause of trouble, so make sure that the temperature change is within 4 °C per second.
The bonding portion between the ceramic base and the glass may discolor after reflow soldering, but this has no adverse effects on the hermetic sealing of the product.

(5) UV exposure
This product is not designed to prevent deterioration of characteristics caused by UV exposure, so do not expose it to UV light.

Recommended temperature profile for reflow soldering (typical example)



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- This product supports lead-free soldering. After unpacking, store it in an environment at a temperature of 30 °C or less and a humidity of 60% or less, and perform soldering within 168 hours (S11661) or 4 weeks (S11662).
- The effect that the product receives during reflow soldering varies depending on the circuit board and reflow oven that are used. Before actual reflow soldering, check for any problems by tesitng out the reflow soldering methods in advance.

Recommended baking conditions

Refer to the precautions of "Surface mount type products."

Related information

www.hamamatsu.com/sp/ssd/doc_en.html

■ Precautions

· Disclaimer
· Image sensors
· Surface mount type products

Hamamatsu provides technical information of this product. Please contact our sales office.

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