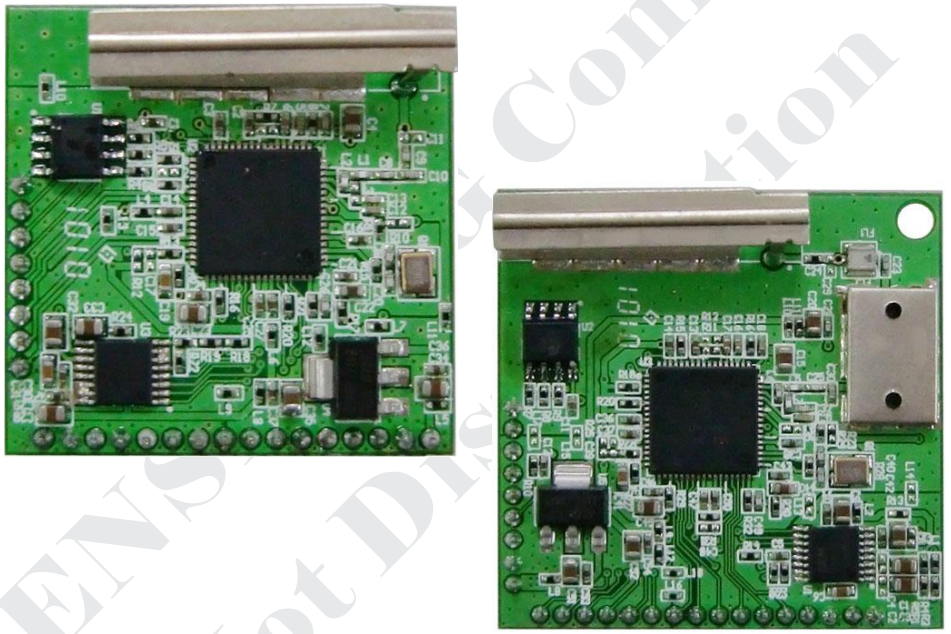
WENSHING®©

WS-AUDIO24-0005-TX
WS-AUDIO24-0005-RX

Wireless Audio core Module



Version History

Version	Date	Changes
V1.0	Jul.15, 2010	1st. Edition

Content

1. Introduction

WS-AUDIO24-0005-TX/ WS-AUDIO24-0005-RX Wireless Audio core Module is a highly integrated digital core module. By meaning of the Intelligent Wireless technology is developed by Syncomm. It can provide high quality wireless audio for the users. Supporting multiple interfaces such as I2S, USB, embedded RF IC and other key blocks such as I2C control interface, voltage detector.

IA2E wireless audio module provides dual transmitter and receiver modes, which enables the seamless transmission of high quality audio.

In the transmitter, Tx receives digitized stereo as input, which is packetized and processed for
synchronization and data integrity. After that, the data are modulated and radiated at 2.4 GHz ISM band.

In the receiver, Rx receives RF signal, demodulated and processed to restore the transmitted signal, and then streamed as digital audio output.

2. Key Features

2.1 RF Features

- Worldwide 2.4 GHz ISM band operation by 2406 MHz ~ 2472MHz.
- Up to 2 Mbps RF data rate
- GFSK modulation.
- Long distance > 30m (Line of sight)
- Broadcasting mode
- RF frequency hopping in 34 channels
- Embedded uP/MAC mode settings IA2E RF normal operation mode that support 15 hopping
  channel/Per Sequence. It is included 4 Sequence group/per system. Details refer to the page.12 “6.2 RF Operation Principle”
- According FHSS specification protocol.

2.2 Audio Quality and Interface

- Support Compressed audio
- Analog output: THD+N up to -70dB, SNR up to 85dB.
- Support I2S (Audio In/Out) and USB (Tx Audio Input) with 2 channels downstream.
- Support I2S downstream 32/44.1/48KHz at resolution of 16 bits (2 channels).
- IA2E wireless audio module that support in master mode for Tx and Rx audio interface.
- Control Channel (CCH) up to 2 kbps for downstream by I2C interface via wireless.
- USB 1.1 device controller, Supports LPCM and compressed format at 16-bit 2-channels at sampling frequency of 32, 44.1, and 48KHz downstream.

2.3 General Features

- Programmable audio latency 20ms/50ms(default: ~40ms)
- Integrated pipelined 8-bit CPU, with embedded 4K bytes program RAM, with embedded RFIC in IA2E audio processor.
- Serial 4K byte EEPROM for Boot Register Update.
  I2C interface support blank EEPROM code download, External I2C device read/write, and data.

2.4 Tx Charging Features (Option)

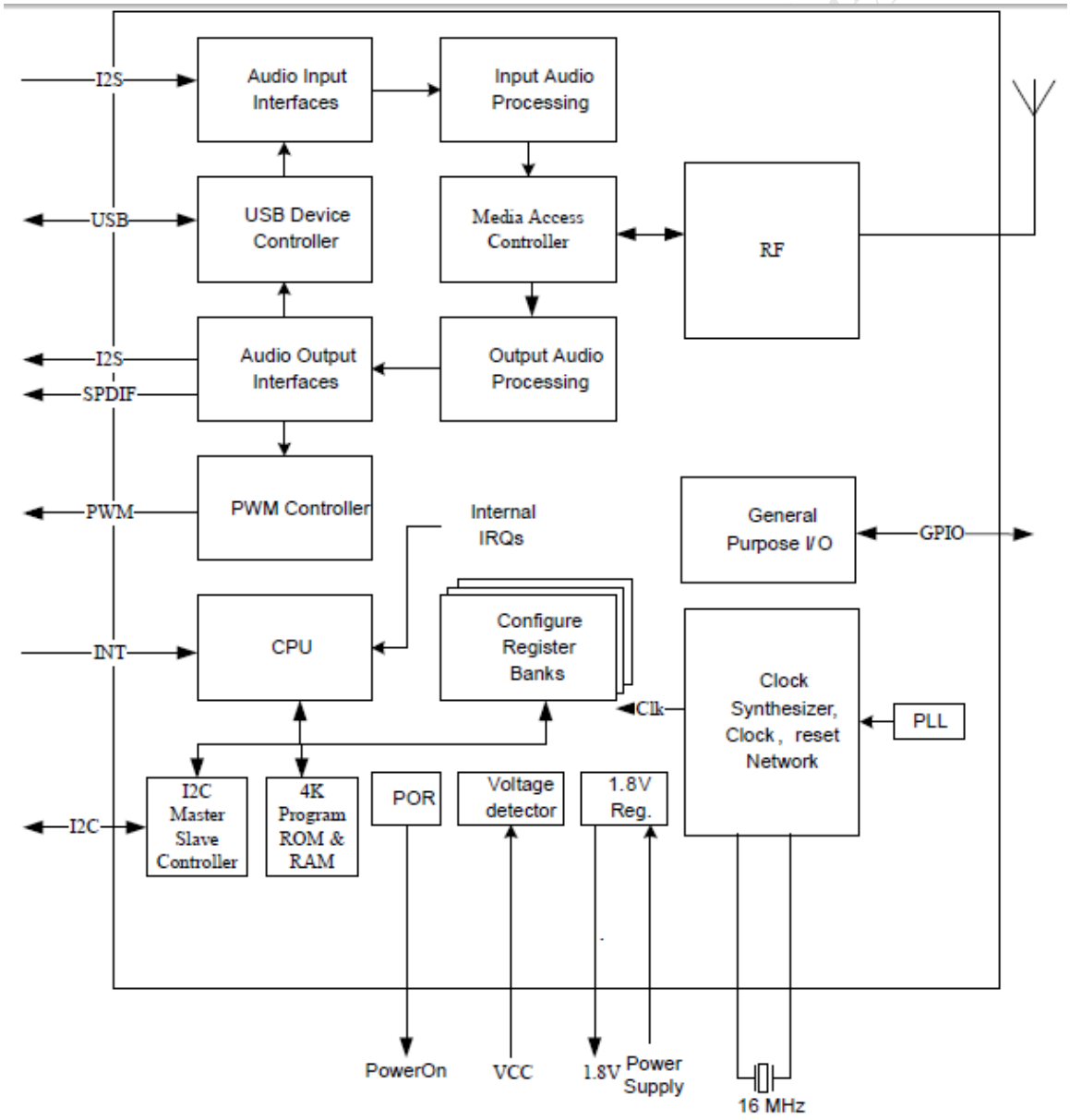
- Support Rechargeable “AAA” size Ni-MH battery for 900mAH to 1000mAH capacity by Tx module internal charging circuit and firmware control.

3. Applications

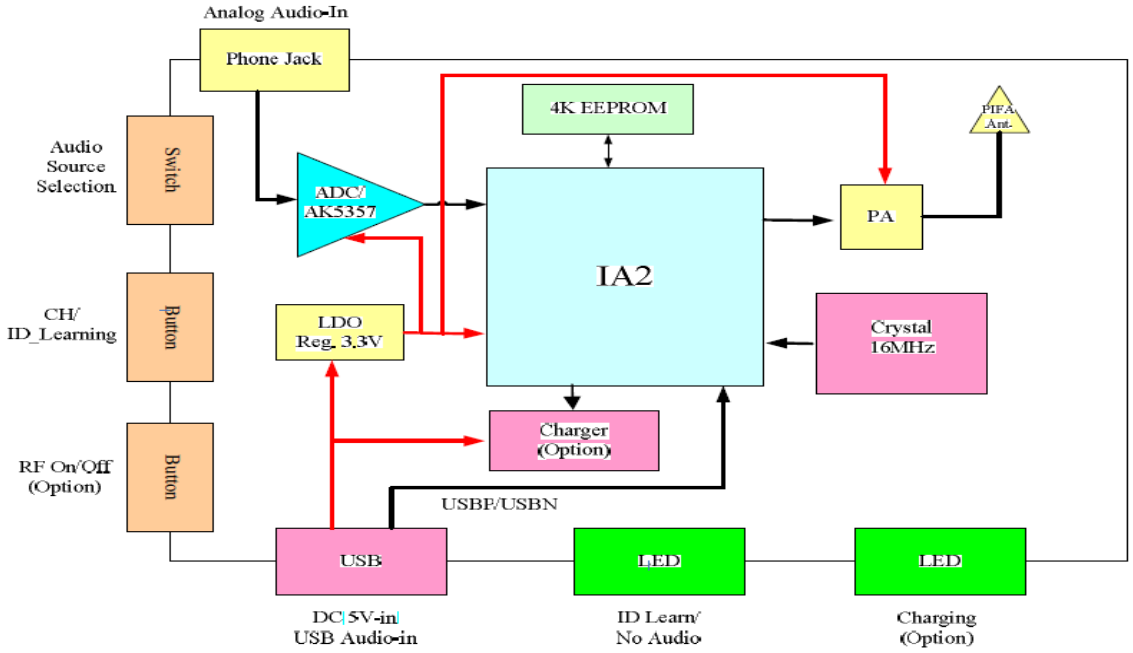
- Wireless Headphone
- Wireless HTiB
- Wireless Mini-Combo
- Wireless Outdoor Speaker
- Wireless Audio Sender

4. Block Diagram

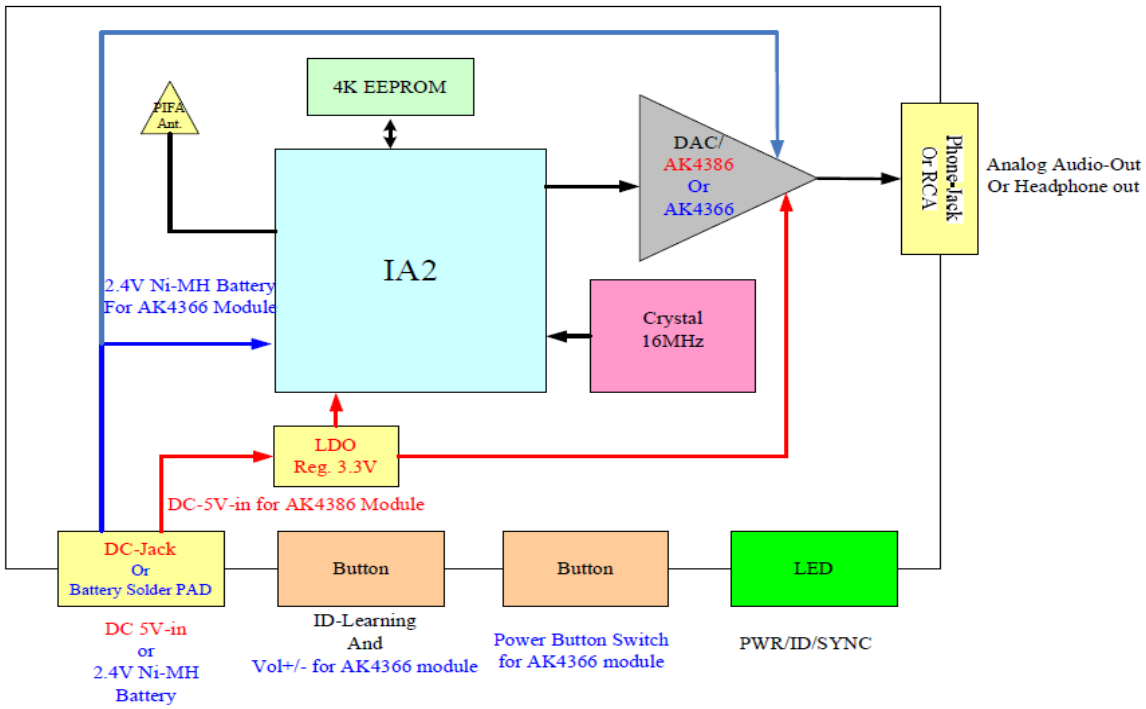
4.1 IC Block Diagram



4.2 Tx Module



4.3 Rx Module



5. Feature Table

Module List	Tx -AK5357 Module	Rx-AK4386 Module
Application	Wireless transmitter	Speaker
Features	Transmitter	Receiver
Audio Processor	QFN68 10*10mm	QFN68 10*10mm
RF IC	Embedded to IA2	Embedded to IA2
Codec	ADC/AK5357	DAC/AK4386
Antenna	PIFA	PIFA
PA/LNA	AP1110	-
Audio Input	I^2S in * 1	-
Audio Output	-	I^2S out * 1
USB 1.1	Yes	-
SNR(dB) @ 1KHz	-96	-95
THD+N(dB) @ 1KHz	-80	-70
Power Consumption	170mA @ 3.3V	40mA @ 3.3V
RF Output Power(Typ.)	16dBm	-
RF Sensitivity(Typ.)	-	-78dBm

6. Functional Operation Principle

6.1 Audio Interface

6.1.1. Analog Audio - I2S Interface

IA2E I2S audio interface can work for master and slave mode. In master mode, IA2E generate SYSCLK/LRCK/BCK for external audio codec. In slave mode, IA2E accept external SYSCLK/LRCK/BCK signal. IA2E will synchronize with external audio clock.

Master mode:

The SYSCLK pin can generate 512 fs or 256 fs clock for external I2S components. Table 6-1 shows system clock format. The SYSCLK can be set by firmware.

LRCK(kHz)	SYSCLK(MHz)		BCK(MHz)
fs	256fs	512fs	64fs
8	2.048	4.096	0.512
32	8.192	16.384	2.048
44.1	11.2896	22.5792	2.8224
48	12.288	24.576	3.072

Table 6-1 I2S sample formats

The support audio formats are 16 bits per sample. I2S formats. Supported sampling frequencies are 8, 32, 44.1 and 48KHz. There are 32 BCK bit clocks per left and right channel select LRCK in both master mode or slave mode. The IA2E supported I2S sample and interface formats are listed in the tables 6-2/6-3 as below:

Bits/Sample	8 KHz	32 KHz	44.1 KHz	48 KHz
1 Channel	16	16	16	16
2 Channels	16	16	16	16

Table 6-2 I2S sample formats

BCK/LRCK	TX audio input	RX audio output
	I^2S	I^2S
Master mode	64 fs	64 fs
Slave mode	64 fs	64fs

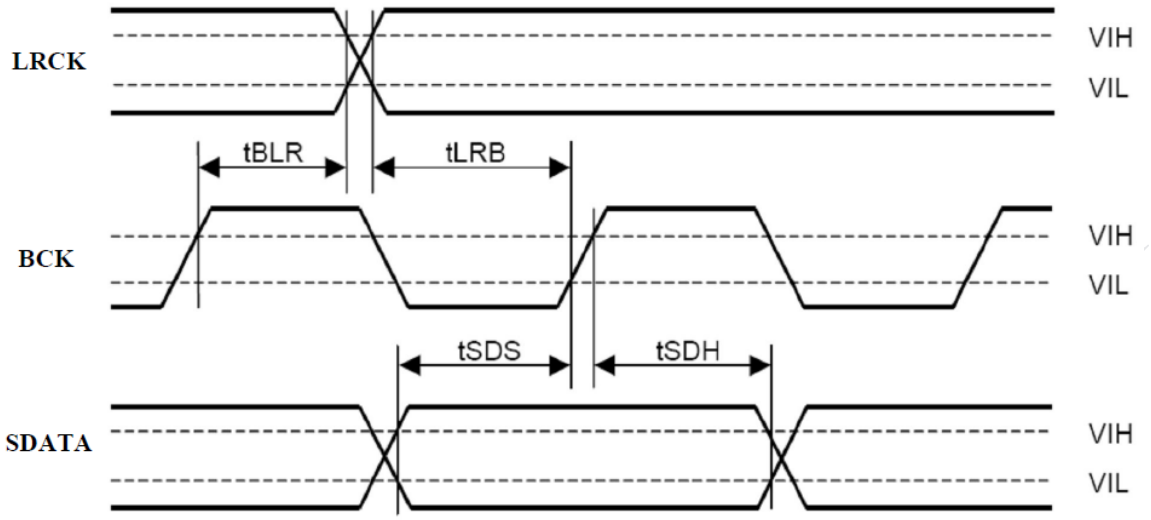
Table 6-3 I2S interface formats

For 1 channel modes, the audio is delivered on left channel of interface 0; for 2 channel modes, audio is on interface 0.This is recommended to set sampling rate at 48KHz for master mode.

Slave mode:

The I2S slave mode can only work for 48KHz sampling rate. IA2E only need BCK and LRCK for I2S synchronization, the external SYSCLK is not required

I2S timing chart as followed,



6.1.2. USB Device Interface

The USB device controller is Universal Serial Bus Specification Revision 1.1 compliant and supports Universal Serial Bus Device Class Definition for Audio Devices Revision 1.0. In addition it implements endpoints for Human Interface Device (HID).
It supports one Control endpoint, two Isochronous-Out endpoint, one Isochronous-In endpoint, and one bi-directional Interrupt-In endpoint. In addition to endpoint 0, there are three interfaces; interface 1 consists of 3 alternate settings for PCM or non-PCM audio of different sampling frequencies and number of channels; interface 2 consists of one alternate setting for PCM audio input, while interface 3 consists of an alternate setting for HID control.
The supported audio formats are linear PCM or non-PCM 32, 44.1 and 48KHz sampling rate with 16 bits resolution at 2 channels for playback; and 8kHz with 16bit resolution at 2 channels for recording. All data to/from the IA2E are transferred at full speed.

The USB End point summary as followed:

	Function	RAM size(Byte)
End Point 0	Control in	8
	Control out	16
End Point 1	Isochronous out	192 x 2
End Point 2	Isochronous in	32 x 2
End Point 4	Interrupt in	5
	Interrupt out	5

Table 6-4 IA2E supports I2S interface formats

6.2 RF Operation Principle

6.2.1 Carrier Frequency Separation

According the FCC rules part 15 subpart C15.247 frequency hopping system shall have hopping channel carrier frequency separated by a minimum of 25 KHz or 20dB bandwidth of the hopping channel. Channel separation 2 MHz @ per channel

6.2.2 Number of Hopping Frequencies

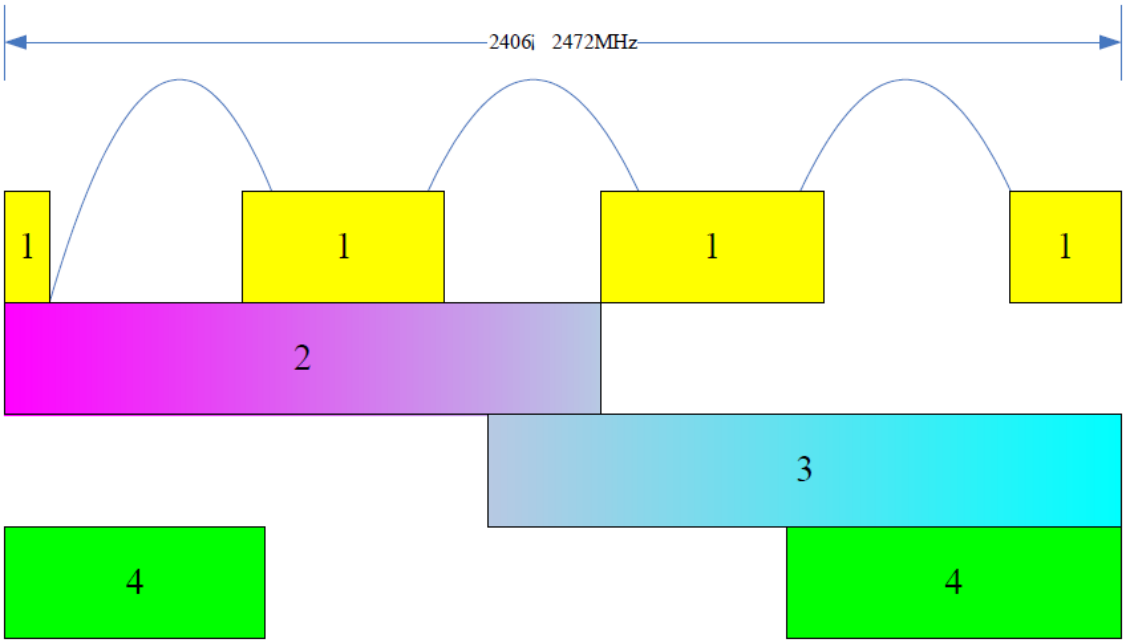
According the FCC rules part 15 subpart C15.247 frequency hopping systems operating in 2400~2483.5 KHz band that meet 15 hopping frequencies.

6.2.2.1 Pseudorandom Frequency Hopping Sequence

This module is controlled by microchip (IA2E embedded uP) to generate Pseudorandom Frequency Hopping Sequence. IA2E module RF normal operation mode support 15 hopping channel/Per Sequence.
There are four hopping sequences list as below:

Sequence 1: 2406, 2420, 2422, 2424, 2426, 2428, 2444, 2446, 2448, 2450, 2452, 2456, 2468, 2470, 2472 MHz
Sequence 2: 2406, 2408, 2410, 2412, 2414, 2416, 2418, 2420, 2422, 2424, 2426, 2428, 2430, 2438, 2446 MHz
Sequence 3: 2432, 2440, 2448, 2450, 2452, 2454, 2456, 2458, 2460, 2462, 2464,2466, 2468, 2470, 2472 MHz
Sequence 4: 2406, 2408, 2410, 2412, 2414, 2416, 2418, 2426, 2454, 2462, 2464, 2466, 2468, 2470, 2472 MHz

The reference diagram drawing as below:



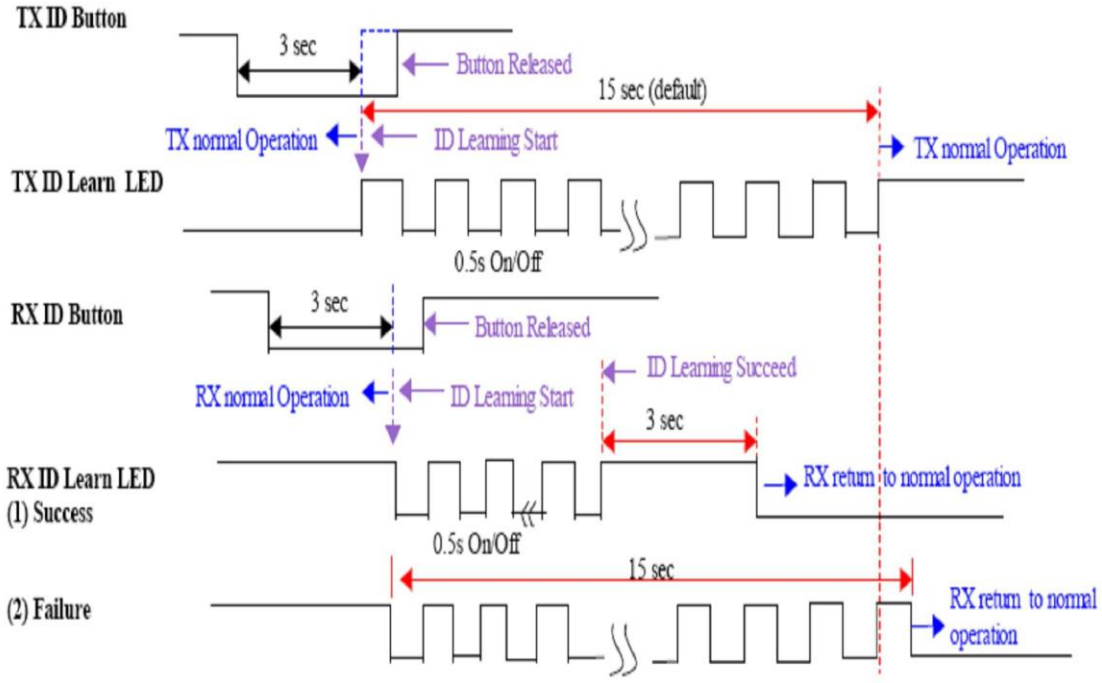
6.2.2.2 Coordination of hopping sequences to other transmitters

This transmitter does not have the ability of being coordinated with other FHSS system for as soon as the transmitter is in operation, the GFSK of modulation of hopping frequency will follow the selected hopping sequence to transmit independently and no coordination is possible. Especially, this transmitter is used as a PC¡s peripheral device, so no coordination of hopping frequency is required.

6.2.2.3 System Receiver Hopping Capability

There is one step to make the receiver to shift the frequency the frequencies in synchronization with transmitter signals.When simultaneously press the CH/ID button both Tx module and ID_LED blinks by 0.25s on/off, ID_Learning process will continue 15s, and Rx module longer than 3s, the ID_Learning will be enable, So the receiver will be able to shift the receiving frequencies in synchronization with the transmitter signals.

The reference diagram drawing as below :



6.2.2.4 Equal Hopping Frequency Use

Due to each the GFSK of modulation of hopping frequency will be transmitted in accordance to the frequency tables described above, there is no any frequency will be able to hop more times than other. Therefore each frequency will be used equally.

6.2.3 Time of Occupancy (Dwell Time)

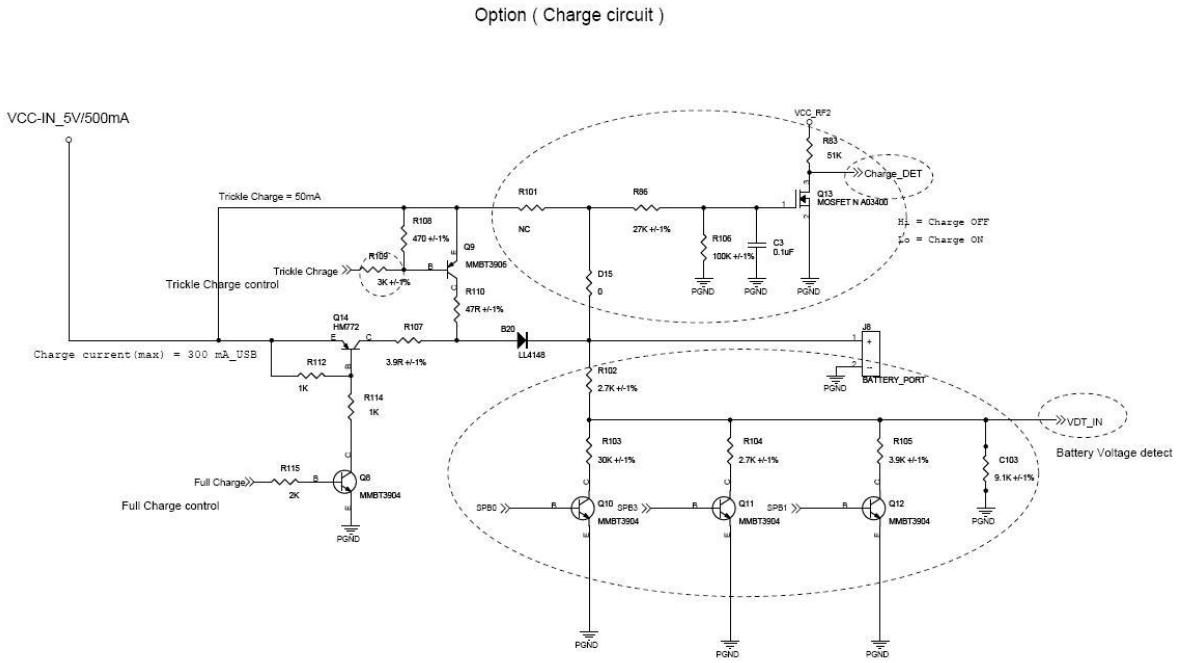
IA2E module operation frequency is in 2400 MHz ~ 2484.5MHz. In this band the average time of occupancy on any channel that required 0.4ms specification by multiplied by number of hopping channel employed. The IA2E module is on normal transmitting operation mode that time of occupancy is 3.84ms/per channel that according the 0.4ms specification. (3.84ms/per channel)

6.3 Charging Operation Principle (Tx module Option)

6.3.1 Features

- Support AAA 1.2V*2pcs (2.4V) Ni-MH rechargeable battery, capacity 900mAH ~1000mAH only.
- Automatic to judgment battery capacity for battery-recharge feature.
- Support full charge current by maximum 300mA and trickle charge by 50mA.
- Required minimum charging DC power input voltage/current by 5V/500mA.
- Support safety charging timer control.
- Smart to judgment non-rechargeable battery.
- Low cost charger function design.
- **Warning: The charger circuit that support Ni-MH rechargeable battery only, if long times to charged non-chargeable battery (Ex: Alkaline battery. and so on) that will be damage IA2E charging circuit and battery**.

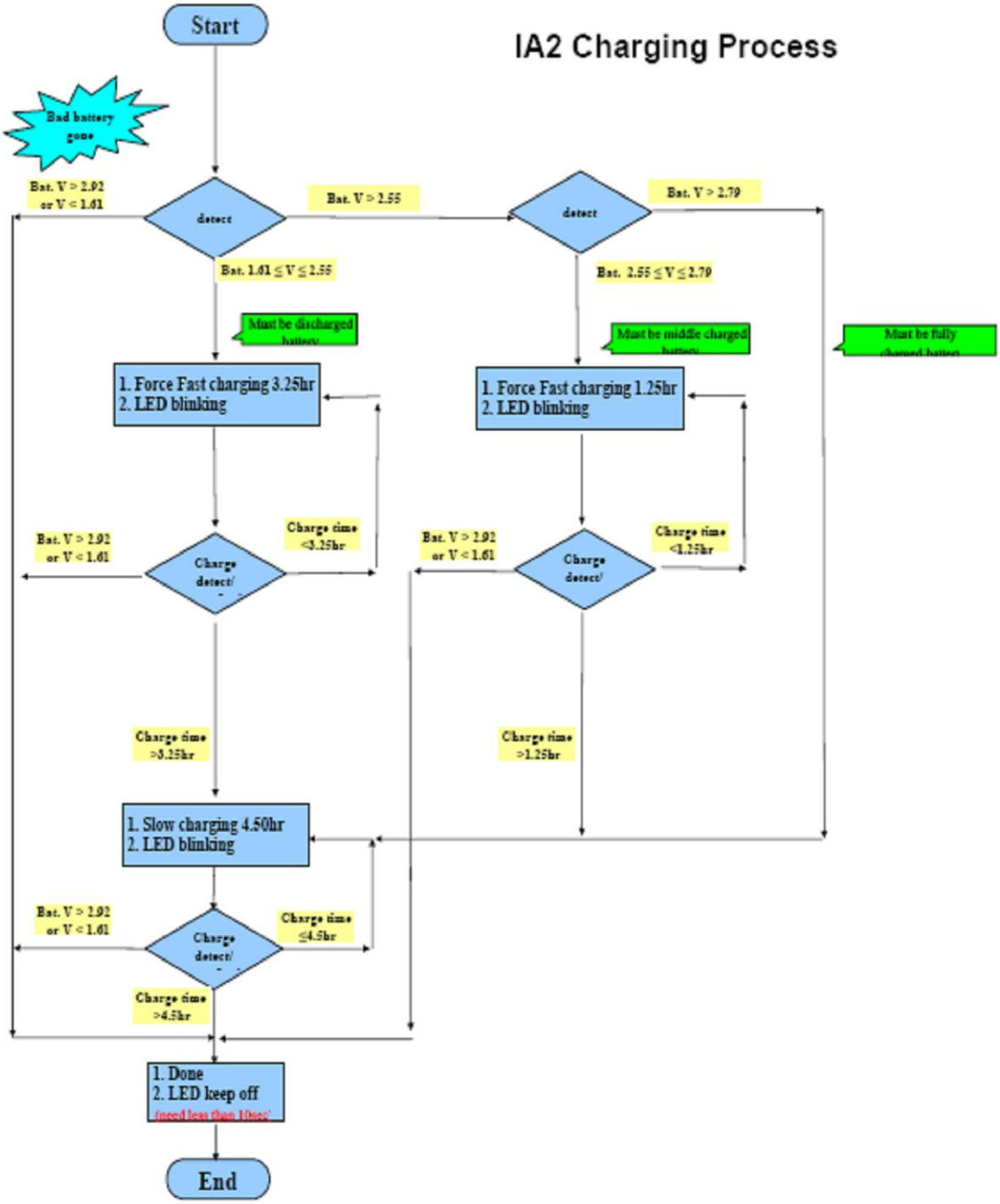
6.3.2 Design Reference Circuit: as the below,



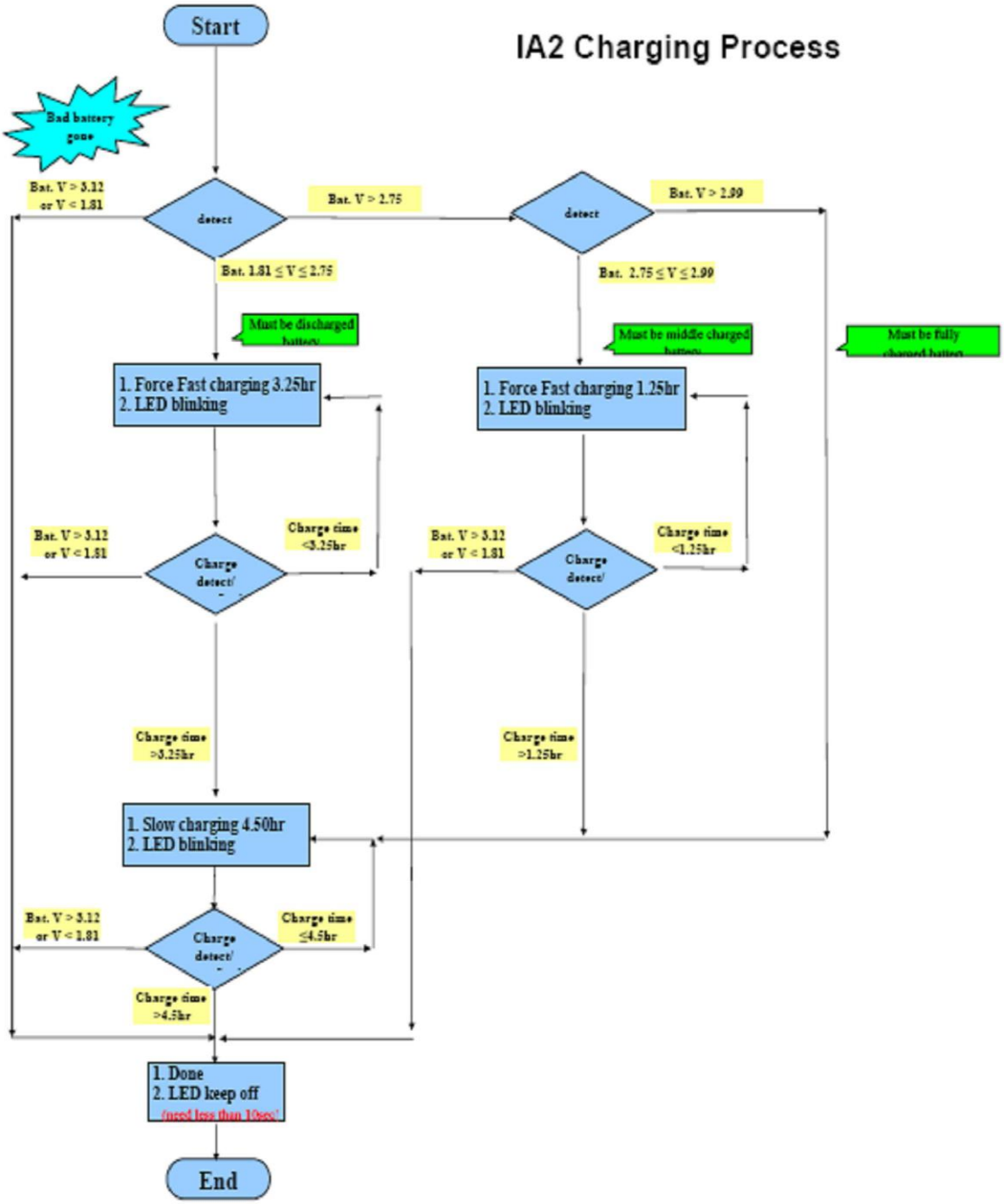
6.3.3 Charging Control Flow Chart:

Base on Ni-MH 1.2V*2pcs (2.4V) voltage that have 3 mode charging flow, details flow reference below flow chart :

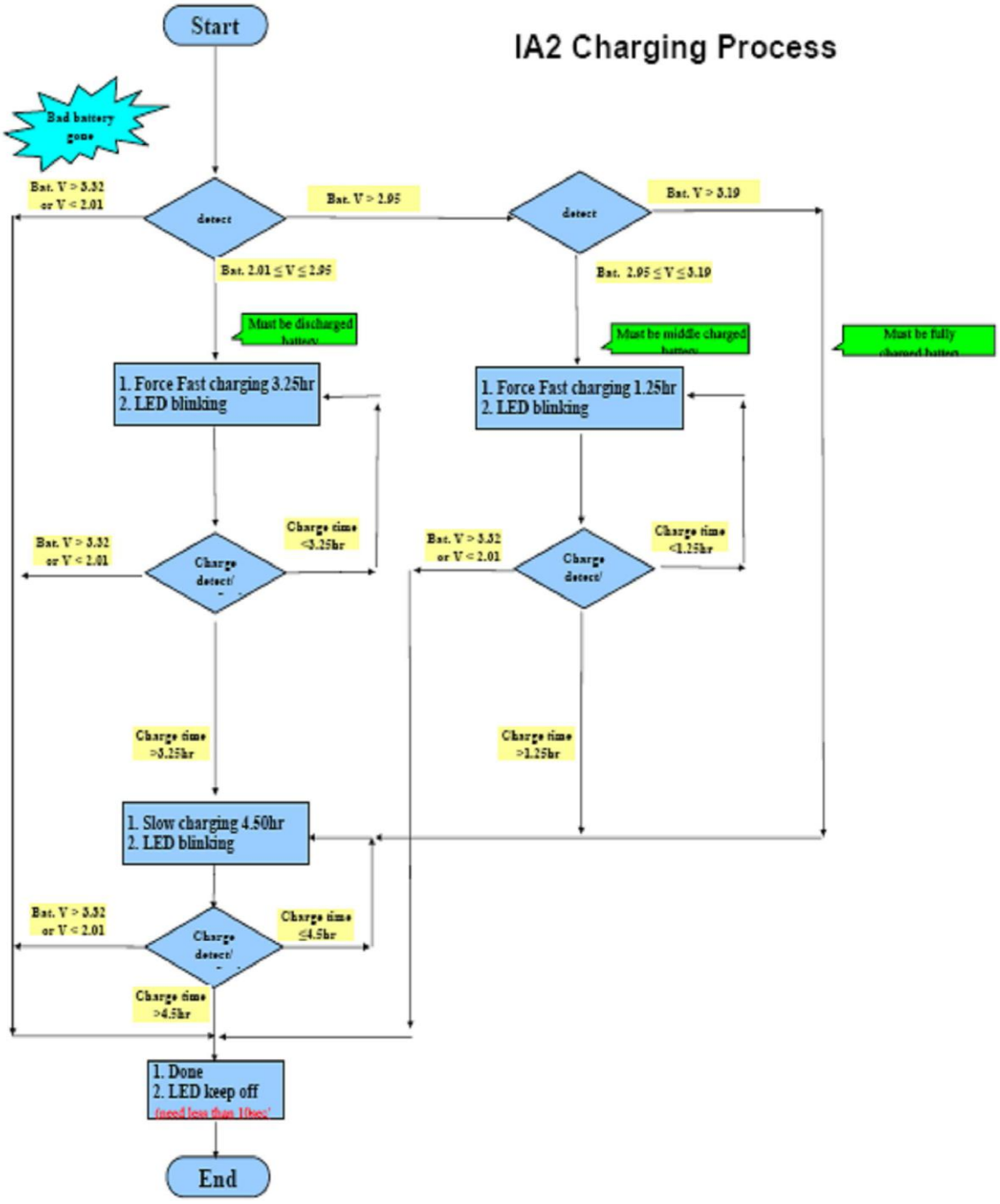
Mode 1: Battery voltage > 2.55V



Mode 2: Battery voltage > 2.75V



Mode 3: Battery voltage > 2.95V



7. Pin definition

TX Module：

Pin	Name	I/O	Description	Condition
1	AGND	P	Analog Ground for Line in	
2	AINR	AI	Analog Line Input Right Channel	FSIV:1Vrms
3	AGND	P	Analog Ground for Line in	
4	AINL	AI	Analog Line Input Left Channel	FSIV:1Vrms
5	SPB1	O	Battery Detect 0	Battery Voltage status detect 0
6	SPB3	O	Battery Detect 2	Battery Voltage status detect 2
7	SPB0	O	Battery Detect 1	Battery Voltage status detect 1
8	Full_Charge	O	Level Input to Enable Fast Charging by High Current	H: Star Charging function L: Stop Charging function
9	Trickle_Charge	O	Level Input to Enable Trickle Charging by small Current	H: Star Charging function L: Stop Charging function
10	VDT_IN	AI	Battery Voltage Detection	Voltage Detector input
11	CH/ID trigger	I	Trigger Input for ID Learning & Hopping Group Selection	Set to Default High, Low active (H:Release Button; L:Press Button)
12	Charging LED	O	LED Indication for Battery Charging	Refer to Firmware function
13	Charge_Det	I	Level Input for Charging Function	H: Star Charging function L: Stop Charging function
14	RF_EN Trigger	I	Trigger Input for RF Transmitting On/Off	Set to Default High, Low active (H:Release Button; L:Press Button)
15	USBP	I	USB D+ Port	
16	USBN	I	USB D- Port	
17	DGND	P	Digital Ground	
18	I2C_Data	IO	I2C Serial Data	Set to Default High
19	I2C_CLK	IO	I2C Clock	Set to Default High
20	EEWP	I	Write Protect for EEPROM	Set to Default High
21	Test	I	Level Input for Production Test Mode Enabling	Set to Default High, Low to enable MP Test mode when power on
22	Audio_Sel	I	Level input for Audio Source Selection	H: USB ; L:Analog
23	ID_Set/RF_On Audio LED	O	LED Indication for ID Learning & RF On/Off	Refer to Firmware function
24	PGND	P	Power Ground	
25	VCC_5V	P	DC5V Power Input	

RX Module：

Pin	Name	I/O	Description	Condition
1	VCC_5V	P	DC 5V Power Input	
2	PGND	P	Power Ground	
3	PWR DN CTL	O	Level Output for Power Down Control of Amplifier circuit	H: RX into standby mode and turn off AMP power; L: RX is normal mode (Refer to Firmware function)
4	VOL_DOWN	I	Trigger Input to turn down IA2 output volume level	Set to Default High, Low active (H:Release Button; L:Press Button) Refer to Firmware function, Option.
5	VOL_UP	I	Trigger Input to enlarge IA2 output volume level	
6	ID trigger	I	Trigger Input for ID Learning	Set to Default High, Low active (H:Release Button; L:Press Button)
7	OTW	O	Audio R/L Out Mute circuit control	
8	AMP_Mute	O	Level Output for Amplifier Circuit Mute Control	Set to Default High, (H:Mute enable; L:Audio output)
9	SPDIF-Out	O	SPDIF Output (Optional GPIO)	SPDIF Output by PCM data format, can be set as a GPIO.
10	ID_SYNC LED	O	LED Indication for Synchronization and ID Learning	Refer to Firmware function
11	Test	I	Level Input for Production Test Mode Enabling	Set to Default High, Low to enable MP Test mode when power on
12	Audio_Sel	I	Level Input for Audio Output Selection	H:DAC AK4386 L: PWM
13	AGND	P	Analog Ground for Line Output	
14	A_out_R	AO	Analog Output from DAC, Right Channel	
15	AGND	P	Analog Ground for Line Output	
16	A_out_L		Analog Output from DAC, Left Channel	
17	DGND	P	Digital Ground	
18	EEWP	I	Write Protect for EEPROM	Set to Default High
19	I2C_CLK	IO	I2C Clock	Set to Default High
20	I2C_Data	IO	I2C Data	Set to Default High
21	PWM_R_Ch_P	O	PWM right channel negative polarity	
22	PWM_R_Ch_N	O	PWM right channel negative polarity	
23	PWM_L_Ch_N	O	PWM left channel positive polarity	
24	PWM_L_Ch_P	O	PWM left channel positive polarity	

8. Mechanical Specification

- Dimension：TX：40*40*7.1mm
  RX(4386)：35*35*7.1mm
- PCB 2 Layers -TX & RX core module
- Mechanical Drawing：

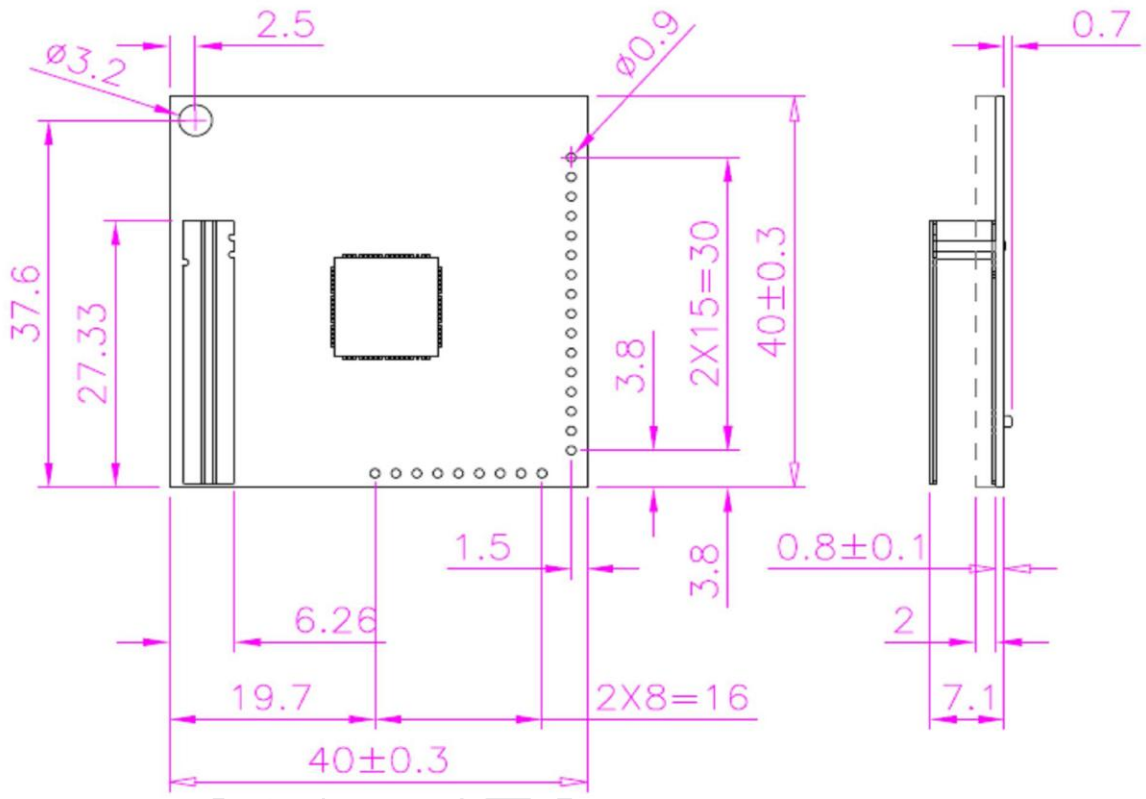


Fig 8.1 TX core module

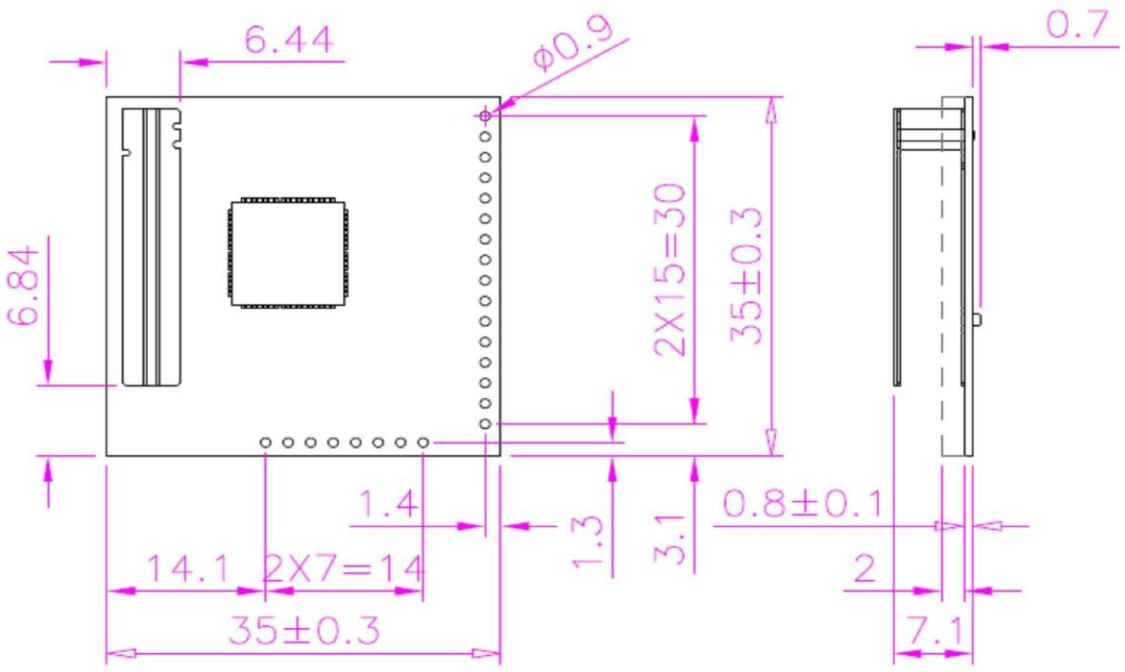


Fig 8.2 RX core module

9. Physical

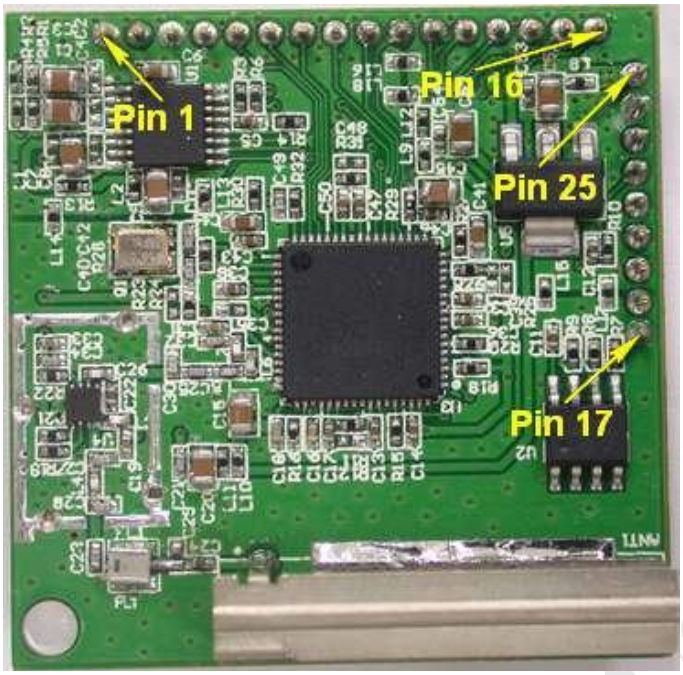


Fig 9.1. TX core module

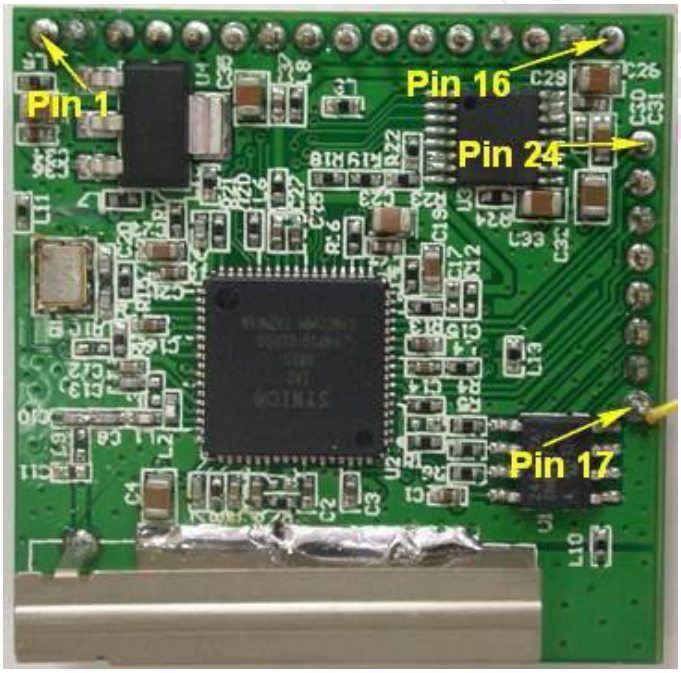


Fig 9.2. RX core module

10. Reference Design

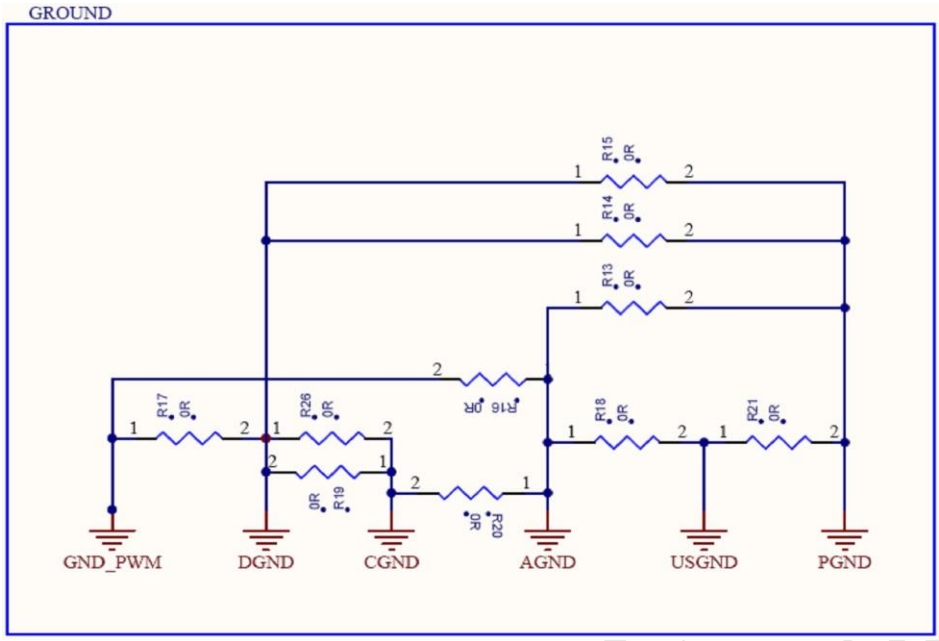


Fig 10.1 Ground circuit

Option: (RF_EN Trigger function by software define).

1.PS2=push-button Switcw , R41=10K , R43=NI

Push Switch , TX change state (ON / OFF).

2.PS2=NC , R41=10K , R43=NI

During charging , TX --> OFF

3.PS2=NC , R41=NI, R43=10K

During charging , TX --> ON

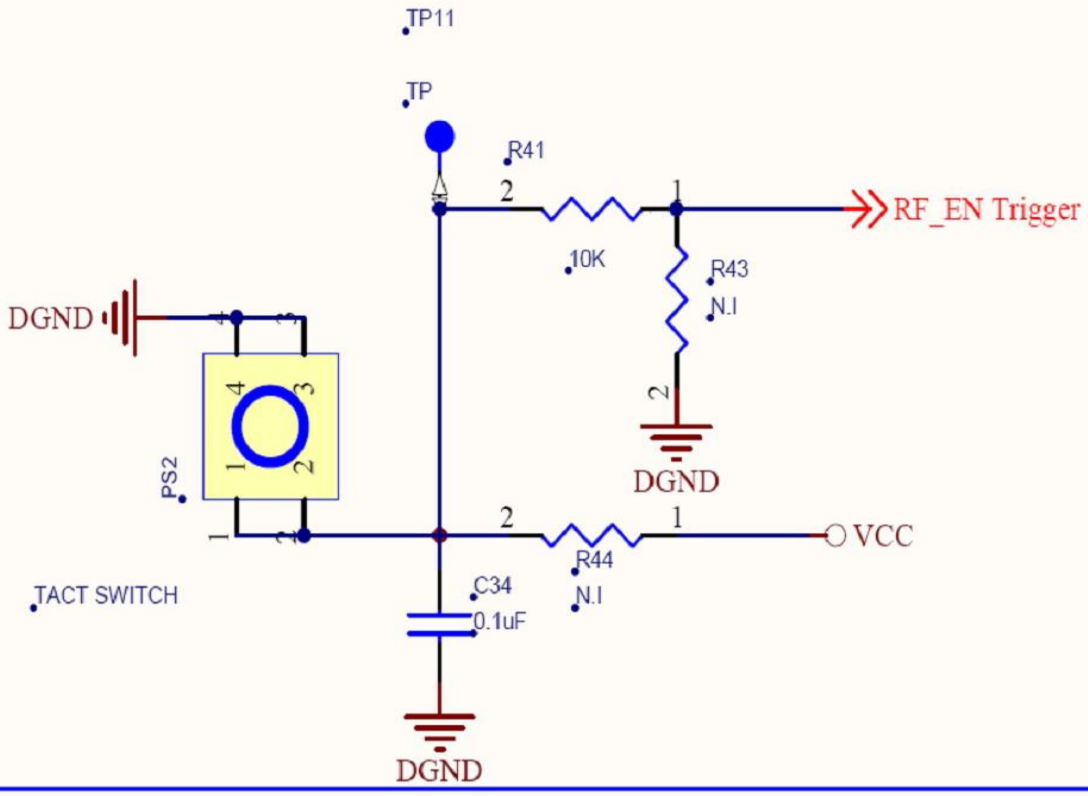


Fig 10.2 RF_EN trigger function

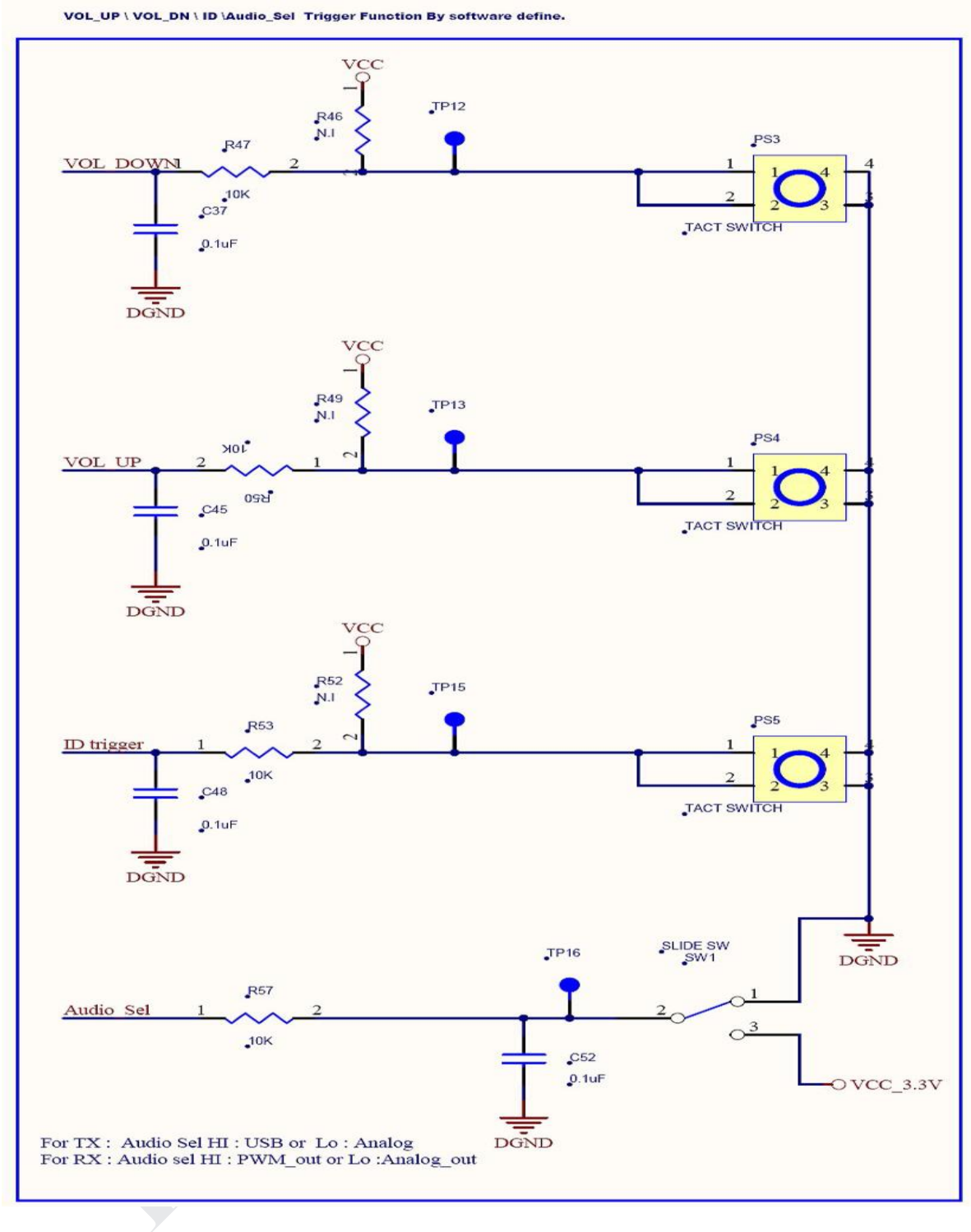


Fig 10.3 VOL/ID_trigger/Audio_Sel design

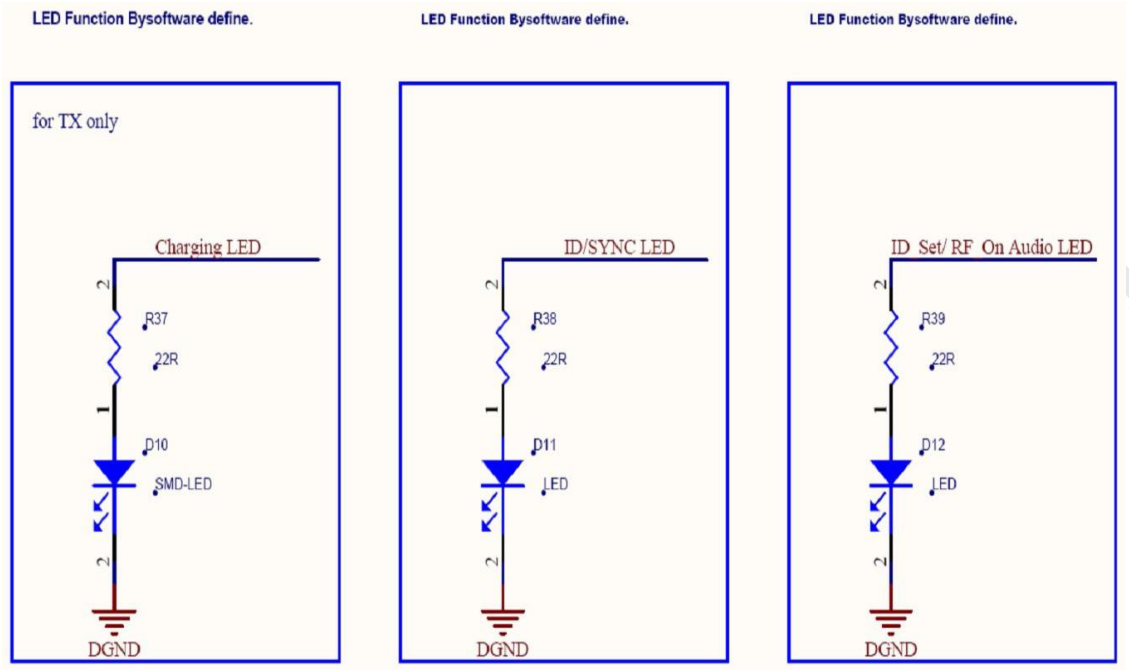


Fig 10.4 Charging LED/ ID_Sync LEC/ID_Set/RF_On Audio LED design

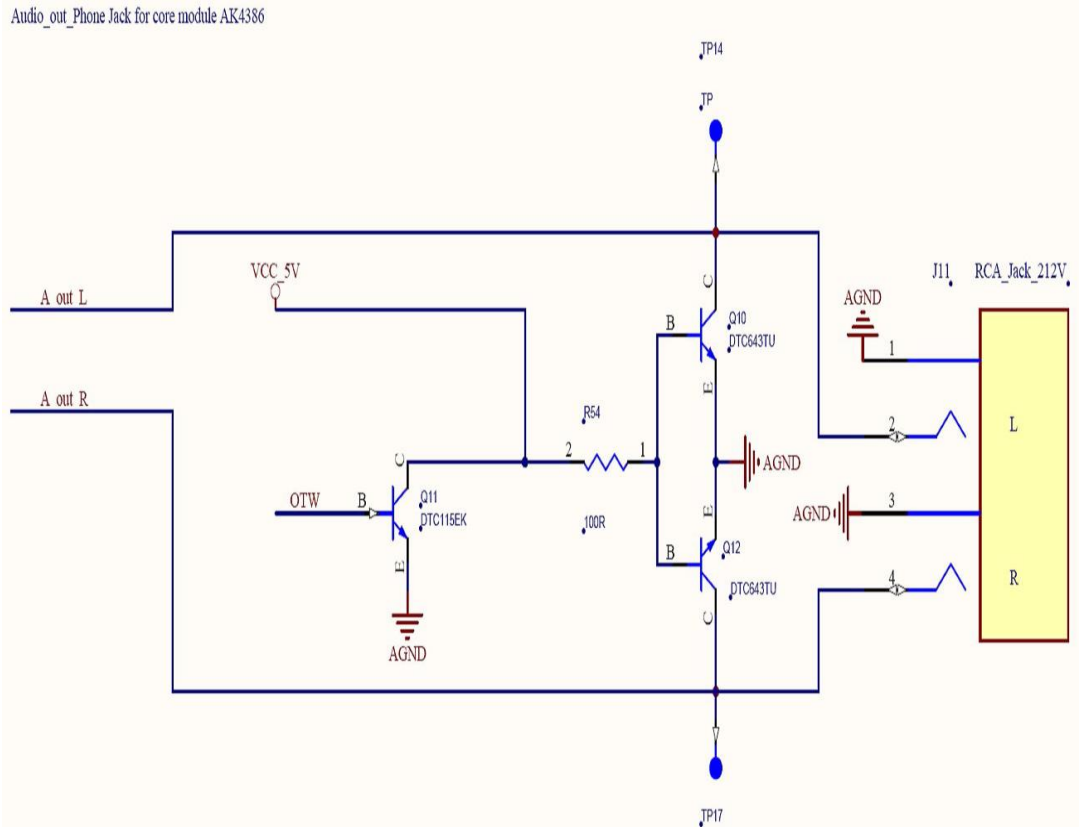


Fig 10.5 Audio Out for RCA Jack