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Renesas Technology Corp. Customer Support Dept. April 1, 2003



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 Remember to give due consideration to safety when making your circuit designs, with appropriate
measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or
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Silicon N Channel MOS FET High Speed Power Switching

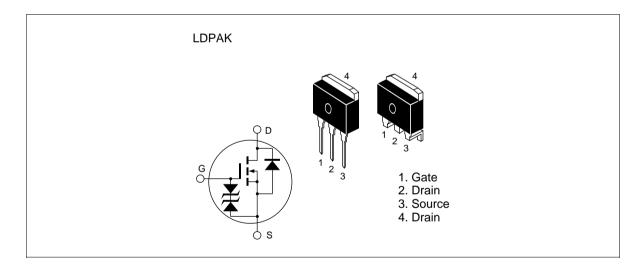


ADE-208-750B (Z) 3rd. Edition Mar. 2001

Features

- Low on-resistance $R_{DS} = 45 \text{m}\Omega$ typ.
- · High speed switching
- 4V gate drive device can be driven from 5V source

Outline



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	$V_{\scriptscriptstyle DSS}$	100	V
Gate to source voltage	$V_{\sf GSS}$	±20	V
Drain current	I _D	20	A
Drain peak current	Note1	80	A
Body-drain diode reverse drain current	I _{DR}	20	A
Avalanche current	I Note3	20	A
Avalanche energy	E _{AR} Note3	40	mJ
Channel dissipation	Pch Note2	50	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

Note: 1. PW \leq 10 μ s, duty cycle \leq 1 %

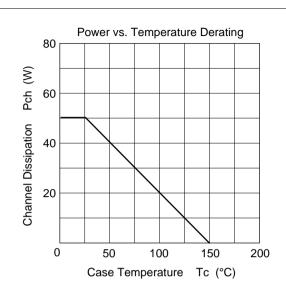
- 2. Value at Tc = 25°C
- 3. Value at Tch = 25° C, Rg $\geq 50\Omega$

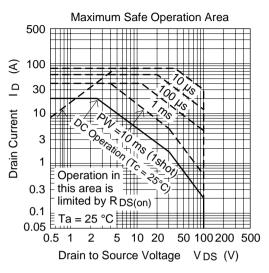
Electrical Characteristics (Ta = 25°C)

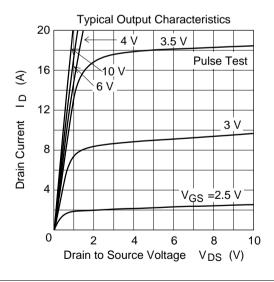
) —		V	$I_D = 10 \text{mA}, V_{GS} = 0$ $I_G = \pm 100 \mu \text{A}, V_{DS} = 0$
) — — —	±10		$I_{G} = \pm 100 \mu A, V_{DS} = 0$
	±10	^	
_		μΑ	$V_{GS} = \pm 16V, V_{DS} = 0$
	10	μΑ	$V_{DS} = 100 \text{ V}, V_{GS} = 0$
_	2.5	V	$I_{D} = 1 \text{mA}, V_{DS} = 10 \text{V}$
45	60	mΩ	$I_{\rm D} = 10 {\rm A}, \ V_{\rm GS} = 10 {\rm V}^{\rm Note4}$
65	85	mΩ	$I_D = 10A$, $V_{GS} = 4V^{Note4}$
14	_	S	$I_{D} = 10A, V_{DS} = 10V^{Note4}$
900	_	pF	V _{DS} = 10V
400	_	pF	$V_{GS} = 0$
210	_	pF	f = 1MHz
15	_	ns	$I_{D} = 10A, V_{GS} = 10V$
120	_	ns	$R_L = 3\Omega$
200	_	ns	
150	_	ns	
0.9	_	V	$I_F = 20A, V_{GS} = 0$
90		ns	$I_{\rm F} = 20A, V_{\rm GS} = 0$
	900 400 210 15 120 200 150	900 — 400 — 210 — 15 — 120 — 200 — 150 — 0.9 —	900 — pF 400 — pF 210 — pF 15 — ns 120 — ns 200 — ns 150 — ns 0.9 — V

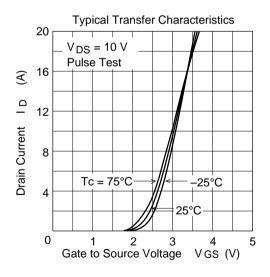
Note: 4. Pulse test

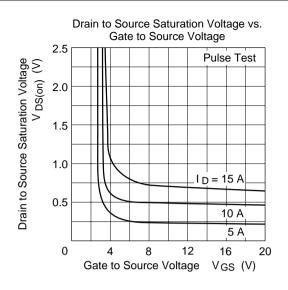
Main Characteristics

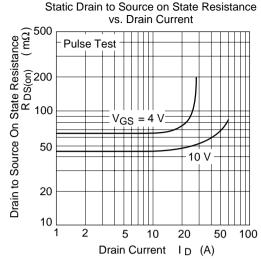


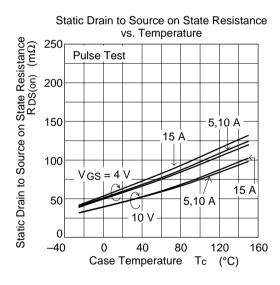


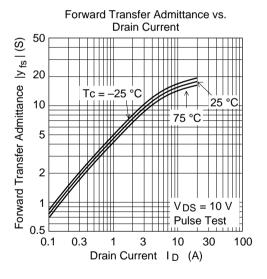


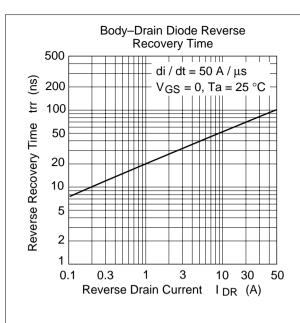


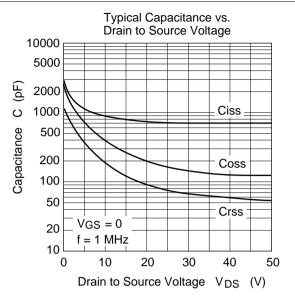


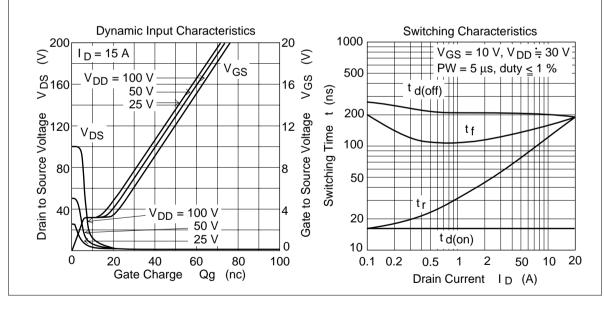


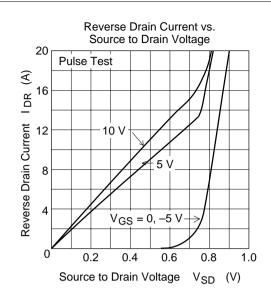


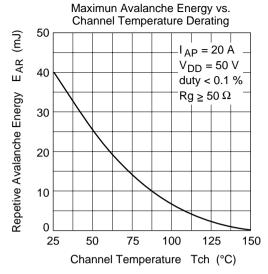




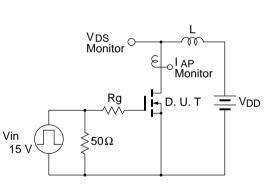




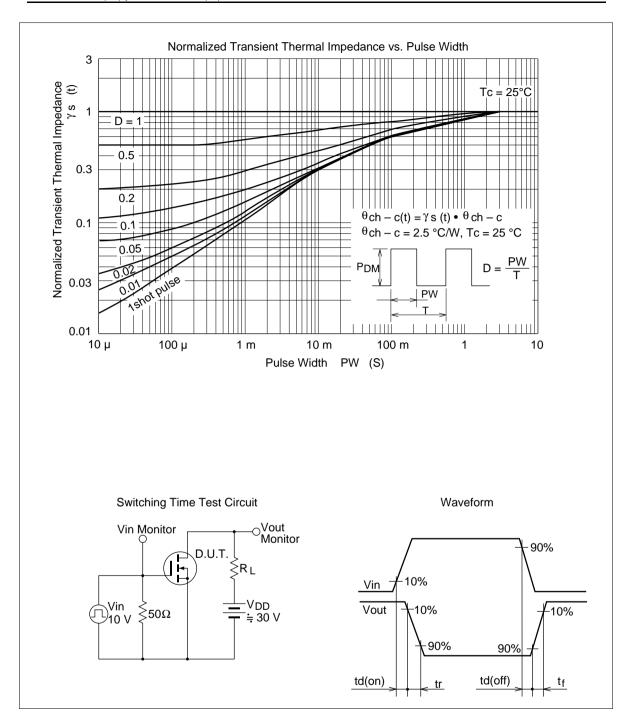




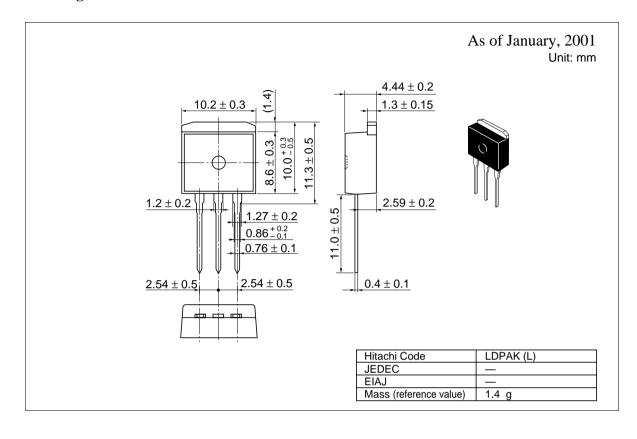
Avalanche Test Circuit

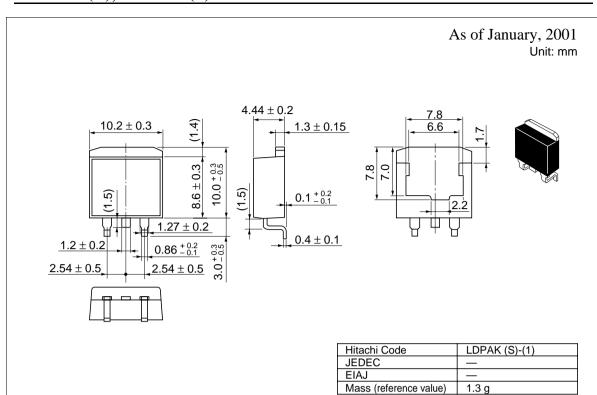


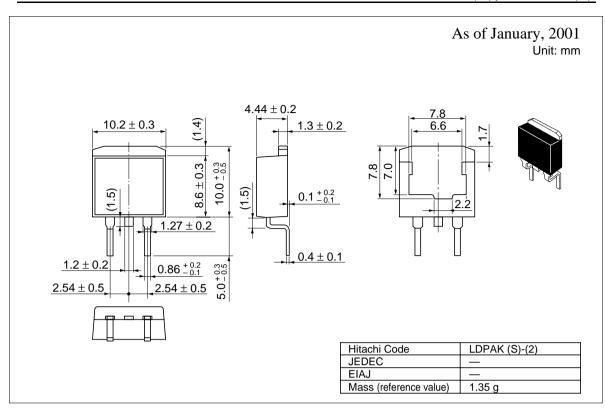
Avalanche Waveform



Package Dimensions







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Semiconductor & Integrated Circuits. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL NorthAmerica http://semiconductor.hitachi.com/ http://www.hitachi-eu.com/hel/ecg Europe Asia http://sicapac.hitachi-asia.com http://www.hitachi.co.jp/Sicd/indx.htm Japan

For further information write to:

Hitachi Semiconductor (America) Inc. 179 East Tasman Drive, San Jose, CA 95134 Tel: <1> (408) 433-1990 Germany

Hitachi Europe GmbH Electronic Components Group Dornacher Straße 3 D-85622 Feldkirchen, Munich Fax: <1>(408) 433-0223 Tel: <49> (89) 9 9180-0 Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd. Electronic Components Group. Whitebrook Park Lower Cookham Road Maidenhead

Berkshire SL6 8YA, United Kingdom Tel: <886>-(2)-2718-3666 Tel: <44> (1628) 585000 Fax: <44> (1628) 585160

Hitachi Asia Ltd. Hitachi Tower 16 Collyer Quay #20-00, Singapore 049318 Tel: <65>-538-6533/538-8577 Fax: <65>-538-6933/538-3877 URL: http://www.hitachi.com.sg

Hitachi Asia Ltd. (Taipei Branch Office) 4/F, No. 167, Tun Hwa North Road, Hung-Kuo Building, Taipei (105), Taiwan

Fax: <886>-(2)-2718-8180 Telex: 23222 HAS-TP URL: http://www.hitachi.com.tw Hitachi Asia (Hong Kong) Ltd. Group III (Electronic Components) 7/F., North Tower, World Finance Centre, Harbour City, Canton Road Tsim Sha Tsui, Kowloon, Hong Kong

Tel: <852>-(2)-735-9218 Fax: <852>-(2)-730-0281 URL: http://www.hitachi.com.hk

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