



## Power MOSFET

PRODUCT SUMMARY	
V <sub>DS</sub> (V)	500
R <sub>DS(on)</sub> (Ω)	V <sub>GS</sub> = 10 V 3.0
Q <sub>g</sub> (Max.) (nC)	17
Q <sub>gs</sub> (nC)	4.3
Q <sub>gd</sub> (nC)	8.5
Configuration	Single

### FEATURES

- Low Gate Charge Q<sub>g</sub> Results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Effective C<sub>oss</sub> Specified
- Lead (Pb)-free Available

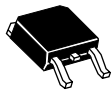


RoHS\*  
COMPLIANT

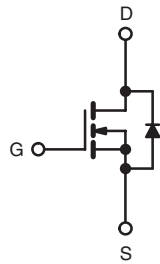
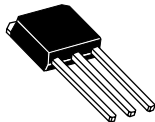
### APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching

DPAK  
(TO-252)



IPAK  
(TO-251)



N-Channel MOSFET

ORDERING INFORMATION				
Package	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)	IPAK (TO-251)
Lead (Pb)-free	IRFR420APbF	IRFR420ATRLPbF <sup>a</sup>	IRFR420ATRLPbF	IRFU420APbF
	SiHFR420A-E3	SiHFR420AT-E3 <sup>a</sup>	SiHFR420ATL-E3	SiHFU420A-E3
SnPb	IRFR420A	-	-	IRFU420A
	SiHFR420A	-	-	SiHFU420A

#### Note


- a. See device orientation.

ABSOLUTE MAXIMUM RATINGS T <sub>C</sub> = 25 °C, unless otherwise noted					
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V <sub>DS</sub>	500	V
Gate-Source Voltage			V <sub>GS</sub>	± 30	
Continuous Drain Current	V <sub>GS</sub> at 10 V	T <sub>C</sub> = 25 °C	I <sub>D</sub>	3.3	A
		T <sub>C</sub> = 100 °C		2.1	
Pulsed Drain Current <sup>a</sup>			I <sub>DM</sub>	10	
Linear Derating Factor				0.67	W/°C
Single Pulse Avalanche Energy <sup>b</sup>			E <sub>AS</sub>	140	mJ
Repetitive Avalanche Current <sup>a</sup>			I <sub>AR</sub>	2.5	A
Repetitive Avalanche Energy <sup>a</sup>			E <sub>AR</sub>	5.0	mJ
Maximum Power Dissipation	T <sub>C</sub> = 25 °C		P <sub>D</sub>	83	W
Peak Diode Recovery dV/dt <sup>c</sup>			dV/dt	3.4	V/ns
Operating Junction and Storage Temperature Range			T <sub>J</sub> , T <sub>stg</sub>	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s			300 <sup>d</sup>	

#### Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).  
 b. Starting T<sub>J</sub> = 25 °C, L = 45 mH, R<sub>G</sub> = 25 Ω, I<sub>AS</sub> = 2.5 A (see fig. 12).  
 c. I<sub>SD</sub> ≤ 2.5 A, dI/dt ≤ 270 A/μs, V<sub>DD</sub> ≤ V<sub>DS</sub>, T<sub>J</sub> ≤ 150 °C.  
 d. 1.6 mm from case.

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	62	°C/W
Case-to-Sink, Flat, Greased Surface	$R_{thCS}$	0.50	-	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	1.5	

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	500	-	-	V	
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = 1\text{ mA}$	-	0.60	-	V/°C	
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	-	4.5	V	
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 30\text{ V}$	-	-	$\pm 100$	nA	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 500\text{ V}, V_{GS} = 0\text{ V}$	-	-	25	$\mu\text{A}$	
		$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	250		
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 1.5\text{ A}^b$	-	-	3.0	$\Omega$	
Forward Transconductance	$g_{fs}$	$V_{DS} = 50\text{ V}, I_D = 1.5\text{ A}$	1.4	-	-	S	
<b>Dynamic</b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$ , see fig. 5	-	340	-	pF	
Output Capacitance	$C_{oss}$		-	53	-		
Reverse Transfer Capacitance	$C_{riss}$		-	2.7	-		
Output Capacitance	$C_{oss}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 1.0\text{ V}, f = 1.0\text{ MHz}$	-	490	-	pF
			$V_{DS} = 400\text{ V}, f = 1.0\text{ MHz}$	-	15	-	
Effective Output Capacitance	$C_{oss\text{ eff.}}$	$V_{DS} = 0\text{ V to } 400\text{ V}^c$	-	28	-		
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}, I_D = 2.5\text{ A}, V_{DS} = 400\text{ V}$ , see fig. 6 and 13 <sup>b</sup>	-	-	17	nC	
Gate-Source Charge	$Q_{gs}$		-	-	4.3		
Gate-Drain Charge	$Q_{gd}$		-	-	8.5		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 250\text{ V}, I_D = 2.5\text{ A}, R_G = 21\text{ }\Omega, R_D = 97\text{ }\Omega$ , see fig. 10 <sup>b</sup>	-	8.1	-	ns	
Rise Time	$t_r$		-	12	-		
Turn-Off Delay Time	$t_{d(off)}$		-	16	-		
Fall Time	$t_f$		-	13	-		
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	3.3	A	
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$		-	-	10		
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 2.5\text{ A}, V_{GS} = 0\text{ V}^b$	-	-	1.6	V	
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = 2.5\text{ A}, di/dt = 100\text{ A}/\mu\text{s}^b$	-	330	500	ns	
Body Diode Reverse Recovery Charge	$Q_{rr}$		-	760	1140	$\mu\text{C}$	
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )					

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- c.  $C_{oss\text{ eff.}}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80 %  $V_{DS}$ .



KERSEMI

# IRFR420A, IRFU420A, SiHFR420A,

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

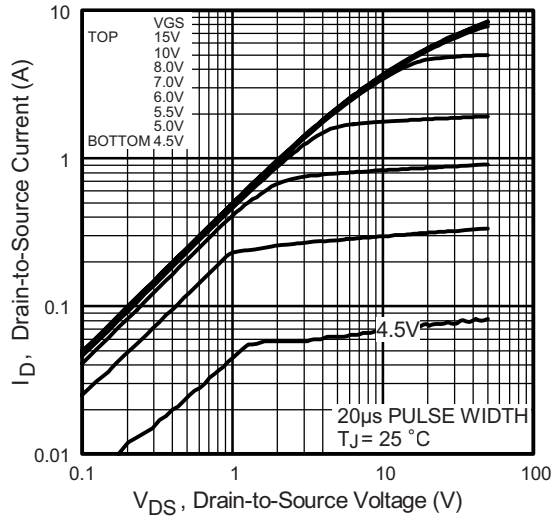


Fig. 1 - Typical Output Characteristics

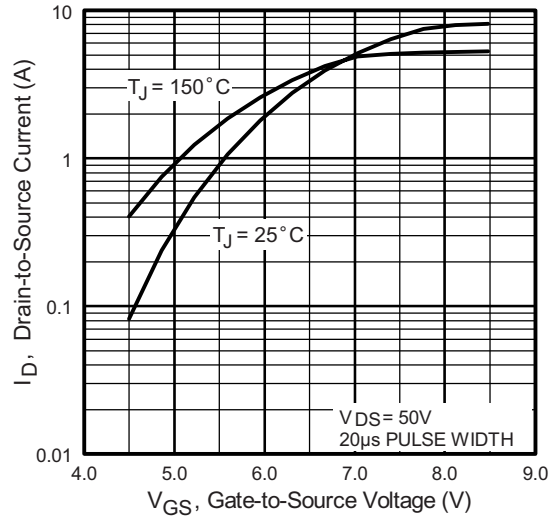


Fig. 3 - Typical Transfer Characteristics

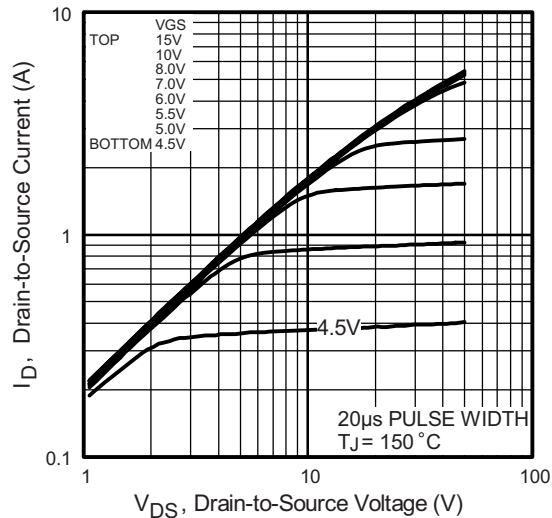


Fig. 2 - Typical Output Characteristics

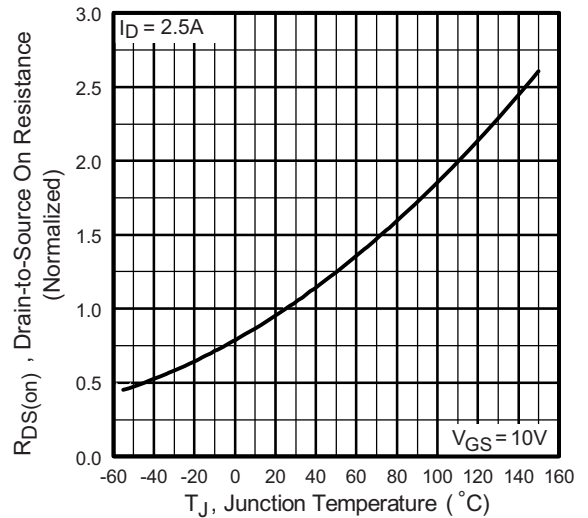


Fig. 4 - Normalized On-Resistance vs. Temperature

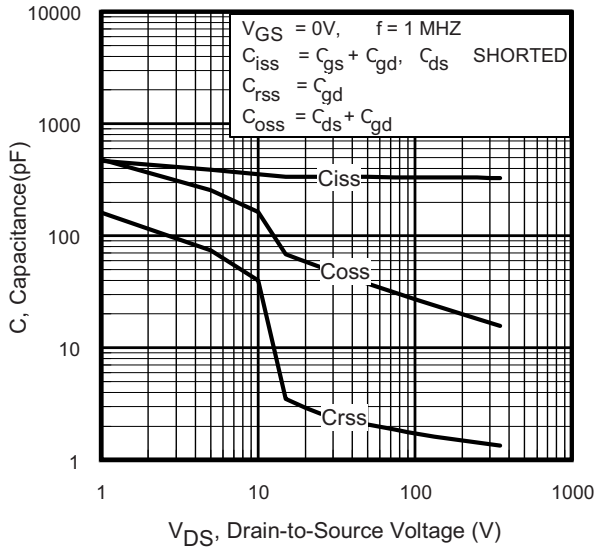


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

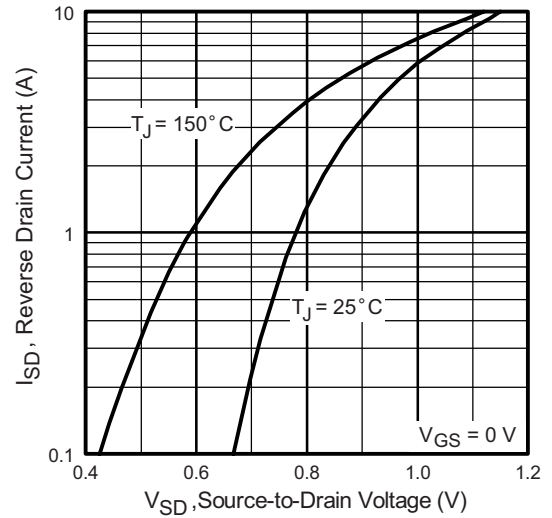


Fig. 7 - Typical Source-Drain Diode Forward Voltage

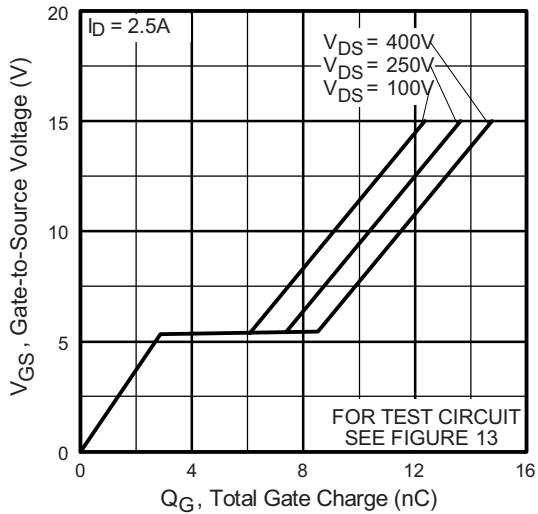


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

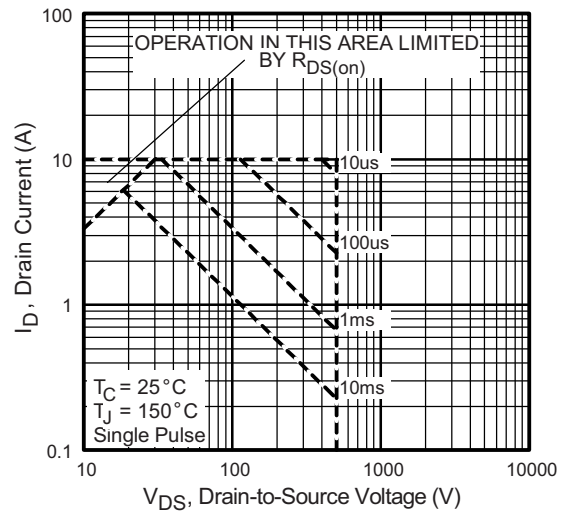
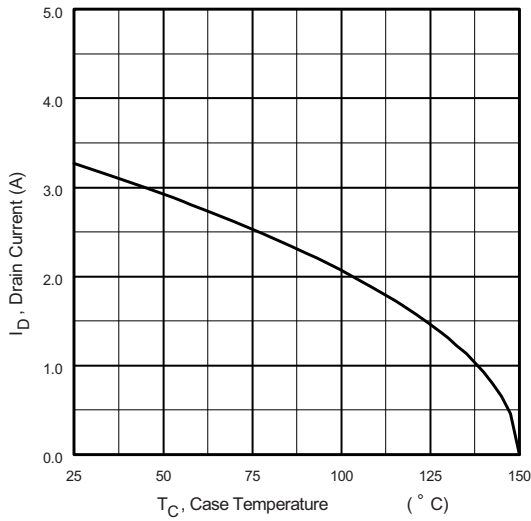
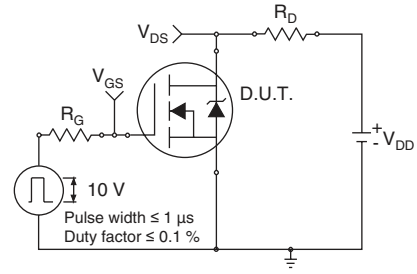


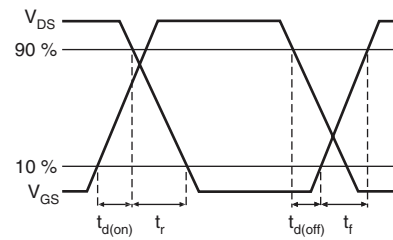
Fig. 8 - Maximum Safe Operating Area



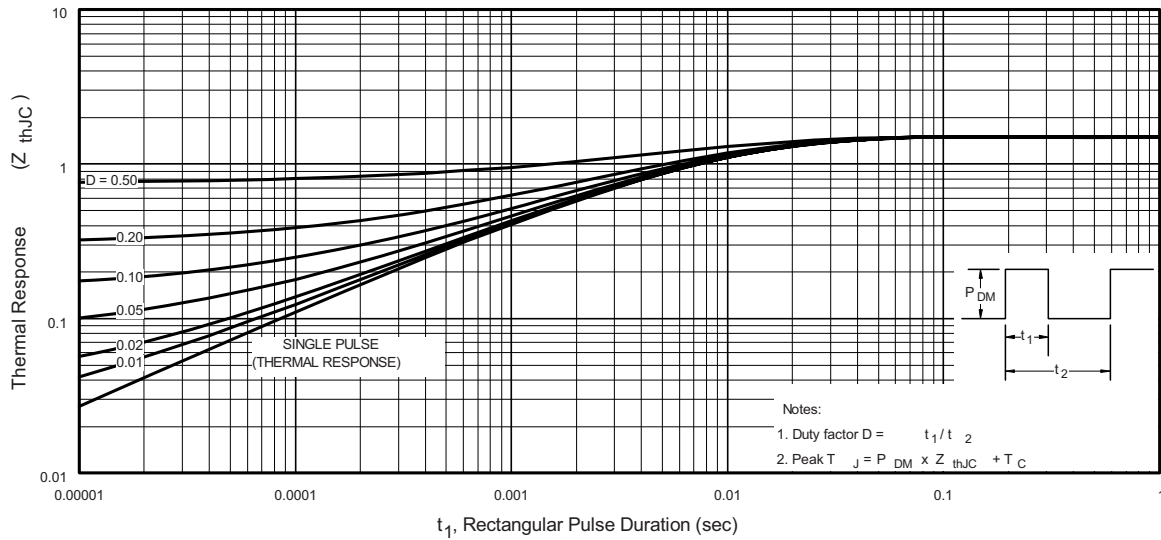
**Fig. 9 - Maximum Drain Current vs. Case Temperature**



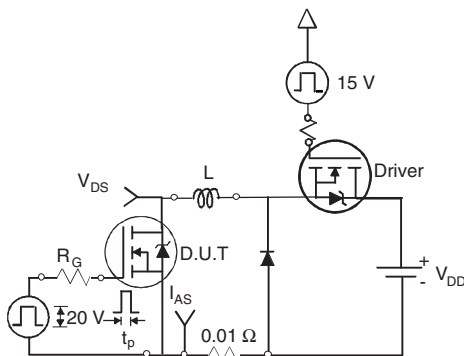
**Fig. 10a - Switching Time Test Circuit**



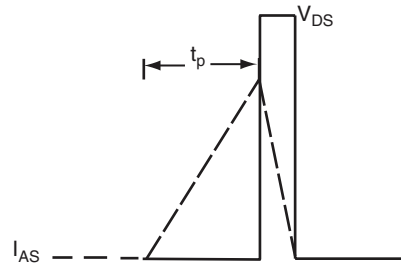
**Fig. 10b - Switching Time Waveforms**



**Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case**



**Fig. 12a - Unclamped Inductive Test Circuit**



**Fig. 12b - Unclamped Inductive Waveforms**

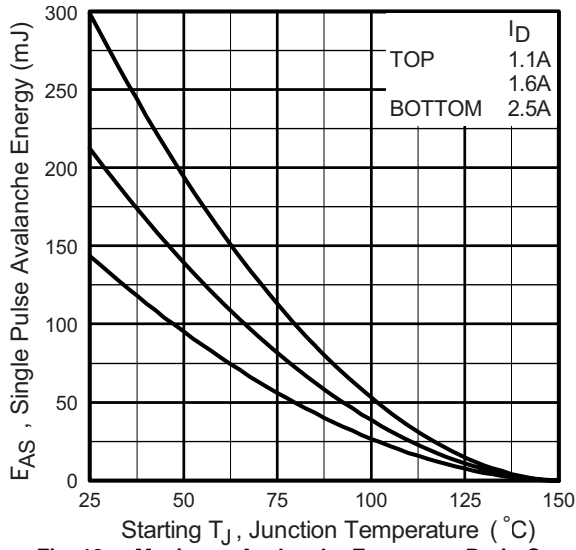


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

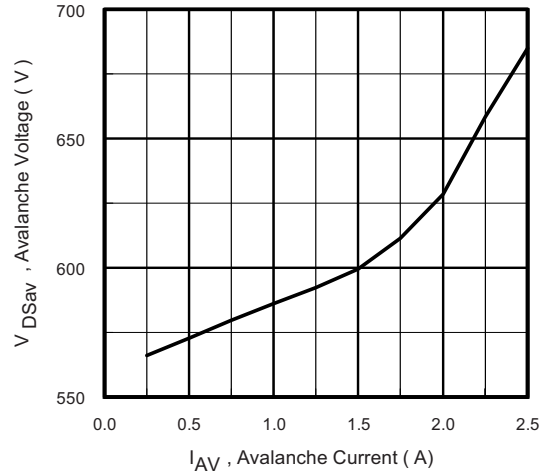


Fig. 12d - Maximum Avalanche Energy vs. Drain Current

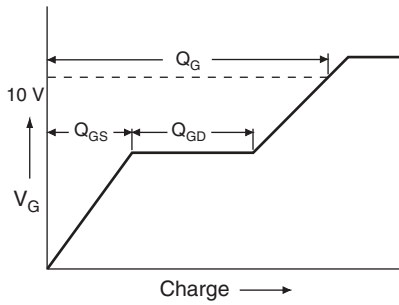


Fig. 13a - Basic Gate Charge Waveform

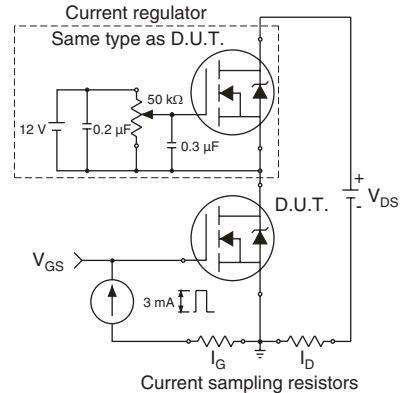
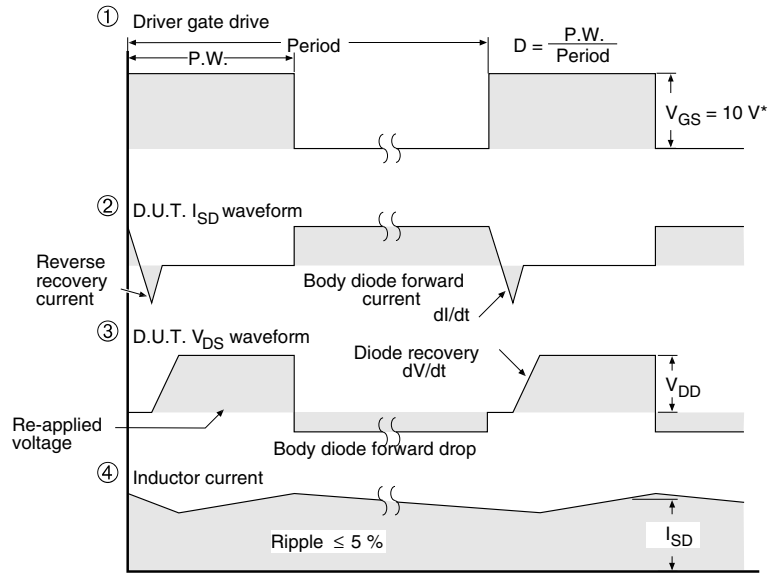
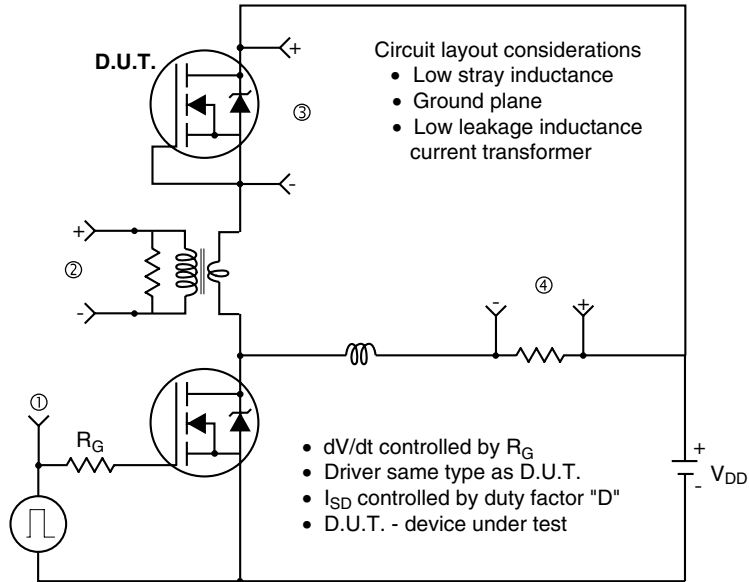


Fig. 13b - Gate Charge Test Circuit

## Peak Diode Recovery $dV/dt$ Test Circuit



\*  $V_{GS} = 5 V$  for logic level devices

Fig. 14 - For N-Channel