PCF8538

Universal 102 x 9 Chip-On-Glass LCD segment driver

Rev. 1 — 18 December 2013 Product data sheet

1. General description

The PCF8538 is a fully featured Chip-On-Glass (COG)[1] Liquid Crystal Display (LCD) driver, designed for high-contrast Vertical Alignment (VA) LCD with multiplex rates up to 1:9. It generates the drive signals for a static or multiplexed LCD containing up to 9 backplanes, 102 segments, and up to 918 elements. The PCF8538 features an internal charge pump with internal capacitors for on-chip generation of the LCD driving voltage. To ensure an optimal and stable contrast over the full temperature range, the PCF8538 offers a programmable temperature compensation of the LCD supply voltage. The PCF8538 can be easily controlled by a microcontroller through either the two-line I^2C-bus or a four-line bidirectional SPI-bus.

For a selection of NXP LCD segment drivers, see Table 61 on page 102.

2. Features and benefits

- Low power consumption
- 102 segments and 9 backplanes allowing to drive:
  - up to 114 7-segment numeric characters
  - up to 57 14-segment alphanumeric characters
  - any graphics of up to 918 elements
- 918-bit RAM for display data storage
- Two sets of backplane outputs providing higher flexibility for optimal COG layout configurations
- Up to 4 chips can be cascaded to drive larger displays with an internally generated or externally supplied V_{LCD}
- Selectable backplane drive configuration: static, 2, 4, 6, 8, or 9 backplane multiplexing
- LCD supply voltage
  - Programmable internal charge pump for on-chip LCD voltage generation up to $5 \times V_{DD2}$
  - External LCD voltage supply possible as well
- Selectable 400 kHz I^2C-bus or 6.5 MHz SPI-bus interface
- Selectable linear temperature compensation of V_{LCD}
- Selectable display bias configuration
- Wide range for digital and analog power supply: from 2.5 V to 5.5 V
- Wide LCD voltage range from 4.0 V for low threshold LCDs up to 12.0 V for high threshold twisted nematic and Vertical Alignment (VA) displays
- Display memory bank switching in static, duplex, and quadruplex drive modes

1. The definition of the abbreviations and acronyms used in this data sheet can be found in Section 19 on page 105.

- Programmable frame frequency in the range of 45 Hz to 300 Hz; factory calibrated with a tolerance of ±3 Hz (at 80 Hz)
- Selectable inversion scheme for LCD driving waveforms: frame or n-line inversion
- Diagnostic features for status monitoring
- Integrated temperature sensor with temperature readout
- On chip calibration of internal oscillator frequency and V_{LCD}

3. Applications

- Consumer
- Medical and health care
- Measuring equipment
- Machine control systems
- Information boards
- White goods
- General-purpose display modules

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCF8538UG	bare die	247 bumps	PCF8538UG

4.1 Ordering options

Table 2. Ordering options

Product type number	Sales item (12NC)	Orderable part number	IC revision	Delivery form
PCF8538UG/2DA/1	935303337033	PCF8538UG/2DA/1Z	1	chips with bumps[1] in tray

[1] Bump hardness, see Table 59 on page 99.

5. Block diagram

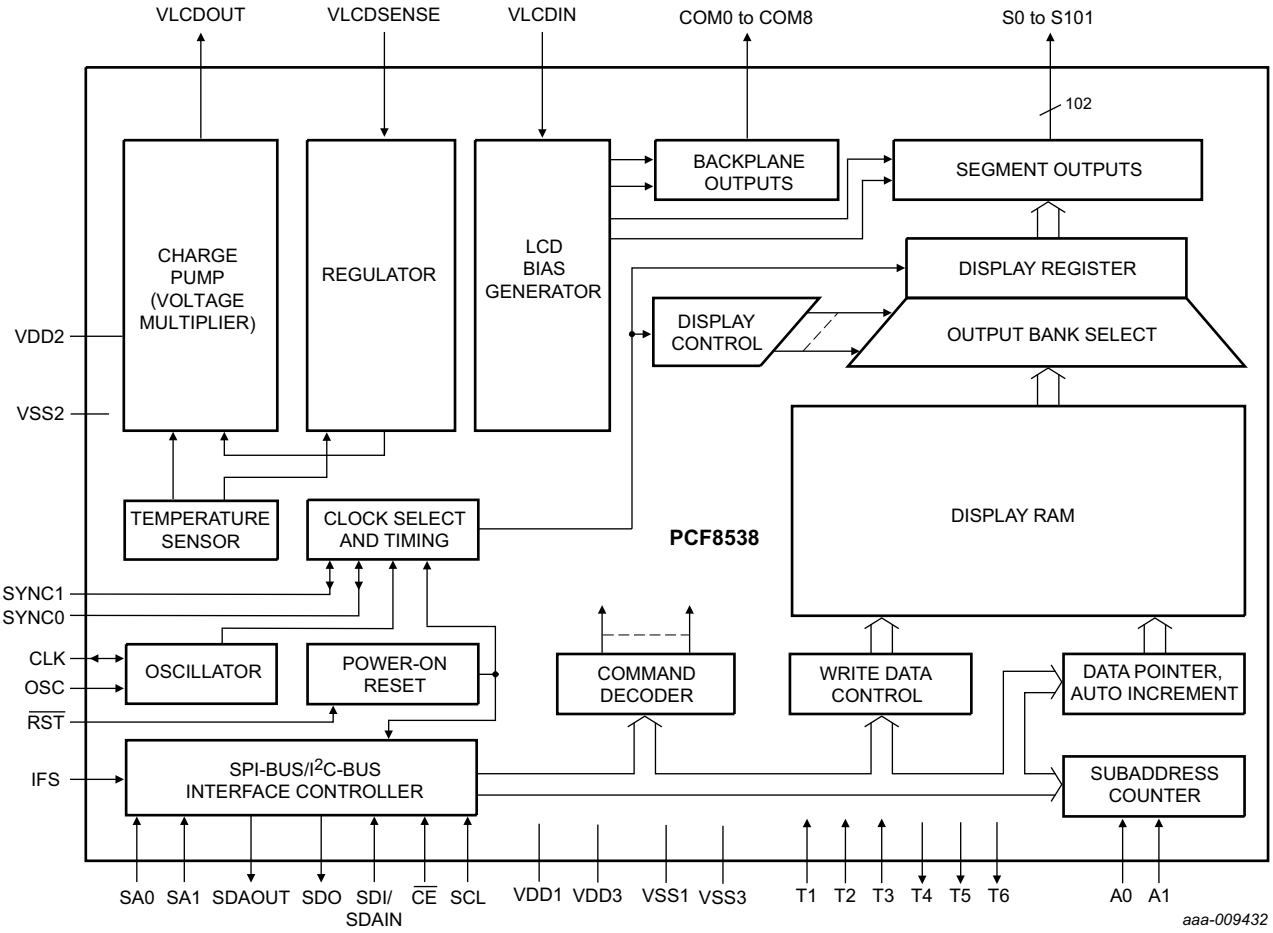
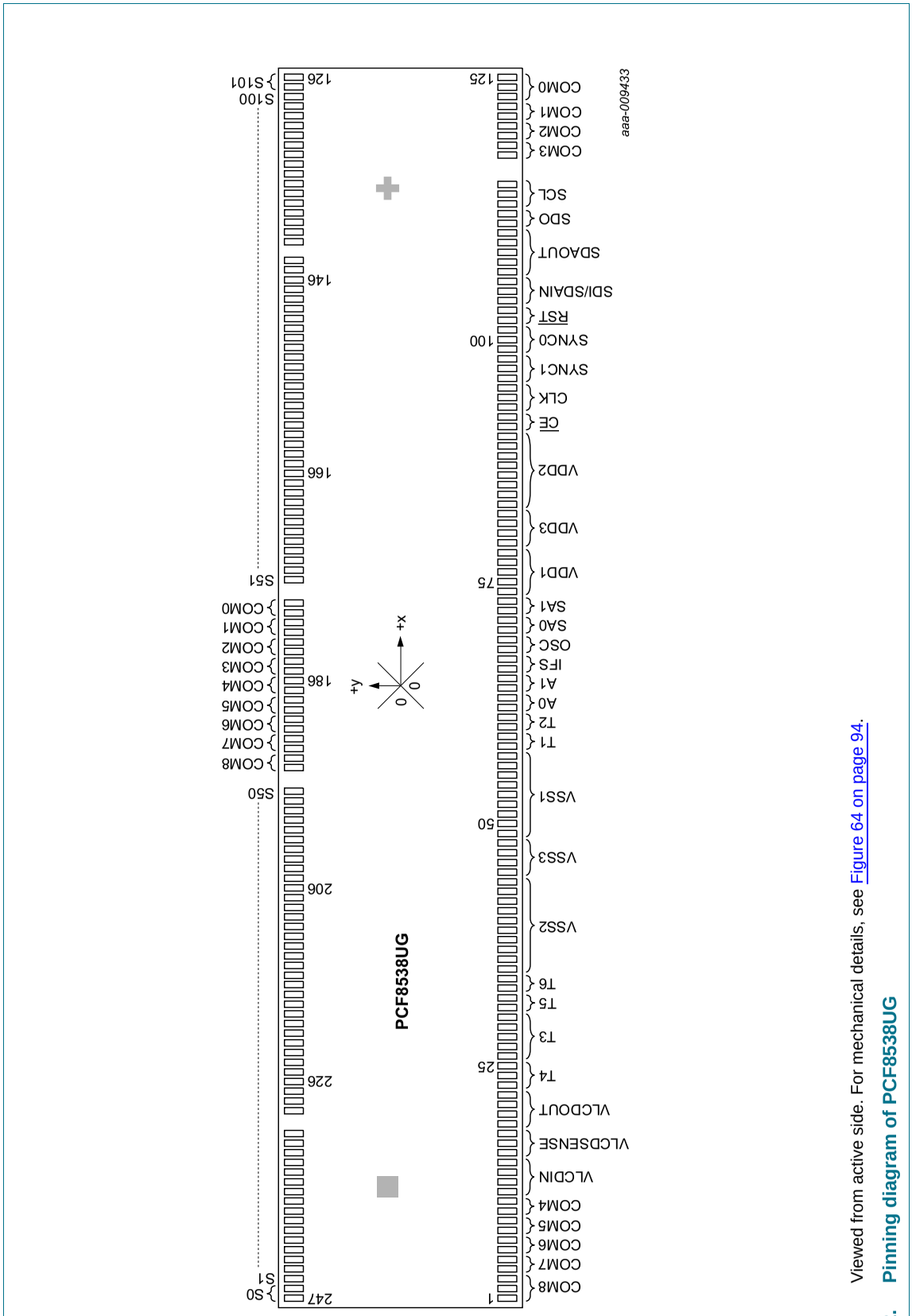


Fig 1. Block diagram of PCF8538

6. Pinning information

6.1 Pinning



Viewed from active side. For mechanical details, see Figure 64 on page 94.

Fig 2. Pinning diagram of PCF8538UG

6.2 Pin description

Table 3. Pin description

Input or input/output pins must always be at a defined level (V_{SS} or V_{DD}) unless otherwise specified.

Symbol	Pin	Type	Description
Backplane output pins			
COM8	1 to 3, 194, 195	output	LCD backplane
COM7	4, 5, 192, 193		
COM6	6, 7, 190, 191		
COM5	8, 9, 188, 189		
COM4	10, 11, 186, 187		
COM3	117, 118, 184, 185		
COM2	119, 120, 182, 183		
COM1	121, 122, 180, 181		
COM0	123 to 125, 178, 179		
Segment output pins			
S101	126, 127	output	LCD segment
S100 to S51	128 to 177		
S50 to S1	196 to 245		
S0	246, 247		
V_{LCD} pins			
VLCDIN	12 to 15	supply	V_{LCD} input
VLCDSENSE	16 to 18	input	V_{LCD} regulation input
VLCDOUT	19 to 22	output	V_{LCD} output
Test pins			
T4	23 to 25	output	not accessible; must be left open
T3	26 to 30	input	not accessible; must be connected to T5
T5	31, 32	output	not accessible; must be connected to T3
T6	33, 34	output	not accessible; must be left open
T1	58, 59	input	not accessible; must be connected to V_{SS1}
T2	60, 61		
Supply pins			
VSS2[1]	35 to 44	supply	ground supply
VSS3[1]	45 to 48		
VSS1[1]	49 to 57		
VDD1	74 to 78	supply	supply voltage 1 (analog and digital)
VDD3	79 to 82	supply	supply voltage 3 (analog)
VDD2	83 to 90	supply	supply voltage 2 (charge pump)

Table 3. Pin description *…continued*

Input or input/output pins must always be at a defined level (V_{SS} or V_{DD}) unless otherwise specified.

Symbol	Pin	Type	Description	
Oscillator, synchronization, addressing, and reset pins				
CLK[2]	93 to 95	input/output	internal oscillator output, external oscillator input	
OSC[2]	68, 69	input	clock (internal/external) selector	
SYNC1[3]	96 to 98	input/output	charge pump synchronization for cascaded devices; must not be connected if V_{LCD} is externally supplied	
SYNC0[3]	99 to 101	input/output	display synchronization for cascaded devices	
$\overline{RST}$	102, 103	input	active LOW reset input	
A0	62, 63	input	hardware device address selection for cascading; • connect to V_{SS1} for logic 0 • connect to V_{DD1} for logic 1	
A1	64, 65			
Bus-related pins				
			SPI-bus	**I²C-bus**
IFS	66, 67	input	interface selector input	
			• connect to V_{SS1}	• connect to V_{DD1}
SA0	70, 71	input	unused; • connect to V_{SS1}	slave address selector; • connect to V_{SS1} for logic 0 • connect to V_{DD1} for logic 1
SA1	72, 73	input		
$\overline{CE}$	91, 92	input	chip enable input (active LOW)	unused; • connect to V_{DD1}
SDI/SDAIN	104 to 106	input	SPI-bus data input	I²C-bus serial data input
SDAOUT	107 to 111	output	unused; • must be connected to V_{SS1}	serial data output
SDO	112, 113	output	SPI serial data output	unused; • must be left open
SCL	114 to 116	input	serial clock input	serial clock input

[1] The substrate (rear side of the die) is connected to V_{SS1} and should be electrically isolated.

[2] If pin OSC is tied to V_{SS1}, CLK is the output pin of the internal oscillator. If pin OSC is tied to V_{DD1}, CLK is the input pin for the external oscillator.

[3] If cascading is not used, pin must be left floating; for cascading see Section 14.2 on page 89.

7. Functional description

7.1 Commands of PCF8538

The PCF8538 is controlled by the commands defined in Table 4.

Remark: Any other combinations of operation code bits that are not mentioned in this document may lead to undesired operation modes of PCF8538.

Table 4. Commands of PCF8538

Command name	R/$\overline{W}$[1]	Register selection RS[1:0][2]		Command bits								Reference
				7	6	5	4	3	2	1	0	
General control commands												
Initialize	0	0	0	0	0	1	1	1	0	1	0	Section 7.2.1
OTP-refresh	0	0	0	1	1	0	1	1	0	0	0	Section 7.2.2
Device-address	0	0	0	0	0	0	1	1	0	A[1:0]		Section 7.2.3
SYNC1_pin	0	0	0	1	0	1	1	1	0	0	OE	Section 7.2.4
Clock-out-ctrl	0	0	0	1	1	0	1	0	1	0	COE	Section 7.2.5
Read-select	0	0	0	0	0	0	1	1	1	0	SO	Section 7.2.6
Status-readout	1	0	0	TD[7:0]								Section 7.2.7
				SR[7:0]								
Clear-reset-flag	0	0	0	0	0	0	1	1	1	1	1	Section 7.2.8
Charge pump and LCD bias control commands												
Charge-pump-ctrl	0	0	0	1	1	0	0	CPE	CPC[2:0]			Section 7.3.1
Set-V_{LCD}	0	0	0	0	1	0	V[8:4]					Section 7.3.2
	0	0	0	0	1	1	0	V[3:0]				
Set-bias-mode	0	0	0	1	1	0	1	0	0	B[1:0]		Section 7.3.3

Table 4. Commands of PCF8538 *…continued*

Command name	R/$\overline{W}$[1]	Register selection RS[1:0][2]	Command bits								Reference
			7	6	5	4	3	2	1	0	
Temperature compensation control commands											
Temperature-ctrl	0	1	0	0	0	0	0	TCE	TMF	TME	Section 7.4.1
TC-slope	0	1	0	0	0	0	1	TSA[2:0]			Section 7.4.3
	0	1	0	0	0	0	1	0	TSB[2:0]		
	0	1	0	0	0	0	1	1	TSC[2:0]		
	0	1	0	0	0	1	0	0	TSD[2:0]		
	0	1	0	0	0	1	0	1	TSE[2:0]		
	0	1	0	0	0	1	1	0	TSF[2:0]		
TC-set	0	1	0	0	0	1	1	1	T1T[2:0]		Section 7.4.2
	0	1	0	0	1	0	0	0	T2T[2:0]		
	0	1	0	0	1	0	0	1	T3T[2:0]		
	0	1	0	0	1	0	1	0	T4T[2:0]		
Display control commands											
Set-MUX-mode	0	0	0	0	0	0	0	0	M[2:0]		Section 7.5.1
Inversion-mode	0	0	0	1	0	1	1	0	INV[2:0]		Section 7.5.2
Display-ctrl	0	0	0	0	0	1	1	1	0	0	DE	Section 7.5.3
Clock and frame frequency command											
Frame-frequency	0	0	0	1	1	1	FF[4:0]				Section 7.6.4
Display RAM commands											
Write-display-data	0	0	1	DB[7:0]							Section 7.7.1
Input-bank-select	0	0	0	0	0	0	0	1	IB[2:0]		Section 7.7.2
Output-bank-select	0	0	0	0	0	0	1	0	OB[2:0]		
Data-pointer-X	0	0	0	1	0	0	0	0	PX[6:4]		Section 7.7.3
	0	0	0	1	0	0	1	PX[3:0]			
Data-pointer-Y	0	0	0	1	0	1	0	0	0	0	PY0	

[1] For further information about the R/$\overline{W}$-bit, see Table 45 on page 65.

[2] For further information about the register selection bits, see Table 45 on page 65.

7.2 General control commands

7.2.1 Command: Initialize

This command generates a chip-wide reset by setting all commands to their default values. For further information, see Section 7.8 on page 25.

Table 5. Initialize command bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 0	-	00111010	fixed value

7.2.2 Command: OTP-refresh

Each IC is calibrated during production and testing of the device in order to achieve the specified accuracy of the V_{LCD}, the frame frequency, and the temperature measurement. This calibration is performed on EPROM cells called One Time Programmable (OTP) cells. These cells are read by the device after a reset and every time when the Initialize command or the OTP-refresh command is sent. This command takes approximately 10 ms to finish.

Table 6. OTP-refresh - OTP-refresh command bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 0	-	11011000	fixed value

7.2.3 Command: Device-address

The Device-address command allows setting the address of the device in a cascaded configuration and corresponds with pins A0 and A1 (see Section 14.2 on page 89).

Table 7. Device-address - device address command bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 2	-	000110	fixed value
1 to 0	A[1:0]		**set address**
		00[1]	master
		01	slave 1
		10	slave 2
		11	slave 3

[1] Default value.

7.2.4 Command: SYNC1_pin

With the SYNC1_pin command, the SYNC1 pin can be configured for using the PCF8538 as a single chip or a master in a cascade. If the PCF8538 is a slave in a cascade, the command has no effect.

Table 8. SYNC1_pin - SYNC1 pin configuration command bit description

This command has no effect if the PCF8538 is a slave in a cascade.

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 1	-	1011100	fixed value
0	OE		**SYNC1 pin configuration**
		0[1]	pin SYNC1 is an output; gated to 0 V; to be used when PCF8538 is a single chip
		1	pin SYNC1 is an output; providing the synchronization signal; to be used when PCF8538 is a master in a cascade

[1] Default value.

7.2.5 Command: Clock-out-ctrl

When pin CLK is configured as an output pin, the Clock-out-ctrl command enables or disables the clock output on pin CLK (Section 7.6.1 on page 21).

Table 9. Clock-out-ctrl - CLK pin input/output switch command bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 1	-	1101010	fixed value
0	COE		**control pin CLK**
		0[1]	clock signal not available on pin CLK; pin CLK is in 3-state
		1	clock signal available on pin CLK

[1] Default value.

7.2.6 Command: Read-select

The Read-select command allows choosing to readout the temperature or the device status.

Table 10. Read-select - status read select command bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 1	-	0001110	fixed value
0	SO		**readout**
		0[1]	temperature; the Status-readout command allows to readout the temperature TD[7:0], see Table 11
		1	device status: the Status-readout command allows to readout some information about the status of the device, see Table 11

[1] Default value.

7.2.7 Command: Status-readout

The Status-readout command offers to readout some status bits of the PCF8538. These bits indicate the status of the device at the moment of reading.

Table 11. Status-readout - status and temperature read command bit description

For this command, bit R/$\overline{W}$ has to be set logic 1.

Bit	Symbol	Value	Description
-	R/$\overline{W}$	1	fixed value
-	RS[1:0]	00	fixed value
Temperature readout if SO = 0 (see Table 10)			
7 to 0	TD[7:0]	00000000 to 11111111[1]	**temperature readout** (see Section 7.10.4.1 on page 40)
Device status readout if SO = 1 (see Table 10)			
7	SR7		**display status** (see Table 21 on page 20)
		0[1]	display is disabled
		1	display is enabled
6	SR6		**charge pump switching status** (status of bit CPE, see Table 13 on page 14)
		0[1]	charge pump disabled
		1	charge pump enabled
5	SR5		**charge pump charge status**
		0[1]	charge pump has not reached programmed value
		1	charge pump has reached programmed value

Table 11. Status-readout - status and temperature read command bit description *...continued*

For this command, bit R/$\overline{W}$ has to be set logic 1.

Bit	Symbol	Value	Description
4	SR4		**reset status flag**
		0	no reset has occurred since the reset status flag was cleared last time
		1[1]	reset has occurred since the reset status flag was cleared last time[2]
3 to 0	SR[3:0]		**EMC detection**
		01SA1SA0	pre-defined code for EMC detection when I^2C interface is used
		0101	pre-defined code for EMC detection when SPI interface is used

[1] Default value.

[2] The flag is set whenever a reset occurs, induced by $\overline{RST}$ pin, Power-On Reset (POR), or Initialize command. After power-on, the flag is set and should be cleared for reset monitoring.

Some bits of the Status-readout command have a certain probability of being changed by an EMC/ESD event. For example, an EMC/ESD event can cause a change of the hard-wired settings of SA1 or SA0. Therefore SR[3:0] can help to detect if an EMC/ESD event has occurred which has caused the change of a bit. In environments where EMC/ESD events may occur, it could be helpful to compare the result of the Status-readout command with the initial bit settings periodically.

7.2.8 Command: Clear-reset-flag

The Clear-reset-flag command clears the reset flag SR4, see Table 11.

Table 12. Clear-reset-flag - Clear-reset-flag command bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 0	-	00011111	fixed value

7.3 Charge pump and LCD bias control commands

7.3.1 Command: Charge-pump-ctrl

The Charge-pump-ctrl command enables or disables the internal V_{LCD} generation and controls the charge pump voltage multiplier settings.

Table 13. Charge-pump-ctrl - charge pump control command bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 4	-	1100	fixed value
3	CPE		**charge pump status**
		0[1]	charge pump disabled; no internal V_{LCD} generation; external supply of V_{LCD}
		1	charge pump enabled; internal V_{LCD} generation; no external supply of V_{LCD}
2 to 0	CPC[2:0]		**charge pump voltage multiplier setting**
		000[1]	$V_{LCD} = 2 \times V_{DD2}$
		001	$V_{LCD} = 3 \times V_{DD2}$
		010	$V_{LCD} = 4 \times V_{DD2}$
		011	$V_{LCD} = 5 \times V_{DD2}$
		100 to 111	$V_{LCD} = V_{DD2}$ (direct mode)

[1] Default value.

7.3.2 Command: Set-V_{LCD}

The Set-V_{LCD} command allows setting the LCD voltage.

Table 14. Set-V_{LCD} - Set-V_{LCD} command bit description

Bit	Symbol	Value	Description
Set-V_{LCD}-MSB			
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 5	-	010	fixed value
4 to 0	V[8:4]		**set V_{LCD} MSB**
		00000[1] to 11111	the 5 most significant bits of V[8:0]
Set-V_{LCD}-LSB			
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 4	-	0110	fixed value
3 to 0	V[3:0]		**set V_{LCD} LSB**
		0000[1] to 1111	the 4 least significant bits of V[8:0]

[1] Default value.

A value of 0h corresponds to V_{LCD} = 4 V and values equal or higher than 10Ch correspond to V_{LCD} = 12 V without temperature compensation. Every LSB change corresponds to a V_{LCD} programming step of 0.03 V. For further information, see Equation 2 on page 35 and Section 7.10.3 on page 34.

7.3.3 Command: Set-bias-mode

Table 15. Set-bias-mode - set bias mode command bit description

This command is not applicable for the static drive mode.

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 2	-	110100	fixed value
1 to 0	B[1:0]		**set bias mode**
		00[1], 01	$\frac{1}{4}$ bias
		11	$\frac{1}{3}$ bias
		10	$\frac{1}{2}$ bias

[1] Default value.

7.4 Temperature compensation control commands

7.4.1 Command: Temperature-ctrl

The Temperature-ctrl command enables or disables the temperature measurement block and the temperature compensation of V_{LCD} (see Section 7.10.4 on page 40).

Table 16. Temperature-ctrl - temperature measurement control command bit description

For this command, the register selection bits have to be set RS[1:0] = 10.

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	10	fixed value
7 to 3	-	00000	fixed value
2	TCE		**temperature compensation control**
		0[1]	temperature compensation of V_{LCD} disabled
		1	temperature compensation of V_{LCD} enabled
1	TMF		**temperature measurement filter**
		0[1]	digital temperature filter disabled[2]
		1	digital temperature filter enabled
0	TME		**temperature measurement control**
		0[1]	temperature measurement disabled; no temperature readout possible
		1	temperature measurement enabled; temperature readout possible

[1] Default value.

[2] The unfiltered digital value of TD[7:0] is immediately available for the readout and V_{LCD} compensation.

7.4.2 Command: TC-set

The TC-set command allows defining six temperature intervals in the operating temperature range from −40 °C to +85 °C. For each of the temperature intervals, the TC-slope command (see Section 7.4.3) allows setting the temperature coefficient of V_{LCD}.

Table 17. TC-set - V_{LCD} temperature compensation set command bit description

For this command, the register selection bits have to be set RS[1:0] = 10.

Bit	Symbol	Value	Description
TC-set-1			
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	10	fixed value
7 to 3	-	00111	fixed value
2 to 0	T1T[2:0]	000[1] to 111	see Table 32 on page 42
TC-set-2			
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	10	fixed value
7 to 3	-	01000	fixed value
2 to 0	T2T[2:0]	000[1] to 111	see Table 32 on page 42
TC-set-3			
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	10	fixed value
7 to 3	-	01001	fixed value
2 to 0	T3T[2:0]	000[1] to 111	see Table 32 on page 42
TC-set-4			
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	10	fixed value
7 to 3	-	01010	fixed value
2 to 0	T4T[2:0]	000[1] to 111	see Table 32 on page 42

[1] Default value.

7.4.3 Command: TC-slope

The TC-slope command allows setting the temperature coefficients of V_{LCD} corresponding to six temperature intervals defined by the TC-set command.

Table 18. TC-slope - V_{LCD} temperature compensation slope command bit description

For this command, the register selection bits have to be set RS[1:0] = 10.

Bit	Symbol	Value	Description
TC-slope-A			
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	10	fixed value
7 to 3	-	00001	fixed value
2 to 0	TSA[2:0]	000[1] to 111	see Table 33 on page 43
TC-slope-B			
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	10	fixed value
7 to 3	-	00010	fixed value
2 to 0	TSB[2:0]	000[1] to 111	see Table 33 on page 43
TC-slope-C			
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	10	fixed value
7 to 3	-	00011	fixed value
2 to 0	TSC[2:0]	000[1] to 111	see Table 33 on page 43
TC-slope-D			
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	10	fixed value
7 to 3	-	00100	fixed value
2 to 0	TSD[2:0]	000[1] to 111	see Table 33 on page 43
TC-slope-E			
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	10	fixed value
7 to 3	-	00101	fixed value
2 to 0	TSE[2:0]	000[1] to 111	see Table 33 on page 43
TC-slope-F			
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	10	fixed value
7 to 3	-	00110	fixed value
2 to 0	TSF[2:0]	000[1] to 111	see Table 33 on page 43

[1] Default value.

7.5 Display control commands

7.5.1 Command: Set-MUX-mode

The Set-MUX-mode command allows setting the multiplex drive mode.

Table 19. Set-MUX-mode - set multiplex drive mode command bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 3	-	00000	fixed value
2 to 0	M[2:0]		**set multiplex drive mode**
		000[1]	1:9 multiplex drive mode
		001	
		010	
		011	1:8 multiplex drive mode
		100	1:6 multiplex drive mode
		101	1:4 multiplex drive mode
		110	1:2 multiplex drive mode
		111	static

[1] Default value.

7.5.2 Command: Inversion-mode

The Inversion-mode command allows changing the drive scheme inversion mode.

The waveforms used to drive LCD displays (see Figure 25 on page 47 to Figure 33 on page 55) inherently produce a DC voltage across the display cell. The PCF8538 compensates for the DC voltage by inverting the waveforms on alternate frames or alternate lines. The choice of the compensation method is determined with INV[2:0] in Table 20.

Table 20. Inversion-mode - inversion mode command bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 3	-	10110	fixed value
2 to 0	INV[2:0]		**set inversion mode**
		000[1]	frame inversion mode
		001	1-line inversion mode
		010	2-line inversion mode
		011	3-line inversion mode
		100	4-line inversion mode
		101	5-line inversion mode
		110	6-line inversion mode
		111	7-line inversion mode

[1] Default value.

7.5.2.1 Line inversion mode (driving scheme A)

In line inversion mode, the DC value is compensated every n^{th} line. Changing the inversion mode to line inversion mode reduces the possibility for flickering but increases the power consumption (see example waveforms in Figure 25 on page 47 to Figure 32 on page 54)

7.5.2.2 Frame inversion mode (driving scheme B)

In frame inversion mode, the DC value is compensated across two frames and not within one frame (see example waveform in Figure 33 on page 55). Changing the inversion mode to frame inversion reduces the power consumption, therefore it is useful when power consumption is a key point in the application.

Frame inversion may not be suitable for all applications. The RMS voltage across a segment is better defined, however since the switching frequency is reduced there is possibility for flicker to occur.

7.5.3 Command: Display-ctrl

The Display-ctrl command enables or disables the display.

Table 21. Display-ctrl - display on and off switch command bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 1	-	0011100	fixed value
0	DE		**display control**
		0[1]	display disabled
		1	display enabled

[1] Default value.

7.6 Clock and frame frequency command

7.6.1 Oscillator

The internal logic and LCD drive signals of the PCF8538 are timed by the clock frequency f_{clk}, which is either internally generated by an on-chip oscillator circuit or externally supplied.

The clock frequency f_{clk} determines the internal data flow of the device that includes the transfer of display data from the display RAM to the display segment outputs and the generation of the LCD frame frequency.

7.6.2 External clock

When an external clock is used, the input pin OSC must be connected to V_{DD1}. The clock must be supplied to the CLK pin and must have an amplitude equal to the V_{DD1} voltage supplied to the chip and be referenced to V_{SS1}.

Remark: If an external clock is used, then this clock signal must always be supplied to the device. Removing the clock may freeze the LCD in a DC state, which is not suitable for the liquid crystal. Removal of the clock is possible when following the correct procedures as described in Section 7.8.4 on page 29.

7.6.3 Internal clock

In applications where the internal clock is used, the input pin OSC must be connected to V_{SS1}. It is possible to make the clock frequency available on pin CLK by setting bit COE logic 1 (see Table 9 on page 11). If pin CLK is not used, it should be left open. At power-on the signal at pin CLK is disabled and pin CLK is in 3-state.

7.6.4 Command: Frame-frequency

With this command the clock and frame frequency can be programmed when using the internal clock.

Table 22. Frame-frequency - frame frequency select command bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 5	-	111	fixed value
4 to 0	FF[4:0]	see Table 23	**clock and frame frequency (Hz)**

The duty ratio of the clock output may change when choosing different values for the frame frequency (see Table 23).

The LCD frame frequency is derived from the clock frequency by a fixed division (see Equation 1).

$$f_{fr} = \frac{f_{clk}}{144} \quad (1)$$

The Frame-frequency command allows configuring the frame frequency in the range of 45 Hz to 300 Hz with steps of

- 5 Hz from 45 Hz to 100 Hz
- 10 Hz from 100 Hz to 300 Hz

The default frame frequency of 80 Hz is factory calibrated with a tolerance of ±3 Hz at 25 °C.

Table 23. Clock and frame frequency values

Duty cycle definition: % HIGH-level time : % LOW-level time.

FF[4:0]	Frame frequency (Hz)	Clock frequency (Hz)	Typical duty cycle (%)[1]
00000	45	6472	29 : 71
00001	50	7200	20 : 80
00010	55	7945	12 : 88
00011	60	8662	4 : 96
00100	65	9366	48 : 52
00101	70	10105	44 : 56
00110	75	10766	41 : 59
00111[1]	80	11520	36 : 64
01000	85	12255	32 : 68
01001	90	12944	29 : 71
01010	95	13714	24 : 76
01011	100	14400	20 : 80
01100	110	15781	13 : 87
01101	120	17194	5 : 95
01110	130	18581	49 : 51
01111	140	20211	44 : 56
10000	150	21736	40 : 60
10001	160	23040	36 : 64
10010	170	24511	32 : 68
10011	180	26182	28 : 72
10100	190	27429	24 : 76
10101	200	28800	20 : 80
10110	210	30316	16 : 84
10111	220	32000	12 : 88
11000	230	32914	9 : 91
11001	240	34909	4 : 96
11010	250	36000	50 : 50
11011	260	37161	49 : 51
11100	270	38400	47 : 53
11101	280	39724	45 : 55
11110	290	41143	43 : 57
11111	300	42667	41 : 59

[1] Default value.

7.7 Display RAM commands

7.7.1 Command: Write-display-data

The Write-display-data command writes data byte-wise to the RAM. After Power-On Reset (POR) the RAM content is random and should be brought to a defined status by clearing it (setting it logic 0).

Table 24. Write-display-data - write display data command bit description

For this command, the register selection bits have to be set RS[1:0] = 01.

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	01	fixed value
7 to 0	DB[7:0]	00000000 to 11111111	**writing data byte-wise to RAM**

More information about the display RAM can be found in Section 7.14 on page 57.

7.7.2 Bank select commands

For multiplex drive modes 1:4, 1:2, and static drive mode, it is possible to write data to one area of the RAM while displaying from another. These areas are named as RAM banks. Input and output banks can be set independently from one another with the Input-bank-select and the Output-bank-select command. More information about RAM bank switching can be found in Section 7.14.3 on page 62.

7.7.2.1 Command: Input-bank-select

Table 25. Input-bank-select - input bank select command bit description

This command is not applicable for multiplex drive mode 1:6, 1:8, and 1:9.

Bit	Symbol	Value	Description		
-	R/$\overline{W}$	0	fixed value	-	R/$\overline{W}$
-	RS[1:0]	00	fixed value	-	RS[1:0]
7 to 3	-	00001	fixed value		
2 to 0	IB[2:0]		**selects RAM bank to write to**		
			static drive mode	**1:2 drive mode**	**1:4 drive mode**
		000[1]	bank 0: RAM-row 0	bank 0: RAM-rows 0 and 1	bank 0: RAM-rows 0, 1, 2, and 3
		001	bank 1: RAM-row 1		
		010	bank 2: RAM-row 2	bank 2: RAM-rows 2 and 3	
		011	bank 3: RAM-row 3		
		100	bank 4: RAM-row 4	bank 4: RAM-rows 4 and 5	bank 4: RAM-rows 4, 5, 6, and 7
		101	bank 5: RAM-row 5		
		110	bank 6: RAM-row 6	bank 6: RAM-rows 6 and 7	
		111	bank 7: RAM-row 7		

[1] Default value.

7.7.2.2 Command: Output-bank-select

Table 26. Output-bank-select - output bank select command bit description

This command is not applicable for multiplex drive mode 1:6, 1:8, and 1:9.

Bit	Symbol	Value	Description		
-	R/$\overline{W}$	0	fixed value	-	R/$\overline{W}$
-	RS[1:0]	00	fixed value	-	RS[1:0]
7 to 3	-	00010	fixed value		
2 to 0	OB[2:0]		**selects RAM bank to read from to the LCD**		
			static drive mode	**1:2 drive mode**	**1:4 drive mode**
		000[2]	bank 0: RAM-row 0	bank 0: RAM-rows 0 and 1	bank 0: RAM-rows 0, 1, 2, and 3
		001	bank 1: RAM-row 1		
		010	bank 2: RAM-row 2	bank 2: RAM-rows 2 and 3	
		011	bank 3: RAM-row 3		
		100	bank 4: RAM-row 4	bank 4: RAM-rows 4 and 5	bank 4: RAM-rows 4, 5, 6, and 7
		101	bank 5: RAM-row 5		
		110	bank 6: RAM-row 6	bank 6: RAM-rows 6 and 7	
		111	bank 7: RAM-row 7		

[2] Default value.

7.7.3 Commands: Data-pointer-X and Data-pointer-Y

The Data-pointer-X and Data-pointer-Y commands define the display RAM address where the following display data will be sent to.

Table 27. Data-pointer-X and Data-pointer-Y - set data pointer command bit description

Bit	Symbol	Value	Description
Data-pointer-X-MSB: PX[6:4]			
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 3	-	10000	fixed value
2 to 0	PX[6:4]	000[1] to 111	3-bit binary value
Data-pointer-X-LSB: PX[3:0]			
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 4	-	1001	fixed value
3 to 0	PX[3:0]	0000[1] to 1111	4-bit binary value
Data-pointer-Y: PY0			
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 1	-	1010000	fixed value
0	PY0	0[1] to 1	1-bit binary value

[1] Default value.

7.8 Start-up and shut-down

7.8.1 Power-On Reset (POR)

At power-on, the PCF8538 resets to the following starting conditions:

1. All backplane and segment outputs are set to V_{SS1}.
2. Selected drive mode is: 1:9 with $\frac{1}{4}$ bias.
3. Input and output bank selectors are reset.
4. The interface is initialized.
5. The data pointer is cleared (set logic 0).
6. The internal oscillator is disabled.
7. Temperature measurement is disabled.
8. Temperature filter is disabled.
9. The internal V_{LCD} voltage generation is disabled. The charge pump is switched off.
10. The V_{LCD} temperature compensation is disabled.
11. The display is disabled.

The reset state is as shown in Table 28.

Table 28. Reset state of PCF8538

Command name	Command bits							
	7	6	5	4	3	2	1	0
General control commands								
Device-address	0	0	0	1	1	0	0	0
SYNC1_pin	1	0	1	1	1	0	0	0
Clock-out-ctrl	1	1	0	1	0	1	0	0
Read-select	0	0	0	1	1	1	0	0
Status-readout	1	1	1	1	1	1	1	1
	0	0	0	1	0	1	0/SA1	1/SA0
Charge pump and LCD bias control commands								
Charge-pump-ctrl	1	1	0	0	0	0	0	0
Set-V_{LCD}	0	1	0	0	0	0	0	0
	0	1	1	0	0	0	0	0
Set-bias-mode	1	1	0	1	0	0	0	0

Table 28. Reset state of PCF8538 *...continued*

Command name	Command bits							
	7	6	5	4	3	2	1	0
Temperature compensation control commands								
Temperature-ctrl	0	0	0	0	0	0	0	0
TC-slope-A	0	0	0	0	1	0	0	0
TC-slope-B	0	0	0	1	0	0	0	0
TC-slope-C	0	0	0	1	1	0	0	0
TC-slope-D	0	0	1	0	0	0	0	0
TC-slope-E	0	0	1	0	1	0	0	0
TC-slope-F	0	0	1	1	0	0	0	0
TC-set-1	0	0	1	1	1	0	0	0
TC-set-2	0	1	0	0	0	0	0	0
TC-set-3	0	1	0	0	1	0	0	0
TC-set-4	0	1	0	1	0	0	0	0
Display control commands								
Set-MUX-mode	0	0	0	0	0	0	0	0
Inversion-mode	1	0	1	1	0	0	0	0
Display-ctrl	0	0	1	1	1	0	0	0
Clock and frame frequency command								
Frame-frequency	1	1	1	0	0	1	1	1
Display RAM commands								
Input-bank-select	0	0	0	0	1	0	0	0
Output-bank-select	0	0	0	1	0	0	0	0
Data-pointer-X-MSB	1	0	0	0	0	0	0	0
Data-pointer-X-LSB	1	0	0	1	0	0	0	0
Data-pointer-Y	1	0	1	0	0	0	0	0

Remarks:

1. Do not transfer data for at least 1 ms after a power-on to allow the reset action to complete.
2. The first command sent to the device after the power-on event must be the Initialize command (see Section 7.2.1 on page 10).
3. After Power-On Reset (POR) and before enabling the display, the RAM content should be brought to a defined status
   - by clearing it (setting it all logic 0) or
   - by writing meaningful content (for example, a graphic)

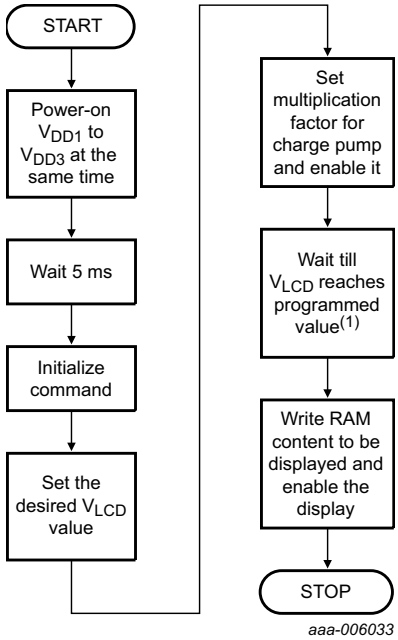
   otherwise unwanted display artifacts may appear on the display.

7.8.2 Reset pin function

The reset pin of the PCF8538 resets all the registers to their default state (see Table 28). The RAM contents remain unchanged. After the reset signal is removed, the PCF8538 will behave in the same manner as at POR. See Section 7.8.1 for details.

7.8.3 Recommended start-up sequences

This section describes how to proceed with the initialization of the chip in different application modes.



(1) This time depends on the external capacitor on the V_{LCD} pins. For a capacitor of 100 nF a delay of about 55 ms to 65 ms is expected.

Fig 3. Recommended start-up sequence when using the internal charge pump and the internal clock signal

When using the internal V_{LCD} generation, the display must not be enabled before the generation of V_{LCD} with the internal charge pump is completed. Otherwise unwanted display artifacts may appear on the display.

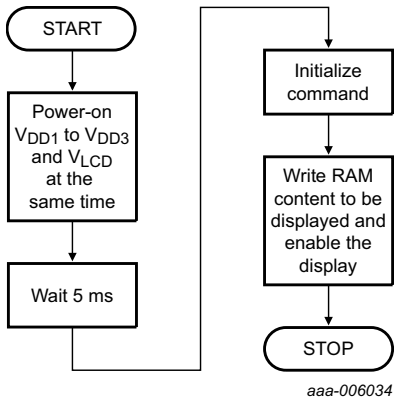
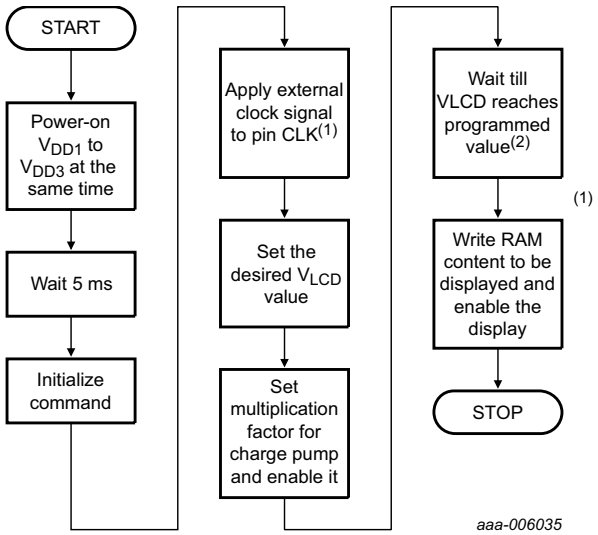


Fig 4. Recommended start-up sequence when using an external supplied V_{LCD} and the internal clock signal



(1) Alternatively, the external clock signal can be applied after the generation of the V_{LCD} voltage.

(2) This time depends on the external capacitor on the V_{LCD} pins. For a capacitor of 100 nF a delay of about 55 ms to 65 ms is expected.

Fig 5. Recommended start-up sequence when using the internal charge pump and an external clock signal

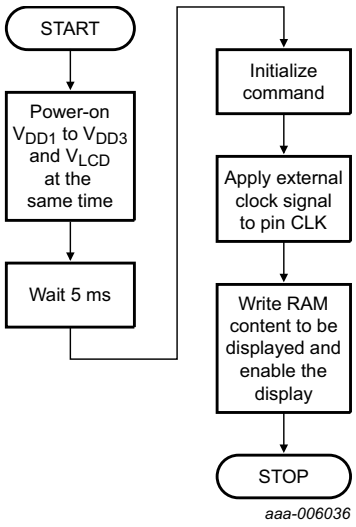
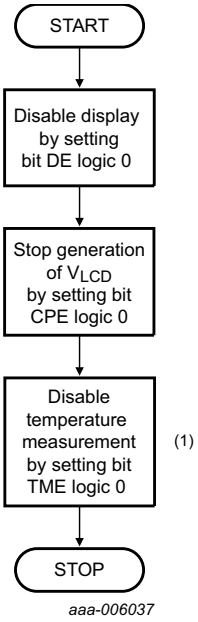


Fig 6. Recommended start-up sequence when using an external supplied V_{LCD} and an external clock signal

7.8.4 Recommended power-down sequences

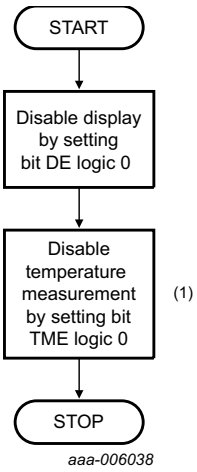
With the following sequences, the PCF8538 can be set to a state of minimum power consumption, called power-down mode.



(1) If previously enabled.

Remark: When bits DE (Table 21 on page 20), CPE (Table 13 on page 14) and TME (Table 16 on page 16) are logic 0, the internal clock signal is switched off.

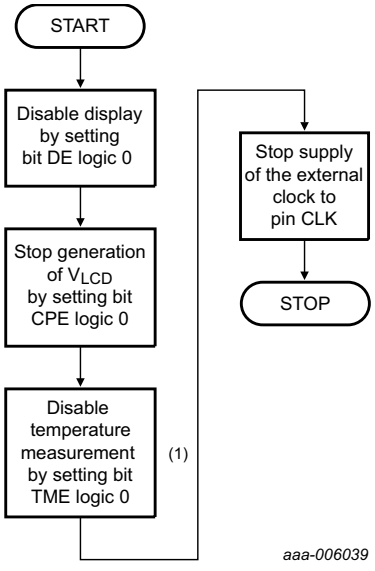
Fig 7. Recommended power-down sequence for minimum power-down current when using the internal charge pump and the internal clock signal



(1) If previously enabled.

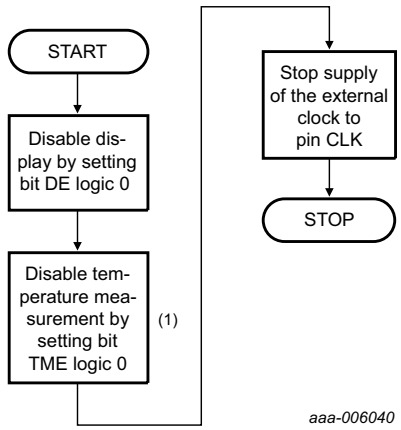
Remark: When bits DE (Table 21 on page 20), CPE (Table 13 on page 14) and TME (Table 16 on page 16) are logic 0, the internal clock signal is switched off.

Fig 8. Recommended power-down sequence when using an external supplied V_{LCD} and the internal clock signal



(1) If previously enabled.

Fig 9. Recommended power-down sequence when using the internal charge pump and an external clock signal



(1) If previously enabled.

Fig 10. Recommended power-down sequence when using an external supplied V_{LCD} and an external clock signal

Remarks:

1. It is necessary to run the power-down sequence before removing the supplies. Depending on the application, care must be taken that no other signals are present at the chip input or output pins when removing the supplies (refer to Section 9 on page 72). Otherwise this may cause unwanted display artifacts. Uncontrolled removal of supply voltages will not damage the PCF8538.
2. Static voltages across the liquid crystal display can build up when the external LCD supply voltage (V_{LCD}) is on while the IC supply voltage (V_{DD1} to V_{DD3}) is off, or the other way round. This may cause unwanted display artifacts. To avoid such artifacts, external V_{LCD}, V_{DD1} to V_{DD3} must be applied or removed together.
3. A clock signal must always be supplied to the device when the device is active. Removing the clock may freeze the LCD in a DC state, which is not suitable for the liquid crystal. It is recommended to disable the display first and to remove the clock signal afterwards.

7.9 Possible display configurations

The display configurations possible with the PCF8538 depend on the number of active backplanes outputs required. A selection of possible display configurations is given in Table 29.

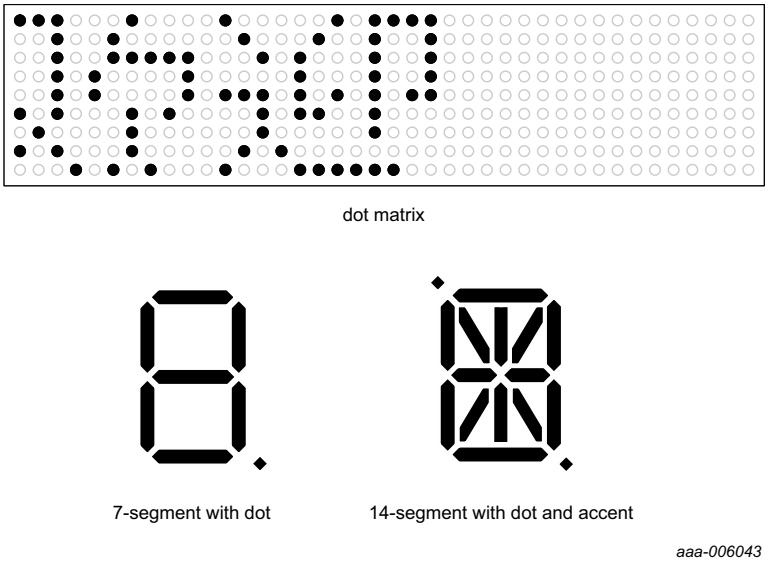


Fig 11. Example of display types suitable for PCF8538

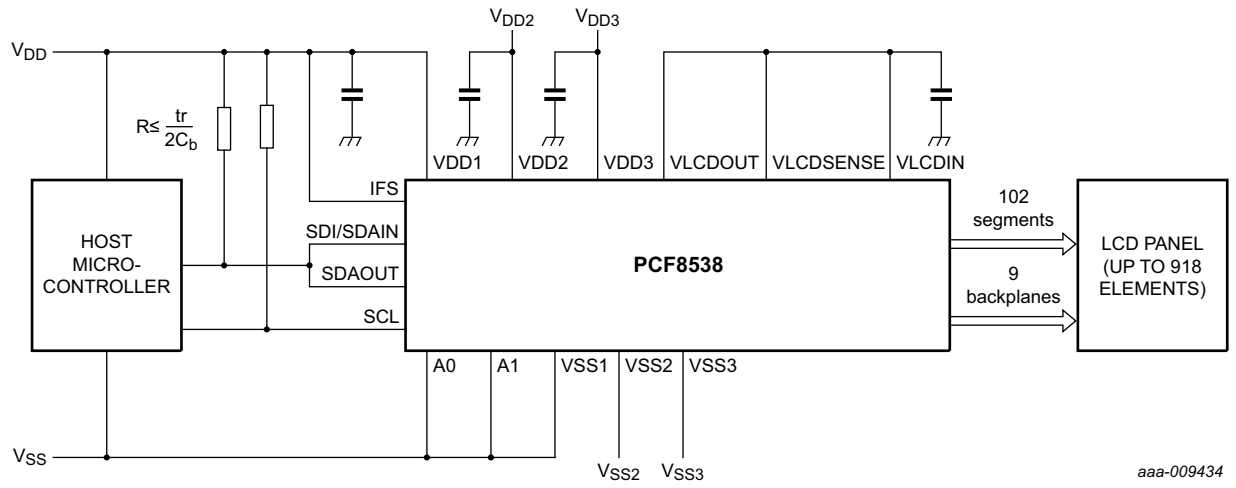
Table 29. Selection of possible display configurations

Number of				
Backplanes	**Icons**	**Digits/Characters**		**Dot matrix/ Elements**
		7-segment[1]	**14-segment[2]**	
9	918	114	57	918 dots (9 × 102)
8	816	102	51	816 dots (8 × 102)
6	612	76	38	612 dots (6 × 102)
4	408	51	25	408 dots (4 × 102)
2	204	25	12	204 dots (2 × 102)
1	102	12	6	102 dots (1 × 102)

[1] 7 segment display has 8 elements including the decimal point.

[2] 14 segment display has 16 elements including decimal point and accent dot.

All the display configurations in Table 29 can be implemented in the typical systems shown in Figure 12 and Figure 13.

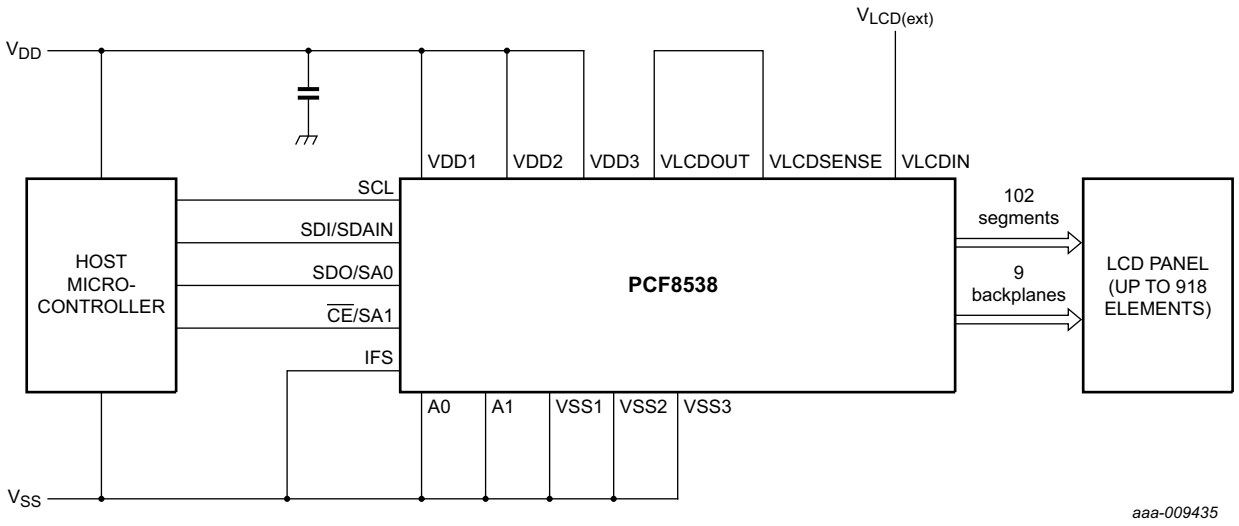


V_{DD1} to V_{DD3} from 2.5 V to 5.5 V.

V_{DD1} to V_{DD3} can be connected to the same power supply.

V_{SS1} to V_{SS3} can be connected to the same ground supply.

Fig 12. Typical system configuration if using the internal V_{LCD} generation and I^2C-bus



V_{DD1} to V_{DD3} from 2.5 V to 5.5 V.

Fig 13. Typical system configuration if using the external V_{LCD} and SPI-bus

The host microcontroller maintains the communication channel with the PCF8538. The only other connections required to complete the system are the power supplies, the V_{LCD} pins, the external capacitors, and the LCD panel selected for the application. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally.

External capacitors of 100 nF minimum are required on each of the pins VDD1 to VDD3. VDD1 to VDD3 can be connected to the same power supply. In this case, a capacitor of 300 nF minimum is required.

VSS1 to VSS3 can be connected to the same ground supply.

The VLCD pins (VLCDOUT, VLCDSENSE, VLCDIN) can be connected if V_{LCD} is supplied from external. An external capacitor of 300 nF minimum is recommended for VLCD. For high display loads, 1 μF is suggested.

7.10 LCD voltage

7.10.1 V_{LCD} pins

The PCF8538 has 3 V_{LCD} pins:

VLCDIN — V_{LCD} supply input

VLCDOUT — V_{LCD} voltage output

VLCDSENSE — V_{LCD} regulation circuitry input

The V_{LCD} voltage can be generated on-chip or externally supplied.

Internal V_{LCD} generation: When the internal V_{LCD} generation is selected (CPE = 1), the V_{LCD} voltage is available on pin VLCDOUT. The pins VLCDIN and VLCDSENSE must be connected to the pin VLCDOUT.

External V_{LCD} supply: When the external V_{LCD} supply is selected (CPE = 0), the V_{LCD} voltage must be supplied to the pin VLCDIN. The pins VLCDOUT and VLCDSENSE should be connected together.

7.10.2 External V_{LCD} supply

V_{LCD} can be directly supplied to the VLCDIN pin. In this case, the internal charge pump must not be enabled, otherwise an extra current may occur on pin VDD2 and pin VLCD. When V_{LCD} is supplied externally, no internal temperature compensation occurs on this voltage even if bit TCE is set logic 1 (see Section 7.10.4). The V_{LCD} voltage which is supplied externally will be available at the segments and backplanes of the device through the chosen bias system. Also programming the V[8:0] bit field has no effect on the externally supplied V_{LCD}.

7.10.3 Internal V_{LCD} generation

V_{LCD} can be generated by an on-chip charge pump and controlled by command (Table 14 on page 14). The V_{LCD} voltage is available on pin VLCDOUT.

The charge pump is controlled by the Charge-pump-ctrl command (see Table 13 on page 14). It can be enabled with the CPE bit. The multiplier setting can be configured with the CPC[2:0] bits. The charge pump can generate a V_{LCD} up to $5 \times V_{DD2}$.

7.10.3.1 V_{LCD} programming

V_{LCD} can be programmed by using the V[8:0] (see Table 14 on page 14).

The final value of V_{LCD} is a combination of the programmed V[8:0] value and the output of the temperature compensation block, VT[8:0] (see Equation 2). The system is exemplified in Figure 14.

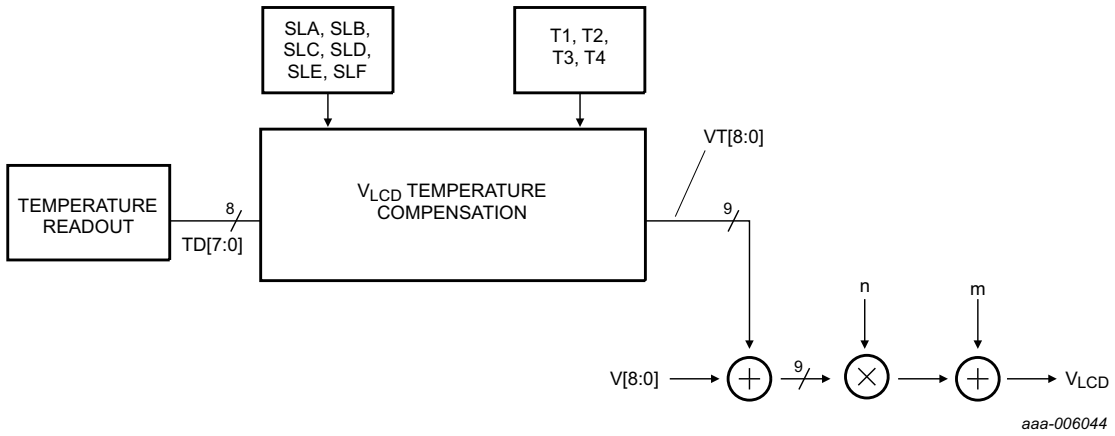


Fig 14. V_{LCD} generation including temperature compensation

In Equation 2 the main parameters are the programmed digital value term and the compensated temperature term.

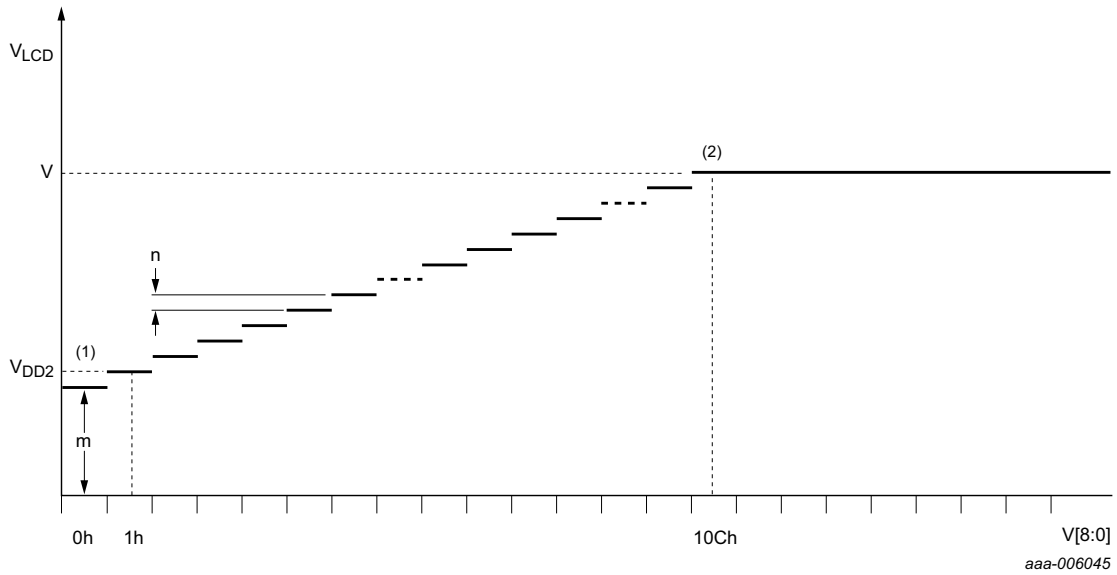
$$V_{LCD} = [V[8:0] + VT[8:0]] \times n + m \quad (2)$$

1. V[8:0] is the binary value of the programmed voltage.
2. VT[8:0] is the binary value of the temperature compensated voltage. Its value comes from the temperature compensation block and is a two's complement which has the value 0h at 20 °C.
3. m and n are fixed values (see Table 30 and Figure 15).

Table 30. Parameters of V_{LCD} generation

Symbol	Value	Unit
m	3.99	V
n	0.03	V

Figure 15 shows how V_{LCD} changes with the programmed value of V[8:0].



(1) V[8:0] must be set so that $V_{LCD} > V_{DD2}$.

(2) Automatic limitation for $V_{LCD} > 12$ V.

Fig 15. V_{LCD} programming of PCF8538 (assuming VT[8:0] = 0h)

Remarks:

1. It is important that V[8:0] is set to such a value that the resultant V_{LCD}, including the temperature compensation VT[8:0], is higher than V_{DD2}.
2. Programmable range of V[8:0] is from 0h to 1FFh. This would allow achieving a V_{LCD} above 12 V but 12 V is the built-in automatic limit.

7.10.3.2 V_{LCD} driving capability

Figure 16 illustrates the main factor determining how much current the charge pump can deliver.

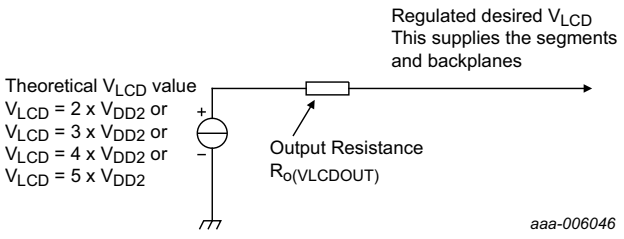


Fig 16. Charge pump model (used to characterize the driving strength)

The output resistance of the charge pump is specified in Table 31.

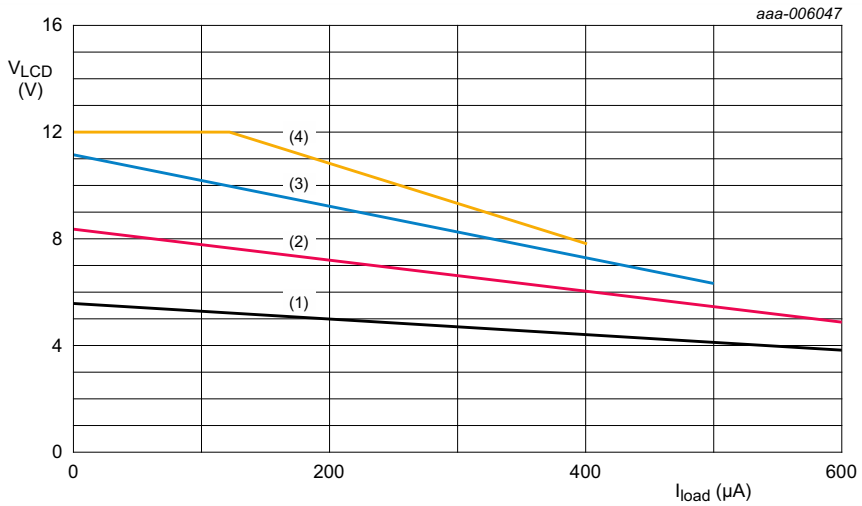
Table 31. Output resistance of the charge pump

$R_{ITO(VSS2)}$, $R_{ITO(VDD2)}$, $R_{ITO(VLCDOUT)}$ = 50 Ω.

Charge pump configuration	$R_{o(VLCDOUT)}$ (typical)	Unit
$V_{LCD} = 2 \times V_{DD2}$	2.5	kΩ
$V_{LCD} = 3 \times V_{DD2}$	6	kΩ
$V_{LCD} = 4 \times V_{DD2}$	10.5	kΩ
$V_{LCD} = 5 \times V_{DD2}$	18	kΩ

Remark: The PCF8538 has a built-in automatic limitation of V_{LCD}, set to 12 V. The maximum V_{LCD} that can be programmed is expressed by the following equation: $V_{LCD(max)} = min(12\ V, n \times V_{DD2} - R_{o(VLCDOUT)} \times I_{load})$, where n is the multiplication factor of the charge pump. I_{load} is the overall current sink by the segments and backplanes outputs depending on the display, plus the on-chip V_{LCD} current consumption.

With these values, it can be calculated how much current the charge pump can drive under certain conditions, as shown in Figure 17 and Figure 18.



Conditions: V_{DD2} = 3.0 V, $R_{ITO(VSS2)}$, $R_{ITO(VDD2)}$, $R_{ITO(VLCDOUT)}$ = 50 Ω, T_{amb} = 27 °C.

Charge pump configuration:

(1) $V_{LCD} = 2 \times V_{DD2}$.

(2) $V_{LCD} = 3 \times V_{DD2}$.

(3) $V_{LCD} = 4 \times V_{DD2}$.

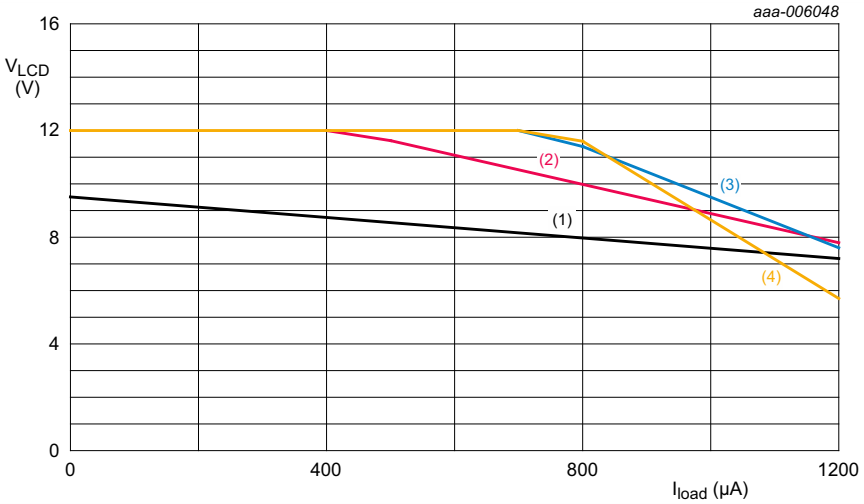
(4) $V_{LCD} = 5 \times V_{DD2}$.

I_{load} is the overall current sink by the segments and backplanes outputs depending on the display, plus the on-chip V_{LCD} current consumption.

Reading example: V_{LCD} can be programmed to 10 V by using the charge pump configuration (3) or (4). With configuration (3), V_{LCD} can be programmed to 10 V for a current load up to about 120 μA. With configuration (4), V_{LCD} can be programmed to 10 V for a current load up to about 260 μA.

Remark: Only the charge pump configuration (4) allows programming V_{LCD} = 12 V when V_{DD2} = 3.0 V.

Fig 17. Charge pump driving capability with V_{DD2} = 3.0 V



Conditions: V_{DD2} = 5.0 V, $R_{ITO(VSS2)}$, $R_{ITO(VDD2)}$, $R_{ITO(VLCDOUT)}$ = 50 Ω, T_{amb} = 27 °C.

Charge pump configuration:

(1) $V_{LCD} = 2 \times V_{DD2}$.

(2) $V_{LCD} = 3 \times V_{DD2}$.

(3) $V_{LCD} = 4 \times V_{DD2}$.

(4) $V_{LCD} = 5 \times V_{DD2}$.

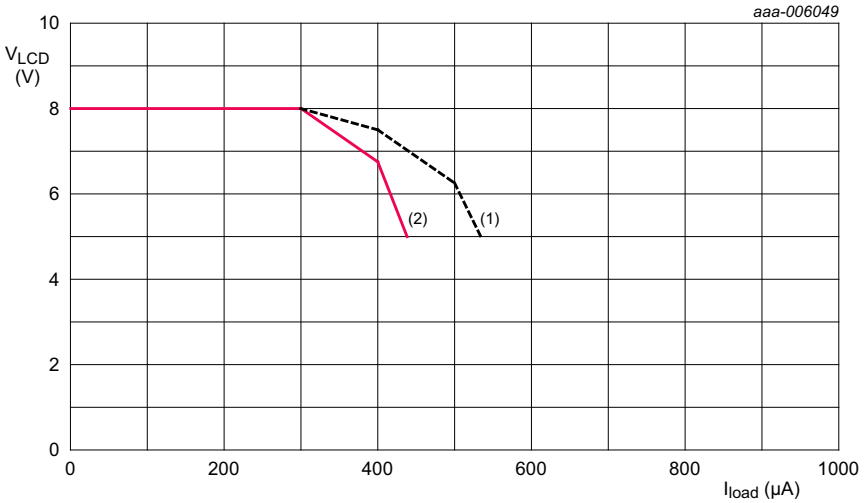
I_{load} is the overall current sink by the segment and backplane outputs depending on the display, plus the on-chip V_{LCD} current consumption.

Reading example: V_{LCD} can be programmed to 10 V by using the charge pump configuration (2) or (3). With configuration (2), V_{LCD} can be programmed to 10 V for a current load up to about 780 μA. With configuration (3), V_{LCD} can be programmed to 10 V for a current load up to about 940 μA.

Remark: The charge pump configuration (4) has no benefit compared to configuration (3) and is therefore not recommended when V_{DD2} = 5.0 V.

Fig 18. Charge pump driving capability with V_{DD2} = 5.0 V

It has to be considered that the driving capability of the charge pump is depending on the resistance of the Indium Tin Oxide (ITO) tracks, see Figure 20 and Figure 19.



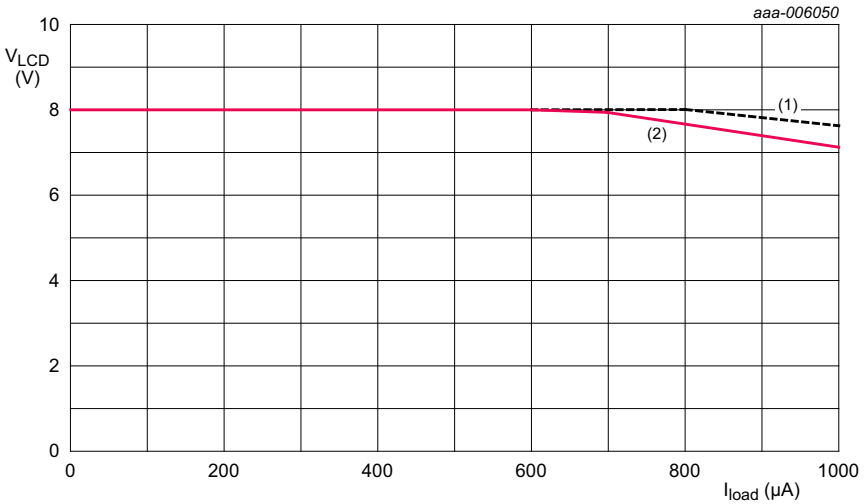
Conditions: V_{DD2} = 3 V; charge pump configuration: $V_{LCD} = 4 \times V_{DD2}$; V_{LCD} = 8 V; T_{amb} = 27 °C.

(1) $R_{ITO(VSS2)}$, $R_{ITO(VDD2)}$, $R_{ITO(VLCDOUT)}$ = 50 Ω.

(2) $R_{ITO(VSS2)}$, $R_{ITO(VDD2)}$, $R_{ITO(VLCDOUT)}$ = 100 Ω.

I_{load} is the overall current sink of the segment and backplane outputs depending on the display, plus the on-chip V_{LCD} current consumption.

Fig 19. V_{LCD} with respect to I_{load} at V_{DD2} = 3 V



Conditions: V_{DD2} = 5 V; charge pump configuration: $V_{LCD} = 2 \times V_{DD2}$; V_{LCD} = 8 V; T_{amb} = 27 °C.

(1) $R_{ITO(VSS2)}$, $R_{ITO(VDD2)}$, $R_{ITO(VLCDOUT)}$ = 50 Ω.

(2) $R_{ITO(VSS2)}$, $R_{ITO(VDD2)}$, $R_{ITO(VLCDOUT)}$ = 100 Ω.

I_{load} is the overall current sink of the segment and backplane outputs depending on the display, plus the on-chip V_{LCD} current consumption.

Fig 20. V_{LCD} with respect to I_{load} at V_{DD2} = 5 V

7.10.4 Temperature measurement and temperature compensation of V_{LCD}

7.10.4.1 Temperature readout

The PCF8538 has a built-in temperature sensor which provides an 8-bit digital value (TD[7:0]) of the ambient temperature. This value can be read by command (see Section 7.2.6 on page 12 and Section 7.2.7 on page 12). The actual temperature is determined from TD[7:0] using Equation 3.

$$T(°C) = 0.6275 \times TD[7:0] - 40 \quad (3)$$

TD[7:0] = FFh means that no temperature readout is available or was performed. FFh is the default value after Power-On Reset (POR). The measurement needs about 8 ms to complete. It is repeated periodically every second as long as bit TME is set logic 1 (see Table 16 on page 16).

Due to the nature of a temperature sensor, oscillations may occur. To avoid this, a filter has been implemented in PCF8538. A control bit, TMF, is implemented to enable or disable the digital temperature filter (see Table 16 on page 16). The system is exemplified in Figure 21.

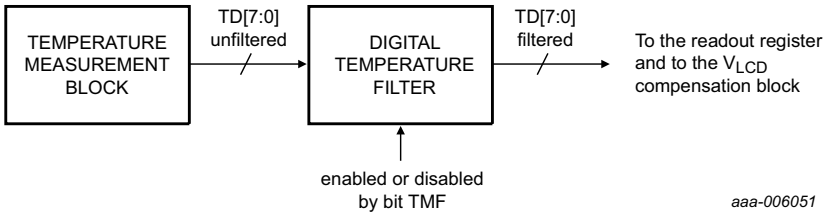
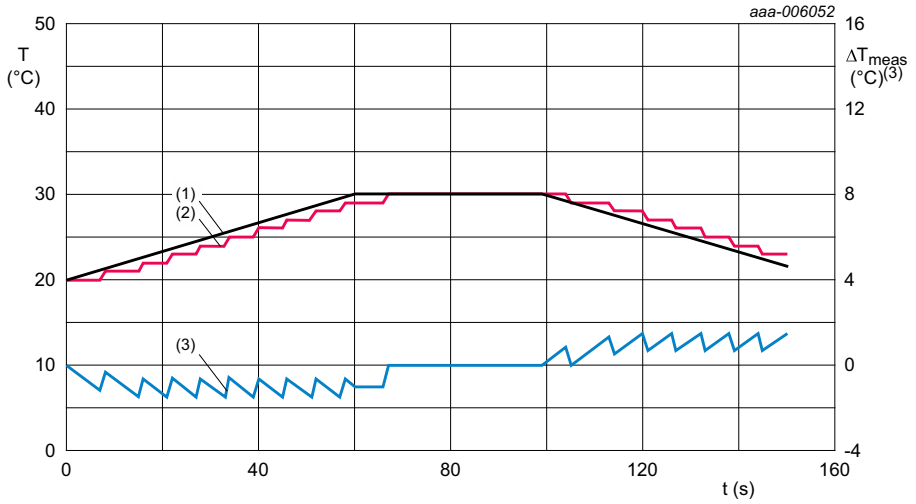


Fig 21. Temperature measurement block with digital temperature filter

The digital temperature filter introduces a certain delay in the measurement of the temperature. This behavior is illustrated in Figure 22.



(1) Environment temperature, T1 (°C).

(2) Measured temperature, T2 (°C).

(3) Temperature deviation, ΔT = T2 – T1.

Fig 22. Temperature measurement delay

7.10.4.2 Temperature adjustment of the V_{LCD}

Due to the temperature dependency of the liquid crystal viscosity, the LCD supply voltage may have to be adjusted at different temperatures to maintain optimal contrast. The temperature characteristics of the liquid is provided by the LCD manufacturer. The slope has to be set to compensate for the liquid behavior. Internal temperature compensation can be enabled via bit TCE (see Table 16 on page 16).

The ambient temperature range is split up to six programmable regions and to each a different temperature coefficient can be applied (see Figure 23).

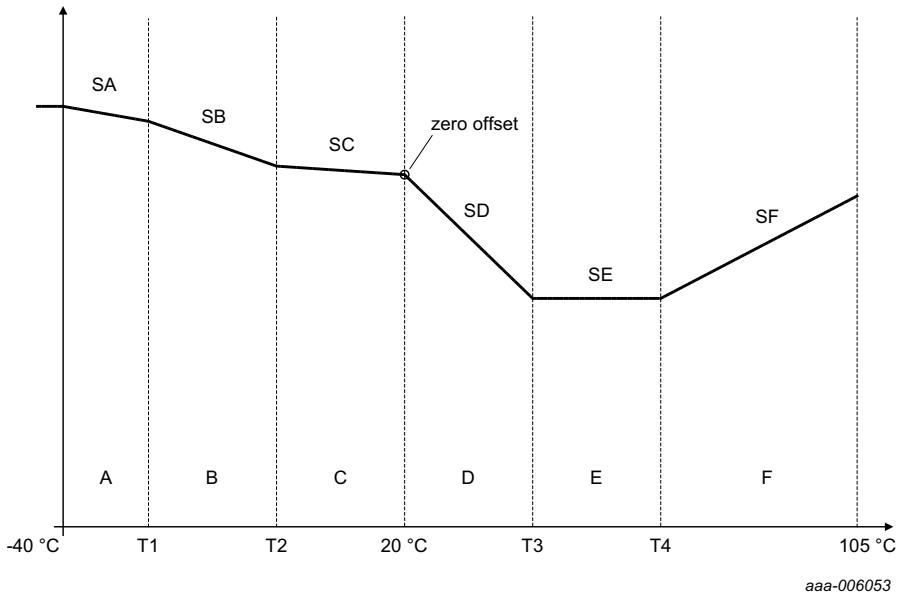


Fig 23. Example of segmented temperature coefficients

The temperature regions are determined by programming the temperature limits T1 to T4 via the TC-set-1 to TC-set-4 commands (see Section 7.4.2 on page 17). The temperature coefficients can be selected from a choice of eight different slopes. Each one of theses coefficients is independently selected via the TC-slope command (see Section 7.4.3 on page 18).

Table 32. Temperature regions

T1T[2:0] to T4T[2:0]	Temperature region 1 and 2		Temperature region 3 and 4	
	T1, T2 (°C)	Corresponding TD value[1]	T3, T4 (°C)	Corresponding TD value[1]
000	–34	10	+29	110
001	–27	20	+38	124
010	–21	30	+47	138
011	–15	40	+55	152
100	–9	50	+64	166
101	–2	60	+73	180
110	+4	70	+82	194
111	+10	80	+91	208

[1] The relation between the actual temperature and TD[7:0] is derived from Equation 3 on page 40.

Remark: The programming has to be made such that T1 < T2 and T3 < T4 otherwise the V_{LCD} temperature compensation will not be executed.

Table 33. Temperature coefficients

TSA[2:0] to TSF[2:0] value	Slope factor (mV/°C)	Temperature coefficients SA to SF[1]
000[2]	0	0.000
001	–6	–0.125
010	–12	–0.250
011	–24	–0.500
100	–60	–1.250
101	+6	+0.125
110	+12	+0.250
111	+24	+0.500

[1] The relationship between the temperature coefficients SA to SF and the slope factor is derived from the following equation: $Sn = \frac{0.6275(°C)}{\text{LSB of V[8:0]}(mV)} \times \text{slope factor (mV/°C)}$, where LSB of V[8:0] ≅ 30 mV.

[2] Default value.

The binary value of the temperature compensated voltage VT[8:0] is calculated according to Table 34.

Table 34. Calculation of the temperature compensated value VT

Temperature (°C)	Digital temperature: TD[7:0]	Binary value of the temperature compensated voltage: VT[8:0]
$T \leq -40\ °C$	$TD[7:0] = 0$	$-(96 - T2) \times SC - (T2 - T1) \times SB - T1 \times SA$
$-40\ °C < T \leq T1$	$0 < TD[7:0] \leq T1$	$-(96 - T2) \times SC - (T2 - T1) \times SB - (T1 - TD[7:0]) \times SA$
$T1 < T \leq T2$	$T1 < TD[7:0] \leq T2$	$-(96 - T2) \times SC - (T2 - TD[7:0]) \times SB$
$T2 < T \leq 20\ °C$	$T2 < TD[7:0] \leq 96$	$-(96 - TD[7:0]) \times SC$
$20\ °C < T \leq T3$	$96 < TD[7:0] \leq T3$	$(TD[7:0] - 96) \times SD$
$T3 < T \leq T4$	$T3 < TD[7:0] \leq T4$	$(T3 - 96) \times SD + (TD[7:0] - T3) \times SE$
$T4 < T \leq 85\ °C$	$T4 < TD[7:0] \leq 231$	$(T3 - 96) \times SD + (T4 - T3) \times SE + (TD[7:0] - T4) \times SF$

7.10.5 LCD voltage selector

The LCD voltage selector co-ordinates the multiplexing of the LCD in accordance with the selected LCD drive configuration. The operation of the voltage selector is controlled by the Set-bias-mode command (see Table 15 on page 15) and the Set-MUX-mode command (see Table 19 on page 19).

Table 35. LCD drive modes: summary of characteristics

LCD drive mode	Number of:		LCD bias configuration	$\frac{V_{off(RMS)}}{V_{LCD}}$	$\frac{V_{on(RMS)}}{V_{LCD}}$	$D = \frac{V_{on(RMS)}}{V_{off(RMS)}}$ [1]	V_{LCD} [2]
	Backplanes	Levels					
static	1	2	static	0	1	∞	$V_{on(RMS)}$
1:2 multiplex	2	3	½	0.354	0.791	2.236	$2.828 \times V_{off(RMS)}$
1:2 multiplex	2	4	⅓	0.333	0.745	2.236	$3.0 \times V_{off(RMS)}$
1:2 multiplex[3]	2	5	¼	0.395	0.729	1.845	$2.529 \times V_{off(RMS)}$
1:4 multiplex[3]	4	3	½	0.433	0.661	1.527	$2.309 \times V_{off(RMS)}$
1:4 multiplex	4	4	⅓	0.333	0.577	1.732	$3.0 \times V_{off(RMS)}$
1:4 multiplex	4	5	¼	0.331	0.545	1.646	$3.024 \times V_{off(RMS)}$
1:6 multiplex[3]	6	3	½	0.456	0.612	1.341	$2.191 \times V_{off(RMS)}$
1:6 multiplex	6	4	⅓	0.333	0.509	1.527	$3.0 \times V_{off(RMS)}$
1:6 multiplex	6	5	¼	0.306	0.467	1.527	$3.266 \times V_{off(RMS)}$
1:8 multiplex[3]	8	3	½	0.467	0.586	1.254	$2.138 \times V_{off(RMS)}$
1:8 multiplex	8	4	⅓	0.333	0.471	1.414	$3.0 \times V_{off(RMS)}$
1:8 multiplex	8	5	¼	0.293	0.424	1.447	$3.411 \times V_{off(RMS)}$
1:9 multiplex[3]	9	3	½	0.471	0.577	1.225	$2.121 \times V_{off(RMS)}$
1:9 multiplex	9	4	⅓	0.333	0.454	1.374	$3.000 \times V_{off(RMS)}$
1:9 multiplex	9	5	¼	0.289	0.408	1.414	$3.464 \times V_{off(RMS)}$

[1] Determined from Equation 6.

[2] Determined from Equation 5.

[3] In these examples, the discrimination factor and hence the contrast ratios are smaller. The advantage of these LCD drive modes is a power saving from a reduction of V_{LCD}.

Intermediate LCD biasing voltages are obtained from an internal voltage divider. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of V_{LCD} and the resulting discrimination ratios (D), are given in Table 35. Discrimination is a term which is defined as the ratio of the on and off RMS voltage across a segment. It can be thought of as a measurement of contrast.

A practical value for V_{LCD} is determined by equating $V_{off(RMS)}$ with a defined LCD threshold voltage ($V_{th(off)}$), typically when the LCD exhibits approximately 10 % contrast. In the static drive mode, a suitable choice is $V_{LCD} > 3V_{th(off)}$.

Bias is calculated by $\frac{1}{1+a}$, where the values for a are

a = 1 for ½ bias

a = 2 for ⅓ bias

a = 3 for ¼ bias

The RMS on-state voltage ($V_{on(RMS)}$) for the LCD is calculated with Equation 4:

$$V_{on(RMS)} = V_{LCD}\sqrt{\frac{a^2 + 2a + n}{n \times (1+a)^2}} \quad (4)$$

where V_{LCD} is the resultant voltage at the LCD segment and where the values for n are

n = 1 for static mode

n = 2 for 1:2 multiplex

n = 4 for 1:4 multiplex

n = 6 for 1:6 multiplex

n = 8 for 1:8 multiplex

n = 9 for 1:9 multiplex

The RMS off-state voltage ($V_{off(RMS)}$) for the LCD is calculated with Equation 5:

$$V_{off(RMS)} = V_{LCD}\sqrt{\frac{a^2 - 2a + n}{n \times (1 + a)^2}} \quad (5)$$

Discrimination is the ratio of $V_{on(RMS)}$ to $V_{off(RMS)}$ and is determined from Equation 6:

$$D = \frac{V_{on(RMS)}}{V_{off(RMS)}} = \sqrt{\frac{a^2 + 2a + n}{a^2 - 2a + n}} \quad (6)$$

V_{LCD} is sometimes referred as the LCD operating voltage.

7.10.5.1 Electro-optical performance

Suitable values for $V_{on(RMS)}$ and $V_{off(RMS)}$ are dependent on the LCD liquid used. The RMS voltage, at which a pixel is switched on or off, determine the transmissibility of the pixel.

For any given liquid, there are two threshold values defined. One point is at 10 % relative transmission (at $V_{th(off)}$) and the other at 90 % relative transmission (at $V_{th(on)}$), see Figure 24.

For a good contrast performance, the following rules should be followed:

$$V_{on(RMS)} \geq V_{th(on)} \quad (7)$$

$$V_{off(RMS)} \leq V_{th(off)} \quad (8)$$

$V_{on(RMS)}$ and $V_{off(RMS)}$ are properties of the display driver and are affected by the selection of a, n (see Equation 4 to Equation 6) and the V_{LCD} voltage.

$V_{th(off)}$ and $V_{th(on)}$ are properties of the LCD liquid and can be provided by the module manufacturer. $V_{th(off)}$ is sometimes named V_{th}. $V_{th(on)}$ is sometimes named saturation voltage V_{sat}.

It is important to match the module properties to those of the driver in order to achieve optimum performance.

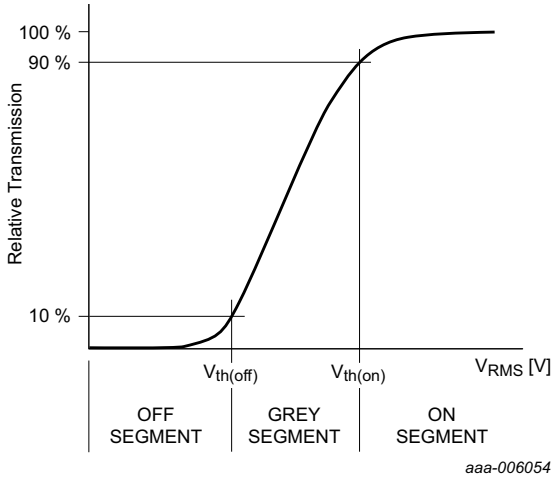
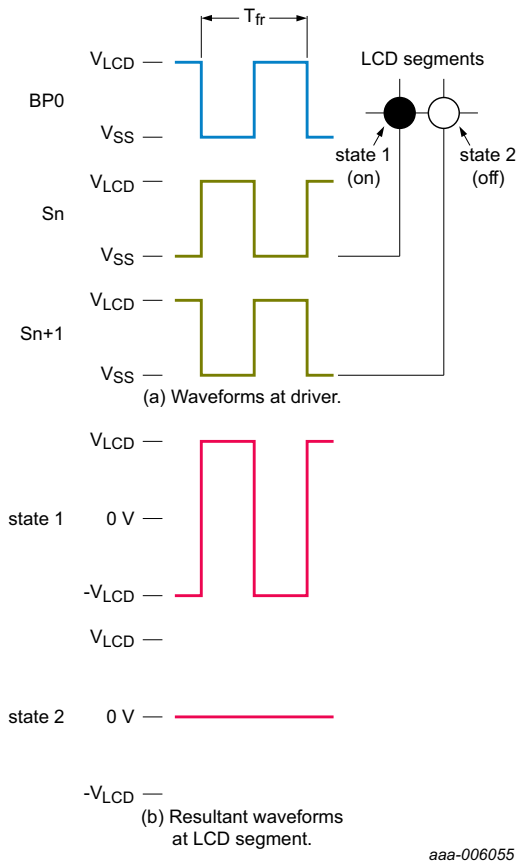


Fig 24. Electro-optical characteristic: relative transmission curve of the liquid

7.10.6 LCD drive mode waveforms

7.10.6.1 Static drive mode

The static LCD drive mode is used when a single backplane is provided in the LCD.



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{state2}(t) = V_{(Sn + 1)}(t) - V_{BP0}(t)$.

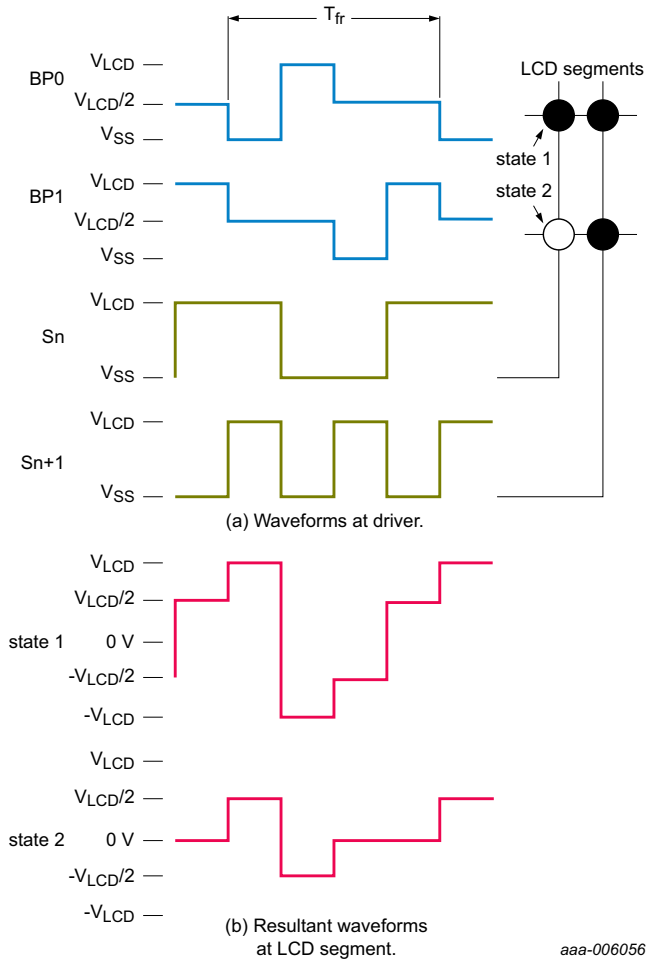
$V_{on(RMS)}(t) = V_{LCD}$.

$V_{off(RMS)}(t) = 0$ V.

Fig 25. Static drive mode waveforms, line inversion mode (n = 1)

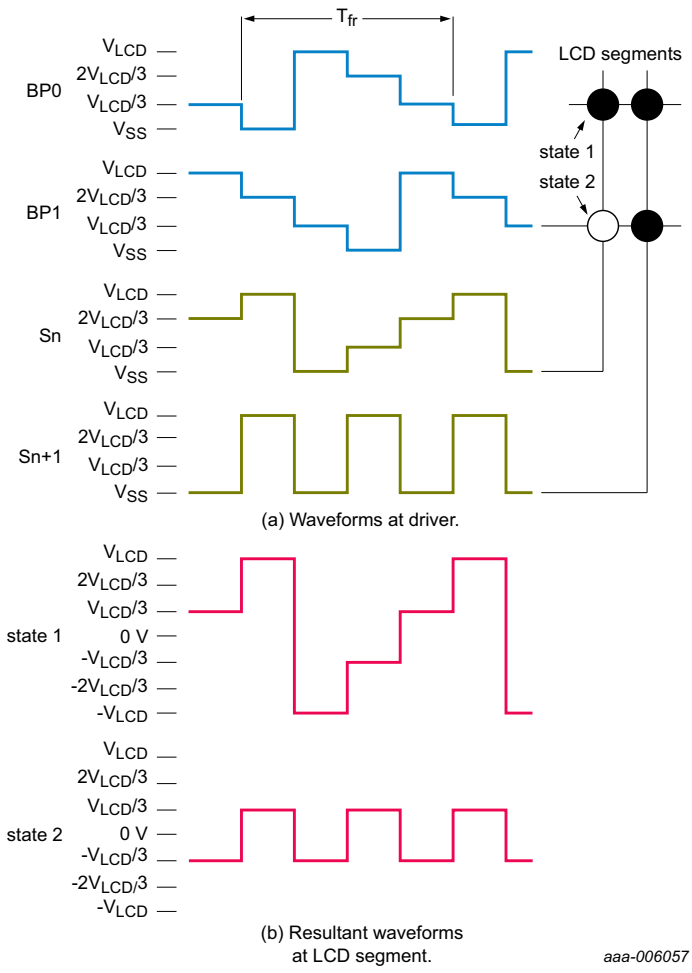
7.10.6.2 1:2 Multiplex drive mode

When two backplanes are provided in the LCD, the 1:2 multiplex mode applies. The PCF8538 allows the use of ½ bias or ⅓ bias in this mode as shown in Figure 26 and Figure 27.



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.
$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.
$V_{on(RMS)}(t) = 0.791V_{LCD}$.
$V_{off(RMS)}(t) = 0.354V_{LCD}$.

Fig 26. Waveforms for the 1:2 multiplex drive mode, ½ bias, line inversion mode (n = 1)



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

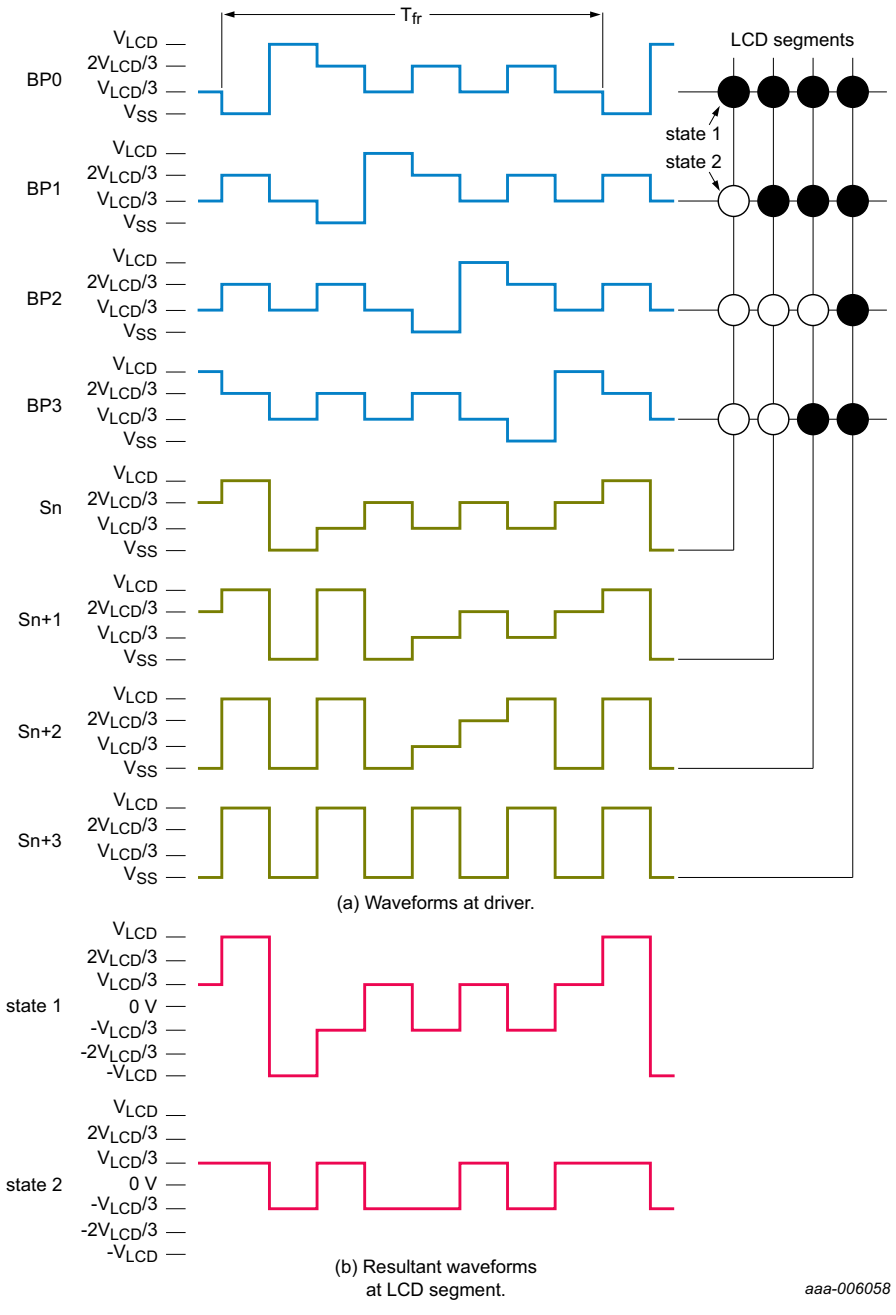
$V_{on(RMS)}(t) = 0.745V_{LCD}$.

$V_{off(RMS)}(t) = 0.333V_{LCD}$.

Fig 27. Waveforms for the 1:2 multiplex drive mode, ⅓ bias, line inversion mode (n = 1)

7.10.6.3 1:4 Multiplex drive mode

When four backplanes are provided in the LCD, the 1:4 multiplex drive mode applies, as shown in Figure 28.



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

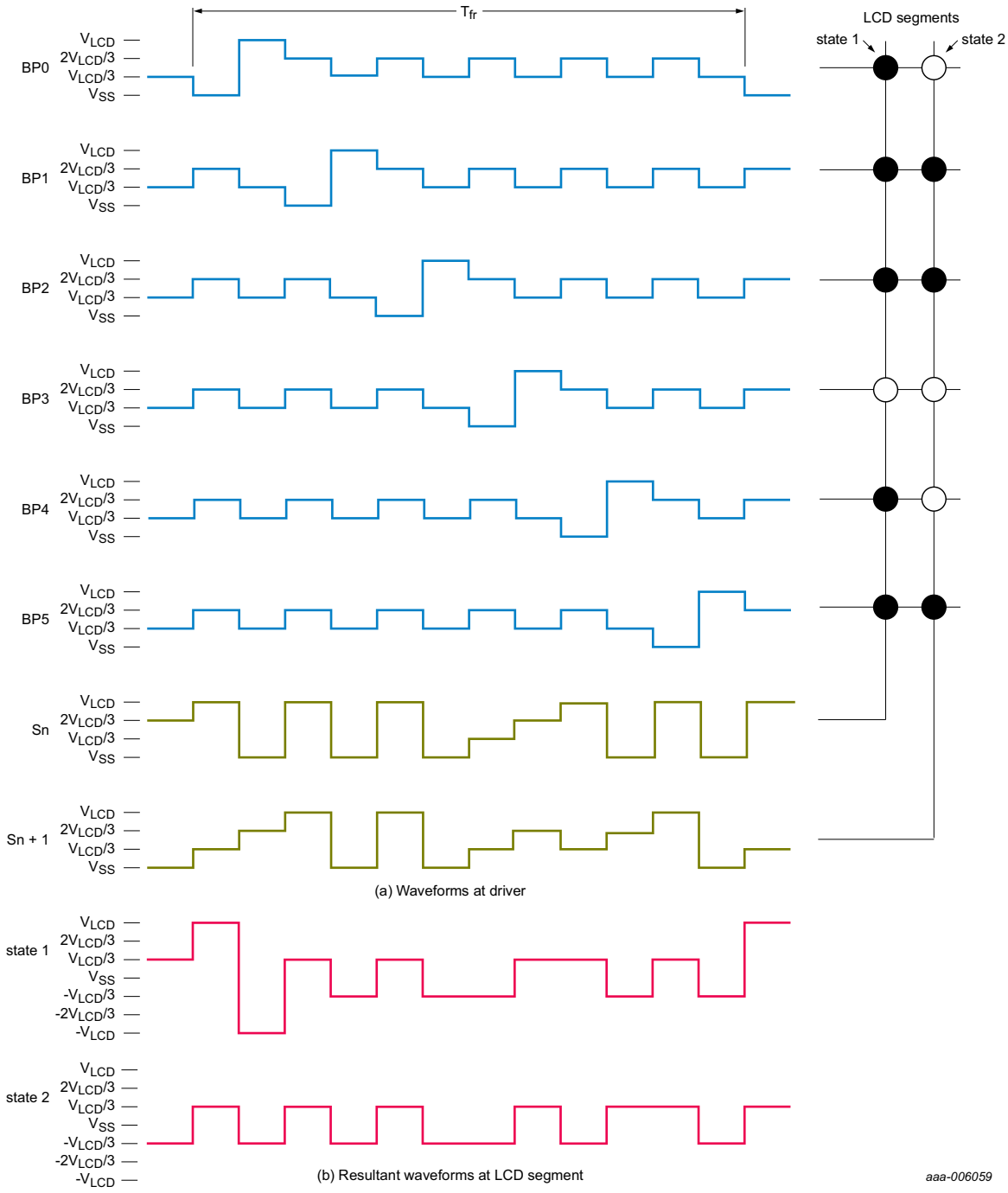
$V_{on(RMS)}(t) = 0.577V_{LCD}$.

$V_{off(RMS)}(t) = 0.333V_{LCD}$.

Fig 28. Waveforms for the 1:4 multiplex drive mode, ⅓ bias, line inversion mode (n = 1)

7.10.6.4 1:6 Multiplex drive mode

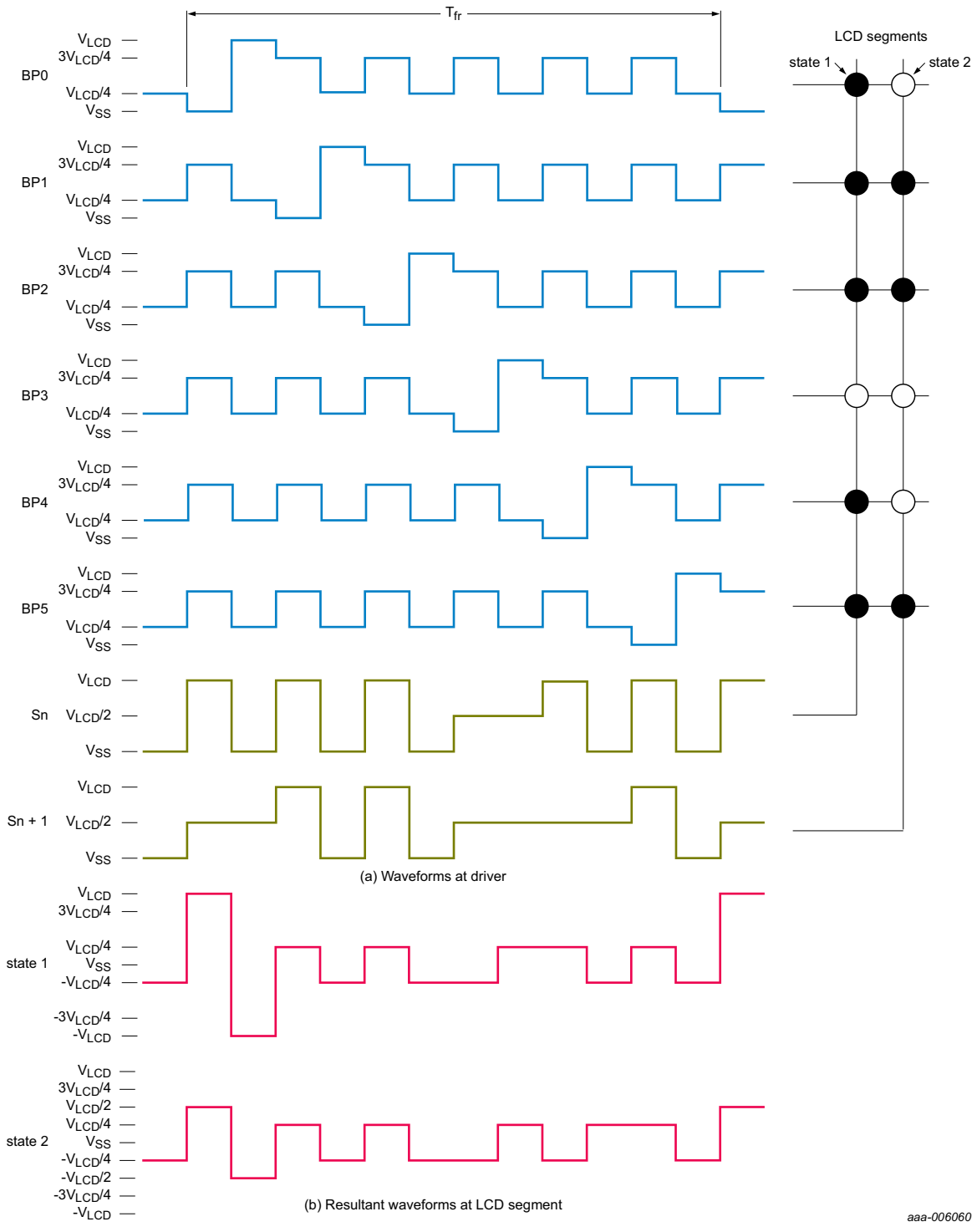
When six backplanes are provided in the LCD, the 1:6 multiplex drive mode applies. The PCF8538 allows the use of ⅓ bias or ¼ bias in this mode as shown in Figure 29 and Figure 30.



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$. $V_{state2}(t) = V_{Sn+1}(t) - V_{BP0}(t)$.

$V_{on(RMS)}(t) = 0.509V_{LCD}$. $V_{off(RMS)}(t) = 0.333V_{LCD}$.

Fig 29. Waveforms for 1:6 multiplex drive mode, ⅓ bias, line inversion mode (n = 1)

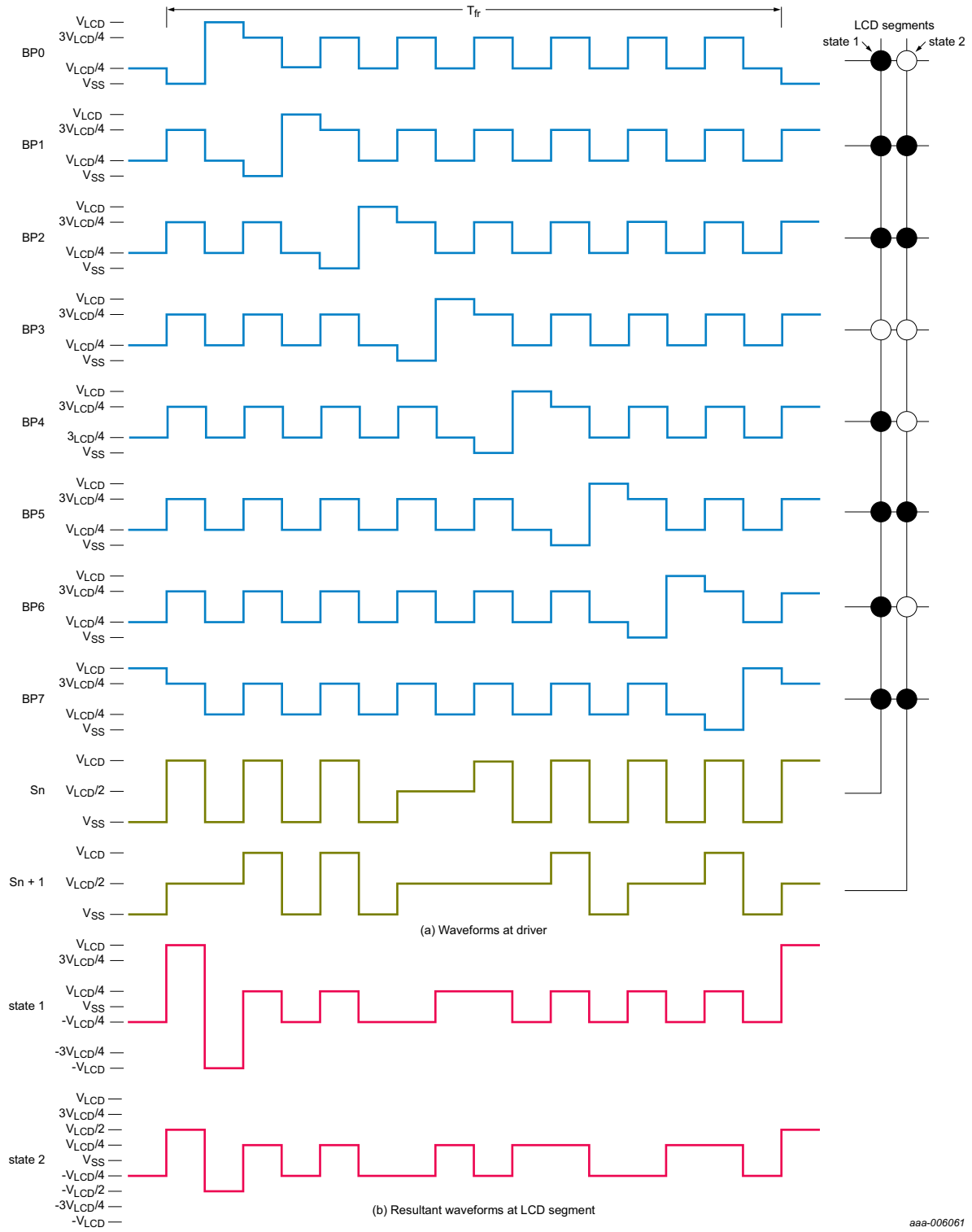


$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$. $V_{state2}(t) = V_{Sn+1}(t) - V_{BP0}(t)$.

$V_{on(RMS)}(t) = 0.467V_{LCD}$. $V_{off(RMS)}(t) = 0.306V_{LCD}$.

Fig 30. Waveforms for 1:6 multiplex drive mode, ¼ bias, line inversion mode (n = 1)

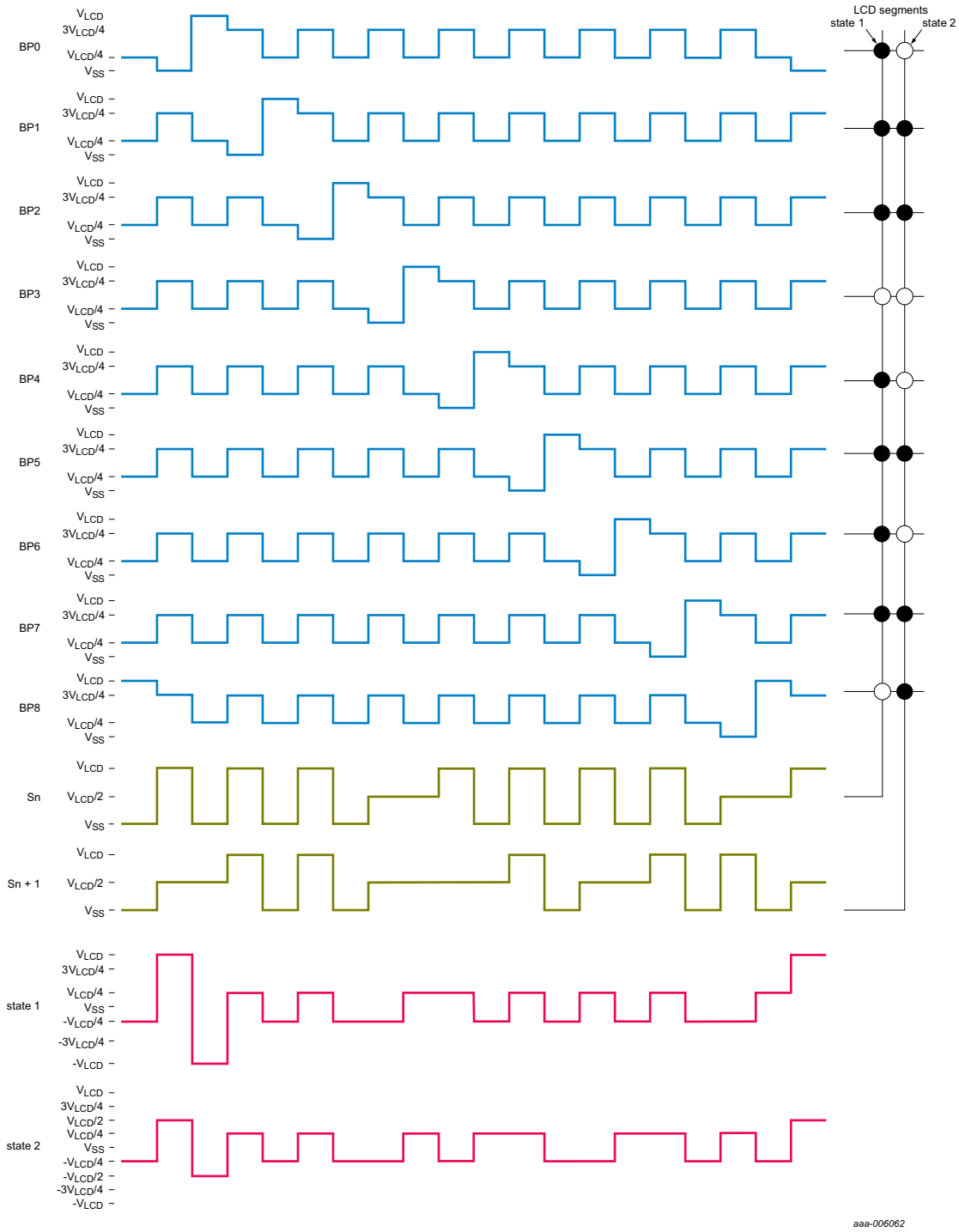
7.10.6.5 1:8 Multiplex drive mode



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$. $V_{state2}(t) = V_{Sn+1}(t) - V_{BP0}(t)$. $V_{on(RMS)}(t) = 0.424V_{LCD}$. $V_{off(RMS)}(t) = 0.293V_{LCD}$.

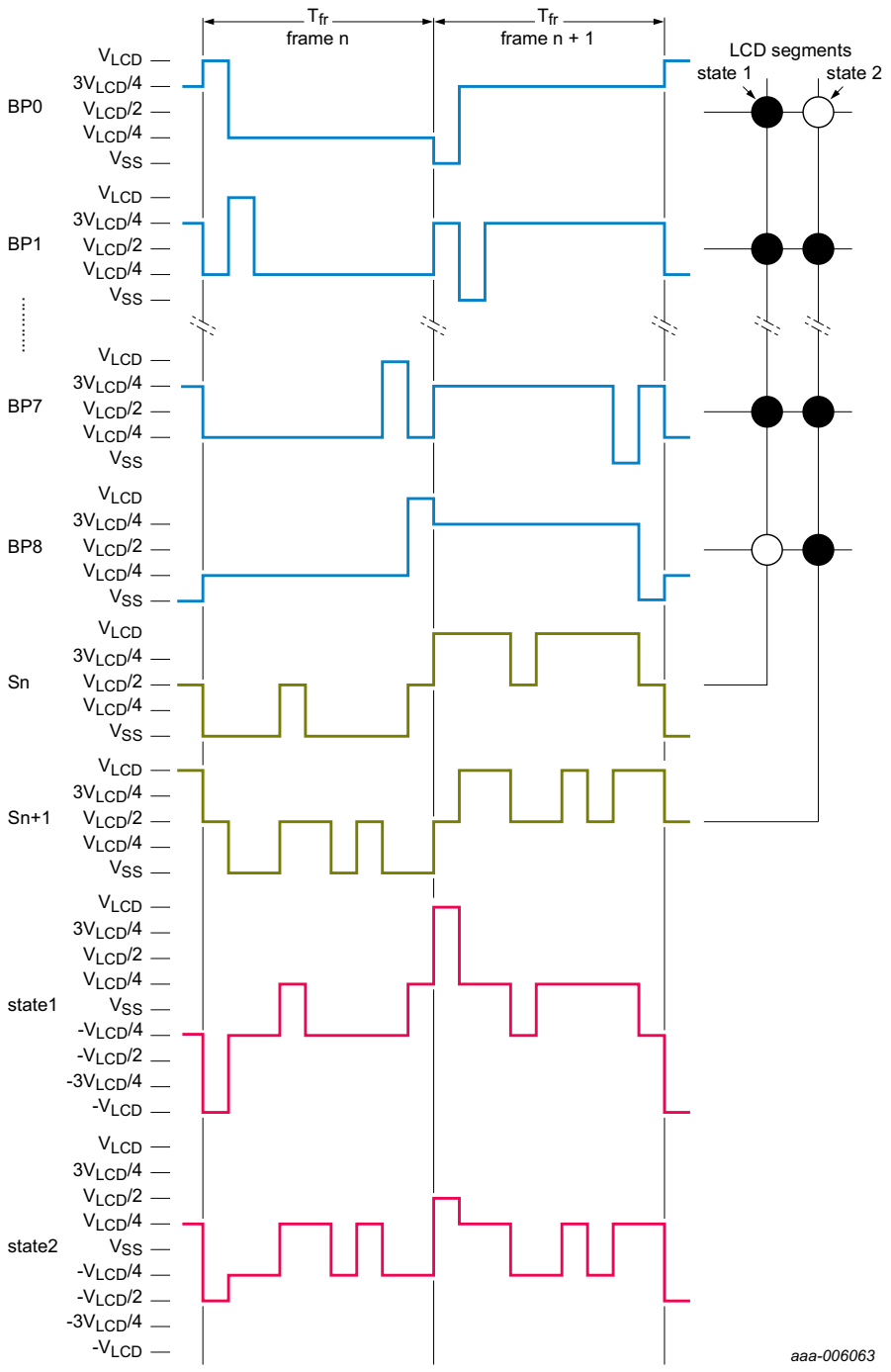
Fig 31. Waveforms for 1:8 multiplex drive mode, ¼ bias, line inversion mode (n = 1)

7.10.6.6 1:9 Multiplex drive mode



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$. $V_{state2}(t) = V_{Sn+1}(t) - V_{BP0}(t)$. $V_{on(RMS)}(t) = 0.408V_{LCD}$. $V_{off(RMS)}(t) = 0.289V_{LCD}$.

Fig 32. Waveforms for 1:9 multiplex drive mode with ¼ bias and line inversion mode (n = 1)



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$. $V_{state2}(t) = V_{Sn+1}(t) - V_{BP0}(t)$. $V_{on(RMS)}(t) = 0.408V_{LCD}$. $V_{off(RMS)}(t) = 0.289V_{LCD}$.

Fig 33. Waveforms for 1:9 multiplex drive mode with ¼ bias and frame inversion mode

7.11 Backplane outputs

The LCD drive section includes nine backplane outputs: COM0 to COM8. The backplanes are double implemented to offer a higher flexibility for the glass layout.

The backplane output signals are generated based on the selected LCD multiplex drive mode. Table 36 describes which outputs are active for each of the multiplex drive modes and what signal is generated.

Table 36. Mapping of output pins and corresponding output signals with respect to the multiplex driving mode

Multiplex drive mode	Output pin								
	COM0	COM1	COM2	COM3	COM4	COM5	COM6	COM7	COM8
	Signal								
static	BP0	BP0	BP0	BP0	BP0	BP0	BP0	BP0	BP0
1:2	BP0	BP1	BP0	BP1	BP0	BP1	BP0	BP1	BP0
1:4	BP0	BP1	BP2	BP3	BP0	BP3	BP2	BP1	BP0
1:6	BP0	BP1	BP2	BP3	BP4	BP5	BP2	BP1	BP0
1:8	BP0	BP1	BP2	BP3	BP4	BP5	BP6	BP7	BP0
1:9	BP0	BP1	BP2	BP3	BP4	BP5	BP6	BP7	BP8

Table 37 describes the corresponding layout topology.

Table 37. Layout topology of output pins and corresponding output signals with respect to the multiplex driving mode

Multiplex drive mode												
Static		1:2		1:4		1:6		1:8		1:9		
Signal	On pin	Signal	On pin	Signal	On pin	Signal	On pin	Signal	On pin	Signal	On pin	
BP0	COM0	BP0	COM0	BP0	COM0	BP0	COM0	BP0	COM0	BP0	COM0	
	COM1		COM2		COM4		COM8		COM8	BP1	COM1	
	COM2		COM4		COM8	BP1	COM1	BP1	COM1	BP2	COM2	
	COM3		COM6	BP1	COM1		COM7	BP2	COM2	BP3	COM3	
	COM4		COM8		COM7	BP2	COM2	BP3	COM3	BP4	COM4	
	COM5	BP1	COM1	BP2	COM2		COM6	BP4	COM4	BP5	COM5	
	COM6		COM3		COM6	BP3	COM3	BP5	COM5	BP6	COM6	
	COM7		COM5	BP3	COM3	BP4	COM4	BP6	COM6	BP7	COM7	
	COM8		COM7		COM5	BP5	COM5	BP7	COM7	BP8	COM8	

7.11.1 Driving strength on the backplanes

Corresponding output pins (COMx), which are carrying the same signal (BPn), may optionally be connected to the display. This allows gaining a higher driving strength. If not required, the unused pins can be left open-circuit.

7.12 Segment outputs

The LCD drive section includes 102 segment outputs (S0 to S101) which must be connected directly to the LCD. The segment output signals are generated based on the multiplexed backplane signals and with data resident in the display register. When less than 102 segment outputs are required, the unused segment outputs must be left open-circuit.

7.13 Display register

The display register holds the display data while the corresponding multiplex signals are generated.

7.14 Display RAM

The display RAM is a static 102 × 9-bit RAM which stores LCD data. Logic 1 in the RAM bit map indicates the on-state, logic 0 the off-state of the corresponding LCD element.

There is a one-to-one correspondence between

- the bits in the RAM bitmap and the LCD elements
- the RAM columns and the segment outputs
- the RAM rows and the backplane outputs.

The display RAM bit map, Figure 34 on page 62, shows row 0 to row 8 which correspond with the backplane outputs COM0 to COM8, and column 0 to column 101 which correspond with the segment outputs S0 to S101. In multiplexed LCD applications, the data of each row of the display RAM is time-multiplexed with the corresponding backplane (row 0 with COM0, row 1 with COM1, and so on).

When display data is transmitted to the PCF8538, the display bytes received are stored in the display RAM in accordance with the selected LCD multiplex drive mode. The data is stored as it arrives and does not wait for the acknowledge cycle as with the commands. Depending on the current multiplex drive mode, data is stored singularly, in pairs, quadruples, sextuples or bytes.

7.14.1 Data pointer

The addressing mechanism for the display RAM is realized using a data pointer. This allows the loading of an individual display data byte, or a series of display data bytes into any location of the display RAM. The sequence commences with the initialization of the data pointer by the Data-pointer-X and Data-pointer-Y commands. Following these commands, an arriving data byte is stored starting at the display RAM address indicated by the data pointer.

The data pointer is automatically incremented in accordance with the chosen LCD multiplex drive mode configuration. After each byte is stored, the contents of the data pointer are incremented

- by eight (static drive mode)
- by four (1:2 multiplex drive mode)
- by two (1:4 multiplex drive mode)
- by one or two (1:6 multiplex drive mode)
- by one (1:8 and 1:9 multiplex drive mode)

When the address counter reaches the end of the RAM, it stops incrementing after the last byte is transmitted. Redundant bits of the last byte and subsequent bytes transmitted are discarded. To send new RAM data, the data pointer must be reset.

If a data access with the I^2C- or SPI-bus is terminated early, then the state of the data pointer is unknown. The data pointer must then be re-written before further RAM accesses.

7.14.1.1 Data pointer in cascade configuration

In cascaded applications each PCF8538 in the cascade must be addressed separately. Initially, the first PCF8538 is selected by sending the Device-address command matching the first hardware address. Then the data pointer is set to the preferred display RAM address with the Data-pointer-X and Data-pointer-Y commands.

Storage is allowed only when the content of the device address register matches with the hardware device address applied to A0 and A1 (see Section 7.2.3). If the content of the device address register and the hardware device address do not match, then data storage is inhibited but the data pointer is incremented as if data storage had taken place.

7.14.2 RAM filling

For the following examples showing the RAM filling patterns, it is assumed that the bits shown in Table 38 are transferred to the RAM.

Table 38. Bit scheme used to illustrate the RAM filling patterns

Bit	7	6	5	4	3	2	1	0
Byte	**MSB**							**LSB**
1	aa7	aa6	aa5	aa4	aa3	aa2	aa1	aa0
2	ab7	ab6	ab5	ab4	ab3	ab2	ab1	ab0
:	:	:	:	:	:	:	:	:
204	hk7	hk6	hk5	hk4	hk3	hk2	hk1	hk0

7.14.2.1 RAM filling in static drive mode

In the static drive mode the eight transmitted data bits are placed in eight successive display RAM columns in row 0 (see Table 39).

Table 39. RAM filling in static drive mode

RAM row/ backplane output (COM)	RAM column/Segment output (S)																			
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	:	99	100	101
0	aa7	aa6	aa5	aa4	aa3	aa2	aa1	aa0	ab7	ab6	ab5	ab4	ab3	ab2	ab1	ab0	:	am4	am3	am2
1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	:	-	-	-
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
8	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	:	-	-	-

In order to fill the whole RAM row, 13 bytes must be sent to the PCF8538. Any data bits that spill over the RAM and additional data bytes sent are discarded.

7.14.2.2 RAM filling in 1:2 multiplex drive mode

In the 1:2 multiplex drive mode the eight transmitted data bits are placed in four successive display RAM columns of two rows (see Table 40).

Table 40. RAM filling in 1:2 multiplex drive mode

RAM row/ backplane output (COM)	RAM column/Segment output (S)											
	0	1	2	3	4	5	6	7	:	99	100	101
0	aa7	aa5	aa3	aa1	ab7	ab5	ab3	ab1	:	ay1	az7	az5
1	aa6	aa4	aa2	aa0	ab6	ab4	ab2	ab0	:	ay0	az6	az4
2	-	-	-	-	-	-	-	-	:	-	-	-
:	:	:	:	:	:	:	:	:	:	:	:	:
8	-	-	-	-	-	-	-	-	:	-	-	-

In order to fill the whole two RAM rows 26 bytes need to be sent to the PCF8538. Any data bits that spill over the RAM and additional data bytes sent are discarded.

7.14.2.3 RAM filling in 1:4 multiplex drive mode

In the 1:4 multiplex drive mode the eight transmitted data bits are placed in two successive display RAM columns of four rows (see Table 41).

Table 41. RAM filling in 1:4 multiplex drive mode

RAM row/ backplane output (COM)	RAM column/Segment output (S)							
	0	**1**	**2**	**3**	**:**	**99**	**100**	**101**
0	aa7	aa3	ab7	ab3	:	bx3	by7	by3
1	aa6	aa2	ab6	ab2	:	bx2	by6	by2
2	aa5	aa1	ab5	ab1	:	bx1	by5	by1
3	aa4	aa0	ab4	ab0		bx0	by4	by0
4	-	-	-	-	:	-	-	-
:	:	:	:	:	:	:	:	:
8	-	-	-	-	:	-	-	-

In order to fill the whole four RAM rows 51 bytes need to be sent to the PCF8538. Depending on the start address of the data pointer, there is the possibility for a boundary condition. This occurs when more data bits are sent than fit into the remaining RAM. The additional data bits are discarded.

7.14.2.4 RAM filling in 1:6 multiplex drive mode

In the 1:6 multiplex drive mode the eight transmitted data bits are placed as shown in Table 42.

Table 42. RAM filling in 1:6 multiplex drive mode

RAM row/ backplane output (COM)	RAM column/Segment output (S)							
	0	**1**	**2**	**3**	**:**	**99**	**100**	**101**
0	aa7	aa1	ab3	ac5	:	cw5	cx7	cx1
1	aa6	aa0	ab2	ac4	:	cw4	cx6	cx0
2	aa5	ab7	ab1	ac3	:	cw3	cx5	cy7
3	aa4	ab6	ab0	ac2	:	cw2	cx4	cy6
4	aa3	ab5	ac7	ac1	:	cw1	cx3	cy5
5	aa2	ab4	ac6	ac0	:	cw0	cx2	cy4
6	-	-	-	-	:	-	-	-
7	-	-	-	-	:	-	-	-
8	-	-	-	-	:	-	-	-

The remaining bits of a byte are wrapped up into the next column. In order to fill the whole RAM addresses 77 bytes need to be sent to the PCF8538. Any data bits that spill over the RAM and additional data bytes sent are discarded.

7.14.2.5 RAM filling in 1:8 multiplex drive mode

In the 1:8 multiplex drive mode the eight transmitted data bits are placed into eight rows of one display RAM column (see Table 43).

Table 43. RAM filling in 1:8 multiplex drive mode

RAM row/ backplane output (COM)	RAM column/Segment output (S)						
	0	1	2	:	99	100	101
0	aa7	ab7	ac7	:	dv7	dw7	dx7
1	aa6	ab6	ac6	:	dv6	dw6	dx6
2	aa5	ab5	ac5	:	dv5	dw5	dx5
3	aa4	ab4	ac4	:	dv4	dw4	dx4
4	aa3	ab3	ac3	:	dv3	dw3	dx3
5	aa2	ab2	ac2	:	dv2	dw2	dx2
6	aa1	ab1	ac1	:	dv1	dw1	dx1
7	aa0	ab0	ac0	:	dv0	dw0	dx0
8	-	-	-	:	-	-	-

In order to fill the whole RAM addresses 102 bytes need to be sent to the PCF8538. Additional data bytes sent are discarded.

7.14.2.6 RAM filling in 1:9 multiplex drive mode

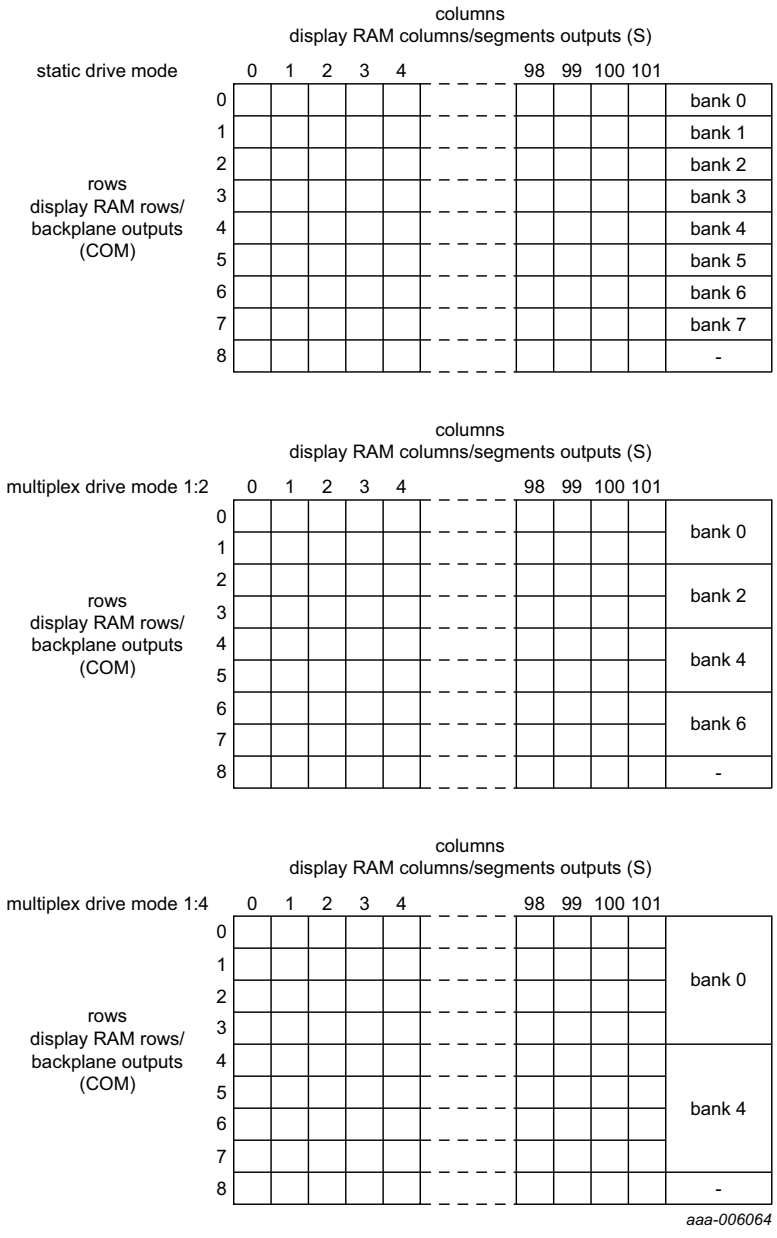
In the 1:9 multiplex drive mode the transmitted bytes are stored continuously in the eight RAM rows until RAM column 101 while the data pointer X is automatically wrapped around from RAM column 0 to RAM column 101 (data pointer Y remains logic 0). Then the data pointer X wraps around to RAM column 0 while data pointer Y is set to logic 1 to fill RAM row 8. From the next bytes sent, only the LSB (bit 0) is stored in RAM row 8. The 7 most significant data bits are discarded. In order to fill the whole RAM addresses 204 bytes need to be sent to the PCF8538 but any data bits that spill over the RAM and additional data bytes sent are discarded.

Table 44. RAM filling in 1:9 multiplex drive mode

RAM row/ backplane output (COM)	RAM column/Segment output (S)						
	0	1	2	:	99	100	101
0	aa7	ab7	ac7	:	dv7	dw7	dx7
1	aa6	ab6	ac6	:	dv6	dw6	dx6
2	aa5	ab5	ac5	:	dv5	dw5	dx5
3	aa4	ab4	ac4	:	dv4	dw4	dx4
4	aa3	ab3	ac3	:	dv3	dw3	dx3
5	aa2	ab2	ac2	:	dv2	dw2	dx2
6	aa1	ab1	ac1	:	dv1	dw1	dx1
7	aa0	ab0	ac0	:	dv0	dw0	dx0
8	dy0	dz0	ea0	:	hi0	hj0	hk0

7.14.3 Bank selection

The PCF8538 includes a RAM bank switching feature in the static, 1:2, and 1:4 multiplex drive modes. A bank can be thought of as a collection of RAM rows. The RAM bank switching gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is complete. Figure 34 shows the location of the banks relative to the RAM map.



The display RAM bitmap shows the direct relationship between the display RAM column and the segment outputs, between the bits in a RAM row and the backplane outputs, and between the RAM rows and banks.

Fig 34. Display RAM bitmap and bank definition

Input and output banks can be set independently from one another with the bank-select commands (see Section 7.7.2 on page 23). Figure 35 shows the concept.

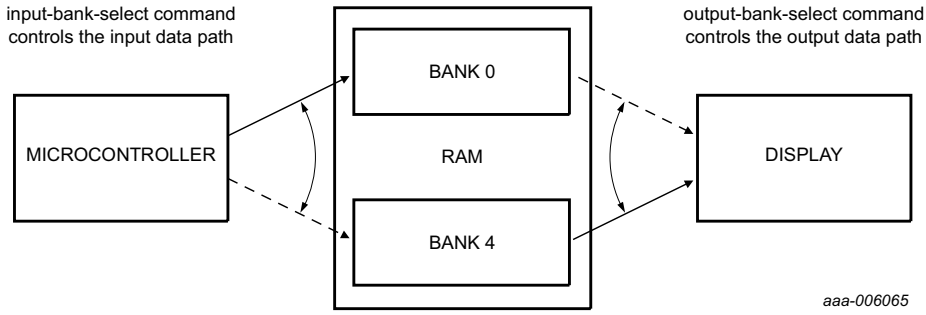


Fig 35. Example of bank selection in 1:4 multiplex mode

In Figure 36 an example is shown for the 1:4 multiplex drive mode where the displayed data is read from the first four rows of the memory (bank 0), while the transmitted data is stored in the second four rows of the memory (bank 4). Theses second four rows are currently not accessed for reading. Therefore different content can be loaded into the first and second four RAM rows. When switching to reading with the Output-bank-select command it will be immediately displayed on the LCD.

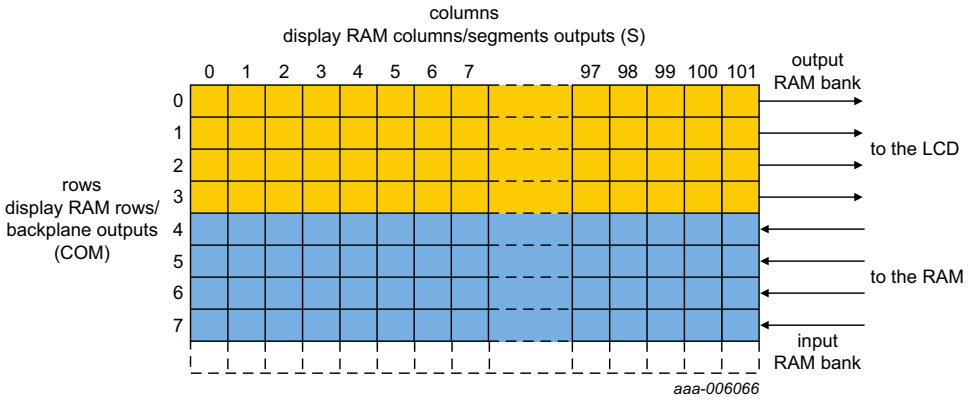


Fig 36. Example of the Input-bank-select and the Output-bank-select command with multiplex drive mode 1:4

7.14.3.1 Input-bank-select

The Input-bank-select command (see Table 25 on page 23) loads display data into the display RAM in accordance with the selected LCD drive configuration (see Figure 34 on page 62).

- In static drive mode, an individual content can be stored in each RAM bank (bank 0 to bank 7 which corresponds to row 0 to row 7).
- In 1:2 multiplex drive mode, individual content for RAM bank 0 (row 0 and row 1), RAM bank 2 (row 2 and row 3), RAM bank 4 (row 4 and 5) and RAM bank 6 (row 6 and row 7) can be stored.
- In 1:4 multiplex drive mode individual content can be stored in RAM bank 0 (row 0 to row 3) and RAM bank 4 (row 4 to row 7).

The Input-bank-select command works independently to the Output-bank-select command.

7.14.3.2 Output-bank-select

The Output-bank-select command (see Table 26 on page 24) selects the display RAM transferring it to the display register in accordance with the selected LCD drive configuration (see Figure 34 on page 62).

- In the static drive mode, it is possible to request the content of RAM bank 1 (row 1) to RAM bank 7 (row 7) for display instead of the default RAM bank 0 (row 0).
- In 1:2 multiplex drive mode, the content of RAM bank 2 (row 2 and row 3) or of RAM bank 4 (row 4 and row 5) or of RAM bank 6 (row 6 and row 7) may be selected instead of the default RAM bank 0 (row 0 and row 1).
- In 1:4 multiplex drive mode, the content of RAM bank 4 (row 4, 5, 6, and 7) may be selected instead of RAM bank 0 (row 0, 1, 2, and 3).

The Output-bank-select command works independently to the Input-bank-select command.

8. Bus interfaces

8.1 Control byte and register selection

After initiating the communication over the bus and sending the slave address (I^2C-bus, see Section 8.2) or subaddress (SPI-bus, see Section 8.3 on page 70), a control byte follows. The purpose of this byte is to indicate both, the content for the following data bytes (RAM or command) and to indicate that more control bytes will follow.

Typical sequences could be:

- Slave address/subaddress - control byte - command byte - command byte - command byte - end
- Slave address/subaddress - control byte - RAM byte - RAM byte - RAM byte - end
- Slave address/subaddress - control byte - command byte - control byte - RAM byte - end

This allows sending a mixture of RAM and command data in one access or alternatively, to send just one type of data in one access. In this way, it is possible to configure the device and then fill the display RAM with little overhead. The display bytes are stored in the display RAM at the address specified by the data pointer.

Table 45. Control byte description

Bit	Symbol	Value	Description
7	CO		**continue bit**
		0	last control byte
		1	control bytes continue
6 to 5	RS[1:0]		**register selection**
		00, 10	command register
		01	RAM data
		11	unused
4 to 0	-	-	unused

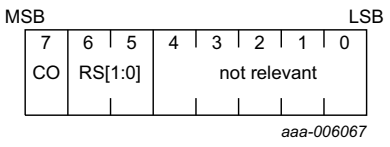


Fig 37. Control byte format

8.2 I²C interface

The I²C-bus is selected by connecting pin IFS to V_{DD1}.

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial DAta line (SDA) and a Serial CLock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

In Chip-On-Glass (COG) applications, where the track resistance between the SDA output pin to the system SDA input line can be significant, the bus pull-up resistor and the Indium Tin Oxide (ITO) track resistance may generate a voltage divider. As a consequence it may be possible that the acknowledge cycle, generated by the LCD driver, cannot be interpreted as logic 0 by the master. Therefore it is an advantage for COG applications to have the acknowledge output separated from the data line. For that reason, the SDA line of the PCF8538 is split into SDI/SDAIN and SDAOUT.

In COG applications where the acknowledge cycle is required, it is necessary to minimize the track resistance from the SDAOUT pin to the system SDI/SDAIN line to guarantee a valid LOW level.

By splitting the SDA line into SDI/SDAIN and SDAOUT (having the SDAOUT open circuit), the device could be used in a mode that ignores the acknowledge cycle. Separating the acknowledge output from the serial data line can avoid design efforts to generate a valid acknowledge level. However, in that case the I²C-bus master has to be set up in such a way that it ignores the acknowledge cycle.[2]

By connecting pin SDAOUT to pin SDI/SDAIN the SDI/SDAIN line becomes fully I²C-bus compatible. The following definition assumes SDI/SDAIN and SDAOUT are connected and refers to the pair as SDA.

8.2.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time are interpreted as a control signal (see Figure 38).

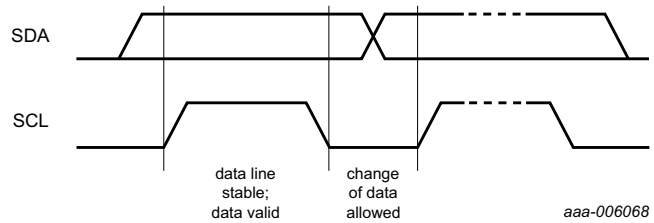


Fig 38. I²C-bus - bit transfer

8.2.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy.

A HIGH-to-LOW change of the data line, while the clock is HIGH is defined as the START condition (S).

2. For further information, consider the NXP application note: Ref. 1 “AN10170”.

A LOW-to-HIGH change of the data line while the clock is HIGH is defined as the STOP condition (P).

The START and STOP conditions are shown in Figure 39.

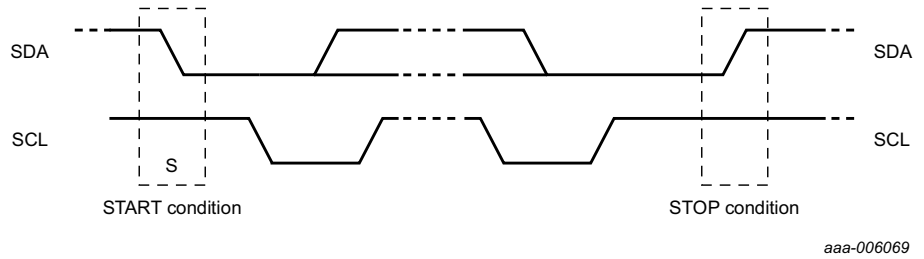


Fig 39. I²C-bus - definition of START and STOP conditions

8.2.3 System configuration

A device generating a message is a transmitter; a device receiving a message is the receiver. The device that controls the message is the master; and the devices which are controlled by the master are the slaves. The system configuration is shown in Figure 40.

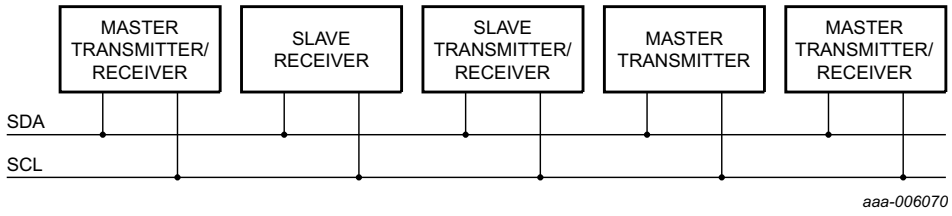


Fig 40. I²C-bus - system configuration

8.2.4 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of 8 bits is followed by an acknowledge cycle.

- A slave receiver which is addressed must generate an acknowledge after the reception of each byte.
- Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.
- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be considered).
- A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

Acknowledgement on the I²C-bus is shown in Figure 41.

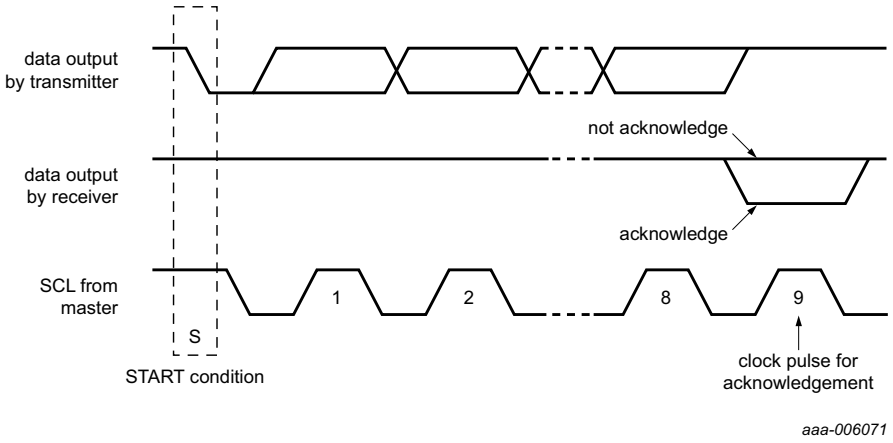


Fig 41. Acknowledgement on the I²C-bus

8.2.5 I²C-bus controller

The PCF8538 acts as an I²C-bus slave receiver. It does not initiate I²C-bus transfers. The only data output from PCF8538 is the acknowledge signals and the temperature readout byte of the selected device.

8.2.6 Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

8.2.7 I²C-bus slave address

Device selection depends on the I²C-bus slave address.

Table 46. I²C slave address byte

Bit	Slave address							
	7 MSB	6	5	4	3	2	1	0 LSB
slave address	0	1	1	1	0	SA1	SA0	R/$\overline{W}$

The least significant bit of the slave address byte is bit R/$\overline{W}$ (see Table 47).

Table 47. R/$\overline{W}$-bit description

R/$\overline{W}$	Description
0	write data
1	read data

Bit 1 and bit 2 of the slave address are defined by connecting the inputs SA0 and SA1 to either V_{SS1} (logic 0) or V_{DD1} (logic 1). Therefore, four instances of PCF8538 can be distinguished on the same I²C-bus.

8.2.8 I²C-bus protocol

The I²C-bus protocol is shown in Figure 42. The sequence is initiated with a START condition (S) from the I²C-bus master which is followed by one of the four PCF8538 slave addresses available. All PCF8538 with the corresponding SA1 and SA0 level acknowledge in parallel to the slave address, but all PCF8538 with the alternative SA1 and SA0 levels ignore the whole I²C-bus transfer.

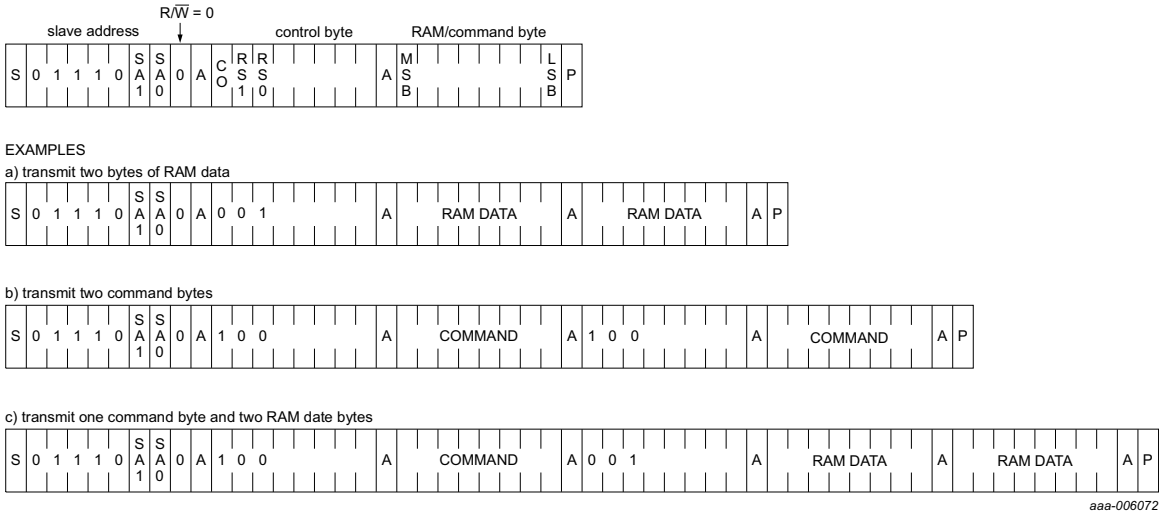


Fig 42. I²C-bus protocol - write mode

After acknowledgement, a control byte follows which defines if the next byte is RAM or command information. The control byte (see Table 45 on page 65) also defines whether the next byte is a control byte or further RAM or command data.

For a temperature readout (see Section 7.10.4.1 on page 40), the R/$\overline{W}$ bit must be logic 1. The next data byte following is provided by the PCF8538 as shown in Figure 43.

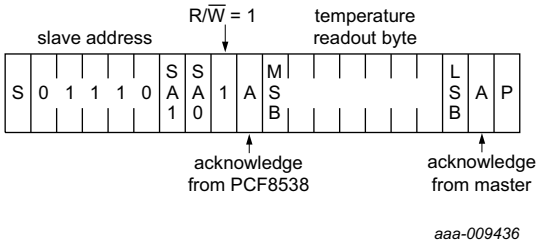


Fig 43. I²C-bus protocol - read mode

8.3 SPI interface

The SPI interface is selected by connecting pin IFS to V_{SS1}.

Data transfer to the device is made via a four-line SPI-bus (see Table 48). The SPI-bus is initialized whenever the chip enable line pin $\overline{CE}$ is LOW.

Table 48. Serial interface

Symbol	Function	Description
$\overline{CE}$	chip enable input; active LOW[1]	when HIGH, the interface is reset
SCL	serial clock input	input may be higher than V_{DD1}
SDI/SDAIN	serial data input	input may be higher than V_{DD1}; input data is sampled on the rising edge of SCL
SDO	serial data output	-

[1] The chip enable must not be wired permanently LOW.

8.3.1 Data transmission

The chip enable signal ($\overline{CE}$) is used to initialize data transmission. Each data transfer is a byte, with the MSB sent first. The first byte transmitted is the subaddress byte.

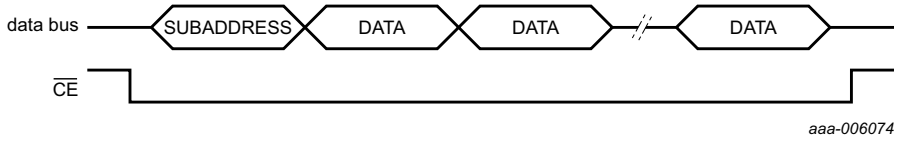


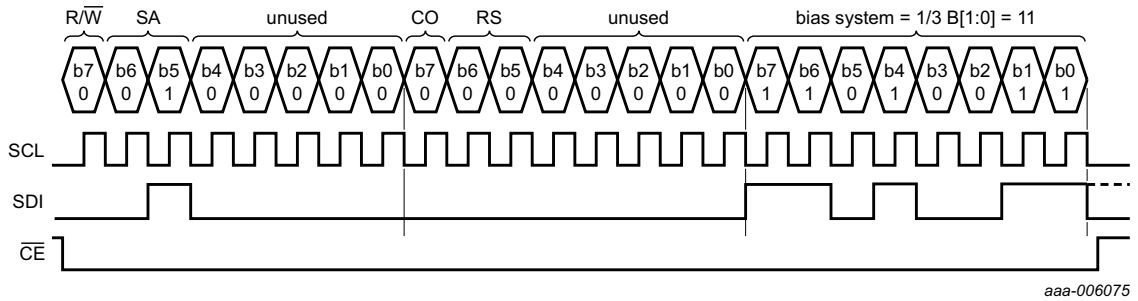
Fig 44. SPI-bus protocol - data transfer overview

The subaddress byte opens the communication with a read/write bit and a subaddress. The subaddress is used to identify multiple devices on one SPI bus.

Table 49. Subaddress byte definition

Bit	Symbol	Value	Description
7	R/$\overline{W}$		**data read or write selection**
		0	write data
		1	read data
6 to 5	SA	01	**subaddress**; other codes cause the device to ignore data transfer
4 to 0	-		unused

Figure 45 shows an example of an SPI data transfer.



In this example, the bias system is set to $\frac{1}{3}$. The transfer is terminated by $\overline{CE}$ returning to logic 1. After the last bit is transmitted, the state of the SDI/SDAIN line is not important.

Fig 45. SPI-bus example

For a temperature readout (see Section 7.10.4.1 on page 40), the R/$\overline{W}$ bit must be logic 1. The next data byte following is provided by the PCF8538 as shown in Figure 46.

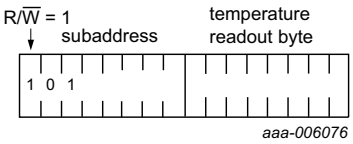
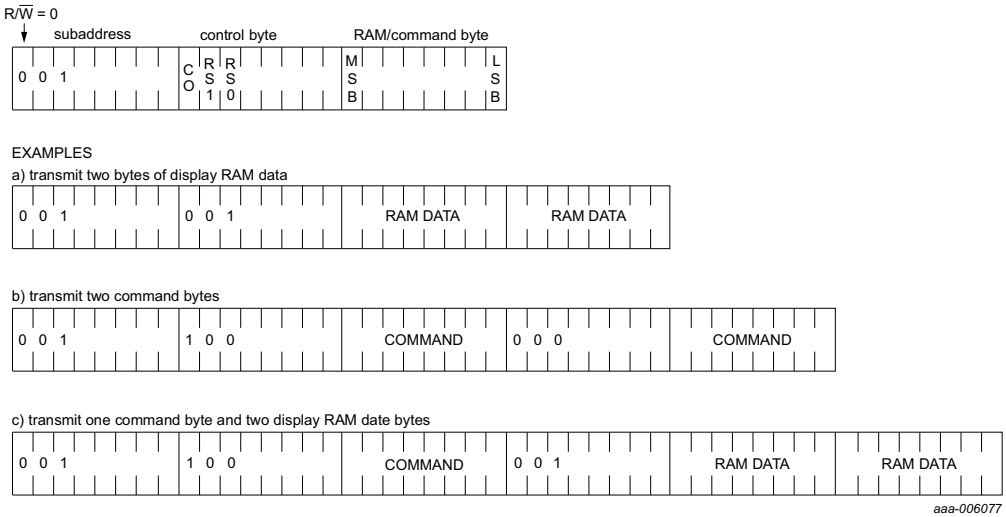


Fig 46. SPI-bus protocol - read example



Data transfers are terminated by de-asserting $\overline{CE}$ ($\overline{CE}$ to logic 1).

Fig 47. SPI-bus protocol - write example

9. Internal circuitry

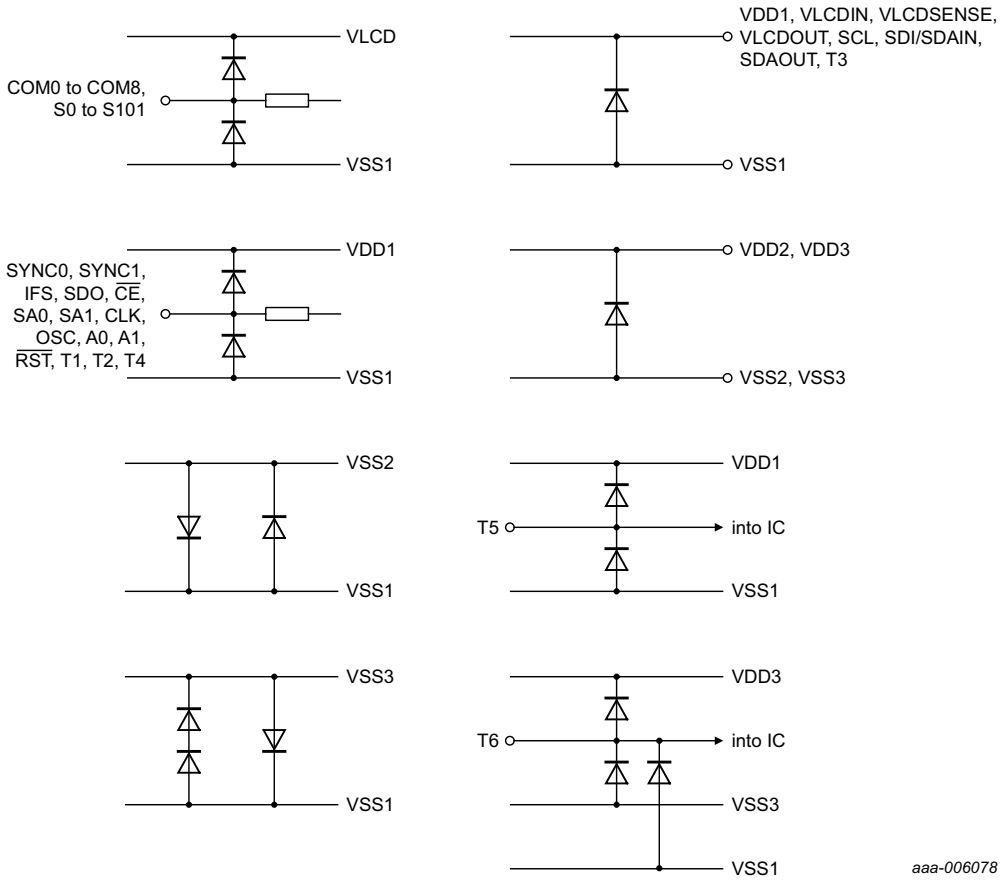


Fig 48. Device protection diagram

10. Safety notes

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

CAUTION

Static voltages across the liquid crystal display can build up when the LCD supply voltage (V_{LCD}) is on while the IC supply voltage (V_{DD}) is off, or vice versa. This may cause unwanted display artifacts. To avoid such artifacts, V_{LCD} and V_{DD} must be applied or removed together.

CAUTION

Semiconductors are light sensitive. Exposure to light sources can cause the IC to malfunction. The IC must be protected against light. The protection must be applied to all sides of the IC.

11. Limiting values

Table 50. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD1}	supply voltage 1	analog and digital		–0.5	+6.5	V
V_{DD2}	supply voltage 2	charge pump		–0.5	+6.5	V
V_{DD3}	supply voltage 3	analog		–0.5	+6.5	V
I_{DD1}	supply current 1	analog and digital		–50	+50	mA
I_{DD2}	supply current 2	charge pump		–50	+50	mA
I_{DD3}	supply current 3	analog		–50	+50	mA
V_{LCD}	LCD supply voltage	external supply, input on pin VLCDIN		–0.5	+20	V
$I_{DD(LCD)}$	LCD supply current			–50	+50	mA
V_i	input voltage	on pins CLK, OSC, A0, A1, $\overline{RST}$, IFS, SCL, SDI/SDAIN, SA0, $\overline{CE}$, SA1, SYNC0, SYNC1		–0.5	+6.5	V
		on pin VLCDSENSE		–0.5	+20	V
I_I	input current			–10	+10	mA
V_O	output voltage	on pins S0 to S101, COM0 to COM8, VLCDOUT		–0.5	+20	V
		on pins SDO, SA0, SDAOUT, CLK, SYNC0, SYNC1		–0.5	+6.5	V
I_O	output current			–10	+10	mA
I_{SS}	ground supply current			–50	+50	mA
P_{tot}	total power dissipation			-	400	mW
P/out	power dissipation per output			-	100	mW
V_{ESD}	electrostatic discharge voltage	HBM	[1]	-	±2000	V
I_{lu}	latch-up current		[2]	-	150	mA
T_{stg}	storage temperature		[3]	–65	+150	°C
T_{amb}	ambient temperature	operating device		–40	+85	°C

[1] Pass level; Human Body Model (HBM), according to Ref. 8 “JESD22-A114”.

[2] Pass level; latch-up testing according to Ref. 9 “JESD78” at maximum ambient temperature ($T_{amb(max)}$).

[3] According to the store and transport requirements (see Ref. 14 “UM10569”) the devices have to be stored at a temperature of +8 °C to +45 °C and a humidity of 25 % to 75 %.

12. Static characteristics

Table 51. Static characteristics

V_{DD1}, V_{DD2}, V_{DD3} = 2.5 V to 5.5 V; V_{SS1} = 0 V; V_{LCD} = 4.0 V to 12.0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
V_{DD1}	supply voltage 1		2.5	-	5.5	V
V_{DD2}	supply voltage 2		2.5	-	5.5	V
V_{DD3}	supply voltage 3		2.5	-	5.5	V
V_{LCD}	LCD supply voltage	$V_{LCD} \geq V_{DD2}$				
		external supply, input on pin VLCDIN	4.0	-	12.0	V
		internal supply, output on pin VLCDOUT	4.0	-	12.0	V
I_{DD1}	supply current 1	on pin VDD1				
		default condition after POR and Initialize command, see Figure 49	-	40[1]	55[2]	µA
		display enabled; internal clock	-	45[1]	-	µA
I_{DD2}	supply current 2	on pin VDD2				
		default condition after POR and Initialize command	-	0	-	µA
		V_{DD2} = 5 V; charge pump at $V_{LCD} = 2 \times V_{DD2}$; V_{LCD} = 8 V; C_{VLCD} = 100 nF; display disabled; see Figure 50	-	25	-	µA
I_{DD3}	supply current 3	on pin VDD3				
		default condition after POR and Initialize command, see Figure 51	-	40[3]	55[4]	µA
		display enabled; internal clock	-	90[3]	-	µA
$I_{DD(LCD)}$	LCD supply current	on pin VLCDIN; external V_{LCD} = 8 V				
		display disabled, see Figure 52	-	6.5	10	µA
		MUX 1:9; 1/4 bias; f_{fr} = 80 Hz; RAM entirely filled with 1; frame inversion mode; display enabled; no display attached	-	85	-	µA
Accuracy						
ΔV_{LCD}	LCD voltage variation	on pin VLCDOUT; internal V_{LCD}; V[8:0] = 86h; T_{amb} = 25 °C; see Figure 53	7950	8010	8070	mV

Table 51. Static characteristics *...continued*

V_{DD1}, V_{DD2}, V_{DD3} = 2.5 V to 5.5 V; V_{SS1} = 0 V; V_{LCD} = 4.0 V to 12.0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Δf_{fr}	frame frequency variation	internal clock; FF[4:0] = 00111; T_{amb} = 25 °C; see Figure 54	77	80	83	Hz
ΔT_{meas}	measurement temperature variation	T_{amb} = 25 °C; see Figure 55	-	±0	-	°C
Output resistance						
$R_{o(COM[0:8])}$	output resistance on pin COM0 to COM8	external V_{LCD} = 8 V	-	1	-	kΩ
$R_{o(S[0:101])}$	output resistance on pin S0 to S101	external V_{LCD} = 8 V	-	2.5	-	kΩ
Logic						
On pins CLK, OSC, A0, A1, SYNC0, SYNC1, $\overline{RST}$, IFS						
V_I	input voltage		V_{SS1} − 0.5	-	V_{DD1} + 0.5	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{DD1}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD1}$	-	-	V
I_{LI}	input leakage current	$V_I = V_{DD1}$ or V_{SS1}	-	0	-	µA
On pins CLK, SYNC0, SYNC1						
V_O	output voltage		−0.5	-	V_{DD1} + 0.5	V
V_{OH}	HIGH-level output voltage		$0.8V_{DD1}$	-	-	V
V_{OL}	LOW-level output voltage		-	-	$0.2V_{DD1}$	V
I_{OH}	HIGH-level output current	output source current; V_{OH} = 4.6 V; V_{DD1} = 5 V	1	-	-	mA
I_{OL}	LOW-level output current	output sink current; V_{OL} = 0.4 V; V_{DD1} = 5 V	1	-	-	mA
I_{LO}	output leakage current	$V_O = V_{DD1}$ or V_{SS1}	-	0	-	µA
I^2C-bus						
On pins SCL, SDI/SDAIN						
V_I	input voltage		V_{SS1} − 0.5	-	5.5	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{DD1}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD1}$	-	-	V
I_{LI}	input leakage current	$V_I = V_{DD1}$ or V_{SS1}	-	0	-	µA

Table 51. Static characteristics *...continued*

V_{DD1}, V_{DD2}, V_{DD3} = 2.5 V to 5.5 V; V_{SS1} = 0 V; V_{LCD} = 4.0 V to 12.0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

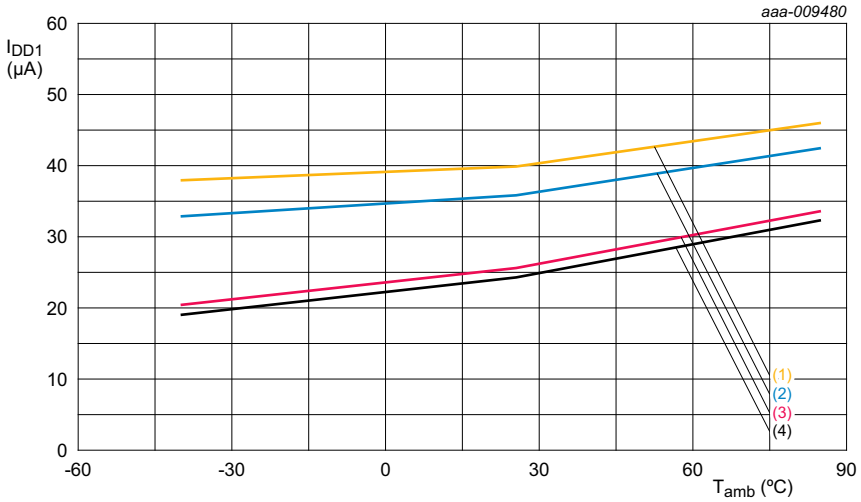
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
On pin SDAOUT						
V_O	output voltage		−0.5	-	+5.5	V
I_{OL}	LOW-level output current	output sink current; V_{OL} = 0.4 V	6	-	-	mA
I_{LI}	input leakage current	$V_I = V_{DD1}$ or V_{SS1}	-	0	-	μA
I_{LO}	output leakage current	$V_O = V_{SS1}$	-	0	-	μA
SPI-bus						
On pins SCL, SDI/SDAIN, $\overline{CE}$						
V_I	input voltage	on pins SCL, SDI/SDAIN	V_{SS1} − 0.5	-	5.5	V
		on pin $\overline{CE}$	V_{SS1} − 0.5	-	V_{DD1} + 0.5	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{DD1}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD1}$	-	-	V
I_{LI}	input leakage current	$V_I = V_{DD1}$ or V_{SS1}	-	0	-	μA
On pin SDO						
V_O	output voltage		−0.5	-	V_{DD1} + 0.5	V
V_{OH}	HIGH-level output voltage		$0.8V_{DD1}$	-	-	V
V_{OL}	LOW-level output voltage		-	-	$0.2V_{DD1}$	V
I_{OH}	HIGH-level output current	output source current; V_{OH} = 4.6 V; V_{DD1} = 5 V	1	-	-	mA
I_{OL}	LOW-level output current	output sink current; V_{OL} = 0.4 V; V_{DD1} = 5 V	1	-	-	mA
I_{LO}	output leakage current	$V_O = V_{DD1}$ or V_{SS1}	-	0	-	μA

[1] V_{DD1} = 5 V; T_{amb} = 25 °C.

[2] V_{DD1} = 5.5 V; T_{amb} = 85 °C.

[3] V_{DD3} = 5 V; T_{amb} = 25 °C.

[4] V_{DD3} = 5.5 V; T_{amb} = 85 °C.



Default conditions after POR and initialization.

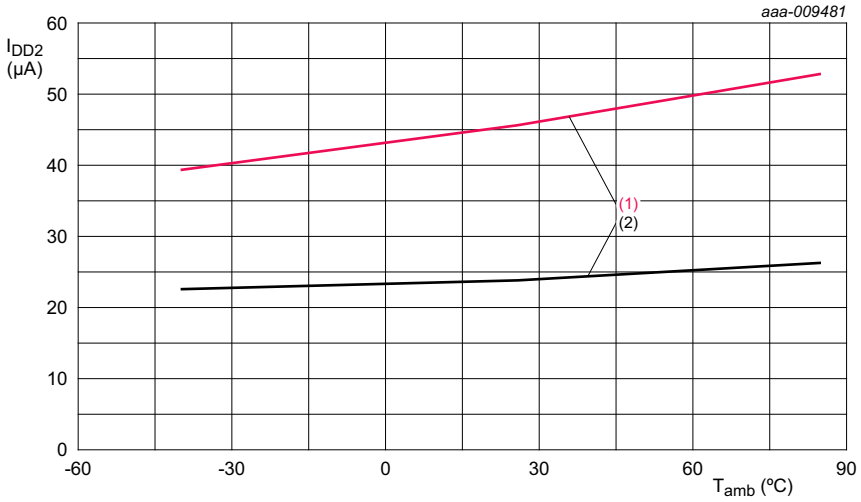
(1) V_{DD1} = 5.5 V.

(2) V_{DD1} = 5 V.

(3) V_{DD1} = 3 V.

(4) V_{DD1} = 2.5 V.

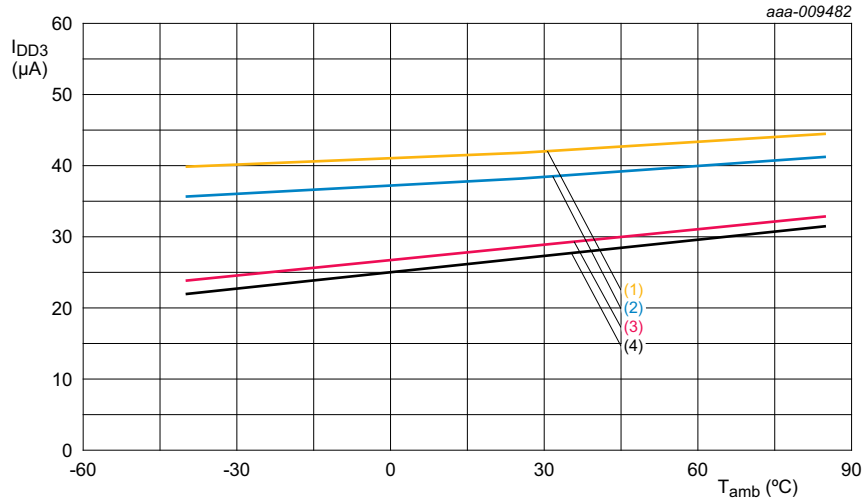
Fig 49. Typical I_{DD1} with respect to temperature



(1) V_{DD2} = 3 V; charge pump at V_{LCD} = 3 × V_{DD2}; V_{LCD} = 8 V; C_{VLCD} = 100 nF; display disabled.

(2) V_{DD2} = 5 V; charge pump at V_{LCD} = 2 × V_{DD2}; V_{LCD} = 8 V; C_{VLCD} = 100 nF; display disabled.

Fig 50. Typical I_{DD2} with respect to temperature



Default conditions after POR.

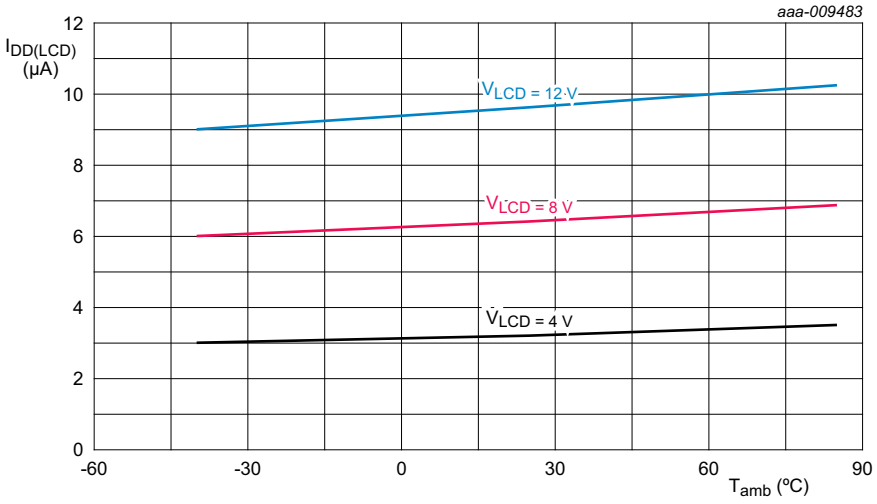
(1) V_{DD1} = 5.5 V.

(2) V_{DD1} = 5 V.

(3) V_{DD1} = 3 V.

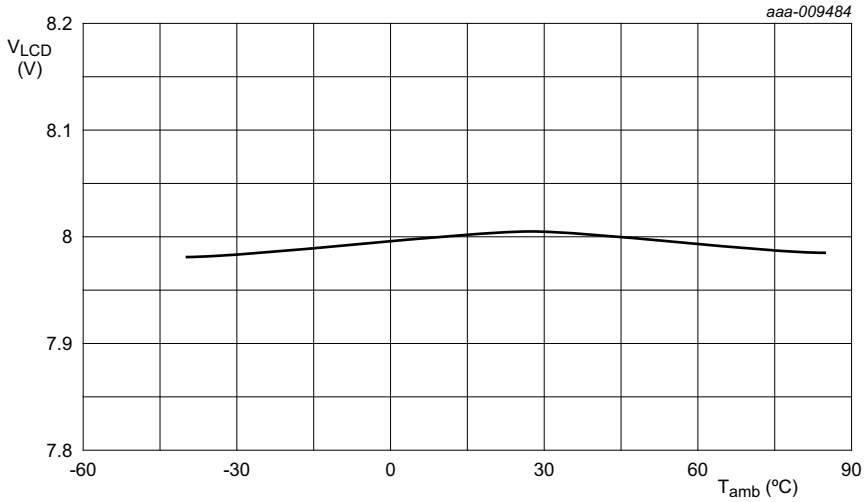
(4) V_{DD1} = 2.5 V.

Fig 51. Typical I_{DD3} with respect to temperature



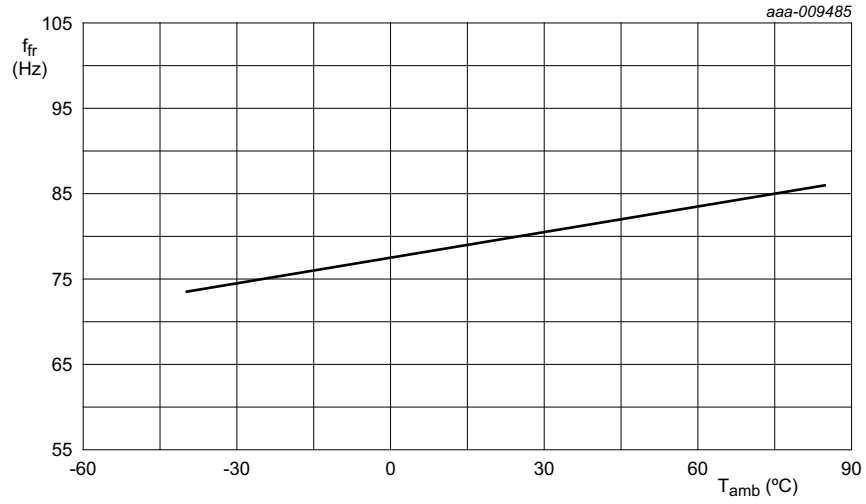
Conditions: External V_{LCD}; display disabled.

Fig 52. Typical $I_{DD(LCD)}$ with respect to temperature



Conditions: V_{DD2} = 5 V; charge pump at $V_{LCD} = 2 \times V_{DD2}$; V_{LCD} = 8 V; V[8:0] = 134h; temperature compensation disabled.

Fig 53. Typical V_{LCD} variation with respect to temperature



Conditions: frame frequency prescaler = 00111; 80 Hz typical.

Fig 54. Typical frame frequency variation with respect to temperature

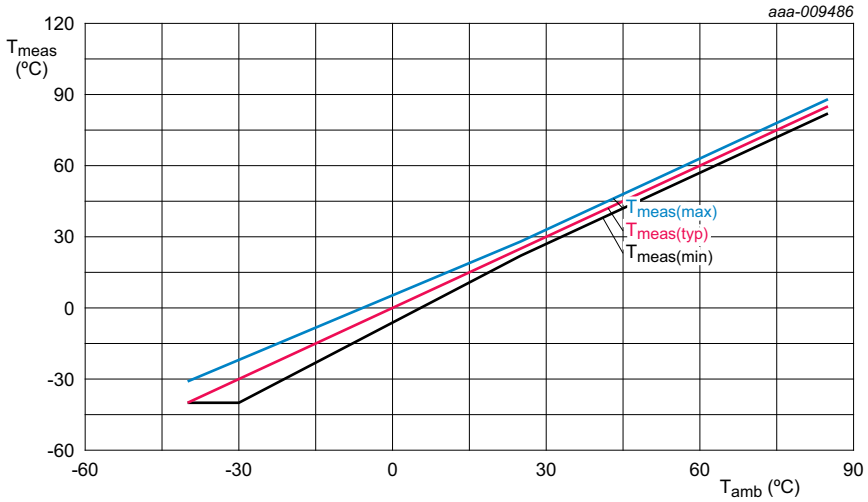


Fig 55. Measurement temperature variation with respect to temperature

13. Dynamic characteristics

13.1 General dynamic characteristics

Table 52. General dynamic characteristics

V_{DD1}, V_{DD2}, V_{DD3} = 2.5 V to 5.5 V; V_{SS1} = 0 V; V_{LCD} = 4.0 V to 12.0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified. All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS1} to V_{DD1}.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{clk(int)}$	internal clock frequency	on pin CLK; FF[4:0] = 00111; T_{amb} = 25 °C	11088	11520	11952	Hz
$f_{clk(ext)}$	external clock frequency	on pin CLK	6400	-	42700	Hz
$t_{clk(H)}$	HIGH-level clock time	external clock source used	5	-	-	µs
$t_{clk(L)}$	LOW-level clock time		5	-	-	µs
$t_{wL(RST\_N)}$	RST_N LOW pulse width		3	-	-	µs
C_b	capacitive load for each bus line	I^2C-bus	-	-	400	pF

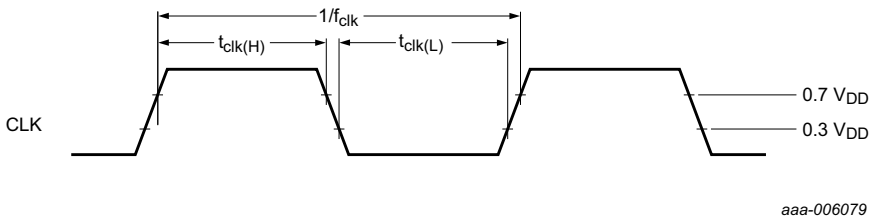


Fig 56. Driver timing waveforms

13.2 I²C-bus timing characteristics

Table 53. I²C-bus timing characteristic

V_{DD1}, V_{DD2}, V_{DD3} = 2.5 V to 5.5 V; V_{SS1} = 0 V; V_{LCD} = 4.0 V to 12.0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified. All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS1} to V_{DD1}.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{SCL}	SCL frequency			-	-	400	kHz
t_{BUF}	bus free time between a STOP and START condition			1.3	-	-	µs
$t_{HD;STA}$	hold time (repeated) START condition			0.6	-	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition			0.6	-	-	µs
$t_{VD;DAT}$	data valid time		[1]	-	-	0.9	µs
$t_{VD;ACK}$	data valid acknowledge time		[2]	-	-	0.9	µs
t_{LOW}	LOW period of the SCL clock			1.3	-	-	µs
t_{HIGH}	HIGH period of the SCL clock			0.6	-	-	µs
t_f	fall time	of both SDA and SCL signals		-	-	0.3	µs
t_r	rise time	of both SDA and SCL signals		-	-	0.3	µs
$t_{SU;DAT}$	data set-up time			100	-	-	ns
$t_{HD;DAT}$	data hold time			0	-	-	ns
$t_{SU;STO}$	set-up time for STOP condition			0.6	-	-	µs
$t_{w(spike)}$	spike pulse width			-	-	50	ns

[1] $t_{VD;DAT}$ = minimum time for valid SDA output following SCL LOW.

[2] $t_{VD;ACK}$ = time for acknowledgement signal from SCL LOW to SDA output LOW.

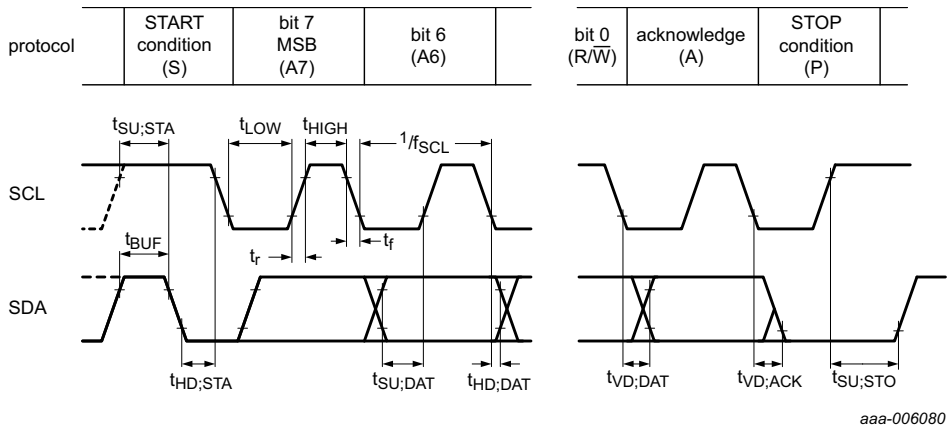


Fig 57. I²C-bus timing

13.3 SPI-bus timing characteristics

Table 54. SPI-bus timing characteristics

V_{DD1}, V_{DD2}, V_{DD3} = 2.5 V to 5.5 V; V_{SS1} = 0 V; V_{LCD} = 4.0 V to 12.0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified. All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS1} to V_{DD1}.

Symbol	Parameter	Conditions	Min	Max	Unit
Pin SCL					
$f_{clk(SCL)}$	SCL clock frequency		-	3.0	MHz
t_{SCL}	SCL time		333	-	ns
$t_{clk(H)}$	clock HIGH time		100	-	ns
$t_{clk(L)}$	clock LOW time		150	-	ns
t_r	rise time	for SCL signal	-	100	ns
t_f	fall time	for SCL signal	-	100	ns
Pin $\overline{CE}$					
$t_{su(CE\_N)}$	CE_N set-up time		30	-	ns
$t_{h(CE\_N)}$	CE_N hold time		30	-	ns
$t_{rec(CE\_N)}$	CE_N recovery time		30	-	ns
Pin SDI/SDAIN					
t_{su}	set-up time	set-up time for SDI data	30	-	ns
t_h	hold time	hold time for SDI data	30	-	ns
Pin SDO					
$t_{d(R)SDO}$	SDO read delay time	C_L = 100 pF	-	150	ns
$t_{dis(SDO)}$	SDO disable time	[1]	-	50	ns
$t_{t(SDI-SDO)}$	transition time from SDI to SDO	to avoid bus conflict	0	-	ns

[1] No load value; bus will be held up by bus capacitance; use RC time constant with application values.

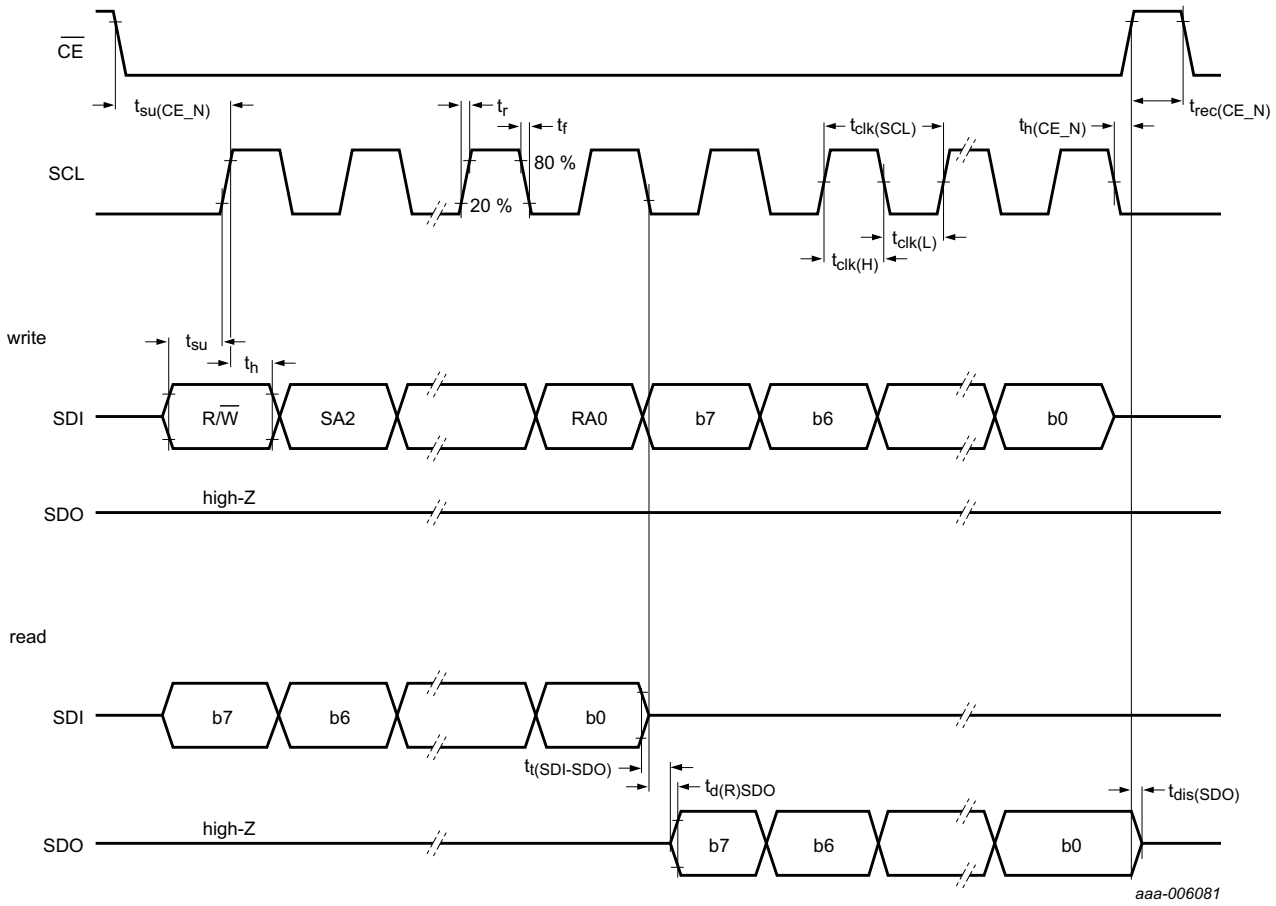


Fig 58. SPI-bus timing

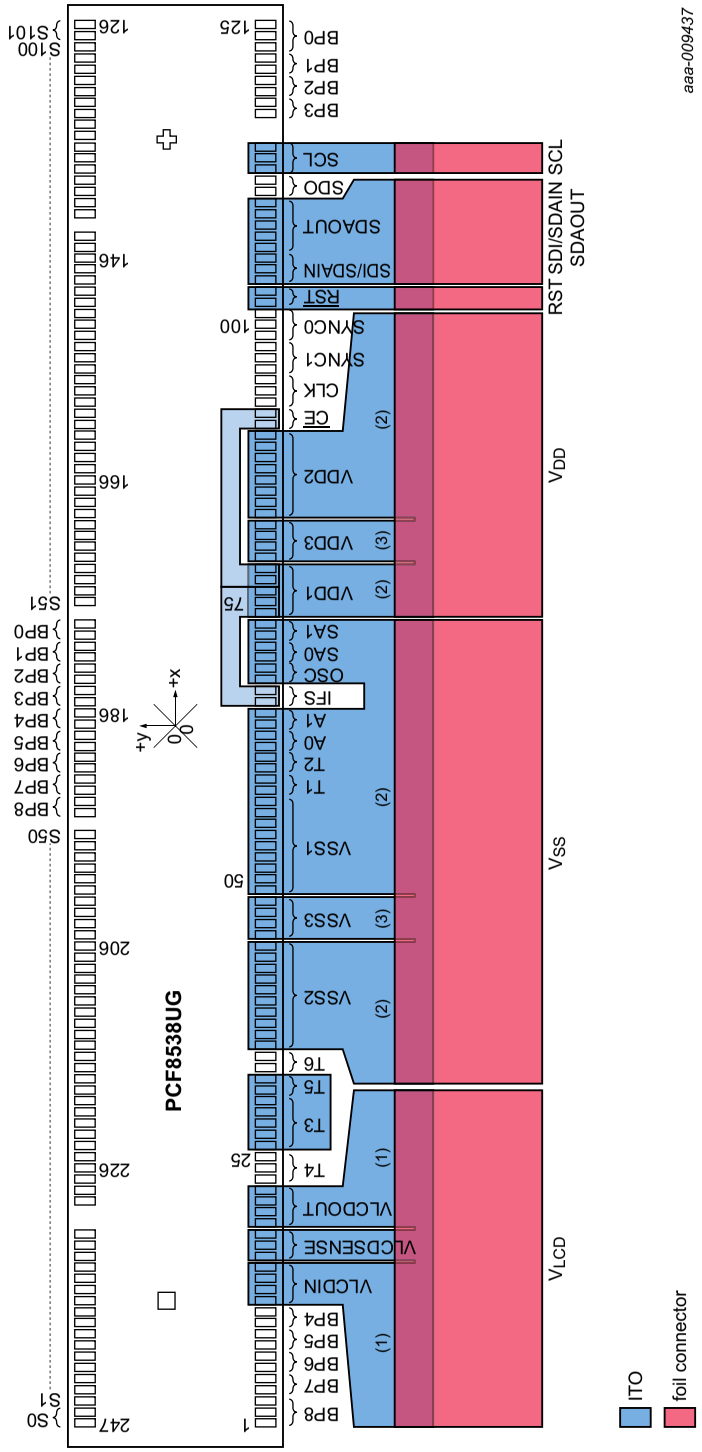
14. Application information

14.1 ITO layout recommendations for ESD/EMC robustness in COG applications

The crucial factor for gaining an EMC and ESD robust application is the quality of the VSS1 line.

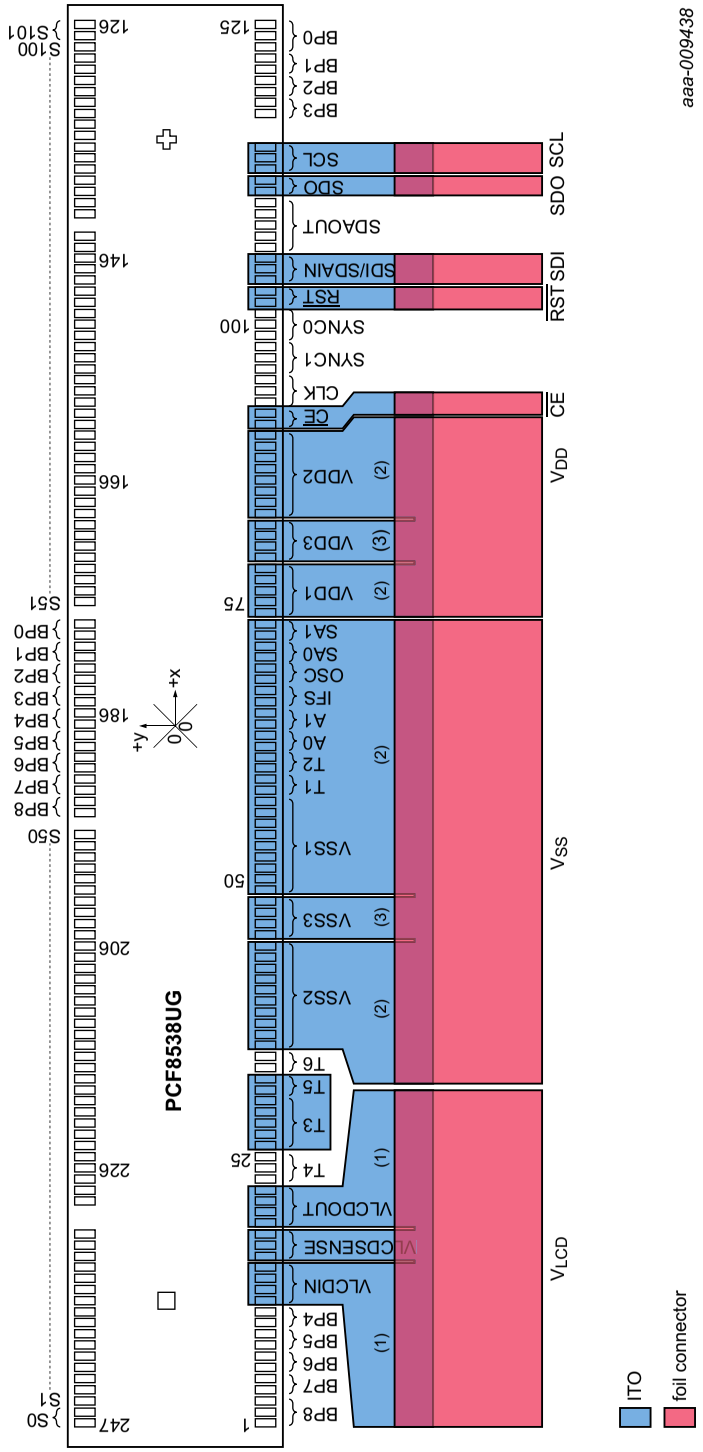
- To get an EMC/ESD robust ITO/glass layout, the $R_{ITO(VSS1)}$ has to be kept as low as possible.
- In the most common applications VSS1 will be connected to the pins T1, T2, A0, A1, OSC, SA0, SA1 and IFS (in the case of using the SPI interface) by using a very wide ITO connection
- If possible, the ITO connection of VSS1 should be made wide, for example by fanning out the other connections
- When the display is enabled, the charge and discharge caused by display activity affects the VSS1 line. This causes a dynamic current in the VSS1 line which means that dynamic voltage peaks in the VSS1 line may interfere with the low voltage part of the PCF8538. Therefore a low $R_{ITO(VSS1)}$ is also important for an improved noise immunity of the PCF8538 especially at high V_{LCD} values (V_{LCD} > 10 V).
- A low $R_{ITO(VSS1)}$ will also improve the communication stability with the microcontroller by reducing the effects of local ground (VSS1) bounce caused by high SDAACK currents.
- It should be considered that VSS1 is internally connected to the IC substrate, therefore noise on the VSS1 line will cause noise inside the IC.

Figure 59 and Figure 60 are showing the recommended ITO connections for a COG layout according to the interface type use.



(1) $R_{ITO} \leq 100\ \Omega$.
(2) $R_{ITO} \leq 50\ \Omega$.
(3) $R_{ITO} \leq 200\ \Omega$.

Fig 59. Recommended ITO connections for the I²C interface



(1) $R_{ITO} \leq 100\ \Omega$.
(2) $R_{ITO} \leq 50\ \Omega$.
(3) $R_{ITO} \leq 200\ \Omega$.

Fig 60. Recommended ITO connections for the SPI interface

14.2 Cascaded operation

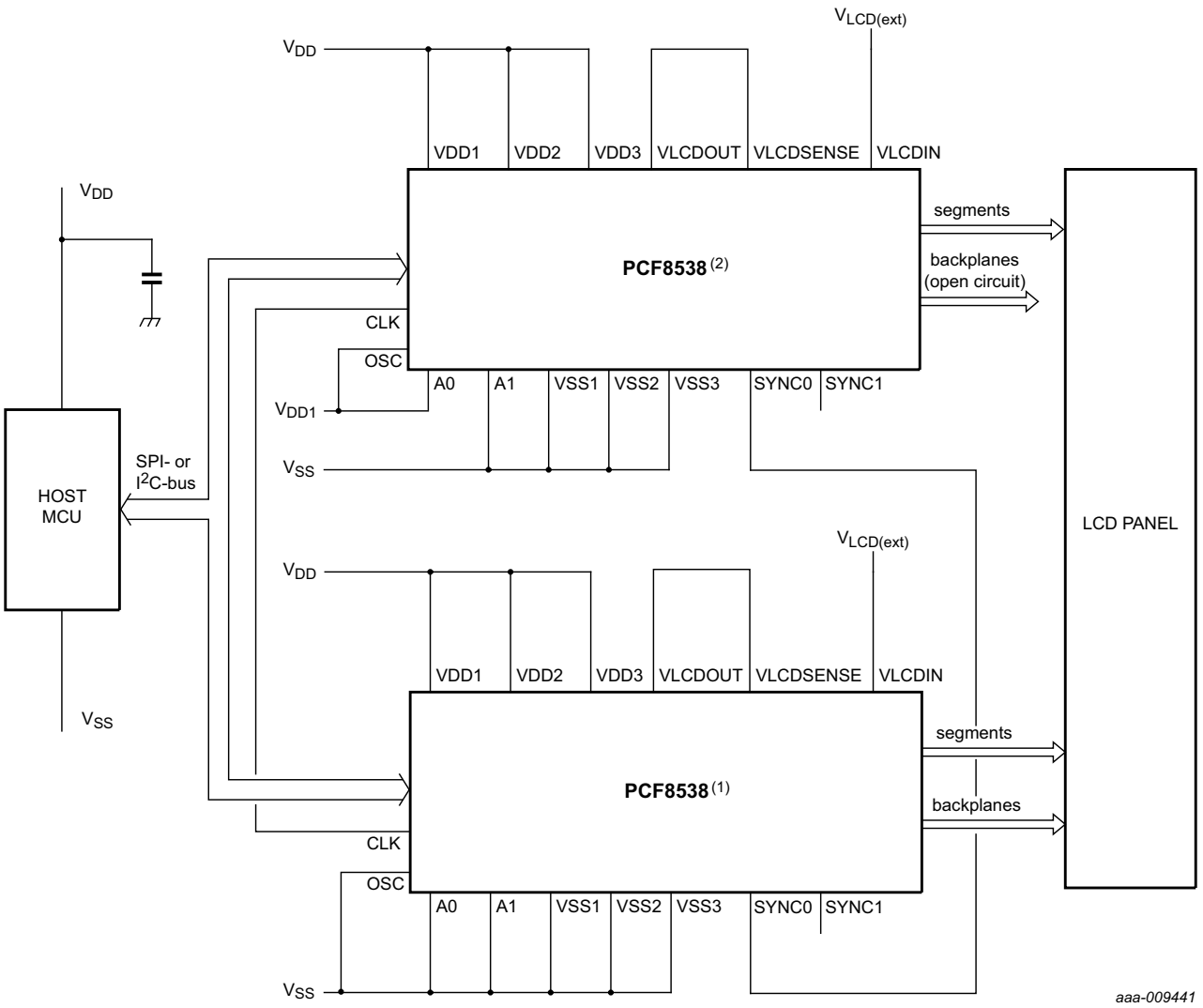
In large display configurations, up to four PCF8538 can be distinguished on the same bus by using the 2-bit hardware device addresses (A0 and A1).

Table 55. Addressing cascaded PCF8538

Pin A1	Pin A0	Device
0	0	0 (master)
0	1	1 (slave)
1	0	2 (slave)
1	1	3 (slave)

14.2.1 Wiring backplane and segment outputs

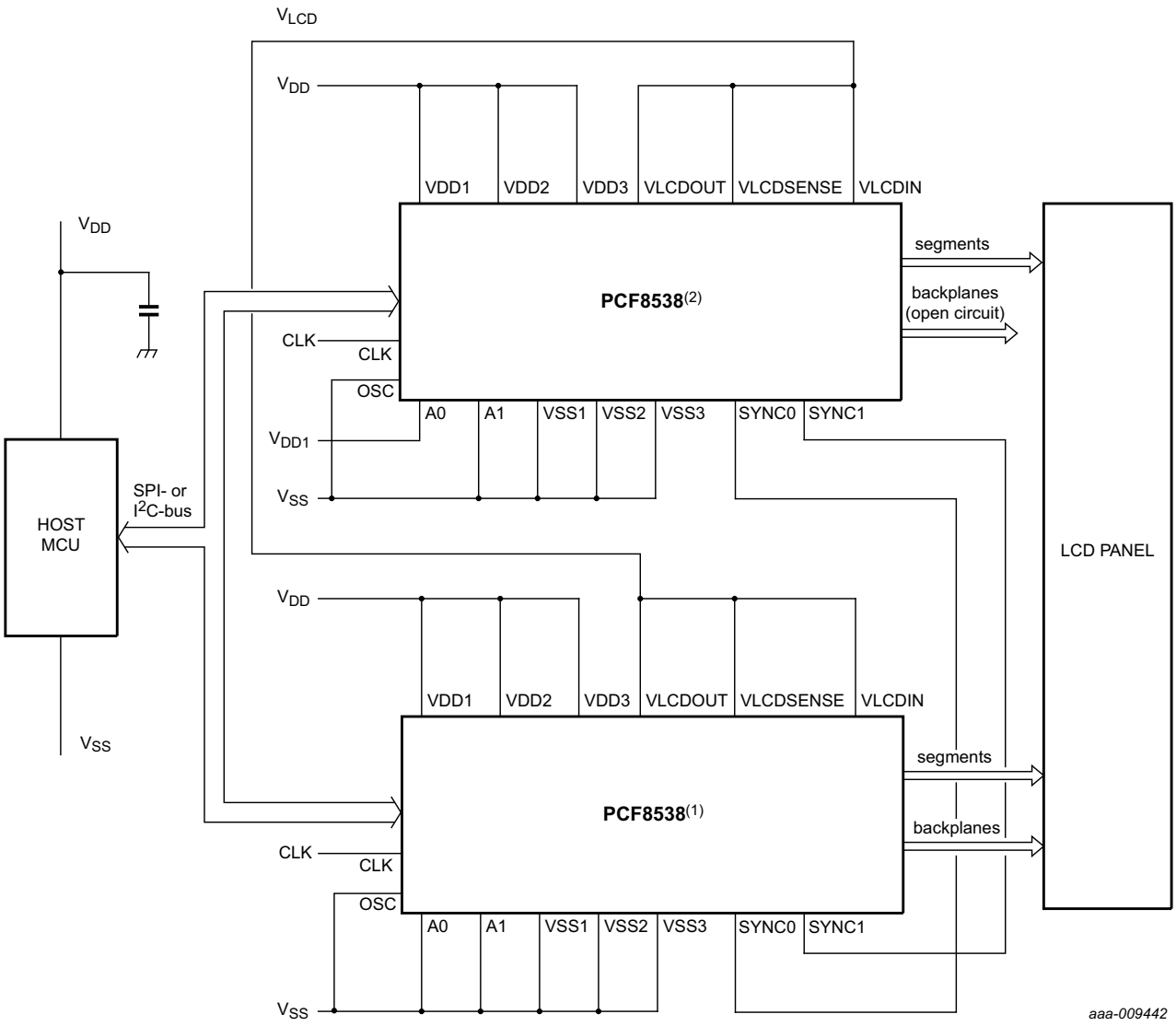
When the cascaded PCF8538 are synchronized, they can share the backplane signals from one of the devices in the cascade. Such an arrangement is cost-effective in large LCD applications since the backplane outputs of only one device need to be through-plated to the backplane electrodes of the display. The other PCF8538 of the cascade contribute additional segment outputs. The backplanes can either be connected together to enhance the drive capability or some can be left open-circuit (such as the ones from the slave in Figure 61 and Figure 62) or just some of the master and some of the slave will be taken to facilitate the layout of the display.



(1) Is master (OSC and A0 connected to V_{SS1}).

(2) Is slave (OSC and A0 connected to V_{DD1}).

Fig 61. Cascaded configuration with two PCF8538 with external V_{LCD} and internal clock



(1) Is master (A0 connected to V_{SS1}).

(2) Is slave (A0 connected to V_{DD1}).

Fig 62. Cascaded configuration with two PCF8538 with internal V_{LCD} and external clock

14.2.2 Device synchronization

The SYNC0 and SYNC1 lines are provided to maintain the correct synchronization between all cascaded PCF8538. (SYNC1 must not be connected when using an externally supplied V_{LCD}.)This synchronization is guaranteed after the Power-On Reset (POR). SYNC0 and SYNC1 are organized as input/output pins.

Both, the internally generated clock frequency or, alternatively, an externally supplied clock signal can be used in cascaded applications.

In cascaded applications that use the internal clock, the master PCF8538 with device address A[1:0] = 00 must have the OSC pin connected to V_{SS1} and the COE bit is set logic 1, so that this device uses its internal clock to generate a clock signal at the CLK pin.

The other PCF8538 devices are having the OSC pin connected to V_{DD1}, meaning that these devices are ready to receive an external clock signal which is provided by the master device with subaddress A[1:0] = 00.

If the master is providing the clock signal to the slave devices, care must be taken that the sending of display enable or disable will be received by both, the master and the slaves at the same time. When the display is disabled, the output from pin CLK is disabled too. The disconnection of the clock may result in a DC component for the display.

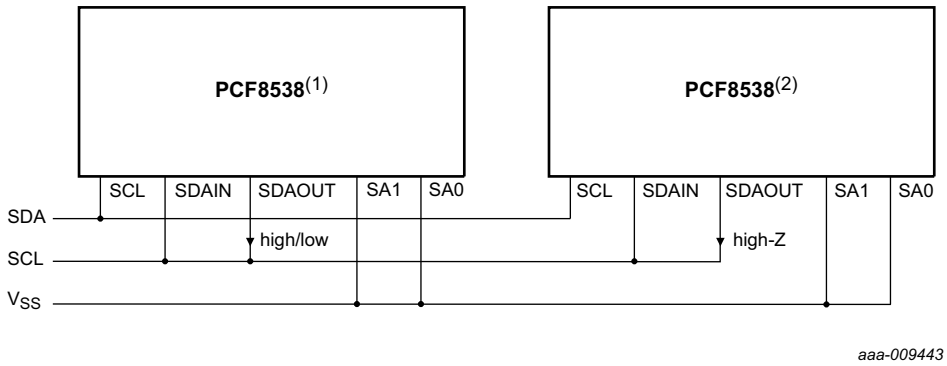
In cascaded applications that use an external clock, all devices have the OSC pin connected to V_{DD1} and thus an external CLK being provided for the system (all devices connected to the same external CLK).

14.2.3 Display data

The storage of display data is determined by the contents of the device address register (see Section 7.2.3 on page 10). Storage is allowed only when the content of the device address register matches with the hardware device address applied to the pins A0 and A1. If the content of the device address register and the hardware device address do not match, data storage is inhibited but the data pointer is incremented as if data storage had taken place. The hardware device address must not be changed while the device is being accessed on the interface.

14.2.4 Data read

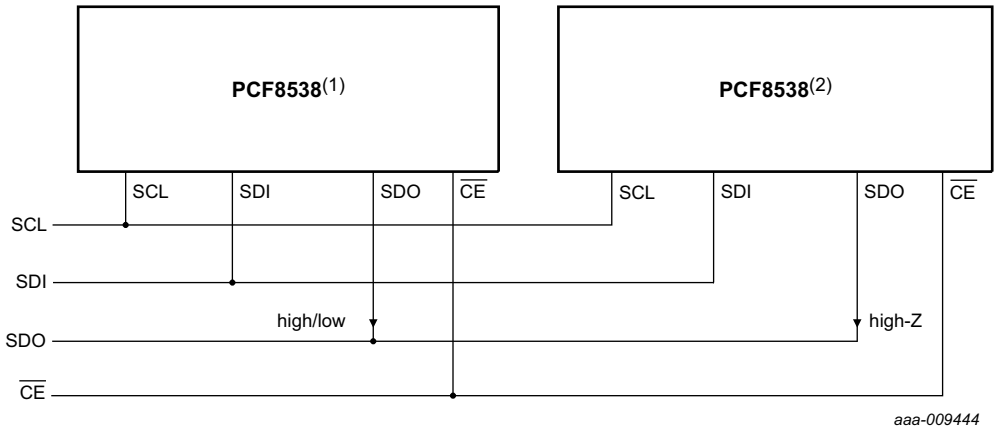
Only when the content of the device address register (see Section 7.2.3 on page 10) matches with the hardware device address applied to the pins A0 and A1, the temperature or device status readout (see Section 7.2.7 on page 12) is activated. If the content of the device address register and the hardware device address do not match, the data output pin (SDA or SDO) of the device is in 3-state. With this, bus conflicts and incorrect reading is prevented.



(1) Master.

(2) Slave.

a. I^2C interface



(1) Master.

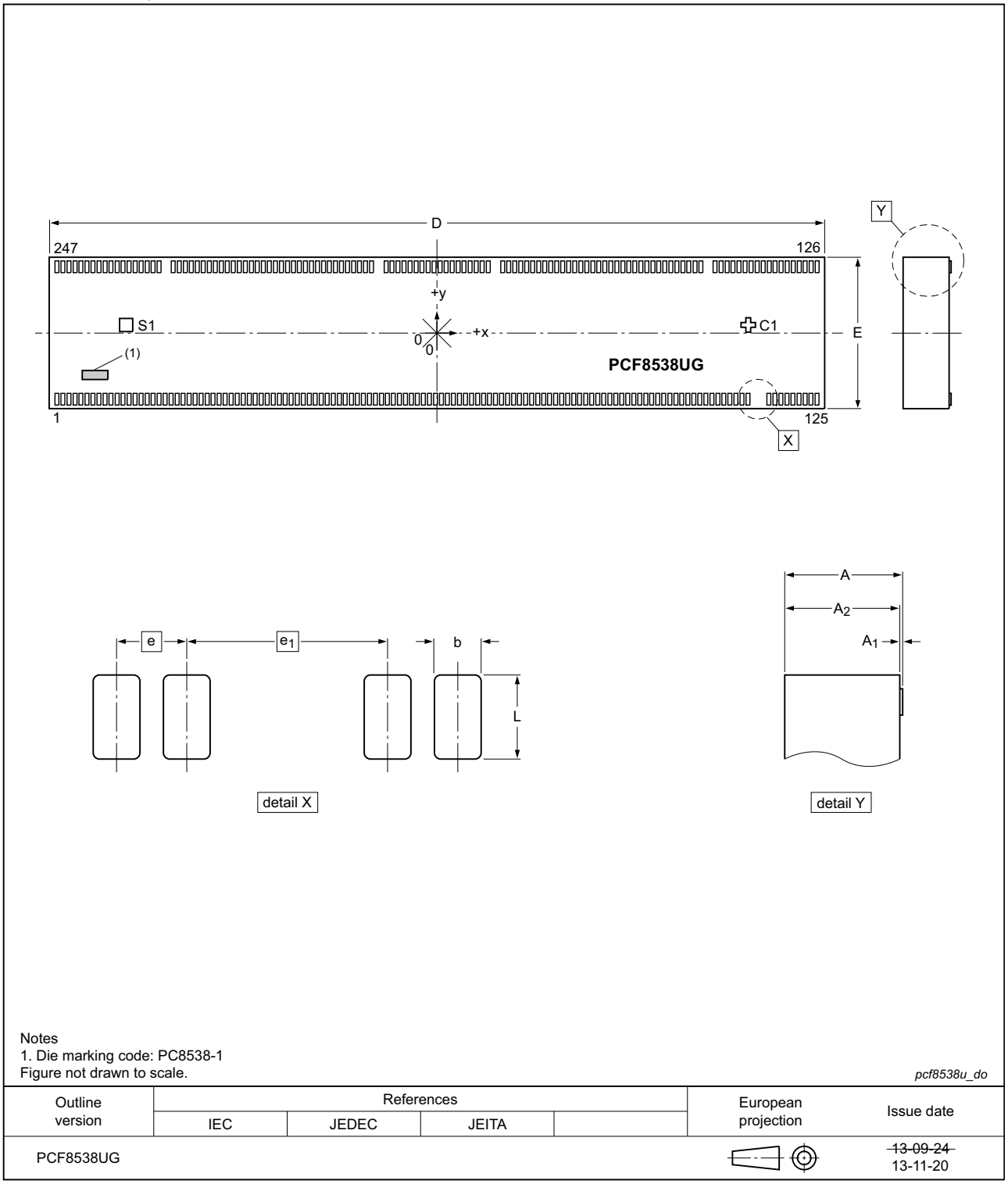
(2) Slave.

b. SPI interface

Fig 63. Cascade configuration for data reading

15. Bare die outline

Bare die; 247 bumps **PCF8538UG**



Notes
1. Die marking code: PC8538-1
Figure not drawn to scale.

pcf8538u_do

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
PCF8538UG						~~13-09-24~~ 13-11-20

Fig 64. Bare die outline of PCF8538UG

Table 56. Dimensions of PCF8538U

Original dimensions are in mm.

Unit (mm)	A	A_1	A_2	b	D	E	e	e_1	L
max	-	0.018	-	-	-	-	-	-	-
nom	0.40	0.015	0.38	0.03	5.88	1.20	0.045	0.158	0.09
min	-	0.012	-	-	-	-	-	-	-

Table 57. Bump locations

All x/y coordinates represent the position of the center of each bump with respect to the center (x/y = 0) of the chip; see Figure 64.

Symbol	Pin	Coordinates		Pitch	Symbol	Pin	Coordinates		Pitch
		X (µm)	Y (µm)	X (µm)			X (µm)	Y (µm)	X (µm)
COM8	1	−2847.5	−495	-	S101	126	2846.7	495	-
	2	−2802.5	−495	45		127	2801.7	495	45
	3	−2757.5	−495	45	S100	128	2756.7	495	45
COM7	4	−2712.5	−495	45	S99	129	2711.7	495	45
	5	−2667.5	−495	45	S98	130	2666.7	495	45
COM6	6	−2622.5	−495	45	S97	131	2621.7	495	45
	7	−2577.5	−495	45	S96	132	2576.7	495	45
COM5	8	−2532.5	−495	45	S95	133	2531.7	495	45
	9	−2487.5	−495	45	S94	134	2486.7	495	45
COM4	10	−2442.5	−495	45	S93	135	2441.7	495	45
	11	−2397.5	−495	45	S92	136	2396.7	495	45
VLCDIN	12	−2352.5	−495	45	S91	137	2351.7	495	45
	13	−2307.5	−495	45	S90	138	2306.7	495	45
	14	−2262.5	−495	45	S89	139	2261.7	495	45
	15	−2217.5	−495	45	S88	140	2216.7	495	45
VLCDSENSE	16	−2172.5	−495	45	S87	141	2171.7	495	45
	17	−2127.5	−495	45	S86	142	2126.7	495	45
	18	−2082.5	−495	45	S85	143	2081.7	495	45
VLCDOUT	19	−2037.5	−495	45	S84	144	1975.7	495	106
	20	−1992.5	−495	45	S83	145	1930.7	495	45
	21	−1947.5	−495	45	S82	146	1885.7	495	45
	22	−1902.5	−495	45	S81	147	1840.7	495	45
T4	23	−1857.5	−495	45	S80	148	1795.7	495	45
	24	−1812.5	−495	45	S79	149	1750.7	495	45
	25	−1767.5	−495	45	S78	150	1705.7	495	45
T3	26	−1722.5	−495	45	S77	151	1660.7	495	45
	27	−1677.5	−495	45	S76	152	1615.7	495	45
	28	−1632.5	−495	45	S75	153	1570.7	495	45
	29	−1587.5	−495	45	S74	154	1525.7	495	45
	30	−1542.5	−495	45	S73	155	1480.7	495	45
T5	31	−1497.5	−495	45	S72	156	1435.7	495	45
	32	−1452.5	−495	45	S71	157	1390.7	495	45

Table 57. Bump locations *...continued*

All x/y coordinates represent the position of the center of each bump with respect to the center (x/y = 0) of the chip; see Figure 64.

Symbol	Pin	Coordinates		Pitch	Symbol	Pin	Coordinates		Pitch
		X (µm)	Y (µm)	X (µm)			X (µm)	Y (µm)	X (µm)
T6	33	−1407.5	−495	45	S70	158	1345.7	495	45
	34	−1362.5	−495	45	S69	159	1300.7	495	45
VSS2	35	−1317.5	−495	45	S68	160	1255.7	495	45
	36	−1272.5	−495	45	S67	161	1210.7	495	45
	37	−1227.5	−495	45	S66	162	1165.7	495	45
	38	−1182.5	−495	45	S65	163	1120.7	495	45
	39	−1137.5	−495	45	S64	164	1075.7	495	45
	40	−1092.5	−495	45	S63	165	1030.7	495	45
	41	−1047.5	−495	45	S62	166	985.7	495	45
	42	−1002.5	−495	45	S61	167	940.7	495	45
	43	−957.5	−495	45	S60	168	895.7	495	45
	44	−912.5	−495	45	S59	169	850.7	495	45
VSS3	45	−867.5	−495	45	S58	170	805.7	495	45
	46	−822.5	−495	45	S57	171	760.7	495	45
	47	−777.5	−495	45	S56	172	715.7	495	45
	48	−732.5	−495	45	S55	173	670.7	495	45
VSS1	49	−687.5	−495	45	S54	174	625.7	495	45
	50	−642.5	−495	45	S53	175	580.7	495	45
	51	−597.5	−495	45	S52	176	535.7	495	45
	52	−552.5	−495	45	S51	177	490.7	495	45
	53	−507.5	−495	45	COM0	178	382.1	495	108.6
	54	−462.5	−495	45		179	337.1	495	45
	55	−417.5	−495	45	COM1	180	292.1	495	45
	56	−372.5	−495	45		181	247.1	495	45
	57	−327.5	−495	45	COM2	182	202.1	495	45
T1	58	−282.5	−495	45		183	157.1	495	45
	59	−237.5	−495	45	COM3	184	112.1	495	45
T2	60	−192.5	−495	45		185	67.1	495	45
	61	−147.5	−495	45	COM4	186	22.1	495	45
A0	62	−102.5	−495	45		187	−22.9	495	45
	63	−57.5	−495	45	COM5	188	−67.9	495	45
A1	64	−12.5	−495	45		189	−112.9	495	45
	65	32.5	−495	45	COM6	190	−157.9	495	45
IFS	66	77.5	−495	45		191	−202.9	495	45
	67	122.5	−495	45	COM7	192	−247.9	495	45
OSC	68	167.5	−495	45		193	−292.9	495	45
	69	212.5	−495	45	COM8	194	−337.9	495	45

Table 57. Bump locations *...continued*

All x/y coordinates represent the position of the center of each bump with respect to the center (x/y = 0) of the chip; see Figure 64.

Symbol	Pin	Coordinates		Pitch	Symbol	Pin	Coordinates		Pitch
		X (µm)	Y (µm)	X (µm)			X (µm)	Y (µm)	X (µm)
SA0	70	257.5	−495	45	COM8	195	−382.9	495	45
	71	302.5	−495	45	S50	196	−491.5	495	108.6
SA1	72	347.5	−495	45	S49	197	−536.5	495	45
	73	392.5	−495	45	S48	198	−581.5	495	45
VDD1	74	437.5	−495	45	S47	199	−626.5	495	45
	75	482.5	−495	45	S46	200	−671.5	495	45
	76	527.5	−495	45	S45	201	−716.5	495	45
	77	572.5	−495	45	S44	202	−761.5	495	45
	78	617.5	−495	45	S43	203	−806.5	495	45
VDD3	79	662.5	−495	45	S42	204	−851.5	495	45
	80	707.5	−495	45	S41	205	−896.5	495	45
	81	752.5	−495	45	S40	206	−941.5	495	45
	82	797.5	−495	45	S39	207	−986.5	495	45
VDD2	83	842.5	−495	45	S38	208	−1031.5	495	45
	84	887.5	−495	45	S37	209	−1076.5	495	45
	85	932.5	−495	45	S36	210	−1121.5	495	45
	86	977.5	−495	45	S35	211	−1166.5	495	45
	87	1022.5	−495	45	S34	212	−1211.5	495	45
	88	1067.5	−495	45	S33	213	−1256.5	495	45
	89	1112.5	−495	45	S32	214	−1301.5	495	45
	90	1157.5	−495	45	S31	215	−1346.5	495	45
$\overline{CE}$	91	1202.5	−495	45	S30	216	−1391.5	495	45
	92	1247.5	−495	45	S29	217	−1436.5	495	45
CLK	93	1292.5	−495	45	S28	218	−1481.5	495	45
	94	1337.5	−495	45	S27	219	−1526.5	495	45
	95	1382.5	−495	45	S26	220	−1571.5	495	45
SYNC1	96	1427.5	−495	45	S25	221	−1616.5	495	45
	97	1472.5	−495	45	S24	222	−1661.5	495	45
	98	1517.5	−495	45	S23	223	−1706.5	495	45
SYNC0	99	1562.5	−495	45	S22	224	−1751.5	495	45
	100	1607.5	−495	45	S21	225	−1796.5	495	45
	101	1652.5	−495	45	S20	226	−1841.5	495	45
$\overline{RST}$	102	1697.5	−495	45	S19	227	−1886.5	495	45
	103	1742.5	−495	45	S18	228	−1931.5	495	45
SDI/SDAIN	104	1787.5	−495	45	S17	229	−1976.5	495	45
	105	1832.5	−495	45	S16	230	−2082.5	495	106
	106	1877.5	−495	45	S15	231	−2127.5	495	45

Table 57. Bump locations *...continued*

All x/y coordinates represent the position of the center of each bump with respect to the center (x/y = 0) of the chip; see Figure 64.

Symbol	Pin	Coordinates		Pitch	Symbol	Pin	Coordinates		Pitch
		X (µm)	Y (µm)	X (µm)			X (µm)	Y (µm)	X (µm)
SDAOUT	107	1922.5	−495	45	S14	232	−2172.5	495	45
	108	1967.5	−495	45	S13	233	−2217.5	495	45
	109	2012.5	−495	45	S12	234	−2262.5	495	45
	110	2057.5	−495	45	S11	235	−2307.5	495	45
	111	2102.5	−495	45	S10	236	−2352.5	495	45
SDO	112	2147.5	−495	45	S9	237	−2397.5	495	45
	113	2192.5	−495	45	S8	238	−2442.5	495	45
SCL	114	2237.5	−495	45	S7	239	−2487.5	495	45
	115	2282.5	−495	45	S6	240	−2532.5	495	45
	116	2327.5	−495	45	S5	241	−2577.5	495	45
COM3	117	2485.2	−495	157.7	S4	242	−2622.5	495	45
	118	2530.2	−495	45	S3	243	−2667.5	495	45
COM2	119	2575.2	−495	45	S2	244	−2712.5	495	45
	120	2620.2	−495	45	S1	245	−2757.5	495	45
COM1	121	2665.2	−495	45	S0	246	−2802.5	495	45
	122	2710.2	−495	45		247	−2847.5	495	45
COM0	123	2755.2	−495	45	-	-	-	-	
	124	2800.2	−495	45	-	-	-	-	
	125	2845.2	−495	45	-	-	-	-	

The alignment marks are shown in Table 58.

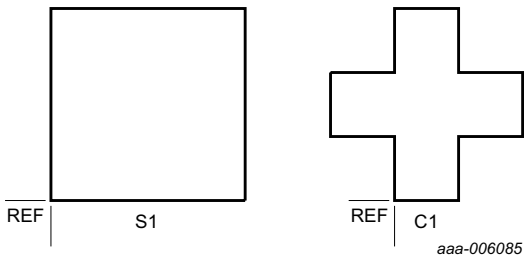


Fig 65. Alignment marks

Table 58. Alignment marking

All x/y coordinates represent the position of the REF point (see Figure 65) with respect to the center (x/y = 0) of the chip; see Figure 64.

Symbol	Size (µm)	X (µm)	Y (µm)
S1	90 × 90	−2375	15
C1	90 × 90	2312	15

Table 59. Gold bump hardness

Type number	Min	Max	Unit[1]
PCF8538UG/2DA/1	60	120	HV

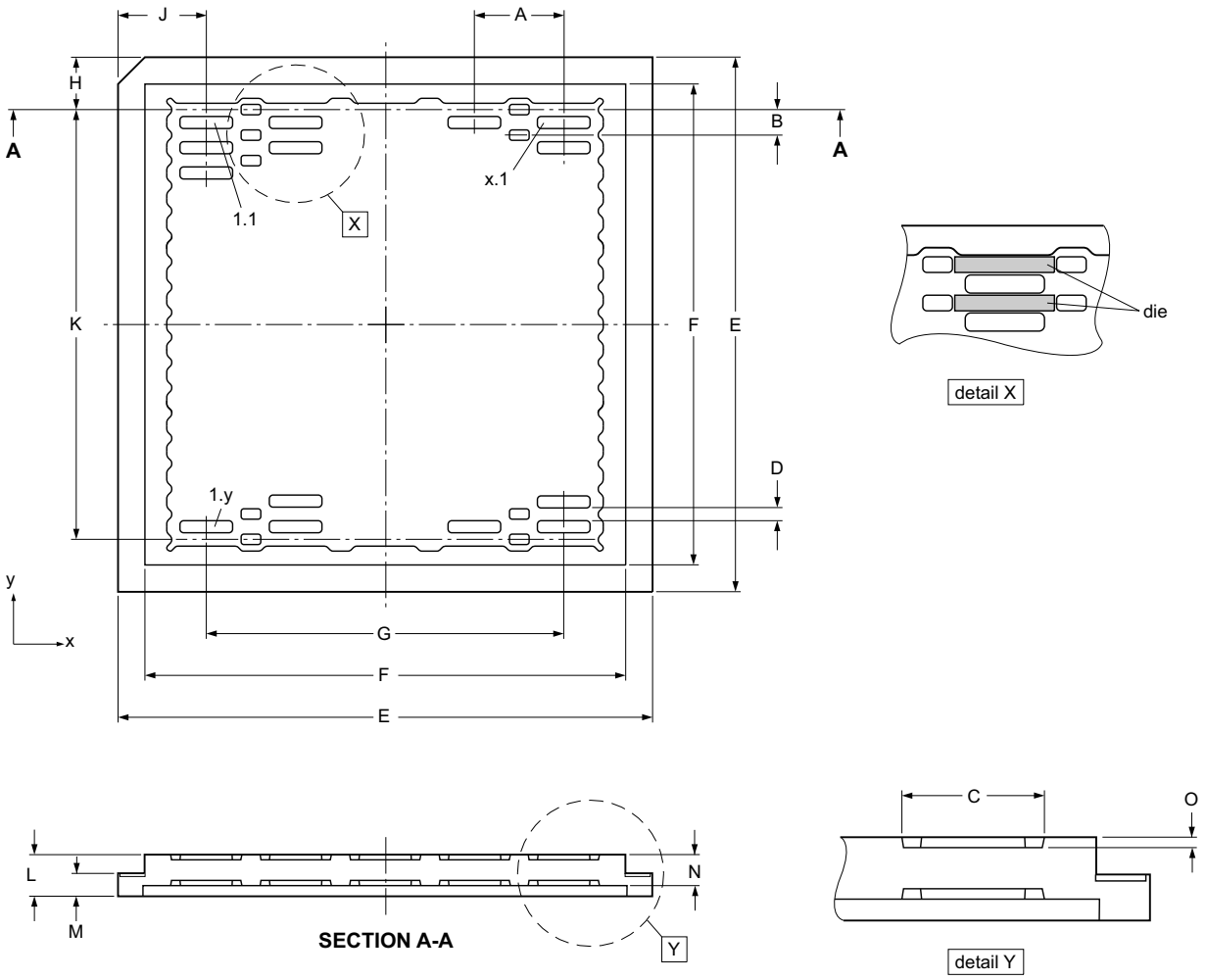
[1] Pressure of diamond head: 10 g to 50 g.

16. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling Metal-Oxide Semiconductor (MOS) devices ensure that all normal precautions are taken as described in *JESD625-A*, *IEC 61340-5* or equivalent standards.

17. Packing information

17.1 Tray information



Dimensions in mm

aaa-003345

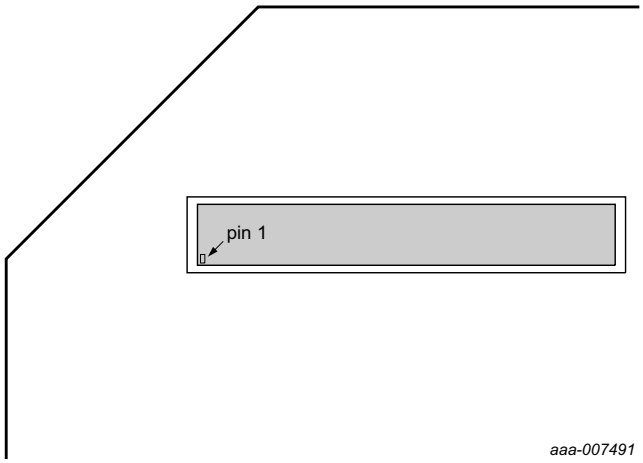
Schematic drawing, not drawn to scale. Top side view. For dimensions see Table 60. Tray has pockets on both, top side and bottom side. The IC is stored with the active side up. To get the active side down, turn the tray.

Fig 66. Tray details of PCF8538U

Table 60. Description of tray details

Tray details are shown in Figure 66.

Tray details														
Dimensions														
A	B	C	D	E	F	G	H	J	K	L	M	N	O	Unit
8	2.5	5.978	1.298	76	68	56	6.75	10	62.5	4.2	2.6	3.2	0.6	mm
Number of pockets														
x direction							y direction							
8							26							



The orientation of the IC in a pocket with active side up is indicated by the position of pin 1 with respect to the chamfer on the upper left corner of the tray.

Fig 67. Die alignment in the tray

18. Appendix

18.1 LCD segment driver selection

Table 61. Selection of LCD segment drivers

Type name	Number of elements at MUX							V_{DD} (V)	V_{LCD} (V)	f_{fr} (Hz)	V_{LCD} (V) charge pump	V_{LCD} (V) temperature compensat.	T_{amb} (°C)	Interface	Package	AEC-Q100
	1:1	1:2	1:3	1:4	1:6	1:8	1:9									
PCA8561AHN[5]	18	36	54	72	-	-	-	1.8 to 5.5	1.8 to 5.5	32 to 256[1]	N	N	–40 to 105	I^2C	HVQFN32	Y
PCA8561BHN[5]	18	36	54	72	-	-	-	1.8 to 5.5	1.8 to 5.5	32 to 256[1]	N	N	–40 to 105	SPI	HVQFN32	Y
PCF8566TS	24	48	72	96	-	-	-	2.5 to 6	2.5 to 6	69	N	N	–40 to 85	I^2C	VSO40	N
PCF85162T	32	64	96	128	-	-	-	1.8 to 5.5	2.5 to 6.5	82	N	N	–40 to 85	I^2C	TSSOP48	N
PCA85162T	32	64	96	128	-	-	-	1.8 to 5.5	2.5 to 8	110	N	N	–40 to 95	I^2C	TSSOP48	Y
PCA85262ATT	32	64	96	128	-	-	-	1.8 to 5.5	2.5 to 8	200	N	N	–40 to 105	I^2C	TSSOP48	Y
PCF8551ATT[5]	36	72	108	144	-	-	-	1.8 to 5.5	1.8 to 5.5	32 to 128[1]	N	N	–40 to 85	I^2C	TSSOP48	N
PCF8551BTT[5]	36	72	108	144	-	-	-	1.8 to 5.5	1.8 to 5.5	32 to 128[1]	N	N	–40 to 85	SPI	TSSOP48	N
PCA8551ATT[5]	36	72	108	144	-	-	-	1.8 to 5.5	1.8 to 5.5	32 to 256[1]	N	N	–40 to 105	I^2C	TSSOP48	Y
PCA8551BTT[5]	36	72	108	144	-	-	-	1.8 to 5.5	1.8 to 5.5	32 to 256[1]	N	N	–40 to 105	SPI	TSSOP48	Y
PCF85176T	40	80	120	160	-	-	-	1.8 to 5.5	2.5 to 6.5	82	N	N	–40 to 85	I^2C	TSSOP56	N
PCA85176T	40	80	120	160	-	-	-	1.8 to 5.5	2.5 to 8	110	N	N	–40 to 95	I^2C	TSSOP56	Y
PCA85276ATT	40	80	120	160	-	-	-	1.8 to 5.5	2.5 to 8	200	N	N	–40 to 105	I^2C	TSSOP56	Y
PCF85176H	40	80	120	160	-	-	-	1.8 to 5.5	2.5 to 6.5	82	N	N	–40 to 85	I^2C	TQFP64	N
PCA85176H	40	80	120	160	-	-	-	1.8 to 5.5	2.5 to 8	82	N	N	–40 to 95	I^2C	TQFP64	Y
PCF8553ATT[5]	40	80	120	160	-	-	-	1.8 to 5.5	1.8 to 5.5	32 to 128[1]	N	N	–40 to 85	I^2C	TSSOP56	N
PCF8553BTT[5]	40	80	120	160	-	-	-	1.8 to 5.5	1.8 to 5.5	32 to 128[1]	N	N	–40 to 85	SPI	TSSOP56	N
PCA8553ATT[5]	40	80	120	160	-	-	-	1.8 to 5.5	1.8 to 5.5	32 to 256[1]	N	N	–40 to 105	I^2C	TSSOP56	Y
PCA8553BTT[5]	40	80	120	160	-	-	-	1.8 to 5.5	1.8 to 5.5	32 to 256[1]	N	N	–40 to 105	SPI	TSSOP56	Y
PCA8546ATT	-	-	-	176	-	-	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	N	N	–40 to 95	I^2C	TSSOP56	Y
PCA8546BTT	-	-	-	176	-	-	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	N	N	–40 to 95	SPI	TSSOP56	Y
PCA8547AHT[5]	44	88	-	176	-	-	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	Y	Y[3]	–40 to 95	I^2C	TQFP64	Y
PCA8547BHT[5]	44	88	-	176	-	-	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	Y	Y[3]	–40 to 95	SPI	TQFP64	Y
PCF85134HL	60	120	180	240	-	-	-	1.8 to 5.5	2.5 to 6.5	82	N	N	–40 to 85	I^2C	LQFP80	N
PCA85134H	60	120	180	240	-	-	-	1.8 to 5.5	2.5 to 8	82	N	N	–40 to 95	I^2C	LQFP80	Y

Table 61. Selection of LCD segment drivers *...continued*

Type name	Number of elements at MUX							V_{DD} (V)	V_{LCD} (V)	f_{fr} (Hz)	V_{LCD} (V) charge pump	V_{LCD} (V) temperature compensat.	T_{amb} (°C)	Interface	Package	AEC-Q100
	1:1	1:2	1:3	1:4	1:6	1:8	1:9									
PCA8543AHL	60	120	-	240	-	-	-	2.5 to 5.5	2.5 to 9	60 to 300[1]	Y	Y	–40 to 105	I^2C	LQFP80	Y
PCF8545ATT	-	-	-	176	252	320	-	1.8 to 5.5	2.5 to 5.5	60 to 300[1]	N	N	–40 to 85	I^2C	TSSOP56	N
PCF8545BTT	-	-	-	176	252	320	-	1.8 to 5.5	2.5 to 5.5	60 to 300[1]	N	N	–40 to 85	SPI	TSSOP56	N
PCF8536AT[4]	-	-	-	176	252	320	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	N	N	–40 to 85	I^2C	TSSOP56	N
PCF8536BT[4]	-	-	-	176	252	320	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	N	N	–40 to 85	SPI	TSSOP56	N
PCA8536AT[4]	-	-	-	176	252	320	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	N	N	–40 to 95	I^2C	TSSOP56	Y
PCA8536BT[4]	-	-	-	176	252	320	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	N	N	–40 to 95	SPI	TSSOP56	Y
PCF8537AH	44	88	-	176	276	352	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	Y	Y[3]	–40 to 85	I^2C	TQFP64	N
PCF8537BH	44	88	-	176	276	352	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	Y	Y[3]	–40 to 85	SPI	TQFP64	N
PCA8537AH	44	88	-	176	276	352	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	Y	Y[3]	–40 to 95	I^2C	TQFP64	Y
PCA8537BH	44	88	-	176	276	352	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	Y	Y[3]	–40 to 95	SPI	TQFP64	Y
PCA9620H	60	120	-	240	320	480	-	2.5 to 5.5	2.5 to 9	60 to 300[1]	Y	Y[3]	–40 to 105	I^2C	LQFP80	Y
PCA9620U	60	120	-	240	320	480	-	2.5 to 5.5	2.5 to 9	60 to 300[1]	Y	Y[3]	–40 to 105	I^2C	bare die	Y
PCF8552DUG[5]	36	72	108	144	-	-	-	1.8 to 5.5	1.8 to 5.5	32 to 128[1]	N	N	–40 to 85	I^2C, SPI	bare die	N
PCA8552DUG[5]	36	72	108	144	-	-	-	1.8 to 5.5	1.8 to 5.5	32 to 256[1]	N	N	–40 to 105	I^2C, SPI	bare die	Y
PCF8576DU	40	80	120	160	-	-	-	1.8 to 5.5	2.5 to 6.5	77	N	N	–40 to 85	I^2C	bare die	N
PCF8576EUG	40	80	120	160	-	-	-	1.8 to 5.5	2.5 to 6.5	77	N	N	–40 to 85	I^2C	bare die	N
PCA8576FUG	40	80	120	160	-	-	-	1.8 to 5.5	2.5 to 8	200	N	N	–40 to 105	I^2C	bare die	Y
PCF85133U	80	160	240	320	-	-	-	1.8 to 5.5	2.5 to 6.5	82, 110[2]	N	N	–40 to 85	I^2C	bare die	N
PCA85133U	80	160	240	320	-	-	-	1.8 to 5.5	2.5 to 8	82, 110[2]	N	N	–40 to 95	I^2C	bare die	Y
PCA85233U	80	160	240	320	-	-	-	1.8 to 5.5	2.5 to 8	150, 220[2]	N	N	–40 to 105	I^2C	bare die	Y
PCA8530DUG[5]	102	204	-	408	-	-	-	2.5 to 5.5	4 to 12	45 to 300[1]	Y	Y[3]	–40 to 105	I^2C, SPI	bare die	Y
PCF85132U	160	320	480	640	-	-	-	1.8 to 5.5	1.8 to 8	60 to 90[1]	N	N	–40 to 85	I^2C	bare die	N
PCA85132U	160	320	480	640	-	-	-	1.8 to 5.5	1.8 to 8	60 to 90[1]	N	N	–40 to 95	I^2C	bare die	Y
PCA85232U	160	320	480	640	-	-	-	1.8 to 5.5	1.8 to 8	117 to 176[1]	N	N	–40 to 95	I^2C	bare die	Y
PCF8538UG	102	204	-	408	612	816	918	2.5 to 5.5	4 to 12	45 to 300[1]	Y	Y[3]	–40 to 85	I^2C, SPI[2]	bare die	N
PCA8538UG	102	204	-	408	612	816	918	2.5 to 5.5	4 to 12	45 to 300[1]	Y	Y[3]	–40 to 105	I^2C, SPI[2]	bare die	Y

[1] Can be selected by command.

[2] Can be selected by pin configuration.

[3] Extra feature: Temperature sensor.

[4] Extra feature: 6 PWM channels.

[5] In development.

19. Abbreviations

Table 62. Abbreviations

Acronym	Description
COG	Chip-On-Glass
DC	Direct Current
EPROM	Erasable Programmable Read-Only Memory
ESD	ElectroStatic Discharge
HBM	Human Body Model
I^2C	Inter-Integrated Circuit bus
IC	Integrated Circuit
ITO	Indium Tin Oxide
LCD	Liquid Crystal Display
LSB	Least Significant Bit
MCU	Microcontroller Unit
MM	Machine Model
MSB	Most Significant Bit
MSL	Moisture Sensitivity Level
MUX	Multiplexer
OTP	One Time Programmable
POR	Power-On Reset
RC	Resistance-Capacitance
RAM	Random Access Memory
RMS	Root Mean Square
SCL	Serial CLock line
SDA	Serial DAta line
SMD	Surface Mount Device
SPI	Serial Peripheral Interface
VA	Vertical Alignment

20. References

[1] **AN10170 —** Design guidelines for COG modules with NXP monochrome LCD drivers

[2] **AN10439 —** Wafer Level Chip Size Package

[3] **AN10853 —** ESD and EMC sensitivity of IC

[4] **AN10706 —** Handling bare die

[5] **AN11267 —** EMC and system level ESD design guidelines for LCD drivers

[6] **IEC 60134 —** Rating systems for electronic tubes and valves and analogous semiconductor devices

[7] **IEC 61340-5 —** Protection of electronic devices from electrostatic phenomena

[8] **JESD22-A114 —** Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)

[9] **JESD78 —** IC Latch-Up Test

[10] **JESD625-A —** Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices

[11] **R_10015 —** Chip-On-Glass (COG) – a cost-effective and reliable technology for LCD displays, White Paper

[12] **SNV-FA-01-02 —** Marking Formats Integrated Circuits

[13] **UM10204 —** I^2C-bus specification and user manual

[14] **UM10569 —** Store and transport requirements

21. Revision history

Table 63. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCF8538 v.1	20131218	Product data sheet	-	-

22. Legal information

22.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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24. Tables

25. Figures

26. Contents

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Date of release: 18 December 2013
Document identifier: PCF8538