AN2823
Application note

Current source for LED driving based on the L5973AD

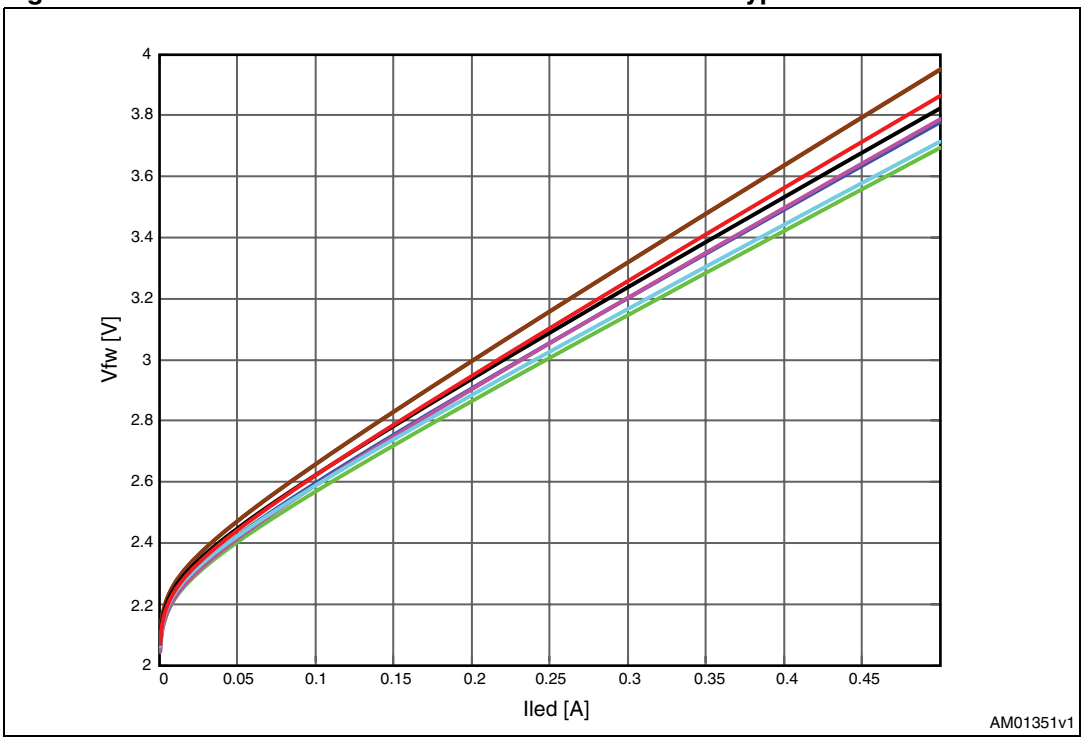
Introduction

LEDs are devices where the light intensity (brightness), measured in millicandelas or in lumens, is proportional to the forward current flowing through them. Two main classes can be identified given the typical forward current of the final application:

- Low current LEDs, from 15 mA to 50 mA, mainly used in the portable market for backlighting and signaling applications
- High current LEDs, with forward current between 350 mA to 1000 mA, typically used in lighting applications

The typical voltage drop across the LEDs when forward-biased depends on the color of the emitted light, and the spread is high even when considering LEDs from the same production lot, as shown in *Figure 1*.

Figure 1. V-I characteristic of 8 white LEDs of the same type



The spread of the forward voltage and the exponential trend of the I-V characteristic makes current mode driving more convenient than voltage driving. As a consequence, the current source regulates the LED current and the output voltage is fixed by the forward voltage across each LED.

Contents

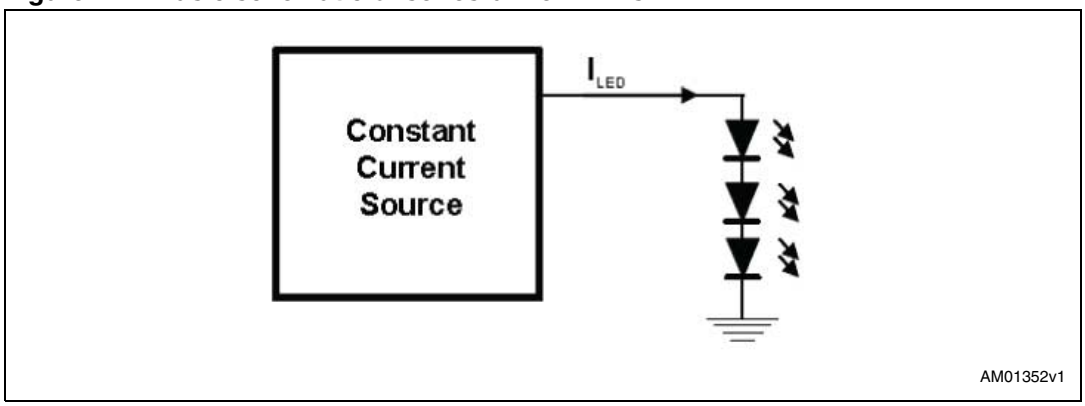
List of figures

1 Basic principles of LED driving

This paragraph deals with different ways to arrange a set of LEDs to generate the required lumen output. Advantages and disadvantages for each topology are also provided.

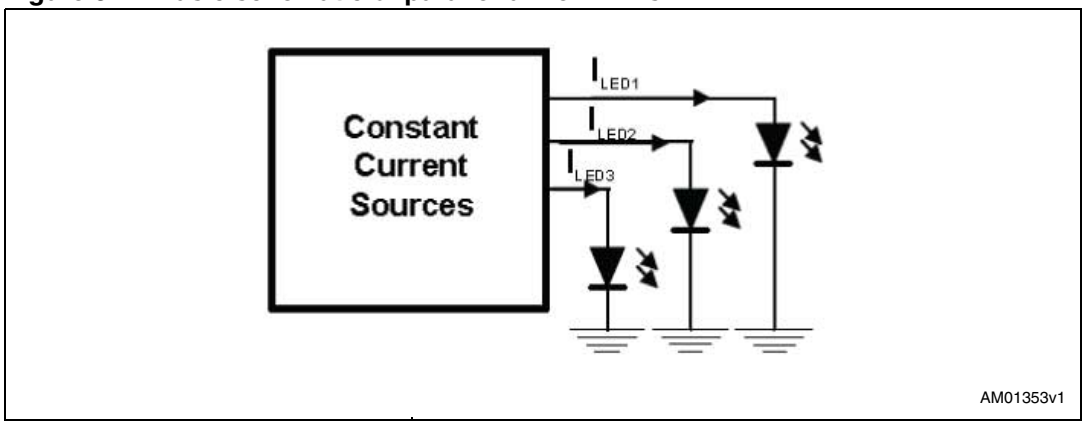
The easiest and cheapest way to drive LEDs is to connect them in series, as shown in *Figure 2*. However, this implies that the LED driver must provide an output voltage that is the sum of the forward voltage of the LEDs.

Figure 2. Basic schematic of series-driven LEDs



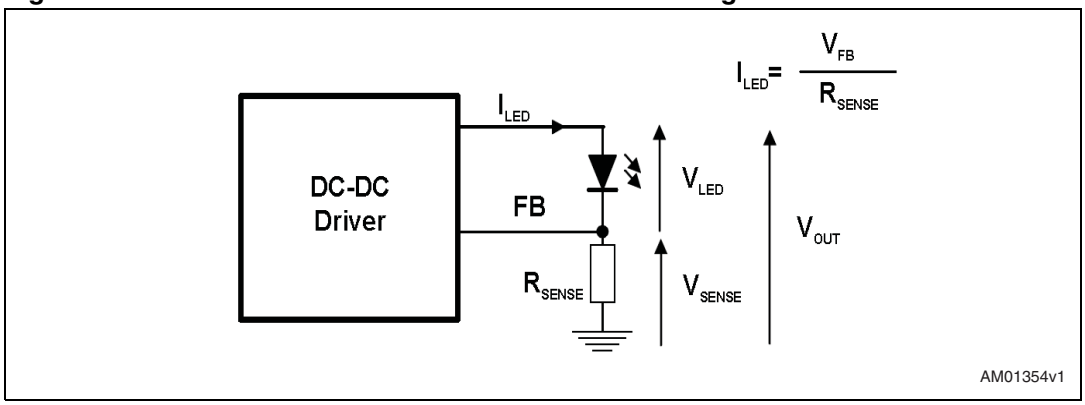
Therefore, in other cases the preferred solution is to drive LEDs in parallel, matching the different current sources (*Figure 3*).

Figure 3. Basic schematic of parallel-driven LEDs



An easy and cost-effective way to design a constant current source to drive LEDs is to use a DC-DC converter, as shown in *Figure 4*. Since the voltage control loop of the device regulates the voltage at the FB pin, a constant current source can be obtained by simply connecting a resistor between this pin and GND. Application note AN1891 from STMicroelectronics provides helpful information for designing a similar application using monolithic DC-DC converters.

Figure 4. Basic schematic of a DC-DC converter driving LEDs



The main drawback of the circuit shown in *Figure 4* is the amount of wasted power on the sense resistor. This can affect the efficiency of the overall application, especially in cases where the voltage reference of the embedded error amplifier is not negligible compared to the voltage drop across the LEDs, or when high current devices are used.

The main objective of this document is to implement a more efficient current source by converting the voltage loop of a monolithic DC-DC converter into a current loop.

2 The L5973AD in LED driving applications

A good candidate within ST's monolithic DC-DC portfolio is the L5973AD. The device is an asynchronous buck regulator and belongs to the L597x family.

Table 1. Main monolithic devices within the L597x family

Device	V_{IN} range	f_{SW}	I_{OUT} DC	V_{OUT}	Features	Package
L5970D	4 V to 36 V	250 kHz	1 A	1.235 V to V_{IN}	V_{REF}, SYNCH, INH	SO-8
L5970AD	4 V to 36 V	500 kHz	1 A	1.235 V to V_{IN}	V_{REF}, SYNCH, INH	SO-8
L5973D	4 V to 36 V	250 kHz	2 A	1.235 V to V_{IN}	V_{REF}, SYNCH, INH	HSOP8
L5973AD	4 V to 36 V	500 kHz	1.5 A	1.235 V to V_{IN}	V_{REF}, SYNCH, INH	HSOP8

The reference for the embedded error amplifier of the devices listed in *Table 1* is 1.235 V, so the topology proposed in *Figure 4* can be improved by increasing the efficiency of the conversion in accordance with application requirements.

In addition to the high efficiency conversion requirement, more and more often customers look for smaller application size and lower cost and count of external components.

The purpose of this document is the implementation of an efficient and dimmable current source for LED driving developed with the L5973AD.

In *Section 2.1*, two resistors are used to implement a simple, helpful trick for decreasing the voltage drop across the sense resistor.

In *Section 2.2*, a general-purpose external operational amplifier is used to further increase the overall efficiency of the conversion. The TS321 selected (in a small SOT23-5 package) is one of the two embedded amplifiers composing the LM158 market standard.

In both cases the compensation network is designed for device operation without the output capacitor filter, to reduce the cost and the count of external components. The main consequence is a load current unfiltered from the ripple current: the high natural switching frequency (500 kHz) of the L5973AD helps keep the ripple current negligible in all operating conditions even compared to the minimum load current (350 mA) given an inductor value of 100 µH.

The maximum accuracy of the load current is finally provided considering the spread of the involved parameters at the end of each section.

2.1 Designing a high efficiency current source (topology 1)

The reference of the embedded error amplifier of the L597x family is 1.235 V.

The sense resistor value when the circuit proposed in *Figure 4* is used to implement a 350 mA current source is:

Equation 1

$$R_{SENSE} = \frac{V_{FB}}{I_{LED}} = \frac{1.235}{0.35} = 3.52\Omega$$

and the power losses across it are:

Equation 2

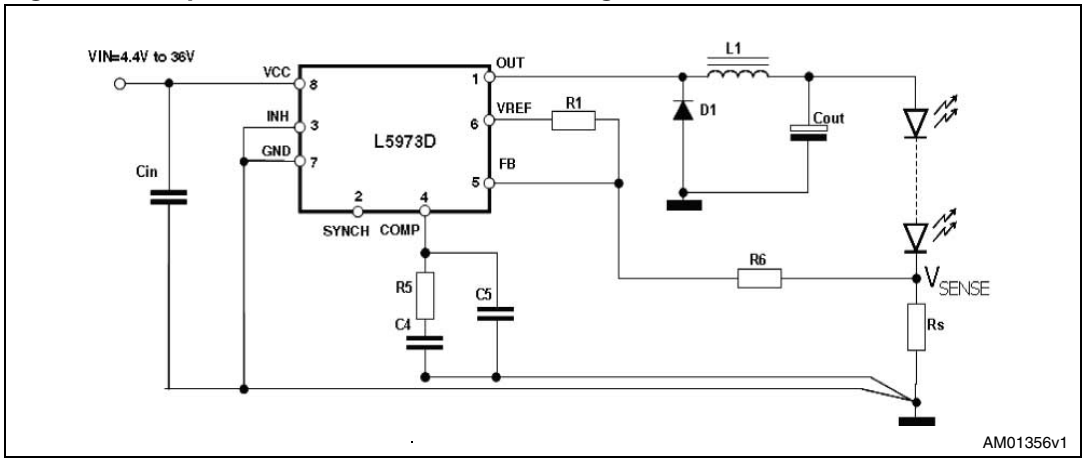
$$P_{LOSSES} = R_{SENSE} \cdot I_{LED}^{2} \cong 430mW$$

So if the current generator is powering a string composed of 1 W LEDs, the total efficiency of the conversion is affected by the sense resistor at a percentage of 43%. Obviously this circuit could be rendered acceptable by increasing the number of LEDs composing the string, but is, in any case, limited when the load is a single 3 W LED.

2.1.1 DC GAIN design

Figure 5 shows the guiding principle to implement an improved current generator using the L5973AD and two additional resistors.

Figure 5. Improved schematic of the current generator



R1 and R6 resistors are used to decrease the magnitude of the regulated voltage across the sense resistor. Applying the superimposition of the effects, the equation of the FB voltage can be written as:

Equation 3

$$V_{FB} = V_{REF} \cdot \frac{R_6}{R_1 + R_6} + V_S \cdot \frac{R_1}{R_1 + R_6}$$

so the regulated V_{SENSE} is:

Equation 4

$$V_S = V_{FB} - \frac{R_6}{R_1} \cdot (V_{REF} - V_{FB}) = 1.235 - \frac{R_6}{R_1} \cdot 2.065$$

The accuracy of the regulated current is mainly affected by the tolerance of the resistors R6, R1 and R_S.

If the selected sense resistor value is equal to R_S=1.5 Ω, the required voltage drop on the sense resistor to set 350 mA flowing through the LED string is 525 mV. The required resistor ratio is:

Equation 5

$$\frac{R_1}{R_6} = 2.9$$

Given R6 = 6.8 kΩ and R1 = 20 kΩ, the nominal LED current is 355 mA. The power wasted on the sense resistor is so decreased from 430 mW to:

Equation 6

$$P_{LOSSES} = R_{SENSE} \cdot I_{LED}^2 \cong 184mW$$

improving the efficiency of the conversion.

2.1.2 The dimming operation

The best way to dim an LED device is by PWM dimming performed on the current flowing through it. The device is powered with a constant current for minimal color shift, even when the amount of emitted light is decreased.

This requirement must be converted in the specifications for the dimmable current source. Devices specifically tailored for the LED market (see the LED7706 and LED7707 as examples) implement additional circuitry to meet these specifications and offer exceptional dimming performance.

The implementation of the dimming feature in a constant current generator developed with standard switching regulators can be tricky, as no dedicated circuitry is embedded in the device to provide this operation. As a consequence, the design of the compensation network must be a trade-off between the response to the small signal necessary for system stability and the large signal during the dimming operation.

The LC filter of the output stage filters the output voltage but the output capacitor value affects the dimming performance. In fact, even if the PWM input signal disables the current generator, the current flowing through the LED string drops to zero only when the voltage across the capacitor does not guarantee the minimum forward voltage across each LED.

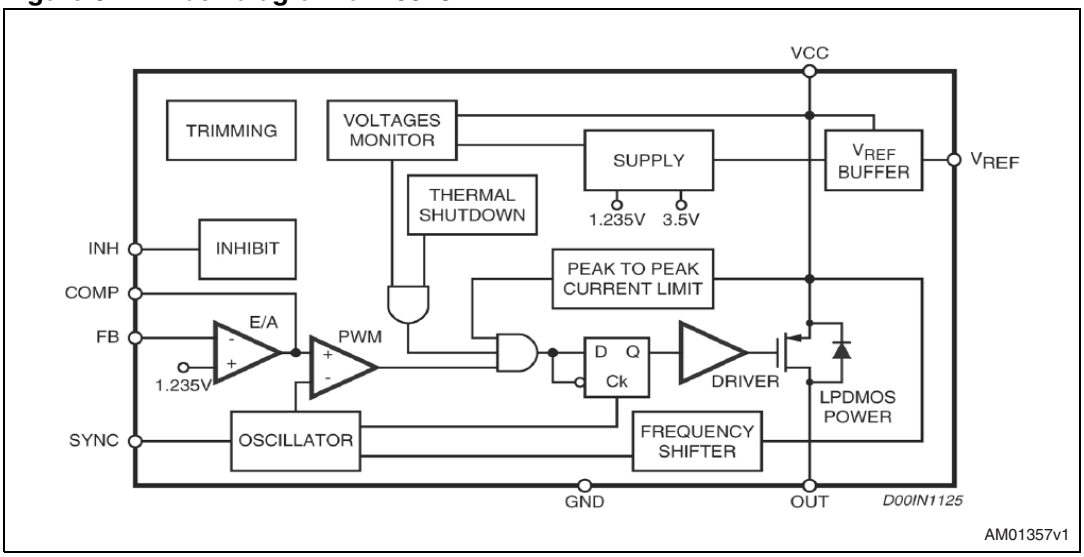
The L5973AD is an asynchronous device: the rectification of the inductor current is given by the external diode. The device is not capable of sinking current and so it can not quickly discharge the output capacitor to power off the emitting diodes.

As a consequence, a large output capacitor value better filters the current flowing in the LED from the current ripple, but significantly limits the dimming performance as it introduces additional delay in the falling edge of the LED current.

The current source schematic in *Figure 7* shows a negligible value for the output capacitor to achieve better performance in the dimming operation. The high switching frequency of the L5973AD helps to keep the unfiltered current ripple in the LED negligible compared to the DC current, so the color shift of the emitted light in all operating conditions can be considered negligible.

The L5973AD is based on a voltage mode control loop. Therefore, the duty ratio of the internal switch is obtained through a comparison between a sawtooth waveform (generated by an oscillator) and the output voltage of the error amplifier (see *Figure 6*). The embedded error amplifier is a transconductance type so its output stage delivers current to the compensation network.

Figure 6. Block diagram of L5973AD



In *Figure 7*, the output of the embedded transconductance error amplifier is clamped by switch Q1, in accordance with the PWM signal.

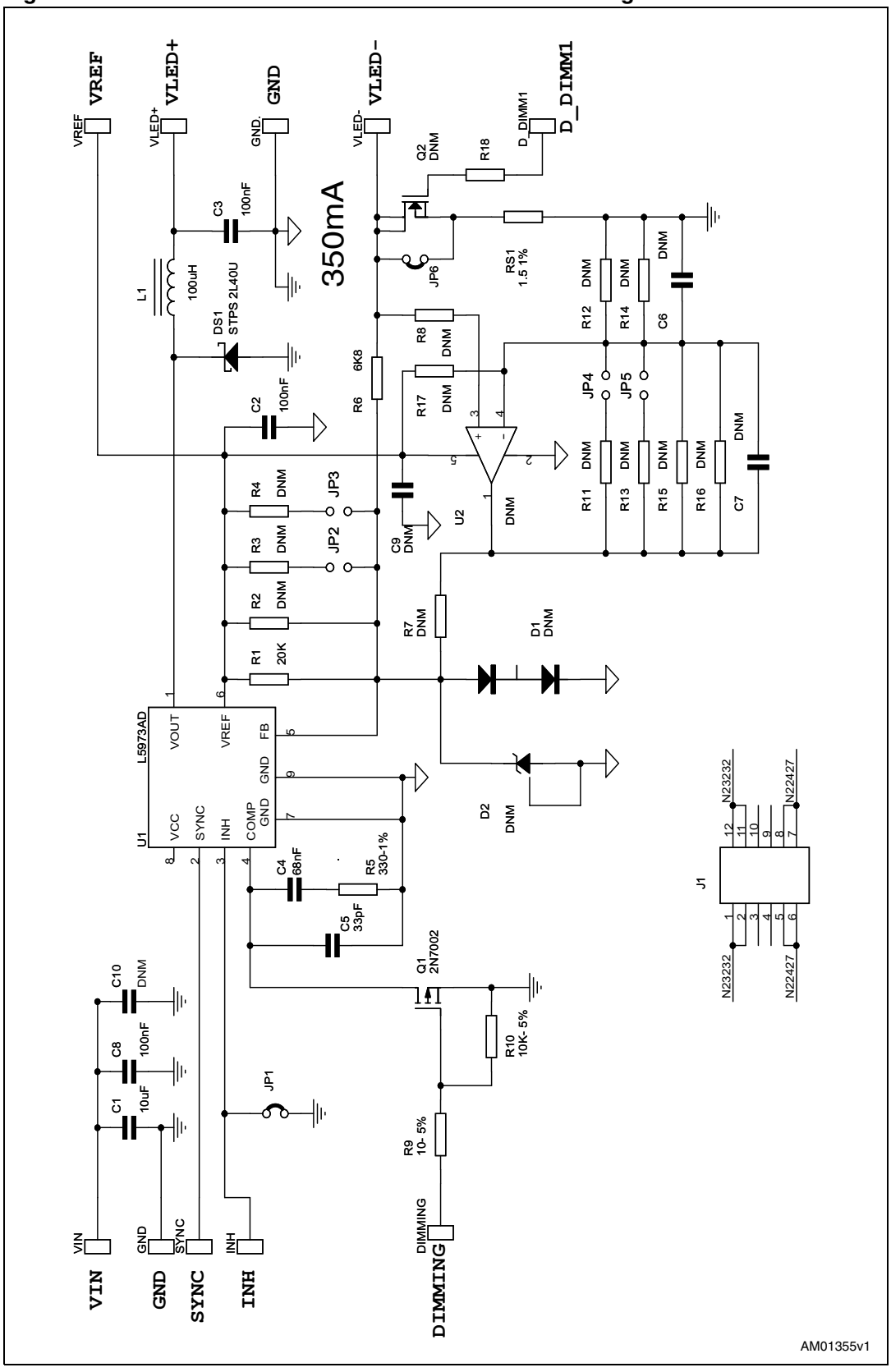
When switch Q1 is ON, the COMP pin is low (see *Figure 9*). Regardless of the FB input there is no intersection between the internal sawtooth waveform and the output of the error amplifier. The internal switch is thus disabled and the inductor current starts decreasing down to zero.

When the PWM signal disables the Q1 switch (see *Figure 10*), no current flows in the sense resistor RS, so the error amplifier is highly unbalanced and free to charge the compensation network composed of C4, C5 and R5. When the voltage of the COMP pin crosses the internal sawtooth ramp, the embedded switch is enabled: the current source starts charging the inductor and the rising edge phase of the LED begins.

The minimum voltage of the internal sawtooth waveform is about 1 V (see the voltage mode architecture in *Figure 8*) so there is a time delay between the disabling of the Q1 switch and the first pulse of the internal MOSFET. The delay is due to the time necessary to charge the compensation network to the minimum voltage to cross the internal ramp. This provides a shift between the duty cycle of the input PWM signal and the real PWM dimming performed on the load current.

Figure 9 and *Figure 10* show the dimming operation monitoring the input dimming signal and the LED current.

Figure 7. Schematic of the dimmable current source using L5973AD



The dimming performance of the circuit depends on the input voltage and number *n* of the LED composing the row. The higher the voltage applied on the inductor (VIN-n*V_{LED_FW}), the higher the rising time of the LED current given the inductor value.

Figure 8. Voltage mode architecture

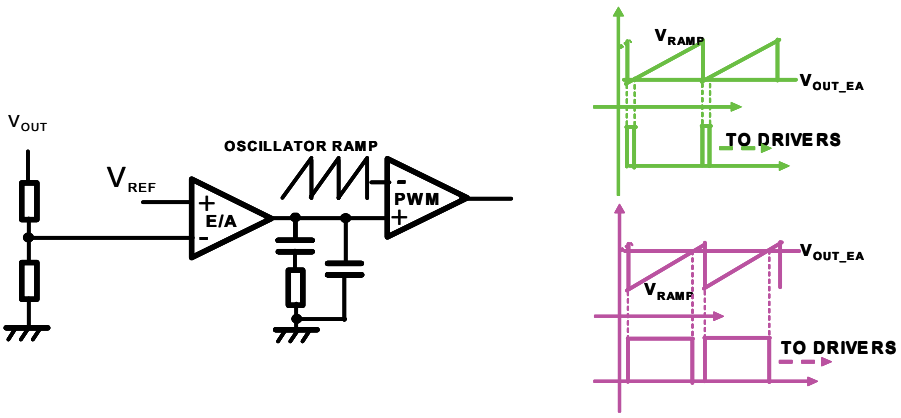


Figure 9. Q1 disables the switching activity clamping the COMP signal

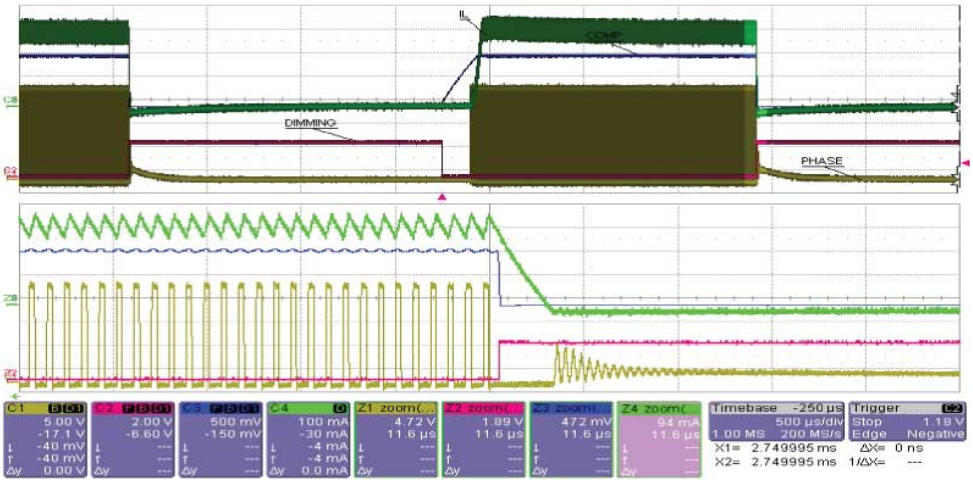
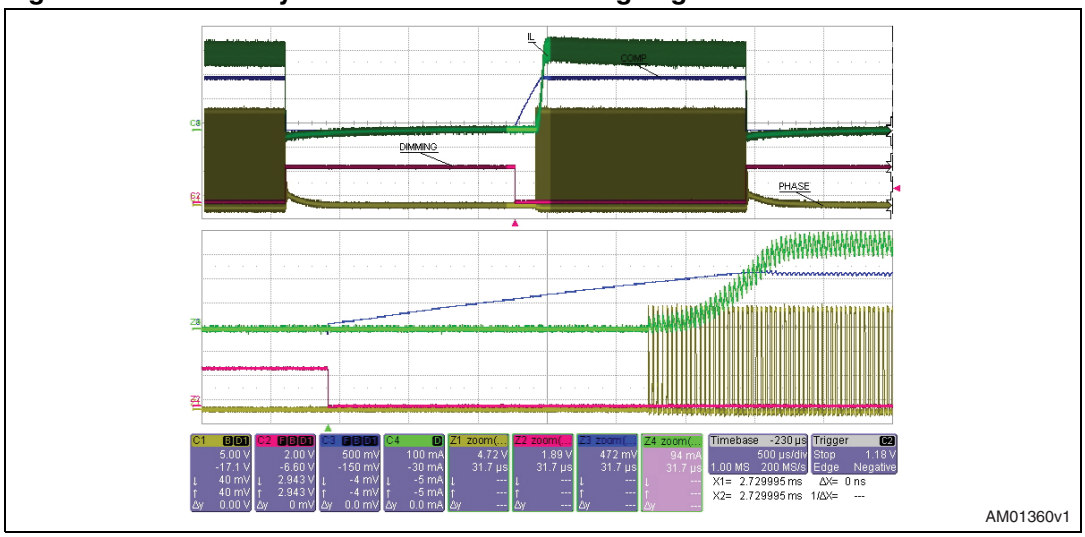
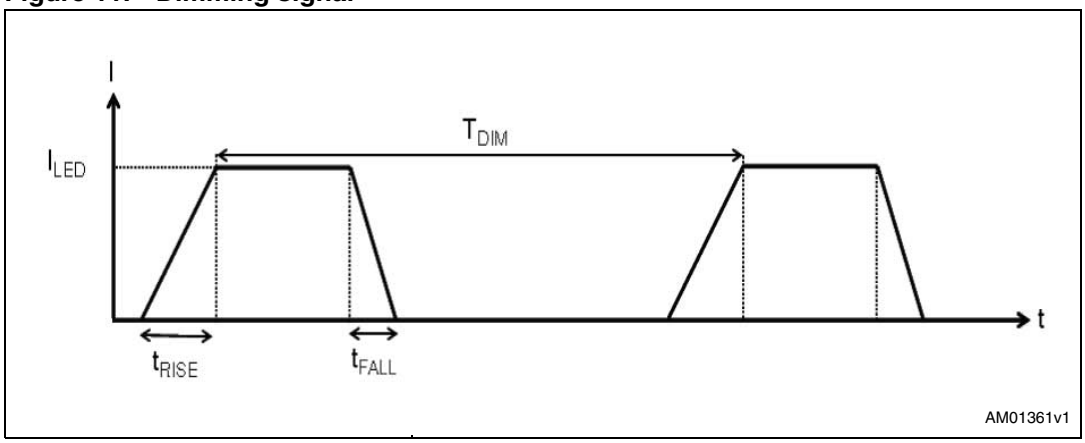


Figure 10. Time delay in the LED current leading edge



The minimum dimming duty cycle is determined based on the specification of the rising / falling time of the LED current referred to the dimming time and on the dimming frequency.

Figure 11. Dimming signal



From *Figure 9* and *10* (VIN = 18 V, string composed of two LEDs) the following data can be inferred:

Equation 7

$$\begin{cases} T_{RISE} = 40\mu s \\ T_{FALL} = 6\mu s \end{cases}$$

Considering a dimming frequency of 250 Hz, the minimum duty cycle of the PWM dimming satisfies the equation:

Equation 8

$$T_{RISE} + T_{FALL} = 0.2 \cdot T_{MIN\_PULSE} = 0.2 \cdot D_{MIN} \cdot T_{DIMMING}$$

so the minimum D is about 5%.

Relaxing the edge requirements or increasing the transient performance of the circuit, which depend on VIN and the number of LEDs composing the string and inductor value, a lower D can achieved.

2.1.3 Frequency compensation

The loop transfer function can be written as the product of meaningful terms.

Equation 9

$$G_{LOOP}(s) = G_{PWM}(f_{SW}) \cdot A_{OTA}(s) \cdot G_{PWR}(s) \cdot \alpha_{LED}(n_{LED})$$

where $G_{PWM}(fsw)$ is a specific parameter of the L5973AD and represents the gain of the PWM stage, AOTA(s) is the transfer function of the error amplifier block, GPWR(s) represents the power stage and αLED(nLED) is the partition of the output voltage directly applied to the FB pin.

The gain of the PWM stage $G_{PWM}(fsw)$ is:

Equation 10

$$G_{PWM}(f_{SW}) = \frac{1}{0.076} \cdot \frac{f_{SW}(kHz)}{250}$$

so it is 26.3 at a switching frequency of 500 kHz.

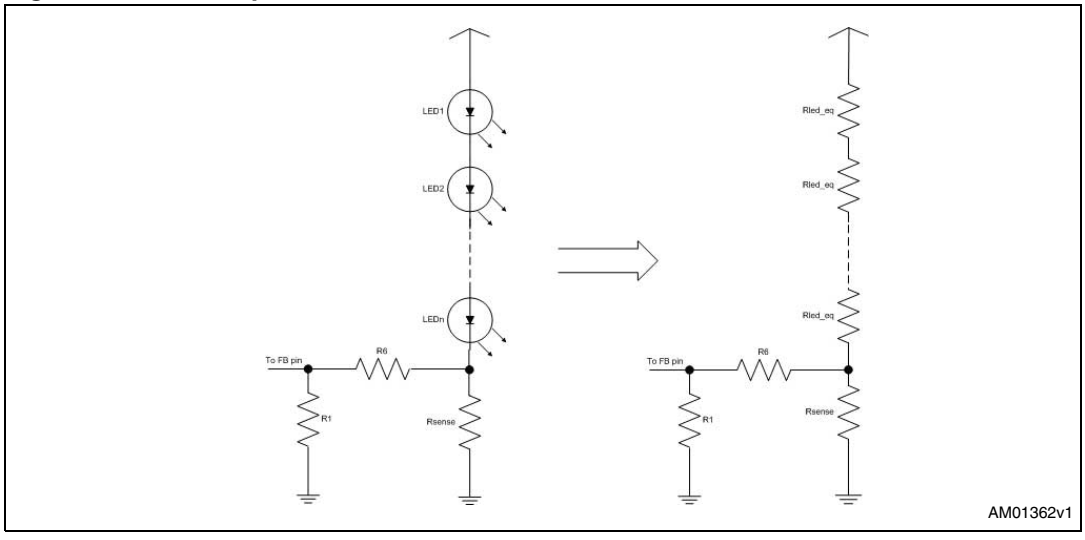
When the system has reached working conditions, the LEDs composing the row are biased and their equivalent circuit can be considered as a resistor for frequency << 1 MHz.

Typically, the manufacturer provides the typical equivalent dynamic resistance of the LED biased with different DC current. This parameter is useful to study the behavior of the system in small signal analysis. The equivalent dynamic resistance of the Luxeon III Star from Lumiled measured with different bias current level is reported below:

Equation 11

$$r_{LED} \begin{cases} 1.3\Omega & I_{LED} = 350mA \\ 0.9\Omega & I_{LED} = 700mA \end{cases}$$

Figure 12. Load equivalent circuit



As a consequence, the term $\alpha_{LED}(s)$ can be calculated as:

Equation 12

$$\alpha_{LED}(n_{LED}) = \frac{R_{SENSE}}{n_{LED} \cdot r_{LED} + R_{SENSE} // (R_1 + R_6)} \cdot \frac{R_1}{R_{SENSE} + R_1 + R_6}$$

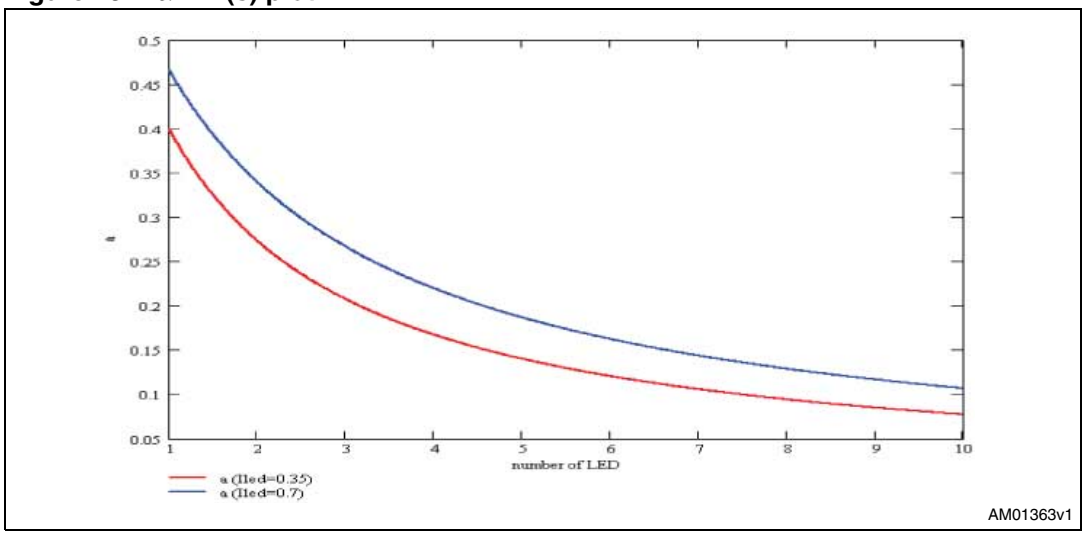
and considering R_{SENSE} << (R1+R6) the equation can be simplified as follows:

Equation 13

$$\alpha_{LED}(n_{LED}) \approx \frac{R_{SENSE}}{n_{LED} \cdot r_{LED} + R_{SENSE}} \cdot \frac{R_1}{R_1 + R_6}$$

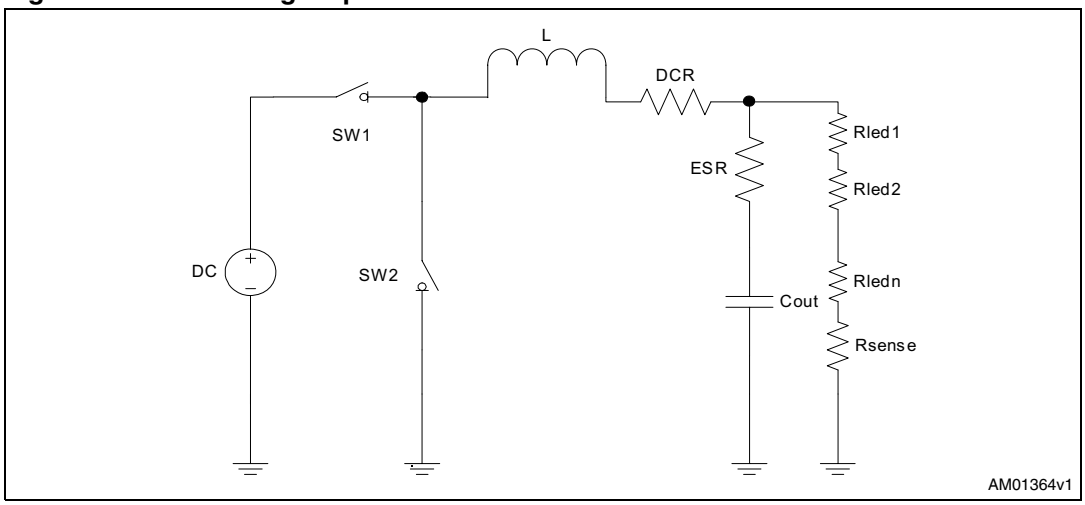
The term is plotted as a function of the LED composing the row and the biasing current, as shown in *Figure 13*.

Figure 13. αLED(s) plot



The power components, their stray contributions and the load constitute the equivalent circuit of the power stage shown in *Figure 14*.

Figure 14. Power stage equivalent circuit



The main contribution is given by the LC filter of the output stage which introduces a double pole in the transfer function of the control loop. The overall contribution to the small signal model can be written as:

Equation 14

$$G_{PWR}(s)= \frac{\dfrac{1}{\dfrac{1}{ESR+\dfrac{1}{s\cdot C_{OUT}}}+\dfrac{1}{n\_led\cdot rled\_eq+R_{sense}}}}{DCR+s\cdot L+\dfrac{1}{\dfrac{1}{ESR+\dfrac{1}{s\cdot C_{OUT}}}+\dfrac{1}{n\_led\cdot rled\_eq+R_{sense}}}}$$

Considering L=100 µH and COUT=100 nF (see *Figure 19*) the frequency of the double pole can be approximated to 50 kHz.

The equivalent circuit of the embedded transconductance error amplifier including the external compensation network is provided in *Figure 15*.

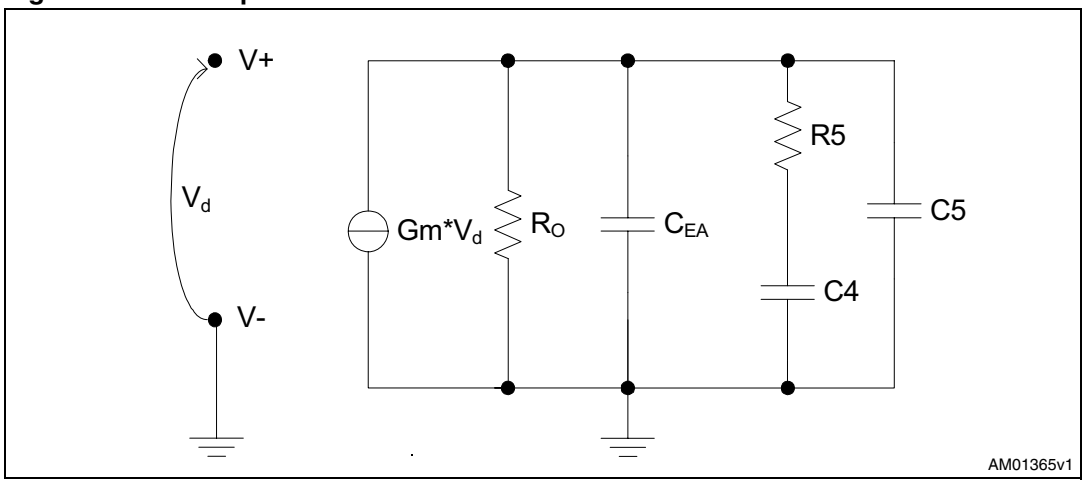
The embedded error amplifier is used to compensate the double pole contribution within the system bandwidth introducing a zero before its frequency; an additional pole outside the bandwidth is also introduced but typically its contribution to the phase margin can be ignored.

The transfer function of the equivalent circuit can be calculated as:

Equation 15

$$A_{OTA}(s)= G_m\cdot\frac{1}{\dfrac{1}{R_0}+s\cdot(C_{EA}+C_5)+\dfrac{1}{R_5+\dfrac{1}{s\cdot C_4}}}$$

Figure 15. OTA equivalent circuit



so the frequencies of the singularities are:

Equation 16

$$f_{ZERO} = \frac{1}{2 \cdot \pi \cdot R_5 \cdot C_4} = 7kHz$$

Equation 17

$$f_{POLE\_LF} = \frac{1}{2 \cdot \pi \cdot R_O \cdot C_4} = 2.9Hz \qquad f_{POLE\_HF} = \frac{1}{2 \cdot \pi \cdot R_5 \cdot (C_{EA} + C_5)} = 13MHz$$

where the values of the components related to the embedded error amplifier are: CEA=3 pF, GM=2.3 mS, R_O=0.8 MΩ.

The plots of magnitude and phase of the overall gain transfer loop of the system are provided in *Figure 16* and *17*.

Figure 16. Module plot

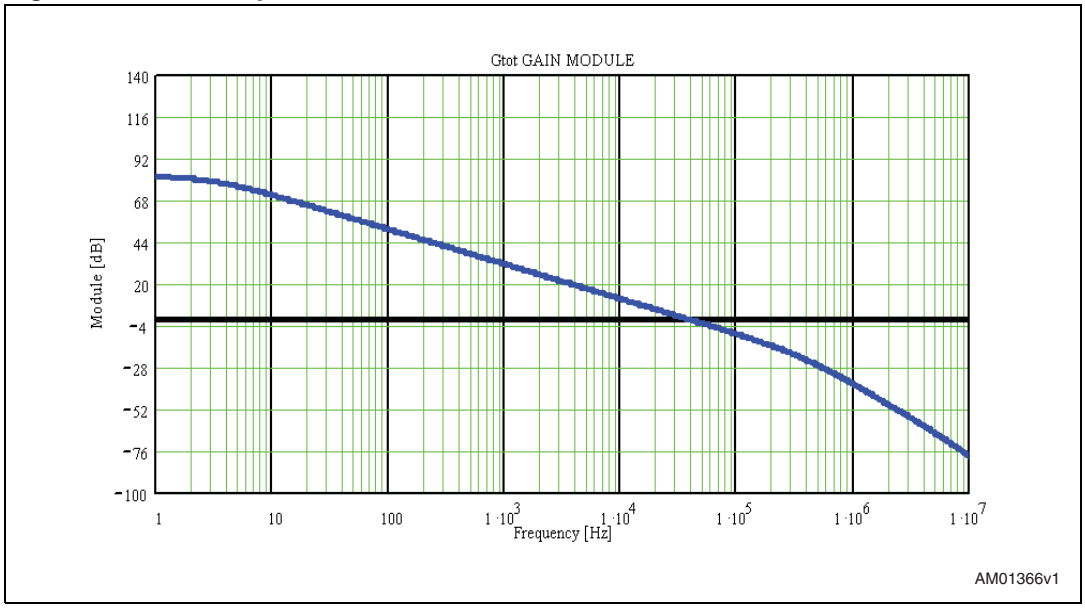
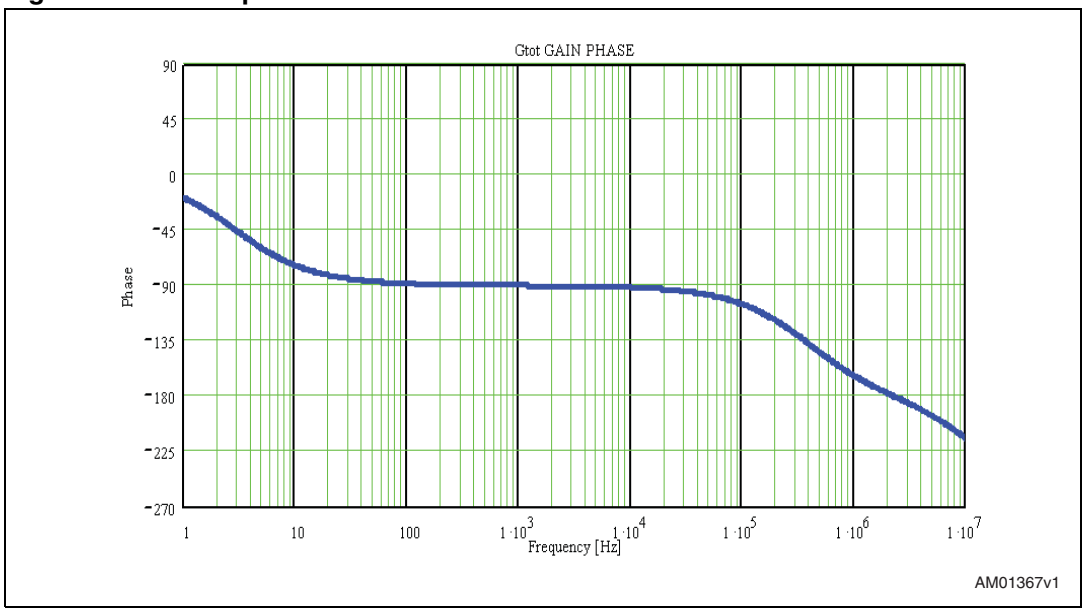


Figure 17. Phase plot



The cutoff frequency and the phase margin are:

Equation 18

$$F_C = 36kHz \qquad \zeta_M = 84^o$$

2.1.4 LED current accuracy

The purpose of this paragraph is to estimate each contribution which affects the accuracy of the DC current flowing through the load (R_6=6.8 kΩ, R1=20 kΩ, R_S=1.5 W, P_{LOSSES}= 184 mW).

The current flowing in the LED satisfies the equation:

Equation 19

$$I_{LED} \cdot R_{SENSE} = V_S = V_{FB} - \frac{R_6}{R_1} \cdot (V_{REF} - V_{FB})$$

The accuracy εL597x of the reference and feedback voltage of the embedded error amplifier is ± 1.2% (see the L5973AD device datasheet). The two parameters are based on the internal bandgap cell of the device, so the relative spread is minimized (they are in tracking).

The spread of the current flowing in the LED is expressed as:

Equation 20

$$I_{LED} = \frac{V_{FB} \cdot (1 \pm \varepsilon_{L597x}) - \frac{R_6 \cdot (1 \pm \varepsilon_{R_6})}{R_1 \cdot (1 \pm \varepsilon_{R_1})} \cdot (V_{REF} - V_{FB}) \cdot (1 \pm \varepsilon_{L597x})}{R_{SENSE} \cdot (1 \pm \varepsilon_{R_{SENSE}})}$$

which can be written as:

Equation 21

$$I_{LED} = \frac{\left(V_{FB} - \frac{R_6 \cdot (1 \pm \varepsilon_{R_6})}{R_1 \cdot (1 \pm \varepsilon_{R_1})} \cdot (V_{REF} - V_{FB})\right) \cdot (1 \pm \varepsilon_{L597x})}{R_{SENSE} \cdot (1 \pm \varepsilon_{R_{SENSE}})}$$

The accuracy of the selected components RS, R8 and R1 is 1%, so the overall positive and negative contributions in the worst case are estimated below:

Equation 22

$$I_{\varepsilon+} = \frac{\left(V_{FB} - \frac{R_6 \cdot (1 - \varepsilon_{R_6})}{R_1 \cdot (1 + \varepsilon_{R_1})} \cdot (V_{REF} - V_{FB})\right) \cdot (1 + \varepsilon_{L597x})}{R_{SENSE} \cdot (1 - \varepsilon_{R_{SENSE}})} \cong \frac{\left(1.235 - \frac{6.8}{20} \cdot \frac{0.99}{1.01} \cdot 2.065\right) \cdot 1.01}{1.5 \cdot 0.99} \cong 0.371\,A$$

Equation 23

$$I_{\varepsilon-} = \frac{\left(V_{FB} - \frac{R_6 \cdot (1 + \varepsilon_{R_6})}{R_1 \cdot (1 - \varepsilon_{R_1})} \cdot (V_{REF} - V_{FB})\right) \cdot (1 - \varepsilon_{L597x})}{R_{SENSE} \cdot (1 + \varepsilon_{R_{SENSE}})} \cong \frac{\left(1.235 - \frac{6.8}{20} \cdot \frac{1.01}{0.99} \cdot 2.065\right) \cdot 0.99}{1.5 \cdot 1.01} \cong 0.338\,A$$

and so the percentage shift is:

Equation 24

$$I_{\varepsilon+}(\%) = \frac{I_{\varepsilon+} - I_{LED}}{I_{LED}} \cdot 100 \cong \frac{0.371\,A - 0.355\,A}{0.355\,A} \cdot 100 \cong +4.5\%$$

Equation 25

$$I_{\varepsilon-}(\%) = \frac{I_{\varepsilon-} - I_{LED}}{I_{LED}} \cdot 100 \cong \frac{0.338\,A - 0.355\,A}{0.355\,A} \cdot 100 \cong -4.78\%$$

so the overall spread of the LED current is:

Equation 26

$$I_{SPREAD}(\%) = I_{\varepsilon+}(\%) - I_{\varepsilon-}(\%) = 9.28\%$$

2.2 Designing a high efficiency current source (topology 2)

The purpose of this section is to improve the topology presented in *Section 2.1*, reducing the power losses on the sense resistor to obtain better efficiency of the conversion.

This is achieved with the use of a few external components to implement a gain block placed between the sense resistor and the inverting input of the embedded error amplifier in order to amplify the DC drop across the sense resistor.

A general-purpose external operational amplifier in non inverting topology implements the DC gain block. The selected TS321 (small SOT23-5 package) is one of the two embedded amplifiers composing the LM158 market standard.

The compensation network is designed for device operation without an output capacitor filter to reduce the count and cost of external components.

The main consequence is a load current unfiltered from the ripple current: the high natural switching frequency (500 kHz) of the L5973AD helps keep the ripple current negligible in all operating conditions even when compared to the minimum load current (350 mA), given an inductor value of 100 µH.

The maximum accuracy of the load current is finally provided considering the spread of the involved parameters.

2.2.1 DC GAIN design

The basic schematic of the enhanced dimmable current generator is shown in *Figure 18*.

Figure 18. Basic schematic of the current source

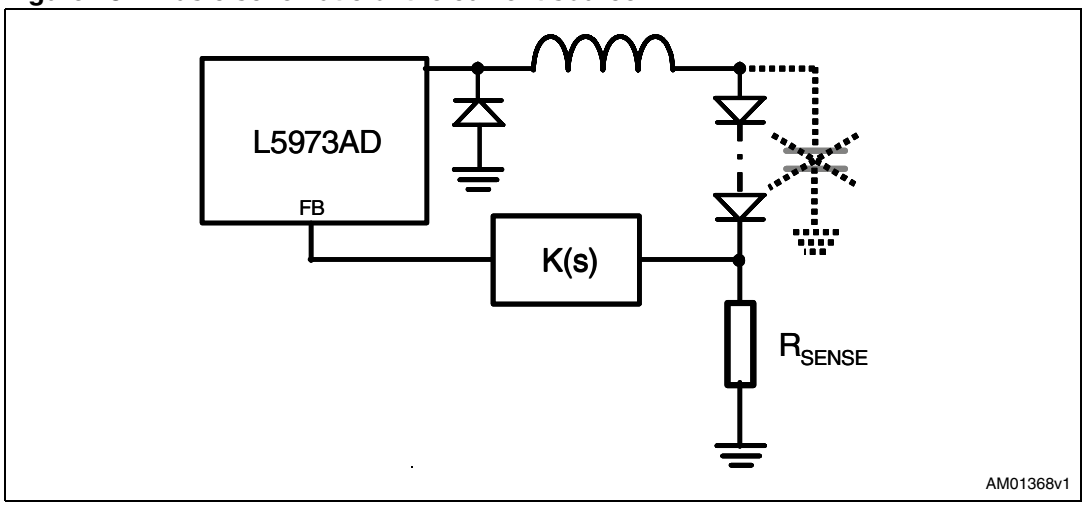
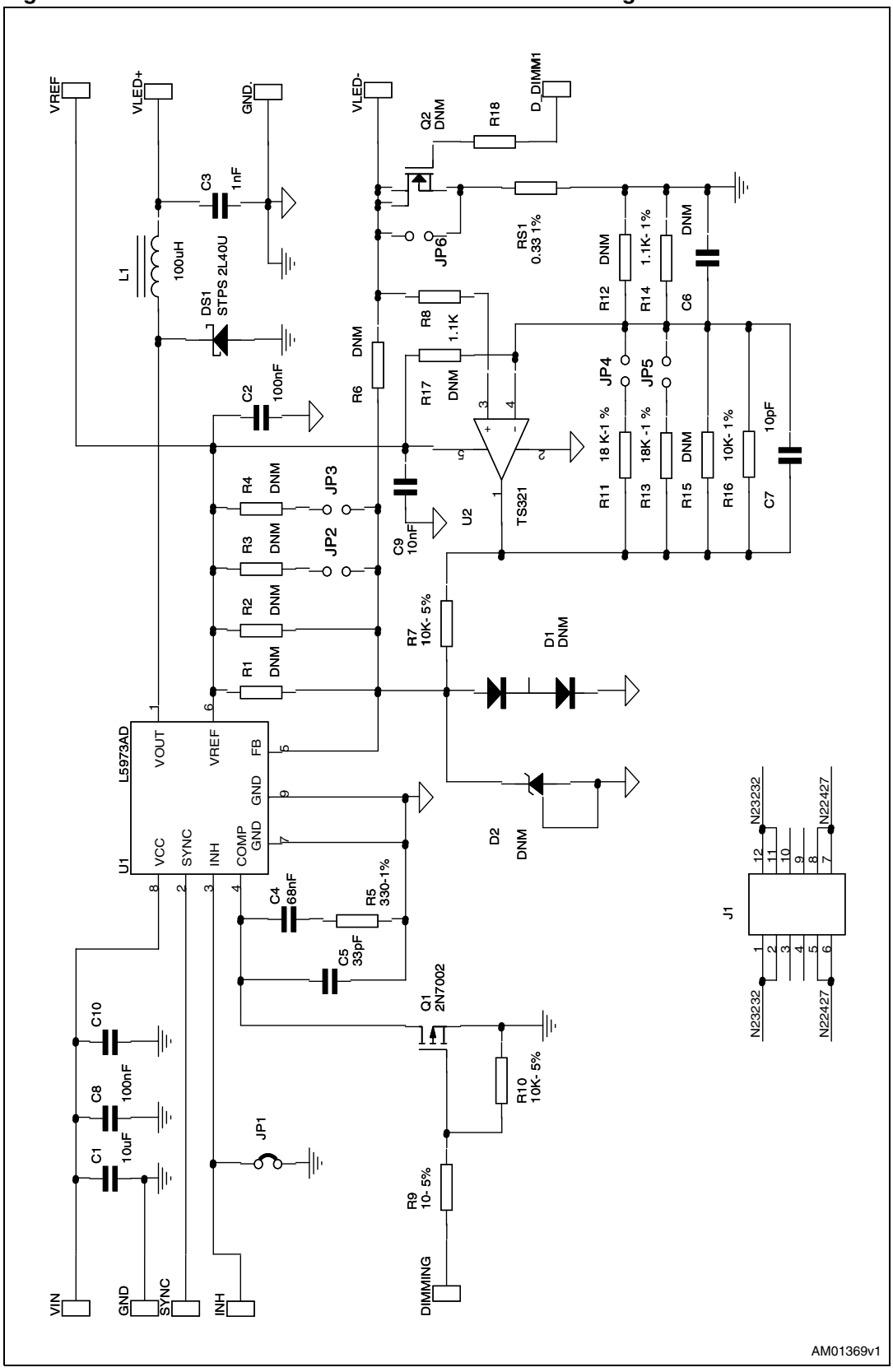


Figure 19. Schematic of the dimmable current source using L5973AD



The gain block K(s) amplifies the voltage sensed on the resistor and thus decreases the power lost across it. Its frequency behavior can also be useful to compensate the loop function, introducing a pole or a zero if needed (see *Figure 19*).

The K(s) is implemented through an operational amplifier working in a non inverting configuration.

In the schematic shown in *Figure 19*, the gain is

Equation 27

$$K(s) = \left(1 + \frac{R15//R16//R11//R13}{R14//R12}\right)$$

so leaving jp4 and jp5 open K(0)≈10.01, otherwise closing both jumper K(0)≈5.7.

Considering the R_{SENSE}=0.33 Ω, the regulated current is:

Equation 28

$$\begin{cases} I_{LED1} = \dfrac{V_{FB}}{K_{JP4\ OPEN,\ JP5\ OPEN}(0) \cdot R_{SENSE}} \cong \dfrac{1.235}{10.01 \cdot 0.33} \cong 375\ mA \\ I_{LED2} = \dfrac{V_{FB}}{K_{JP4\ CLOSE,\ JP5\ CLOSE}(0) \cdot R_{SENSE}} \cong \dfrac{1.235}{5.3 \cdot 0.33} \cong 706\ mA \end{cases}$$

and the power lost across R_{SENSE} is:

Equation 29

$$\begin{cases} P_{LOSS\ 1} = R_{SENSE} \cdot (I_{LED})^2 \cong 46.4\ mW \\ P_{LOSS\ 2} = R_{SENSE} \cdot (I_{LED})^2 \cong 142\ mW \end{cases}$$

It can be considered negligible when compared to the amount of power delivered to the load.

2.2.2 The dimming operation

The dimming operation is implemented as previously described in *Section 2.1.2*: switch Q1 clamps the output of the error amplifier to disable the switching activity.

Figure 20 and *21* show the dimming operation of the schematic in *Figure 19*, monitoring the input dimming signal and the LED current.

Figure 20. Q1 disables the switching activity by clamping the COMP signal

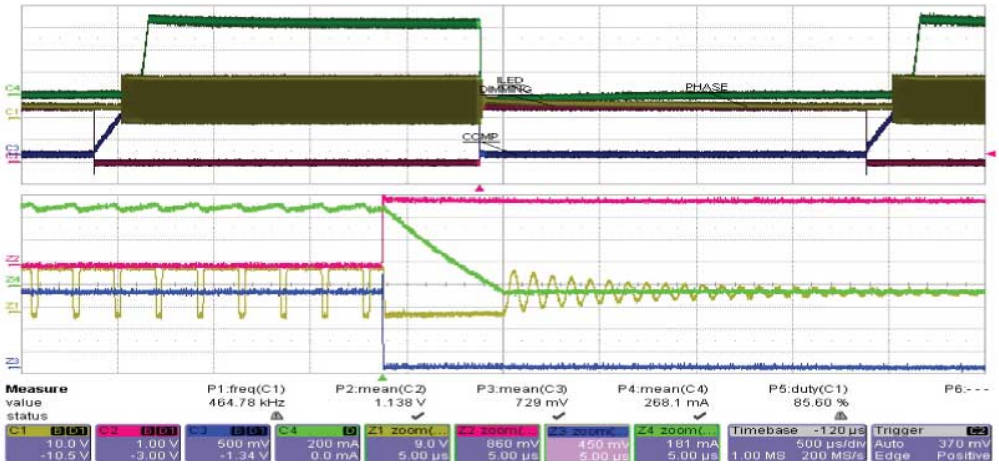
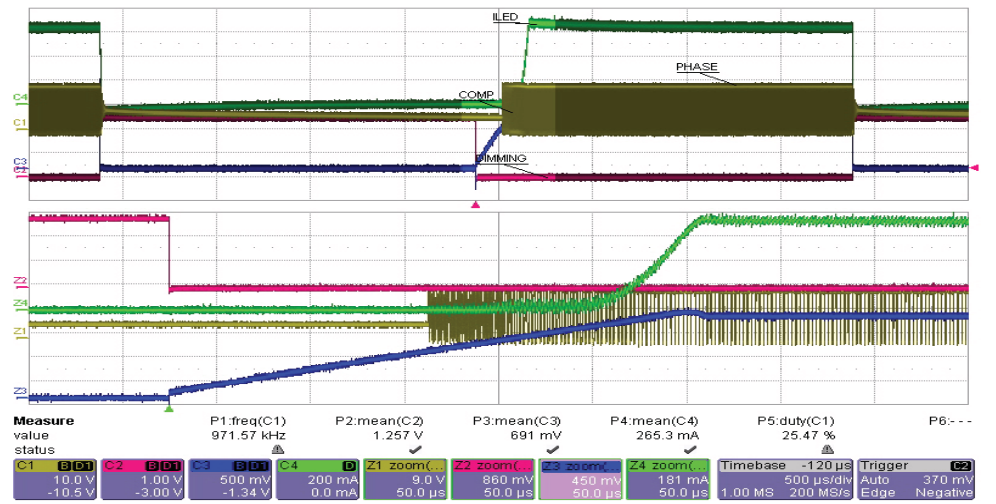


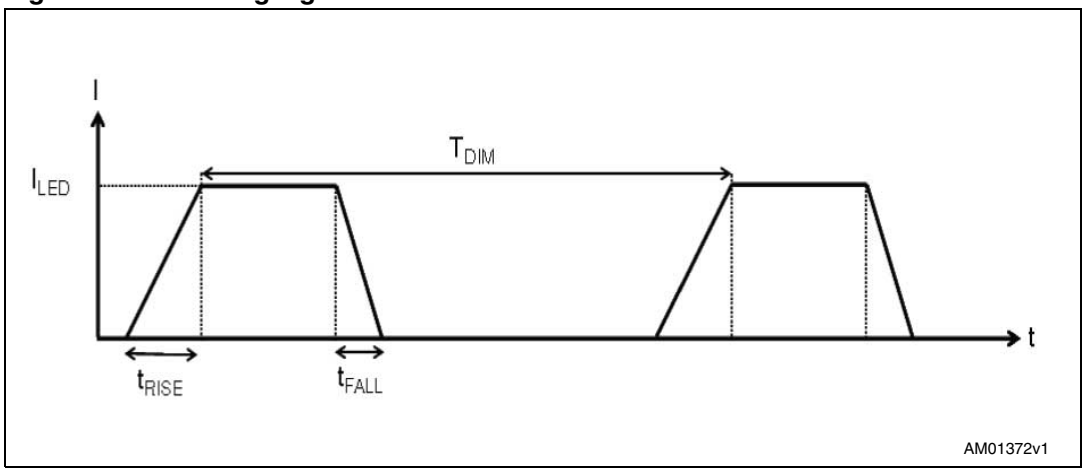
Figure 21. Time delay in the LED current leading edge



The dimming performance of the circuit depends on the input voltage and number *n* of the LED composing the row. The higher the voltage applied on the inductor (VIN-n*V_{LED_FW}) the higher the rising time of the LED current given the inductor value.

The minimum dimming duty cycle is determined based on the specification of the rising / falling time of the LED current referred to the dimming time and on the dimming frequency.

Figure 22. Dimming signal



From *Figure 20* and *21* (VIN = 18 V, string composed of two LEDs) the following data can be inferred:

Equation 30

$$\begin{cases} T_{RISE} = 40\mu s \\ T_{FALL} = 6\mu s \end{cases}$$

Considering a dimming frequency of 250 Hz, the minimum duty cycle of the PWM dimming satisfies the equation:

Equation 31

$$T_{RISE} + T_{FALL} = 0.2 \cdot T_{MIN\_PULSE} = 0.2 \cdot D_{MIN} \cdot T_{DIMMING}$$

so the minimum D is about 5%.

By relaxing the edge requirements or increasing the transient performance of the circuit, which depend on VIN and the number of LED composing the string and inductor value, a lower D can be achieved.

2.2.3 Frequency compensation

Most of the theory explained in *Section 2.1.3 on page 13* is still valid for the circuit in *Figure 19*. The equation of the loop transfer function is:

Equation 32

$$G_{LOOP}(s) = G_{PWM}(f_{SW}) \cdot K(s) \cdot A_{OTA}(s) \cdot G_{PWR}(s) \cdot \alpha_{LED}(n_{LED})$$

where the terms G_{PWM}, A_{OTA} and G_{PWM} are already known.

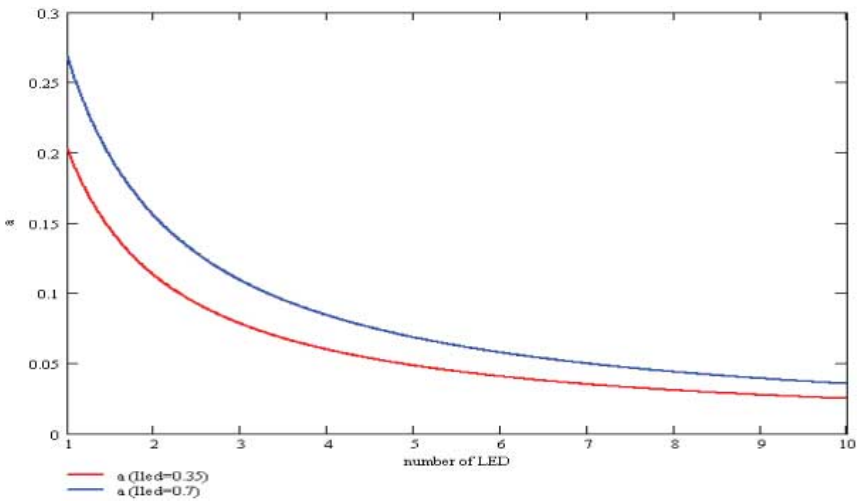
Here, the term αLED(s) is slightly different and can be calculated as:

Equation 33

$$\alpha_{LED}(n_{LED}) = \frac{R_{SENSE}}{n_{LED} \cdot r_{LED} + R_{SENSE}}$$

and it is plotted in *Figure 24*.

Figure 23. αLED(s) plot



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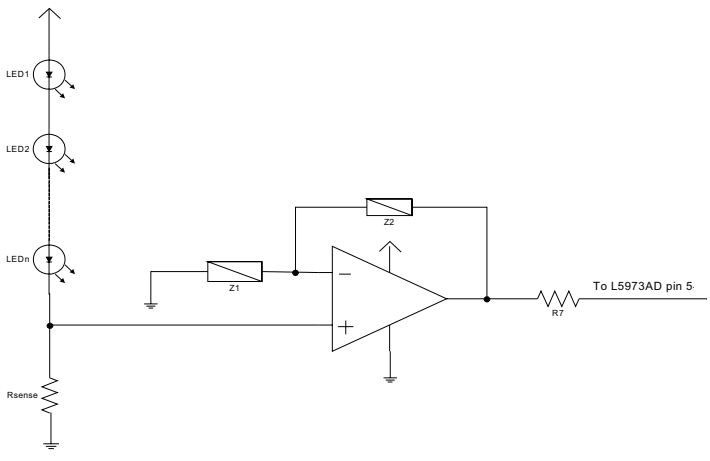
K(s) represents the transfer function of the block implemented through the external amplifier (see *Figure 24*). The external error amplifier bandwidth is 0.8 MHz, so the correction term of the ideal gain is introduced into the calculations to obtain a better analytical description of the real transfer function of the block.

Equation 34

$$K(s) = \frac{1 + \frac{Z_2(s)}{Z_1(s)}}{1 - \frac{1}{G_{loop\_EA}(s)}} = \frac{1 + \frac{Z_2(s)}{Z_1(s)}}{1 - \left(\frac{Z_1(s) + Z_2(s)}{A_{EA}(s)} \cdot \frac{1}{Z_1(s)}\right)}$$

Figure 24. Equivalent circuit of block K(s)



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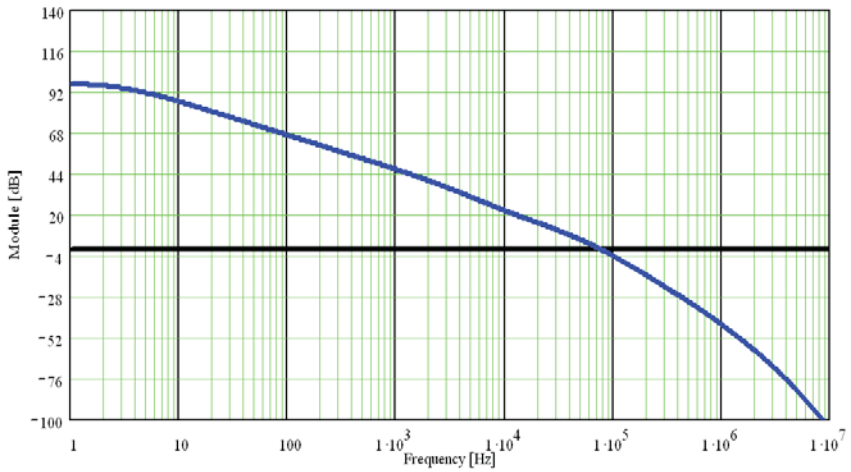
where:

Equation 35

$$Z_1(s) = \frac{1}{s \cdot C_6 + \frac{1}{R_{14}}} \qquad Z_2(s) = \frac{1}{s \cdot C_7 + \frac{1}{R_{16}}}$$

Considering L=100 µH and C_{OUT}=100 nF (see *Figure 19*), the frequency of the double pole can be approximated to 50 kHz.

Figure 25. Module plot

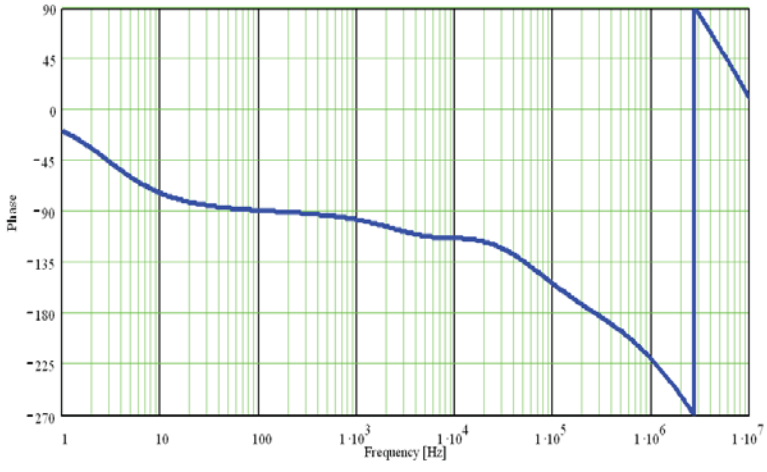


The cutoff frequency and the phase margin are:

Equation 36

$$F_C = 73kHz \qquad \zeta_M = 35^o$$

Figure 26. Phase plot



2.2.4 LED current accuracy

The reference of the embedded error amplifier is 1.235 V ± 1.2% (see the L5973AD device datasheet).

The current flowing through the LED satisfies the equation:

Equation 37

$$I_{LED} \cdot R_{SENSE} \cdot \left(1 + \frac{R_{16}}{R_{14}}\right) = V_{FB}$$

so considering R_{14}=1.1 kΩ, R_{16}=10 kΩ, R_{SENSE}=330 mW (P_{LOSSES}=46.4 mW) the nominal regulated current is:

Equation 38

$$I_{LED} = \frac{V_{FB}}{R_{SENSE} \cdot \left(1 + \frac{R_{16}}{R_{14}}\right)} = \frac{1.235}{330m\Omega \cdot \left(1 + \frac{10}{1.1}\right)} \cong 0.375A$$

The designed DC gain of the K(s) clock equal to:

Equation 39

$$R_{SENSE} \cdot \left(1 + \frac{R_{16}}{R_{14}}\right) \approx 3.3033$$

makes negligible the contribution to the overall LED accuracy introduced by the voltage offset of the embedded OTA compared to the one introduced by the external error amplifier.

The datasheet of the TS321 reports a maximum input voltage offset of ±5 mV (typical value is 0.5 mV) and a maximum bias current of ±50 nA.

The resistor R_8=1.1 kΩ compensates the contribution of R14//R15 ≈ 1.1 kΩ, thus minimizing the error introduced by the bias current, which can be disregarded.

The maximum voltage offset in relation to the nominal drop across the sense resistor is:

Equation 40

$$I_{\varepsilon_{OFFSET}}(\%) = \frac{V_{OFFSET}}{R_{SENSE} \cdot I_{LED}} \cdot 100 = \frac{\pm 5mV}{330m\Omega \cdot 375mA} \cdot 100 = \pm 4\%$$

The typical loop gain of the TS321 is 85 dB, so its magnitude allows the disregard of the error e given in the DC gain set with the resistor R_{14}, R_{16}.

Finally, the spread of the value of the external component affect the LED current. The accuracy of the selected components RS1, R_{14}, R_{16} is 1%, so the overall positive and negative contributions in the worst case are estimated below:

Equation 41

$$I_{\varepsilon+} = \frac{V_{FB} \cdot (1 + \varepsilon_{FB\_OTA})}{R_{SENSE} \cdot (1 - \varepsilon_{SENSE}) \cdot \left(1 + \frac{R_{16} \cdot (1 - \varepsilon_{16})}{R_{14} \cdot (1 + \varepsilon_{14})}\right)} \cong \frac{1.25}{326.7m\Omega \cdot 9.9108} \cong 0.386A$$

Equation 42

$$I_{\varepsilon-} = \frac{V_{FB} \cdot (1 - \varepsilon_{FB\_OTA})}{R_{SENSE} \cdot (1 + \varepsilon_{SENSE}) \cdot \left(1 + \frac{R_{16} \cdot (1 + \varepsilon_{16})}{R_{14} \cdot (1 - \varepsilon_{14})}\right)} \cong \frac{1.22}{333.3m\Omega \cdot 10.27} \cong 0.356A$$

and so the percentage shift is:

Equation 43

$$I_{\varepsilon+}(\%) = \frac{I_{\varepsilon+} - I_{LED}}{I_{LED}} \cdot 100 \cong \frac{0.386A - 0.375A}{0.375A} \cdot 100 \cong +2.93\%$$

Equation 44

$$I_{\varepsilon-}(\%) = \frac{I_{\varepsilon-} - I_{LED}}{I_{LED}} \cdot 100 \cong \frac{0.356A - 0.375A}{0.375A} \cdot 100 \cong -5.06\%$$

Finally, considering the contribution given by the offset of the LM351:

Equation 45

$$I_{\varepsilon-_{LED}}(\%) = I_{\varepsilon-}(\%) - I_{\varepsilon_{OFFSET}}(\%) \cong -9.06\%$$

Equation 46

$$I_{\varepsilon-_{LED}}(\%) = I_{\varepsilon-}(\%) - I_{\varepsilon_{OFFSET}}(\%) \cong -9.06\%$$

so the overall spread of the LED current is:

Equation 47

$$I_{SPREAD}(\%) = I_{\varepsilon+}(\%) - I_{\varepsilon-}(\%) = 15.99\%$$

2.3 Conclusions

This paragraph highlights the benefits and limitations of the two circuit topologies in terms of spread of the regulated LEDs in different operating conditions.

Given the voltage drop on the sense resistor, the efficiency of the conversion depends on the number of LEDs as the output power increases.

Equation 48

$$\eta = \frac{P_{LED}}{P_{LED} + R_{SENSE} \cdot (I_{LED})^2}$$

Figure 27 shows the efficiency of an ideal current generator considering only the loss across the sense resistor. It can be inferred that, when the objective of the design is to reach a certain minimum efficiency of the conversion, higher losses on the sense resistor could be accepted by increasing the number of the LEDs in the string.

Figure 27. Maximum efficiency vs. voltage drop (I_{LED}=350 mA)

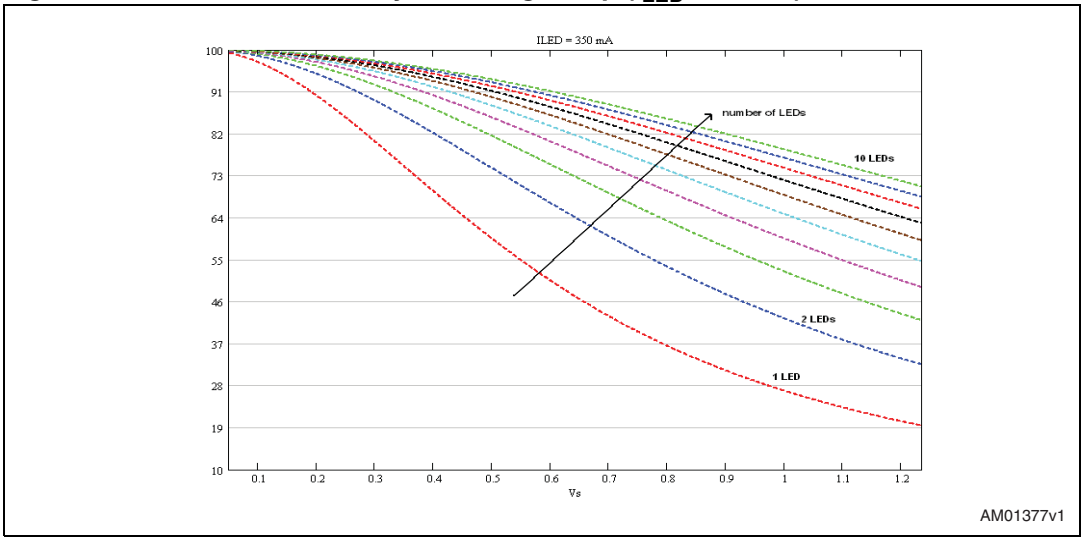


Figure 28 shows the power losses across the resistor:

Equation 49

$$P_{LOSSES} = R_{SENSE} \cdot (I_{LED})^2$$

Figure 28. Power losses across the sense resistor (I_{LED}=350 mA)

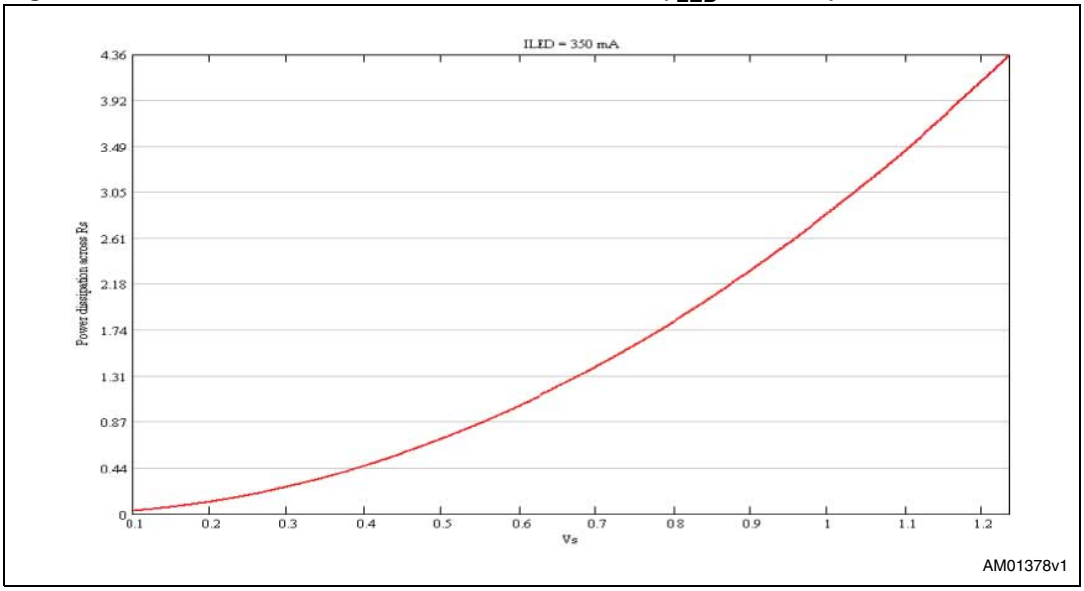


Figure 29 compares the spread of the LED current when implementing the different topologies described in the*Section 2.1* and *2.2* as a function of the voltage across RS and using the same calculations provided in *Section 2.1.4* and *2.1.4*.

Figure 29. Spread of the LED current vs. voltage drop (I_{LED}=350 mA)

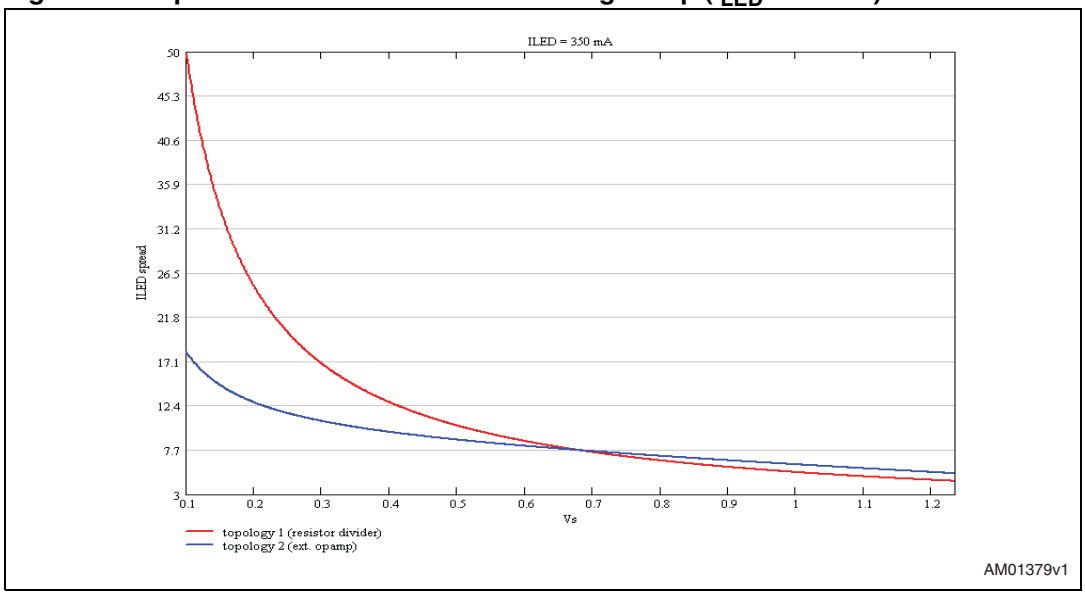


Figure 27 and *28* are useful to choose the required voltage sense to satisfy the efficiency specification. From *Figure 29*, it follows that the circuit topology using the external operational amplifier becomes attractive in terms of parameter spread when the sense voltage is lower than 650 mV (LED current is 350 mA). The trade-off between required current accuracy and efficiency determines the circuit topology to be used in the design. As discussed in *Section 2.1.4* (topology 2), the accuracy of the current is mainly affected by the voltage offset of the external error amplifier: better results can be achieved by selecting an error amplifier with a limited offset (i.e. trimmed). *Figure 29* shows the same data provided in *Figure 28*, but considering a maximum voltage offset of ±0.5 mV (which is also the typical offset of the TS321 device): the spread of the load current drops from 10.7% (*Figure 29*) to 7.7% (*Figure 28*), when V_{SENSE}=300 mV. As a consequence, selecting an external error amplifier with a better offset voltage decreases the intersection point of the two traces in *Figure 29*, making topology II more convenient than topology I, in terms of current accuracy, for a wider V_{SENSE} range.

Figure 30. Power losses across the sense resistor (I_{LED}=350 mA)

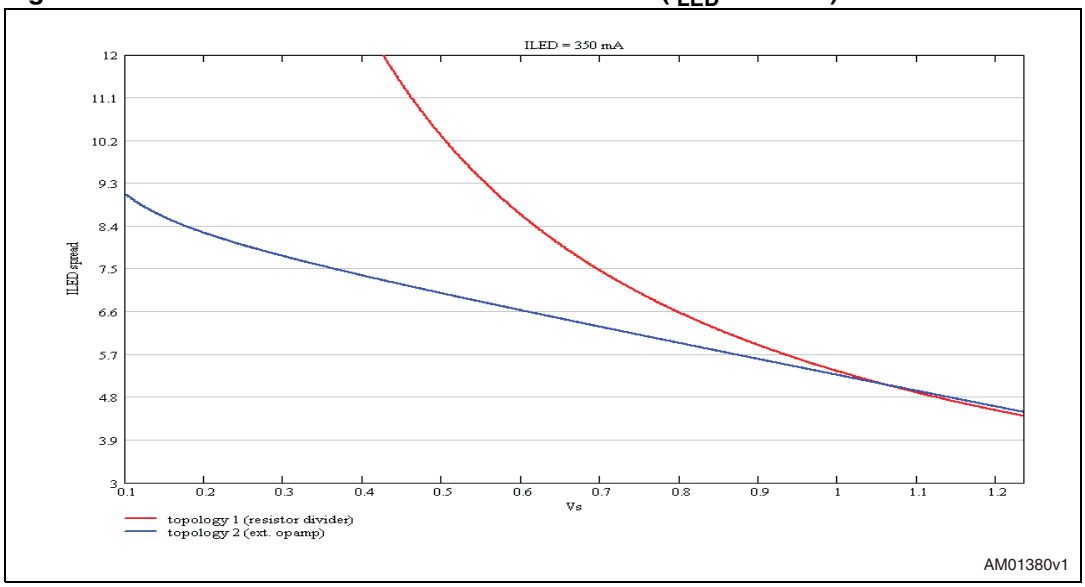


Figure 31, *32* and *33* give the same data when driving 700 mA LEDs.

Figure 31. Maximum efficiency vs. voltage drop (I_{LED}=700 mA)

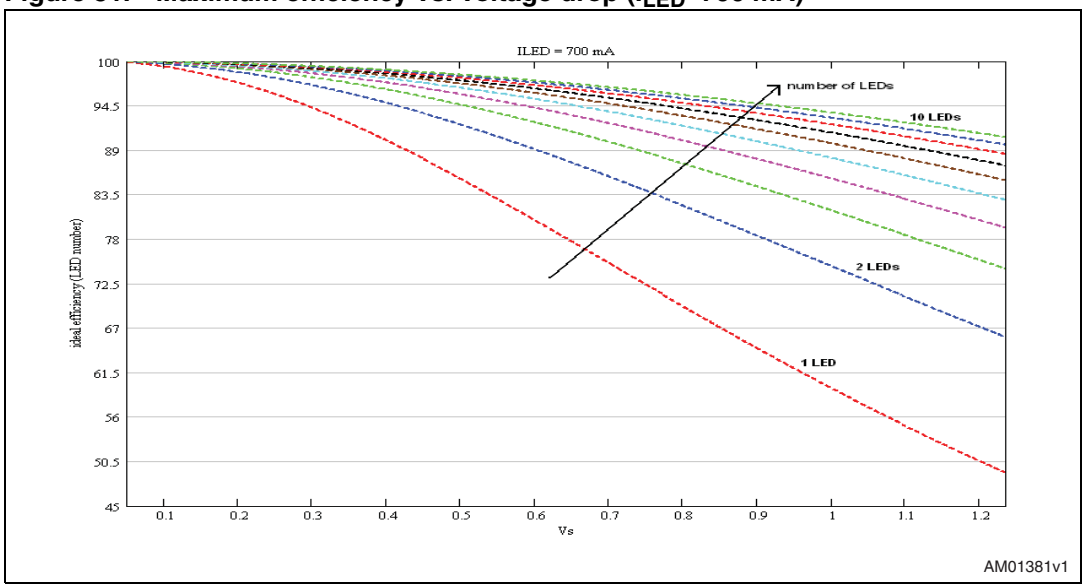


Figure 32. Power losses across the sense resistor (I_{LED}=700 mA)

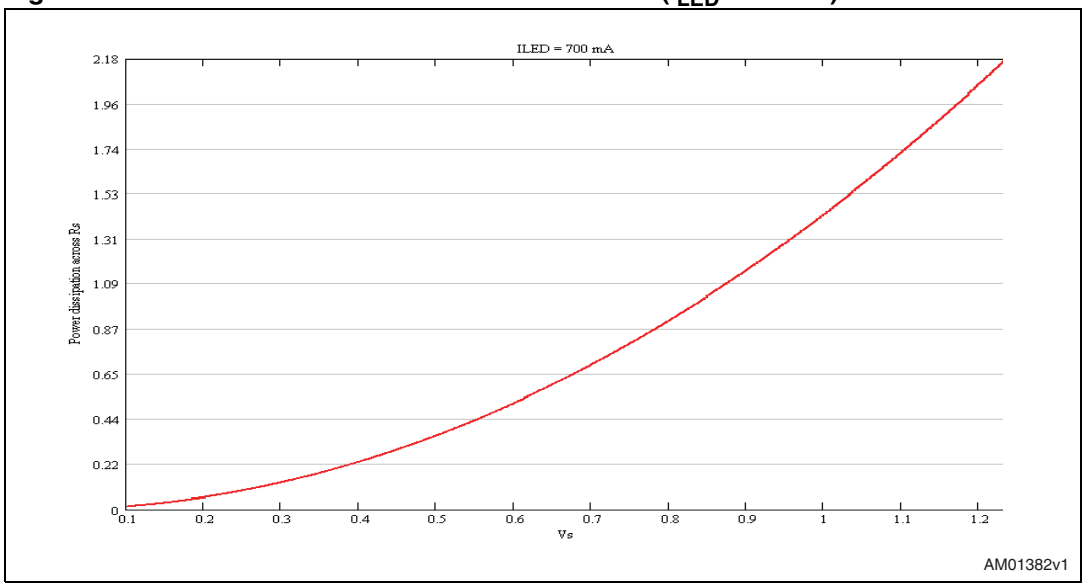
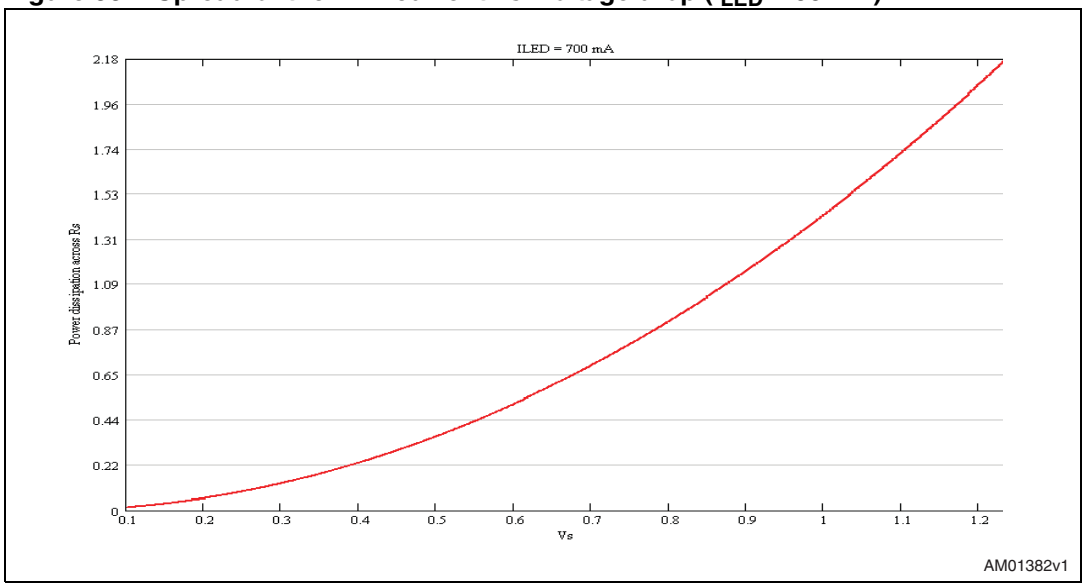


Figure 33. Spread of the LED current vs. voltage drop (I_{LED}=700 mA)



3 Revision history

Table 2. Document revision history

Date	Revision	Changes
11-Aug-2009	1	Initial release