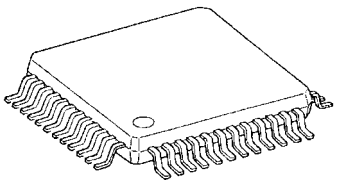
TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

T6N71B

RFID (Radio Frequency tag) Reader and Writer Interface LSI

Features



LQFP48-P-0707-0.50C

Weight: 384 mg (typ.)

- RFID reader and writer interface LSI embedding analog and data processing
- Receive signal demodulation circuit stabilized by a built-in digital PLL. The antenna, capacitors, band pass filter, and other features are external, therefore selectable.
- Built-in modulation circuit for transmit carrier
- Supports RFID LSI (TOSHIBA general-purpose T6N38/46/78).
- Conforms to ISO14443 (type B) and ISO13506.
- Supplied as bare chip or LQFP48
- Clock sync serial interface/start-stop sync serial interface for interfacing with CPU
- Sync circuit (crossed line protection) in case of multiple readers in simultaneous operation
- Transmit/receive control by register
- Built-in oscillator circuit
- Power supply voltage detection circuit for battery use

1. Product Outline

1.1 Product Name: T6N71B

1.2 Structure: CMOS monolithic IC

1.3 Use: Reader interface LSI for RFID reader/writer

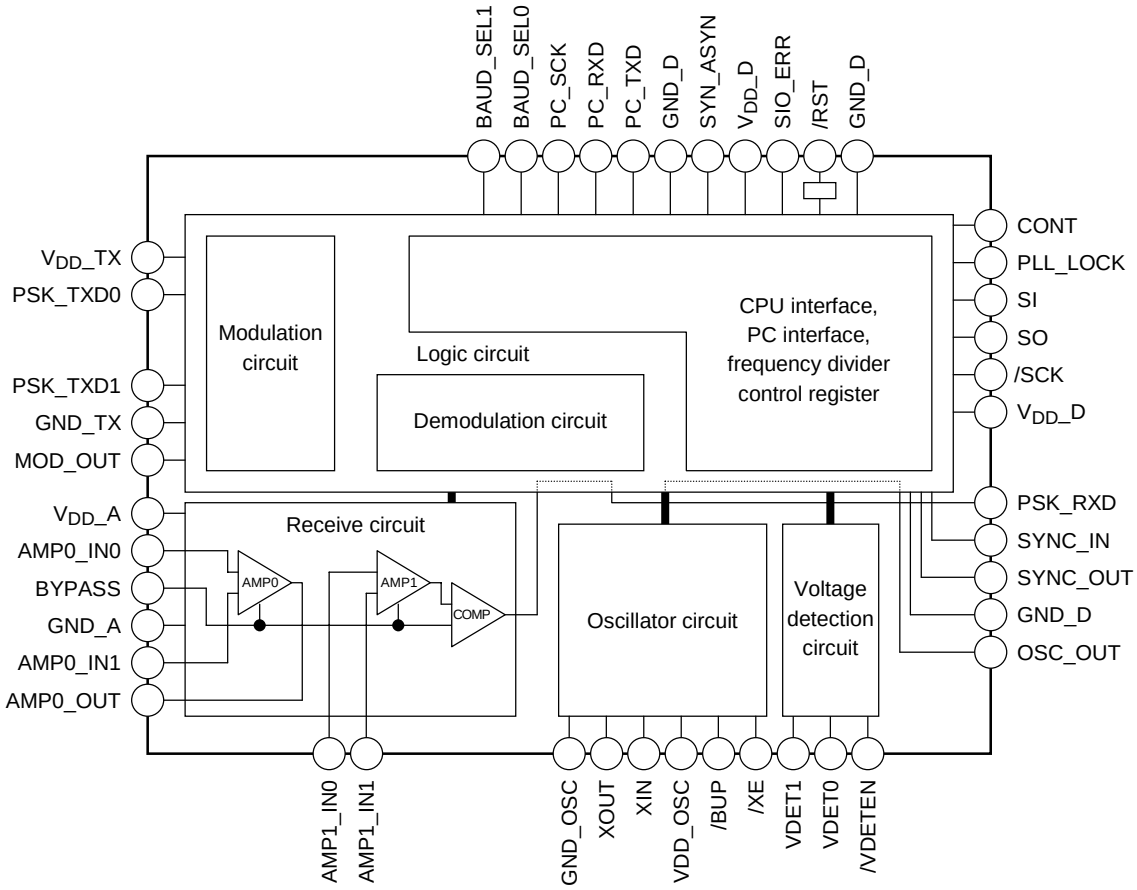
1.4 Function: analog circuit: receive amplifier, voltage detection circuit, and oscillator circuit
logic circuit: transmit circuit, modulation circuit, demodulation circuit, digital PLL circuit, CPU interface, PC interface

2. Absolute Maximum Ratings

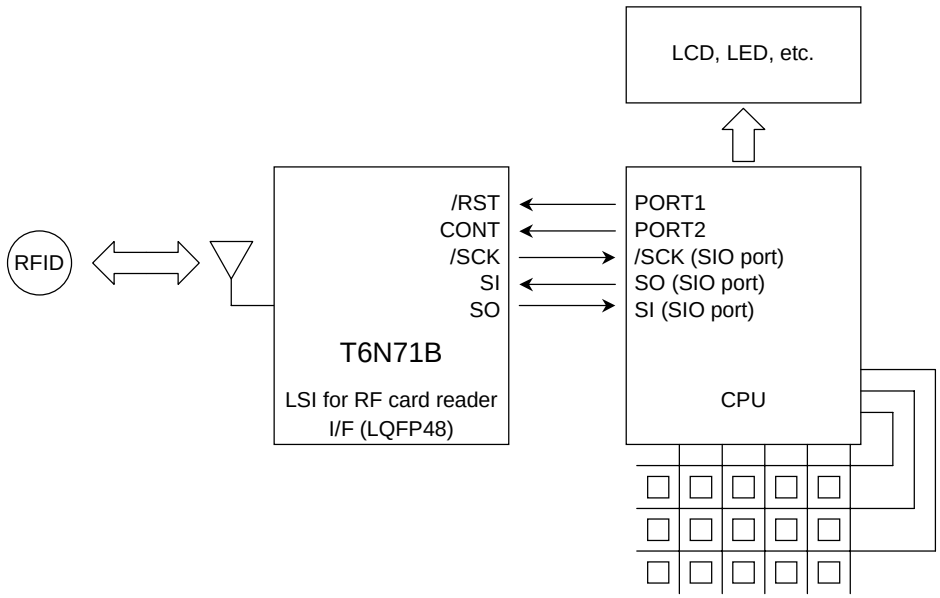
Parameter	Symbol	Operating Rating	Unit
Operating Ambient Temperature	T_{opr}	−20~80	°C
Storage Temperature	T_{stg}	−40~125	°C
Power Supply Voltage	V_{DD}	−0.3~6.0	V
Input Voltage	V_{in}	GND − 0.3~V_{DD} + 0.3	V
Power Dissipation	P_D	150 mW or less (based on heat allowance for plastic package)	—

3. System Configuration

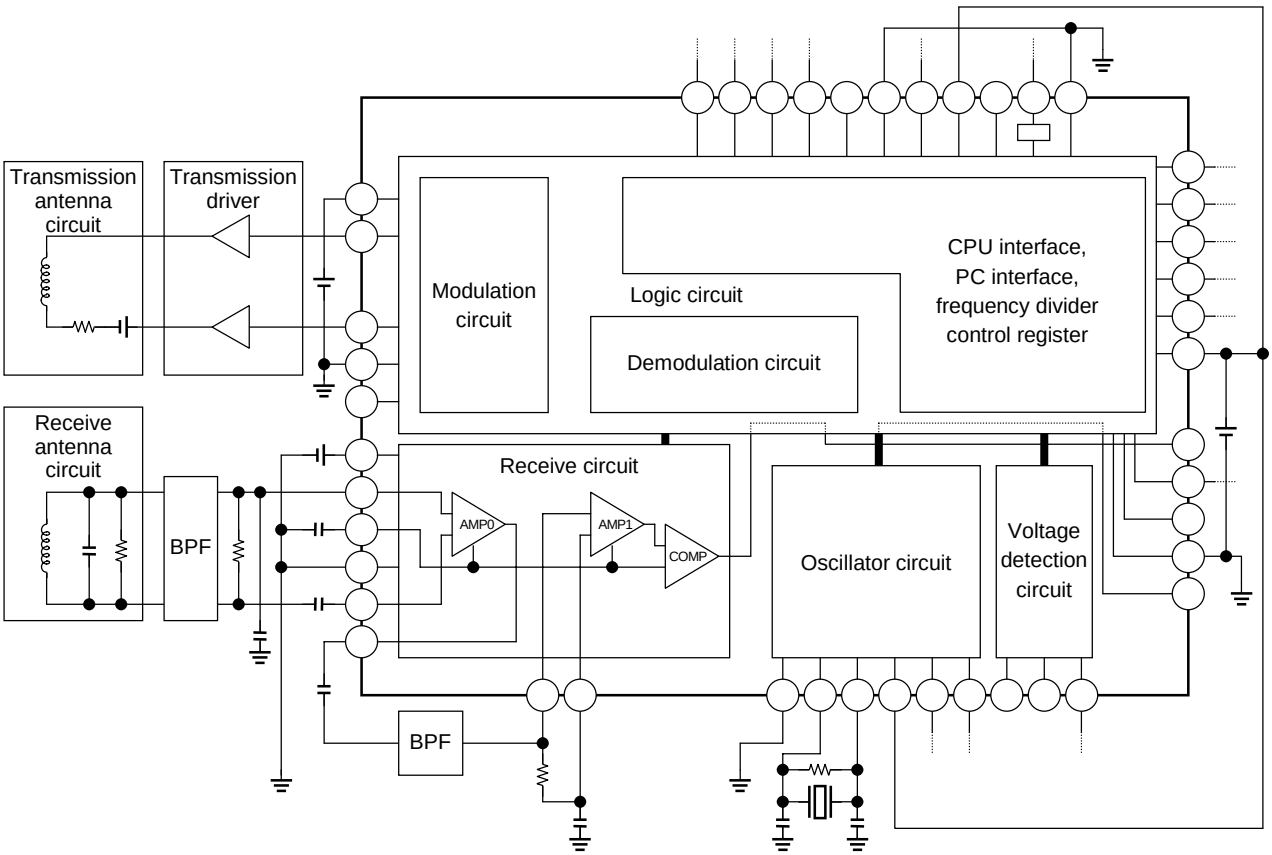
3.1 Diagram of System Configuration



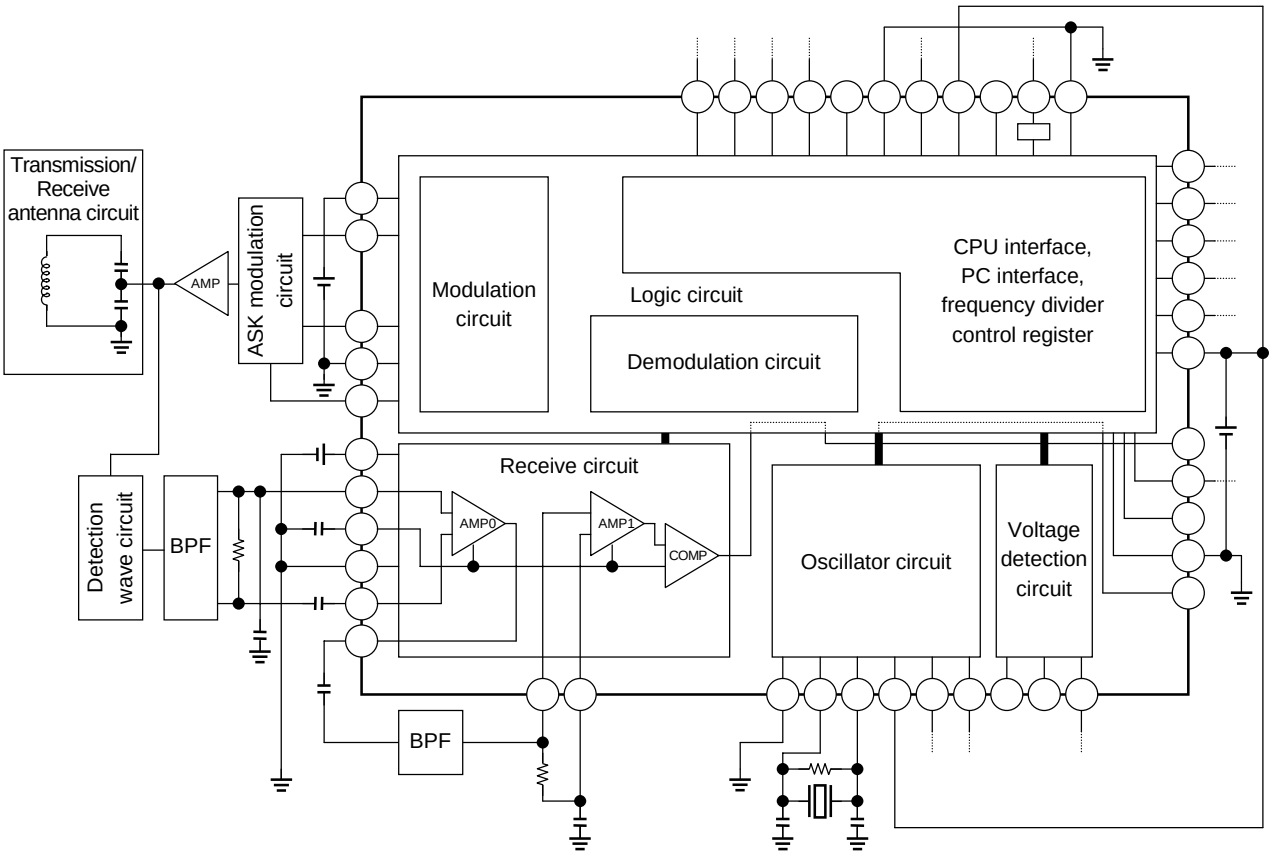
3.2 Example of Overall System Configuration



3.3 Example of Application System Configuration 1
(TOSHIBA general-purpose RFID LSI, T6N38/46/78)



3.4 Example of Application System Configuration 2
(ISO14443 type B RFID)



4. Electrical Characteristics

4.1.1 Operating Characteristics (Ta = –20°C~80°C) (5 V Operation)

Item	Test Condition	Min	Typ.	Max	Unit	Remarks
Operating voltage V_{DD}	GND = 0 V	4.5	5.0	5.5	V	
Operating frequency		2	—	20	MHz	
Operating current 1 (Trans)	V_{DD} = 5.5 V, 8 MHz	—	8	14	mA	*1
Operating current 2 (Receive 1)	V_{DD} = 5.5 V, 8 MHz	—	9	15	mA	*1
Operating current 3 (Receive 2)	V_{DD} = 5.5 V, 8 MHz	—	10	16	mA	*1
BLD operating current	V_{DD} = 5.5 V	—	120	250	μA	*1
HALT current	V_{DD} = 5.5 V	—	3	20	μA	*1

*1: Both operating and HALT currents are consumed only by the LSI. That is, apart from the input pins and oscillation circuit, all related output pins are open and have no load.
Operating current 1: Current consumption at internal logic operation and 125 kHz carrier output
Operating current 2: Current consumption at internal logic operation, 125 kHz carrier output, and amplifier (AMP0 only) in operation
Operating current 3: Current consumption at internal logic operation, 125 kHz carrier output, and amplifiers (both AMP0 and AMP1) in operation
BLD operating current: Current consumption when only voltage detection circuit in operation
HALT current: Dissipation current in HALT mode (wait state)

4.1.2 Operating Characteristics (Ta = –20°C~80°C) (3 V Operation)

Item	Test Condition	Min	Typ.	Max	Unit	Remarks
Operating voltage V_{DD}	GND = 0 V	2.5	3.0	3.3	V	
Operating frequency		2	—	14	MHz	
Operating current 1 (Trans)	V_{DD} = 3.3 V, 8 MHz	—	5	9	mA	*1
Operating current 2 (Receive 1)	V_{DD} = 3.3 V, 8 MHz	—	6	10	mA	*1
Operating current 3 (Receive 2)	V_{DD} = 3.3 V, 8 MHz	—	7	11	mA	*1
BLD operating current	V_{DD} = 3.3 V	—	100	200	μA	*1
HALT current	V_{DD} = 3.3 V	—	1	10	μA	*1

*1: Both operating and HALT currents are consumed only by the LSI. That is, apart from the input pins and oscillation circuit, all related output pins are open and have no load.
Operating current 1: Current consumption at internal logic operation and 125 kHz carrier output
Operating current 2: Current consumption at internal logic operation, 125 kHz carrier output, and amplifier (AMP0 only) in operation
Operating current 3: Current consumption at internal logic operation, 125 kHz carrier output, and amplifiers (both AMP0 and AMP1) in operation
BLD operating current: Current consumption when only voltage detection circuit in operation
HALT current: Dissipation current in HALT mode (wait state)

4.2.1 DC Characteristics (Ta = –20°C~80°C) (5 V Operation)

Item	Symbol	Test Condition	Min	Typ.	Max	Unit	Remarks
L input voltage 1	VIL	V_{DD} = 5 V	0	—	V_{DD} × 0.2	V	*1
H input voltage 1	VIH	V_{DD} = 5 V	V_{DD} × 0.75	—	V_{DD}	V	*1
Input leakage current	IIH	V_{DD} = 5 V, V_{in} = 5 V	—	—	1	μA	*5
Input leakage current	IIL	V_{DD} = 5 V, V_{in} = 0 V	—	—	1	μA	*6
L output current	IOL1	V_{DD} = 5 V, V_{out} = 0.5 V	1.2	—	—	mA	*2
H output current	IOH1	V_{DD} = 5 V, V_{out} = 4.5 V	1.0	—	—	mA	*2
L output current	IOL2	V_{DD} = 5 V, V_{out} = 0.5 V	3.2	—	—	mA	*3
H output current	IOH2	V_{DD} = 5 V, V_{out} = 4.5 V	2.5	—	—	mA	*3
L output current	IOL3	V_{DD} = 5 V, V_{out} = 0.5 V	7.0	—	—	mA	*4
H output current	IOH3	V_{DD} = 5 V, V_{out} = 4.5 V	5.0	—	—	mA	*4
Pull-up resistance		V_{DD} = 5 V, V_{in} = 0 V	66	110	154	kΩ	*7

*1: Applies to the following eleven input pins: /RST, PSK_RXD, SYNC_IN, SI, PC_RXD, SYN_ASYN, BAUD_SEL0, BAUD_SEL1, /XE, /BUP, /VDETEN

*2: Applies to the following seven output pins: PSK_RXD, SO, /SCK, VDET0, VDET1, PLL_LOCK, SIO_ERR

*3: Applies to the following five output pins: MOD_OUT, SYNC_OUT, PC_TXD, PC_SCK, OSC_OUT

*4: Applies to the following two output pins: PSK_TXD0, PSK_TXD1

*5: Applies to the following eleven input pins: /RST, PSK_RXD, SYNC_IN, SI, PC_RXD, SYN_ASYN, BAUD_SEL0, BAUD_SEL1, /XE, /BUP, /VDETEN

*6: Applies to the following ten input pins: /RST, SYNC_IN, SI, PC_RXD, SYN_ASYN, BAUD_SEL0, BAUD_SEL1, /XE, /BUP, /VDETEN

*7: Applies to the PSK_RXD pin.

4.2.2 DC Characteristics (Ta = –20°C~80°C) (3 V Operation)

Item	Symbol	Test Condition	Min	Typ.	Max	Unit	Remarks
L input voltage 1	VIL	V_{DD} = 3 V	0	—	V_{DD} × 0.2	V	*1
H input voltage 1	VIH	V_{DD} = 3 V	V_{DD} × 0.75	—	V_{DD}	V	*1
Input leakage current	IIH	V_{DD} = 3 V, V_{in} = 3 V	—	—	1	μA	*5
Input leakage current	IIL	V_{DD} = 3 V, V_{in} = 0 V	—	—	1	μA	*6
L output current	IOL1	V_{DD} = 3 V, V_{out} = 0.5 V	1.0	—	—	mA	*2
H output current	IOH1	V_{DD} = 3 V, V_{out} = 2.5 V	0.8	—	—	mA	*2
L output current	IOL2	V_{DD} = 3 V, V_{out} = 0.5 V	2.0	—	—	mA	*3
H output current	IOH2	V_{DD} = 3 V, V_{out} = 2.5 V	1.6	—	—	mA	*3
L output current	IOL3	V_{DD} = 3 V, V_{out} = 0.5 V	4.0	—	—	mA	*4
H output current	IOH3	V_{DD} = 3 V, V_{out} = 2.5 V	3.2	—	—	mA	*4
Pull-up resistance		V_{DD} = 3 V, V_{in} = 0 V	66	110	154	kΩ	*7

*1: Applies to the following eleven input pins: /RST, PSK_RXD, SYNC_IN, SI, PC_RXD, SYN_ASYN, BAUD_SEL0, BAUD_SEL1, /XE, /BUP, /VDETEN

*2: Applies to the following seven output pins: PSK_RXD, SO, /SCK, VDET0, VDET1, PLL_LOCK, SIO_ERR

*3: Applies to the following five output pins: MOD_OUT, SYNC_OUT, PC_TXD, PC_SCK, OSC_OUT

*4: Applies to the following two output pins: PSK_TXD0, PSK_TXD1

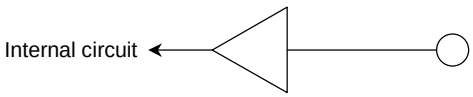
*5: Applies to the following eleven input pins: /RST, PSK_RXD, SYNC_IN, SI, PC_RXD, SYN_ASYN, BAUD_SEL0, BAUD_SEL1, /XE, /BUP, /VDETEN

*6: Applies to the following ten input pins: /RST, SYNC_IN, SI, PC_RXD, SYN_ASYN, BAUD_SEL0, BAUD_SEL1, /XE, /BUP, /VDETEN

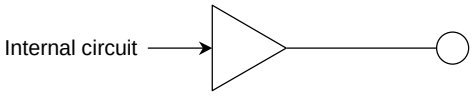
*7: Applies to the PSK_RXD pin.

4.2.3 Internal Equivalent Circuits for Pins

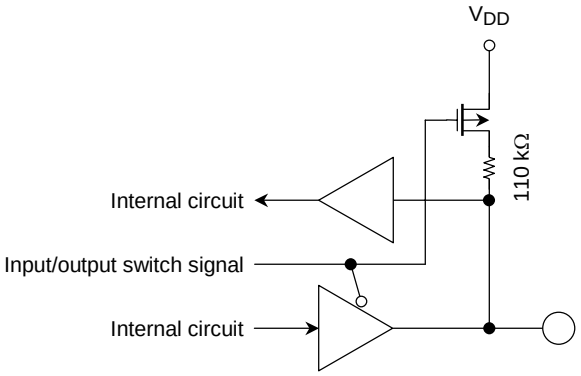
Input pins: /RST, PSK_RXD, SYNC_IN, SI, PC_RXD, SYN_ASYN, BAUD_SEL0, BAUD_SEL1, /XE, /BUP, /VDETEN



Output pins: SO, /SCK, VDET0, VDET1, PLL_LOCK, SIO_ERR, MOD_OUT, SYNC_OUT, PC_TXD, PC_SCK, OSC_OUT, PSK_TXD0, PSK_TXD1



Input/output (with pull-up resistor) pin: PSK_RXD

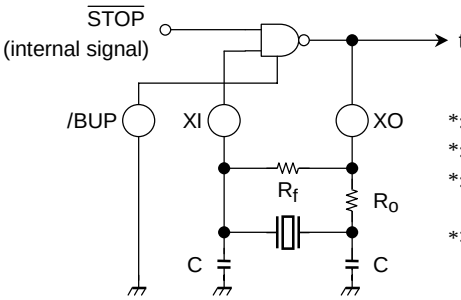


At input: Pull-up resistor connected, output buffer in HiZ
At output: Pull-up resistor disconnected, output buffer in H or L output
When control register EXTRXD = 1, the PSK_RXD pin is set to output mode; when EXTRXD = 0, set to input mode (pull-up resistor connected).

4.3 Oscillation Characteristics (Ta = –20°C~80°C) (for your reference)

Item	Symbol	Test Condition	Min	Typ.	Max	Unit	Remarks
Oscillation start voltage	V_{sta}	Crystal oscillator, 8 MHz C = 10 pF, R_o = 0 Ω, R_f = 1 MΩ	—	—	2.2	V	
Oscillation hold voltage	V_{hold}	Crystal oscillator, 8 MHz C = 10 pF, R_o = 0 Ω, R_f = 1 MΩ	2.2	—	—	V	

Note: Evaluate and decide the external components (R_f, C, R_o) in accordance with the crystal oscillator and ceramic oscillator used. Before using, be sure to check the oscillation characteristics as these vary depending on the crystal or ceramic oscillator.

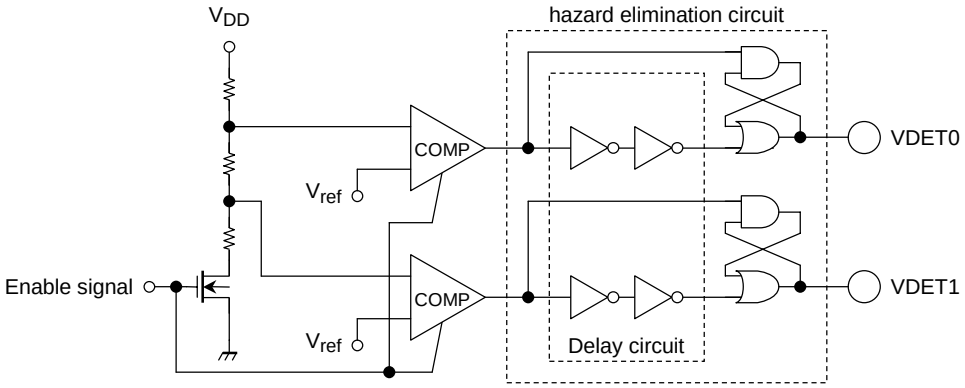


*: Connect the circuit near the XI and XO pins.
*: Use external R_f, R_o, C, and oscillator (crystal).
*: When using an external clock, input from the XI pin. Do not connect XI and XO pin to other external devices.
*: The /BUP pin is used to control the level of current to the oscillation circuit. Setting /BUP = H reduces the dissipation current. However, this also results in a fall in the oscillation characteristics.

4.4 Power Supply Voltage Detection Circuit (Ta = –20°C~80°C)

Item	Test Condition	Min	Typ.	Max	Unit	Remarks
VDET0		2.2	2.4	2.6	V	±0.2 V
VDET1		3.6	4.0	4.4	V	±0.4 V

*: Power supply voltage drop detection: When the circuit is enabled, if the V_{DD} voltage exceeds the detected VDET0 or VDET1, high level is output; if the V_{DD} voltage drops below the detected VDET0 or VDET1, low level is output.



*: The reference voltage (V_{ref}) which is not dependent on the V_{DD} voltage is internal to the LSI. The power supply voltage detection circuit inputs the voltage by extracting it from the resistance dividing block where the V_{DD} voltage is used as the supply to the comparator. The detector compares the voltage with the reference voltage (V_{ref}) to detect whether the V_{DD} voltage is below 2.4 V or 4.0 V.

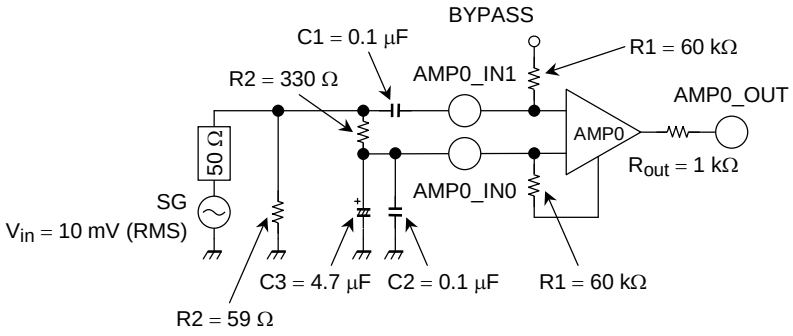
*: Enable signal: In HALT state and external pin /VDETEN = H input, the voltage detection circuit is disabled.

4.5.1 Amplifier Characteristics (Ta = –20°C~80°C) (5 V operation)

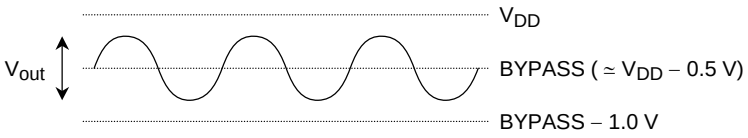
Item	Test Condition	Min	Typ.	Max	Unit	Remarks
Carrier input voltage	Peak-to-Peak	0	—	5.5	V	*1
Amplification ratio	V_{DD} = 4.5 V, V_{in} = 10 mV (RMS) Freq = 500 kHz (sine wave input)	23	37	—	dB	AMP0
Amp waveform duty (sine wave input)		35:65	50:50	65:35	—	AMP1
Input resistance	AMP_IN1 = V_{DD} – 0.5 V BYPASS = V_{DD}	36	60	84	kΩ	Amp input IN1 pin
Output impedance	V_{in} = V_{DD} – 0.5 V	0.6	1	1.4	kΩ	AMP0

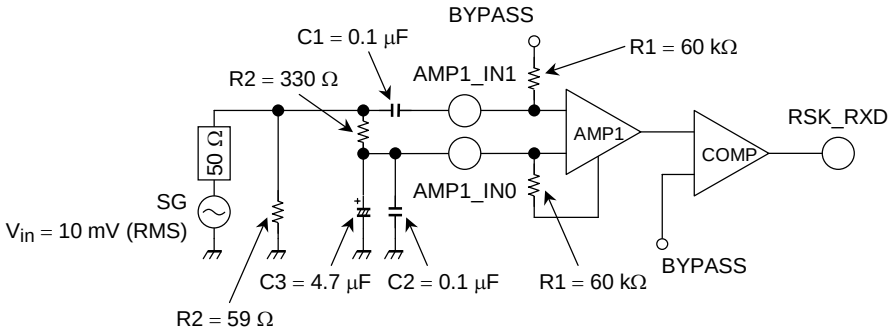
*1: The input voltage is the voltage which can be input to the AMP0_IN0, AMP0_IN1, AMP1_IN0, AMP1_IN1 pins. It does not specify normal operation.

*2: The above characteristic is defined by the following test circuit.

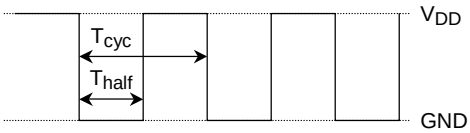


Amp output waveform (AMP0): AMP0_OUT pin





Amp output waveform (AMP1): PSK_RXD pin



[Definition]

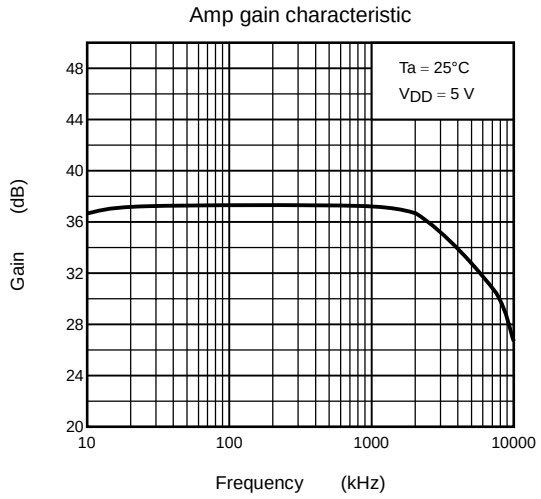
Gain = 20 λog (V_{out}/V_{in}); however, within the range where output does not saturate.

Duty cycle = $T_{half}/T_{cyc} \times 100$

*: AMP0 output AMP0_OUT operates with the BYPASS potential (= V_{DD} – 0.5 V) as the operating point. When V_{in} is sufficiently large, a sine wave limited to between V_{DD} and V_{DD} – 1 V (saturated state: almost a square wave) is output.

*: AMP1 is connected to the binary comparator. The duty cycle is measured on the PSK_RXD pin where the data are output from the comparator.

(Typical characteristic)



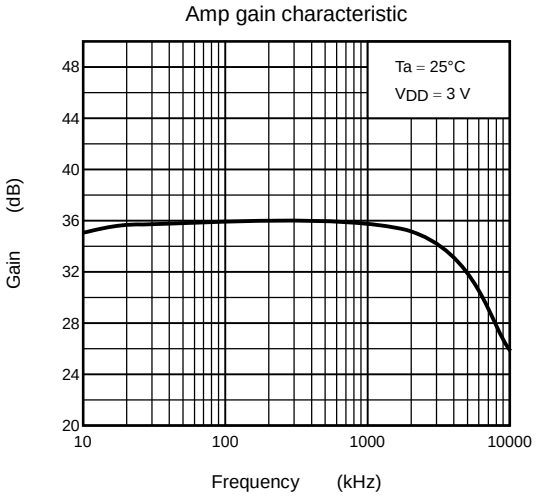
4.5.2 Amplifier Characteristics (Ta = –20°C~80°C) (3 V Operation)

Item	Test Condition	Min	Typ.	Max	Unit	Remarks
Carrier input voltage	Peak-to-Peak	0	—	3.3	V	*1
Amplification ratio	V_{DD} = 3 V, V_{in} = 10 mV (RMS) Freq = 500 kHz (sine wave input)	23	36	—	dB	AMP0
Amp waveform duty (sine wave input)		35:65	50:50	65:35	—	AMP1
Input resistance	AMP_IN1 = V_{DD} – 0.5 V BYPASS = V_{DD}	36	60	84	kΩ	Amp input IN1 pin
Output impedance	V_{in} = V_{DD} – 0.5 V	0.6	1	1.4	kΩ	AMP0

*1: The input voltage is the voltage which can be input to the AMP0_IN0, AMP0_IN1, AMP1_IN0, AMP1_IN1 pins. It does not specify normal operation.

*2: The above characteristics are determined by the same kind of test circuit and definitions as in 4.5.1.

(Typical characteristic)



5. Pin Assignment

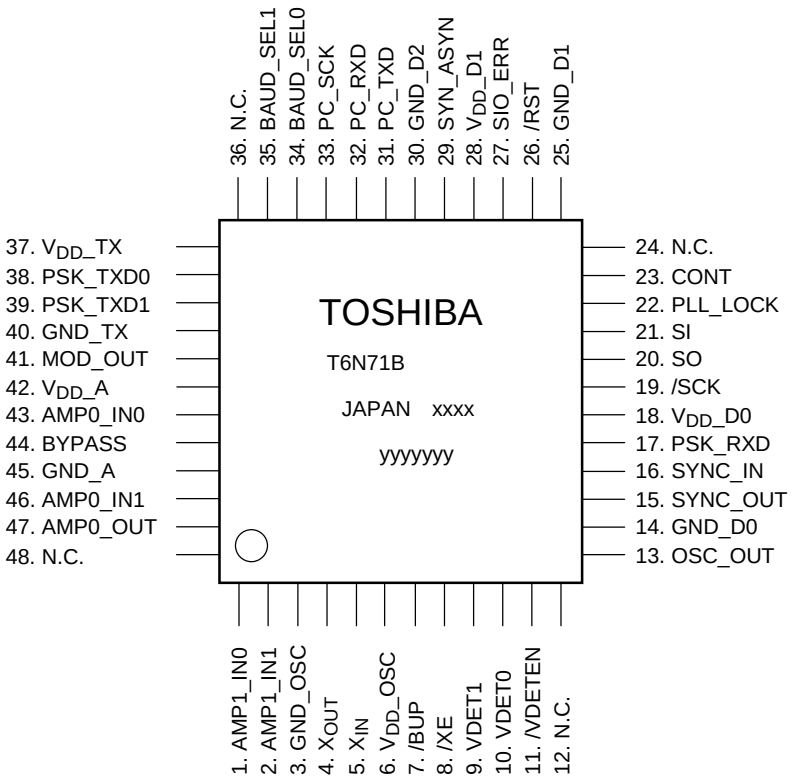
5.1 Outline of Functions

	Pin Name	Input/ output	Function
Transmit circuit	PSK_TXD0/1	Output	Antenna output pin (carrier and data output pin)
	MOD_OUT	Output	Sub carrier output pin
	V_{DD}_TX, GND_TX	—	Transmit-circuit-only power supply pins
Receive circuit	AMP0_IN0	Input	PSK receive wave amp (AMP0) input pin
	AMP0_IN1	Input	PSK receive wave amp (AMP0) input pin
	AMP0_OUT	Output	PSK receive wave amp (AMP0) output pin
	AMP1_IN0	Input	PSK receive wave amp (AMP1) input pin
	AMP1_IN1	Input	PSK receive wave amp (AMP1) input pin
	BYPASS	—	Amp stabilizing capacitor connecting pin
	V_{DD}_A, GND_A	—	Receive-circuit-only power supply pins
Logic circuit	/RST	Input	System reset input pin
	PSK_RXD	Input/ output	Receive carrier input/output pin (pull-up resistor connected at input)
	SYNC_IN	Input	Transmit sync signal input pin
	SYNC_OUT	Output	Transmit sync signal output pin
	SI	Input	CPU interface serial input (sync/start-stop sync) pin
	SO	Output	CPU interface serial output (sync/start-stop sync) pin
	/SCK	Output	Serial clock (sync) /SIO clock (start-stop sync) pin
	CONT	Input	Control pin (when L, register setting mode)
	PC_RXD	Input	External interface receive input (start-stop sync) pin
	PC_TXD	Output	External interface receive output (start-stop sync) pin
	PC_SCK	Input	External interface clock generation baud generator input pin
	SYN_ASYN	Input	CPU interface clock sync/start-stop sync switching pin
	BAUD_SEL0/1	Input	Initial transfer rate select pin
	PLL_LOCK	Output	PLL lock detection pin
	SIO_ERR	Output	RFID receive data (clock sync) error detection pin
	V_{DD}_D0~D01, GND_D0~D02, V_{DD}_OSC, GND_OSC	—	Logic circuit and oscillator power supply pins
Others	XI, XO	—	Oscillation circuit. Crystal oscillator, ceramic oscillator, capacitor, and external resistor are externally connected.
	OSC_OUT	Output	Oscillation frequency output pin
	/XE	Input	Oscillator and receive circuit enable pin. When set to L, oscillation starts.
	/BUP	Input	Oscillator Beta Up mode enable pin. When set to L, Beta Up mode.
	VDET0/1	Output	Pin for detection signal output from power voltage detection circuit
	/VDETEN	Input	Power voltage detection circuit enable pin. When set to L, enables the detector.

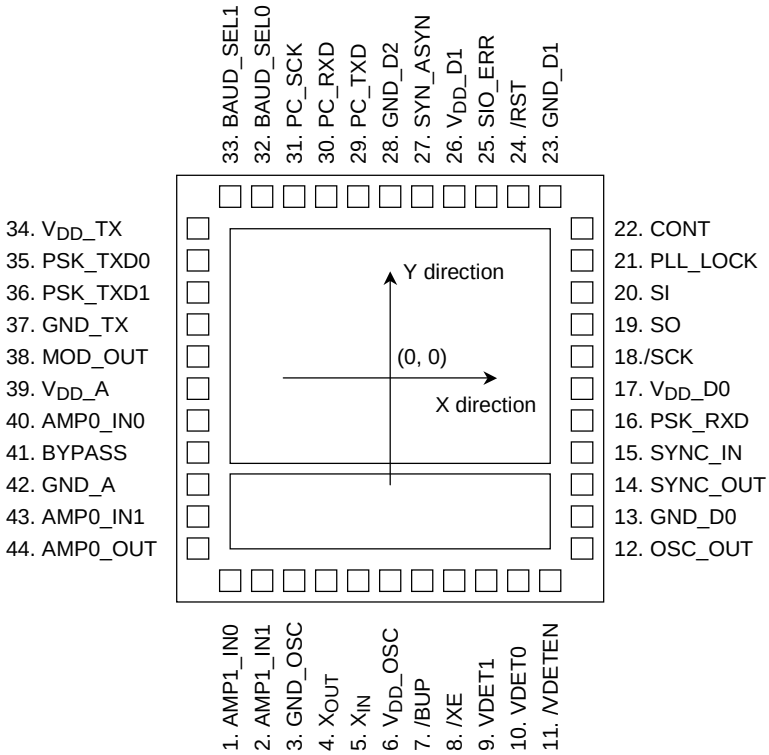
Total: 44 pins (4 NC pins are not included.)

5.2 Pin Assignment

No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	AMP1_IN0	13	OSC_OUT	25	GND_D1	37	V_{DD}_TX
2	AMP1_IN1	14	GND_D0	26	/RST	38	PSK_TXD0
3	GND_OSC	15	SYNC_OUT	27	SIO_ERR	39	PSK_TXD1
4	X_{OUT}	16	SYNC_IN	28	V_{DD}_D1	40	GND_TX
5	X_{IN}	17	PSK_RXD	29	SYN_ASYN	41	MOD_OUT
6	V_{DD}_OSC	18	V_{DD}_D0	30	GND_D2	42	V_{DD}_A
7	/BUP	19	/SCK	31	PC_TXD	43	AMP0_IN0
8	/XE	20	SO	32	PC_RXD	44	BYPASS
9	VDET1	21	SI	33	PC_SCK	45	GND_A
10	VDET0	22	PLL_LOCK	34	BAUD_SEL0	46	AMP0_IN1
11	/VDETEN	23	CONT	35	BAUD_SEL1	47	AMP0_OUT
12	N.C.	24	N.C.	36	N.C.	48	N.C.



5.3 Chip Pad Assignment and Coordinates
Chip size: 3.2 × 3.2 mm



Pad Coordinates

Unit: μm

No.	Pad Name	X Coordinate	Y Coordinate	No.	Pad Name	X Coordinate	Y Coordinate	No.	Pad Name	X Coordinate	Y Coordinate
1	AMP1_IN0	−1102	−1464	16	PSK_RXD	1464	−200	31	PC_SCK	−627	1464
2	AMP1_IN1	−855	−1464	17	V_{DD}_D0	1464	0	32	BAUD_SEL0	−855	1464
3	GND_OSC	−627	−1464	18	/SCK	1464	200	33	BAUD_SEL1	−1102	1464
4	X_{OUT}	−409	−1464	19	SO	1464	409	34	V_{DD}_TX	−1464	1102
5	X_{IN}	−200	−1464	20	SI	1464	627	35	PSK_TXD0	−1464	855
6	V_{DD}_OSC	0	−1464	21	PLL_LOCK	1464	855	36	PSK_TXD1	−1464	627
7	/BUP	200	−1464	22	CONT	1464	1102	37	GND_TX	−1464	409
8	/XE	409	−1464	23	GND_D1	1102	1464	38	MOD_OUT	−1464	200
9	VDET1	627	−1464	24	/RST	855	1464	39	V_{DD}_A	−1464	0
10	VDET0	855	−1464	25	SIO_ERR	627	1464	40	AMP0_IN0	−1464	−200
11	/VDETEN	1102	−1464	26	V_{DD}_D1	409	1464	41	BYPASS	−1464	−409
12	OSC_OUT	1464	−1102	27	SYN_ASYN	200	1464	42	GND_A	−1464	−627
13	GND_D0	1464	−855	28	GND_D2	0	1464	43	AMP0_IN1	−1464	−855
14	SYNC_OUT	1464	−627	29	PC_TXD	−200	1464	44	AMP0_OUT	−1464	−1102
15	SYNC_IN	1464	−409	30	PC_RXD	−409	1464	—	—	—	—

*: Pad coordinates are the pad center coordinates.

*: Pad opening is 100 μm × 100 μm.

6. Caution on Designing Peripheral Circuits

The LSI supports a total of eleven power supply pins (V_{DD} and GND) as follows:
V_{DD}_D0 to D1, GND_D0 to D2, V_{DD}_OSC, GND_OSC, V_{DD}_A, GND_A, V_{DD}_TX, and GND_TX.

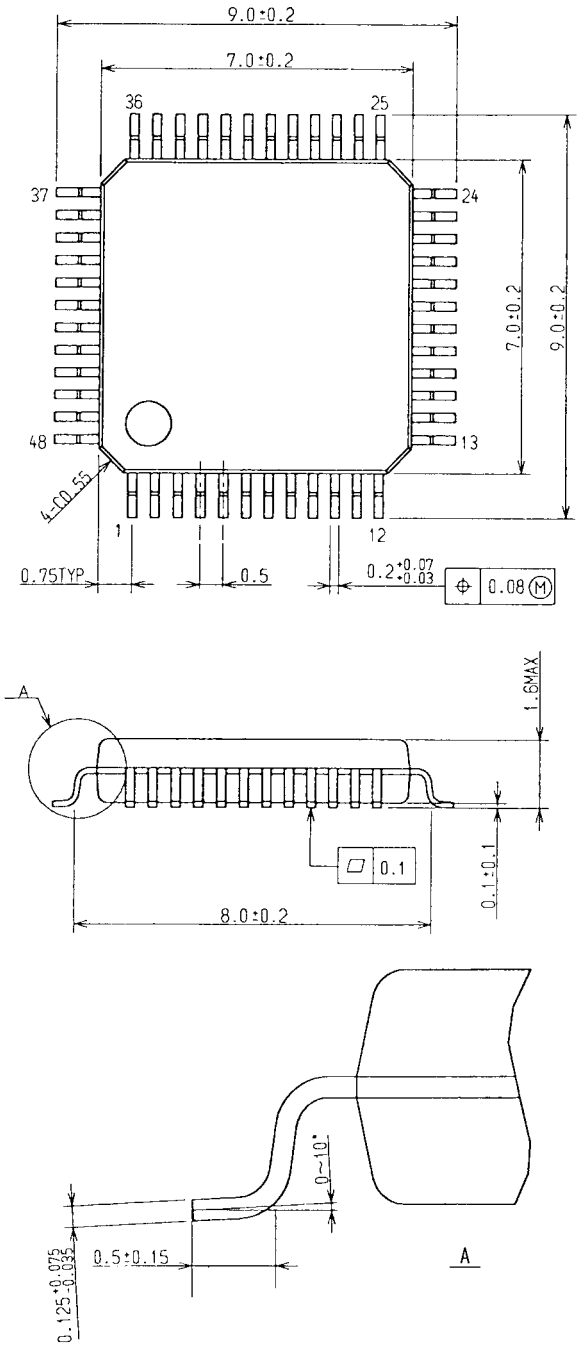
Because the LSI also has analog circuits, to minimize power interference between circuit blocks, the power supply is isolated among logic circuits (V_{DD}_D0 to 1, V_{DD}_D0 to 2, V_{DD}_OSC, and GND_OSC), analog circuits (V_{DD}_A, GND_A), and transmit circuits (V_{DD}_TX, GND_TX). Thus, when designing peripheral circuits, take this into consideration and pay attention to the following points.

(1) How to handle GND pins
Connect the GND pins to GND with the same power supply on the circuit board.

(2) How to handle V_{DD} pins
Connect V_{DD}_D0 to D1 and V_{DD}_OSC to the same power supply on the PCB. For the stability of the internal circuits, apply the same V_{DD} level to the logic, analog, and transmission systems.

Package Dimensions

LQFP48-P-0707-0.50C Unit: mm



Weight: 384 mg (typ.)

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000707EDA

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