# CA3045, CA3046

## General-Purpose N-P-N Transistor Arrays

Three Isolated Transistors and One Differentially-Connected Transistor Pair

For Low-Power Applications at Frequencies from DC through the VHF Range

*Features*

- Two matched pairs of transistors
  $V_{BE}$ matched ± 5 mV
  Input offset current 2 μA max.
  at $I_C$ = 1 mA
- 5 general purpose monolithic transistors
- Operation from DC to 120 MHz
- Wide operating current range
- Low noise figure - - 3.2 dB typ. at 1 kHz
- Full military temperature range for CA3045
  -55 to +125°C

The CA3045 and CA3046 each consist of five general-purpose silicon n-p-n transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially-connected pair.

The transistors of the CA3045 and CA3046 are well suited to a wide variety of applications in low power systems in the DC through VHF range. They may be used as discrete transistors in conventional circuits. However, in addition, they provide the very significant inherent integrated circuit advantages of close electrical and thermal matching.

The CA3045 is supplied in a 14-lead dual-in-line hermetic (welded-seal) ceramic package and the CA3045F in a 14-lead dual-in-line hermetic (frit-seal) ceramic package.

The CA3046 is electrically identical to the CA3045 but is supplied in a dual-in-line plastic package for applications requiring only a limited temperature range.

The CA3045 and CA3046 are available in the packages shown below

| Package | Suffix Letter | CA3045 | CA3046 |
|---|---|---|---|
| 14-Lead Dual-In-Line Plastic | E | | √ |
| 14-Lead Dual-In-Line Ceramic | D | √ | |
| 14-Line Dual-In-Line Frit-Seal Ceramic | F | √ | |
| Chip | H | √ | |

*Applications*

- General use in all types of signal processing systems operating anywhere in the frequency range from DC to VHF
- Custom designed differential amplifiers
- Temperature compensated amplifiers
- See RCA Application Note, ICAN-5296 "Application of the RCA-CA3018 Integrated-Circuit Transistor Array" for suggested applications.

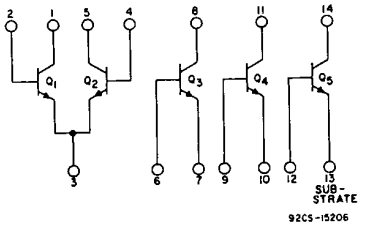



*Fig.1 - Schematic diagram.*

# CA3045, CA3046

T-43-25

**ABSOLUTE MAXIMUM RATINGS AT $T_A$ = 25°C**

| | CA3045 | | CA3046, CA3045F | | |
|---|---|---|---|---|---|
| | Each Transistor | Total Package | Each Transistor | Total Package | |
| Power Dissipation: | | | | | |
| $T_A$ up to 55°C | – | – | 300 | 750 | mW |
| $T_A$ > 55°C | – | – | Derate at 6.67 | | mW/°C |
| $T_A$ up to 75°C | 300 | 750 | – | – | mW |
| $T_A$ > 75°C | Derate at 8 | | – | – | mW/°C |
| Collector-to-Emitter Voltage, $V_{CEO}$ | 15 | – | 15 | – | V |
| Collector-to-Base Voltage, $V_{CBO}$ | 20 | – | 20 | – | V |
| Collector-to-Substrate Voltage, $V_{CIO}$* | 20 | – | 20 | – | V |
| Emitter-to-Base Voltage, $V_{EBO}$ | 5 | – | 5 | – | V |
| Collector Current | 50 | – | 50 | – | mA |
| Temperature Range: | | | | | |
| Operating | –55 to +125 | | –55 to +125 | | °C |
| Storage | –65 to +150 | | –65 to +150 | | °C |
| Lead Temperature (During Soldering): At distance 1/16 ±1/32" (1.59 ±0.79 mm) from case for 10 seconds max. | +265 | | +265 | | °C |

* The collector of each transistor of the CA3045 and CA3046 is isolated from the substrate by an integral diode. *The substrate (terminal 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.*

**ELECTRICAL CHARACTERISTICS, at $T_A$ = 25°C**

***Characteristics apply for each transistor in the CA3045 and CA3046 as specified.***

| CHARACTERISTICS | SYMBOLS | SPECIAL TEST CONDITIONS | LIMITS Type CA3045 Type CA3046 MIN. | TYP. | MAX. | UNITS | CHARACTERISTIC CURVES FIG. |
|---|---|---|---|---|---|---|---|
| STATIC CHARACTERISTICS | | | | | | | |
| Collector-to-Base Breakdown Voltage | $V_{(BR)CBO}$ | $I_C$ = 10 μA, $I_E$ = 0 | 20 | 60 | - | V | - |
| Collector-to-Emitter Breakdown Voltage | $V_{(BR)CEO}$ | $I_C$ = 1 mA, $I_B$ = 0 | 15 | 24 | - | V | - |
| Collector-to-Substrate Breakdown Voltage | $V_{(BR)CIO}$ | $I_C$ = 10 μA, $I_{CI}$ = 0 | 20 | 60 | - | V | - |
| Emitter-to-Base Breakdown Voltage | $V_{(BR)EBO}$ | $I_E$ = 10 μA, $I_C$ = 0 | 5 | 7 | - | V | - |
| Collector-Cutoff Current | $I_{CBO}$ | $V_{CB}$ = 10 V, $I_E$ = 0 | - | 0.002 | 40 | nA | 2 |
| Collector-Cutoff Current | $I_{CEO}$ | $V_{CE}$ = 10 V, $I_B$ = 0 | - | See curve | 0.5 | μA | 3 |
| Static Forward Current-Transfer Ratio (Static Beta) | $h_{FE}$ | $V_{CE}$ = 3 V, $I_C$ = 10 mA | - | 100 | - | - | 4 |
| | | $V_{CE}$ = 3 V, $I_C$ = 1 mA | 40 | 100 | - | - | |
| | | $V_{CE}$ = 3 V, $I_C$ = 10 μA | - | 54 | - | - | |
| Input Offset Current for Matched Pair $Q_1$ and $Q_2$. $\lvert I_{IO_1} - I_{IO_2} \rvert$ | | $V_{CE}$ = 3 V, $I_C$ = 1 mA | - | 0.3 | 2 | μA | 5 |
| Base-to-Emitter Voltage | $V_{BE}$ | $V_{CE}$ = 3 V, $I_E$ = 1 mA | - | 0.715 | - | V | 6 |
| | | $V_{CE}$ = 3 V, $I_E$ = 10 mA | - | 0.800 | - | | |
| Magnitude of Input Offset Voltage for Differential Pair $\lvert V_{BE_1} - V_{BE_2} \rvert$ | | $V_{CE}$ = 3 V, $I_C$ = 1 mA | - | 0.45 | 5 | mV | 6,8 |
| Magnitude of Input Offset Voltage for Isolated Transistors $\lvert V_{BE_3} - V_{BE_4} \rvert$, $\lvert V_{BE_4} - V_{BE_5} \rvert$, $\lvert V_{BE_5} - V_{BE_3} \rvert$ | | $V_{CE}$ = 3 V, $I_C$ = 1 mA | - | 0.45 | 5 | mV | 6,8 |
| Temperature Coefficient of Base-to-Emitter Voltage | $\frac{\Delta V_{BE}}{\Delta T}$ | $V_{CE}$ = 3 V, $I_C$ = 1 mA | - | -1.9 | - | mV/°C | 7 |
| Collector-to-Emitter Saturation Voltage | $V_{CES}$ | $I_B$ = 1 mA, $I_C$ = 10 mA | - | 0.23 | - | V | - |
| Temperature Coefficient: Magnitude of Input-Offset Voltage | $\frac{\lvert \Delta V_{IO} \rvert}{\Delta T}$ | $V_{CE}$ = 3 V, $I_C$ = 1 mA | - | 1.1 | - | μV/°C | 8 |

# CA3045, CA3046

## ELECTRICAL CHARACTERISTICS (Cont'd.)

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| DYNAMIC CHARACTERISTICS | | | | | | | |
| Low-Frequency Noise Figure | NF | f = 1 kHz, $V_{CE}$ = 3 V, $I_C$ = 100 μA, Source Resistance = 1 kΩ | - | 3.25 | - | dB | 9(b) |
| Low-Frequency, Small-Signal Equivalent-Circuit Characteristics: | | | | | | | |
| Forward Current-Transfer Ratio | $h_{fe}$ | f = 1 kHz, $V_{CE}$ = 3 V, $I_C$ = 1 mA | - | 110 | - | - | 10 |
| Short-Circuit Input Impedance | $h_{ie}$ | | - | 3.5 | - | kΩ | |
| Open-Circuit Output Impedance | $h_{oe}$ | | - | 15.6 | - | μmho | |
| Open-Circuit Reverse Voltage-Transfer Ratio | $h_{re}$ | | - | $1.8 \times 10^{-4}$ | - | - | |
| Admittance Characteristics: | | | | | | | |
| Forward Transfer Admittance | $Y_{fe}$ | f = 1 MHz, $V_{CE}$ = 3 V, $I_C$ = 1 mA | - | 31-j1.5 | - | - | 11 |
| Input Admittance | $Y_{ie}$ | | - | 0.3+j0.04 | - | - | 12 |
| Output Admittance | $Y_{oe}$ | | - | 0.001+j0.03 | - | - | 13 |
| Reverse Transfer Admittance | $Y_{re}$ | | - | See curve | - | - | 14 |
| Gain-Bandwidth Product | $f_T$ | $V_{CE}$ = 3 V, $I_C$ = 3 mA | 300 | 550 | - | - | 15 |
| Emitter-to-Base Capacitance | $C_{EB}$ | $V_{EB}$ = 3 V, $I_E$ = 0 | - | 0.6 | - | pF | - |
| Collector-to-Base Capacitance | $C_{CB}$ | $V_{CB}$ = 3 V, $I_C$ = 0 | - | 0.58 | - | pF | - |
| Collector-to-Substrate Capacitance | $C_{CI}$ | $V_{CS}$ = 3 V, $I_C$ = 0 | - | 2.8 | - | pF | - |

## STATIC CHARACTERISTICS

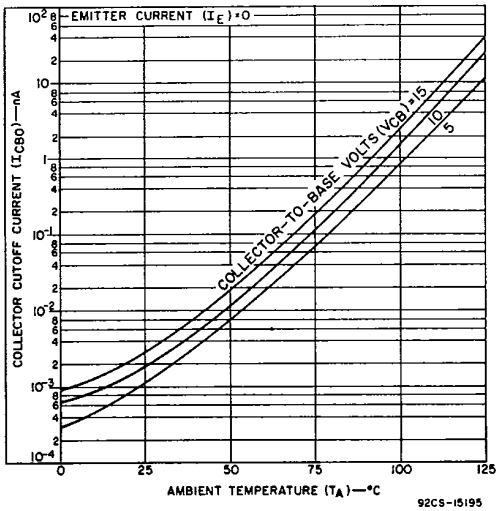
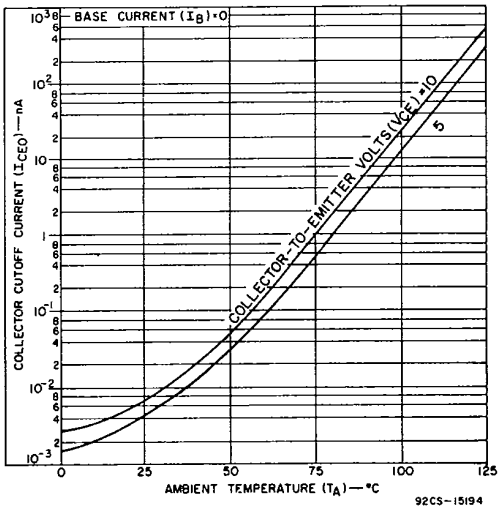



*Fig.2 - Typical collector-to-base cutoff current vs ambient temperature for each trans*




*Typical collector-to-emitter cutoff current vs ient temperature for each transistor.*

# CA3045, CA3046

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## STATIC CHARACTERISTICS

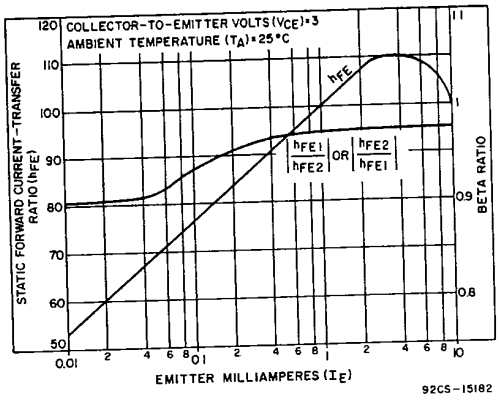


*Fig.4 - Typical static forward current-transfer ratio and beta ratio for transistors $Q_1$ and $Q_2$ vs emitter current.*

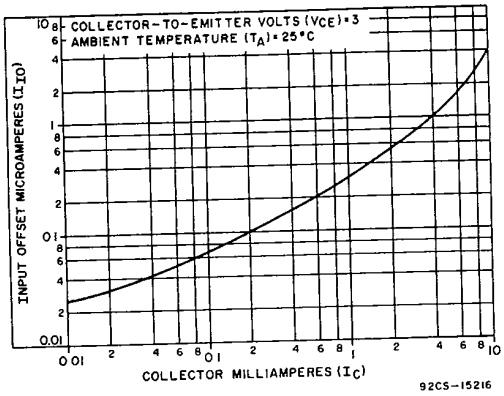


*Fig.5 - Typical input offset current for matched transistor pair $Q_1Q_2$ vs collector current.*

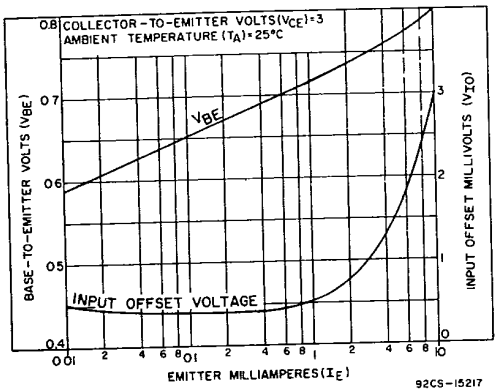


*Fig.6 - Typical static base-to-emitter voltage characteristic and input offset voltage for differential pair and paired isolated transistors vs emitter current.*

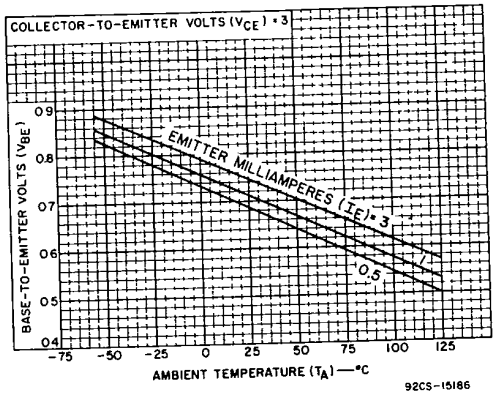


*Fig.7 - Typical base-to-emitter voltage characteristic vs ambient temperature for each transistor.*

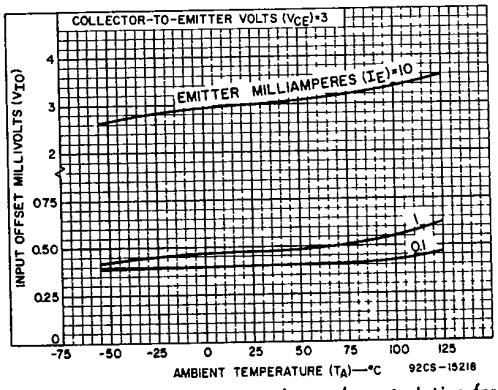


*Fig.8 - Typical input offset voltage characteristics for differential pair and paired isolated transistors vs ambient temperature.*

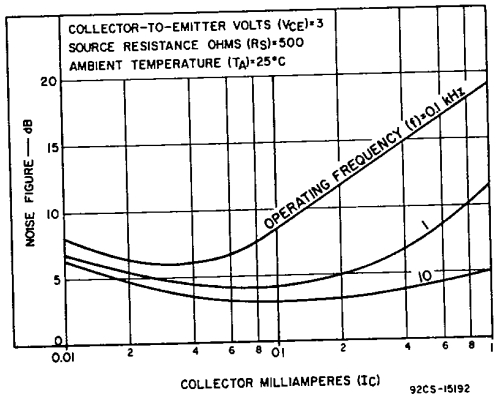


*Fig.9(a) - Typical noise figure vs collector current.*

# CA3045, CA3046

## DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR

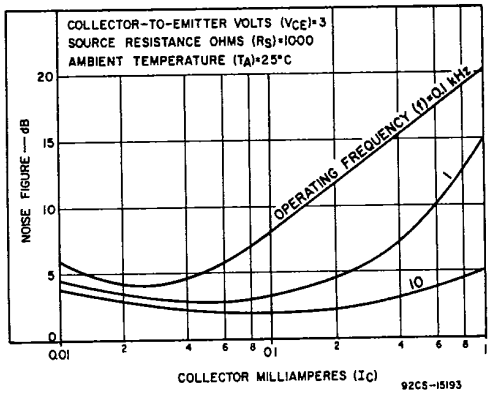


*Fig.9(b) - Typical noise figure vs collector current.*

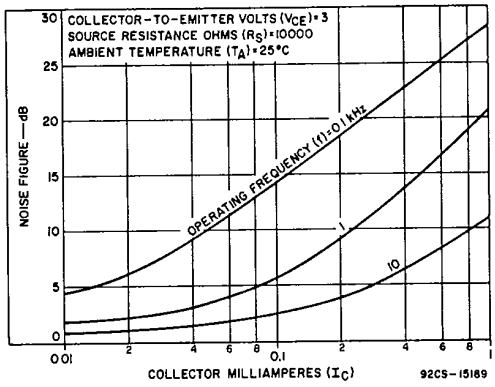


*Fig.9(c) - Typical noise figure vs collector current.*

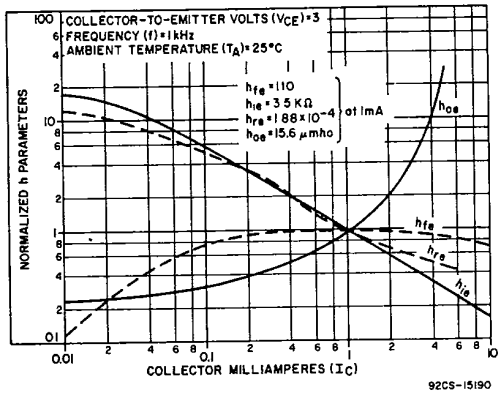


*Fig.10 - Typical normalized forward current-transfer ratio, short-circuit input impedance, open-circuit output impedance, and open-circuit reverse voltage-transfer ratio vs collector current.*

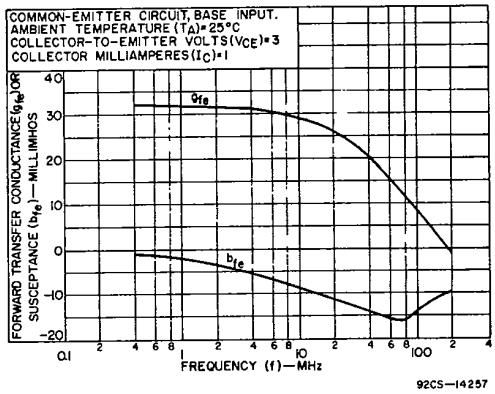


*Fig.11 - Typical forward transfer admittance vs frequency.*

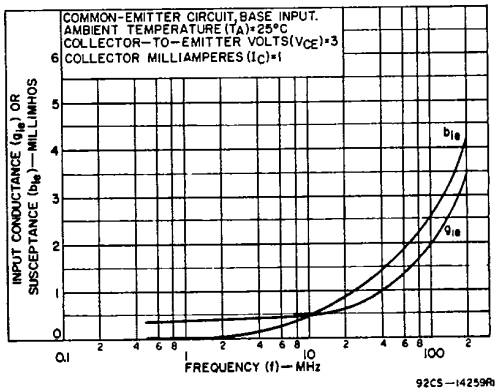


*Fig.12 - Typical input admittance vs frequency.*

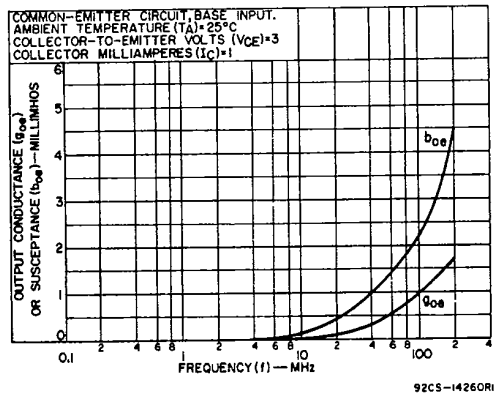


*Fig.13 - Typical output admittance vs frequency.*

# CA3045, CA3046

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## DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR

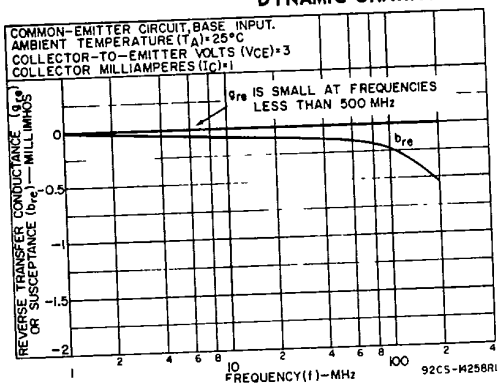


*Fig.14 - Typical reverse transfer admittance vs frequency.*

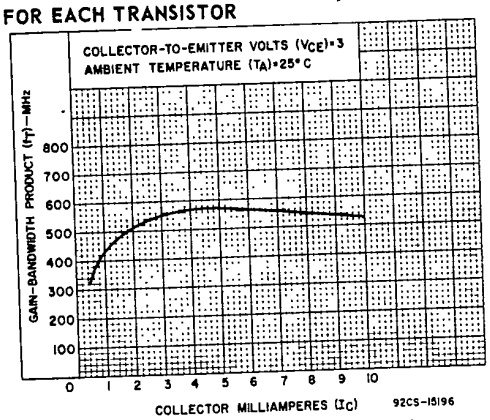


*Fig.15 - Typical gain-bandwidth product vs collector current.*