HOLT INC.
INTEGRATED CIRCUITS

HI-1582

April 2015

MIL-STD-1553 / MIL-STD-1760
3.3V Single Transceiver

DESCRIPTION

The HI-1582 low power CMOS transceiver is designed to meet the requirements of the MIL-STD-1553 and MIL-STD-1760 specifications. It is a pin-compatible, form and fit drop-in replacement for the Data Device Corporation MIL-STD-1553 transceiver, BU-63133L8.

The transmitter section of each bus takes complementary CMOS / TTL Manchester II bi-phase data and converts it to differential voltages suitable for driving the bus isolation transformer. A transmitter inhibit control signal is provided.

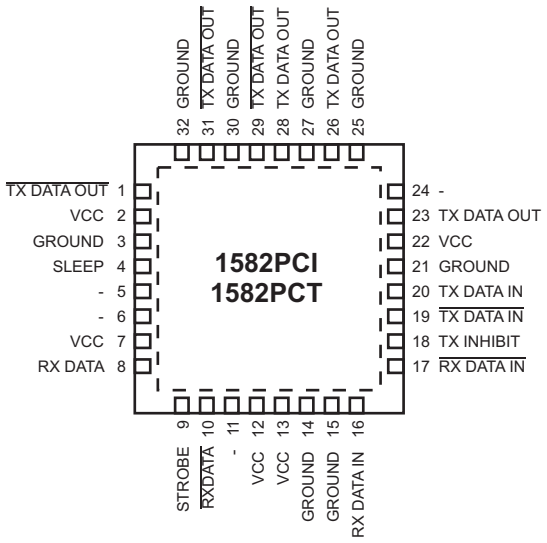
The receiver section converts the 1553 bus bi-phase data to complementary CMOS / TTL data suitable for input to a Manchester decoder. The receiver has a separate enable input pin, STROBE, which, when low, forces the receiver outputs to logic "0".

The HI-1582 is packaged in a 32-pin plastic chip-carrier package (QFN) with an integral exposed heatsink on the package bottom. The heatsink may be soldered to the PCB ground plane for optimal thermal dissipation. The HI-1582 is available in industrial (-40°C to +85°C) or extended (-55°C to +125°C) temperature range options.

FEATURES

- Compliant to MIL-STD-1553A and B, MIL-STD-1760 and ARINC 708A
- 3.3V single supply operation
- Small 7mm x 7mm 32-pin plastic chip-scale package
- Less than 0.5W maximum power dissipation
- Single Transceiver allows full dual redundancy
- Drop in replacement for Data Device Corporation BU-63133L8

PIN CONFIGURATIONS



32 Pin Plastic 7mm x 7mm Chip-scale package

PIN DESCRIPTIONS

PIN	SYMBOL	FUNCTION	DESCRIPTION
1, 29, 31	$\overline{\text{TX DATA OUT}}$	Analog Output	Inverted transmitter output to MIL-STD-1553 bus isolation transformer. Connect all three pins together.
2, 7, 12, 13, 22	VCC	Power Supply	+3.3V power. Connect all five pins.
3, 14, 15, 21 25, 27, 30, 32	GROUND	Power Supply	Ground. Connect all eight pins.
4	SLEEP	Digital Input	If high, inhibits transmitter. Internal 80kΩ pull-down
5, 6, 11, 24	-	-	Not connected
8	RX DATA	Digital Output	Receiver Output
9	STROBE	Digital Input	Receiver strobe input. Receiver outputs are both zero if STROBE is low. Internal 80kΩ pull-up.
10	$\overline{\text{RX DATA}}$	Digital Output	Inverted receiver output
16	RX DATA IN	Analog Input	Receiver input from MIL-STD-1553 bus isolation transformer
17	$\overline{\text{RX DATA IN}}$	Analog Input	Inverted receiver input from MIL-STD-1553 bus isolation transformer
18	TX INHIBIT	Digital Input	If high, inhibits transmitter. Internal 80kΩ pull-up
19	$\overline{\text{TX DATA IN}}$	Digital Input	Inverted transmitter input. Internal 80kΩ pull-down
20	TX DATA IN	Digital Input	Transmitter input. Internal 80kΩ pull-down
23, 26, 28	TX DATA OUT	Analog Output	Transmitter output to MIL-STD-1553 bus isolation transformer. Connect all three pins together.

FUNCTIONAL DESCRIPTION

The HI-1582 data bus transceiver contains differential voltage source drivers and differential receivers. It is intended for applications using a MIL-STD-1553 A/B data bus. The device produces a trapezoidal output waveform during transmission.

TRANSMITTER

Data input to the device's transmitter section is from the complementary CMOS inputs TX DATA IN and $\overline{\text{TX DATA IN}}$. The transmitter accepts Manchester II bi-phase data and converts it to differential voltages on TX DATA OUT and $\overline{\text{TX DATA OUT}}$. The transceiver outputs are either direct-coupled or transformer-coupled to the MIL-STD-1553 data bus. Both coupling methods produce a nominal voltage on the bus of approximately 7.5 volts peak to peak at the MIL-STD-1553 bus.

The transmitter is automatically inhibited and placed in the high impedance state when both TX DATA IN and $\overline{\text{TX DATA IN}}$ are driven with the same logic input state. A logic "1" applied to the TX INHIBIT or SLEEP input forces the transmitter to the high impedance state, regardless of the state of TX DATA IN and $\overline{\text{TX DATA IN}}$.

The SLEEP pin is logically ORed with the TX INHIBIT pin. In the obsolete BU-63133L8, the SLEEP pin also reduced idle-state supply current from 30mA to 6mA maximum. The HI-1582 does not require supply current control; its idle-state (receive mode) current is 4 mA nominal, lower than BU-63133L8 sleep current.

RECEIVER

The receiver accepts bi-phase differential data from the MIL-STD-1553 bus through the same direct or transformer coupled interface at the RX DATA IN and $\overline{\text{RX DATA IN}}$ pins. The receiver's differential input stage drives a filter and threshold comparator to produce CMOS data at the RX DATA OUT and $\overline{\text{RX DATA OUT}}$ output pins.

The receiver outputs are forced to a logic "0" when the STROBE pin is low.

MIL-STD-1553 BUS INTERFACE

A direct-coupled interface (see Figure 4) uses a 1:2.5 ratio isolation transformer and two 55 ohm isolation resistors between the transformer and the bus. The primary center-tap of the isolation transformer must be connected to VDD (3.3V).

In a transformer-coupled interface (see Figure 4), the transceiver is also connected to a 1:2.5 isolation transformer. The far end of the stub cable is connected to a 1:1.4 bus coupling transformer, which requires two coupling resistors equal to 75% of the bus characteristic impedence (Zo) between the coupling transformer and the bus.

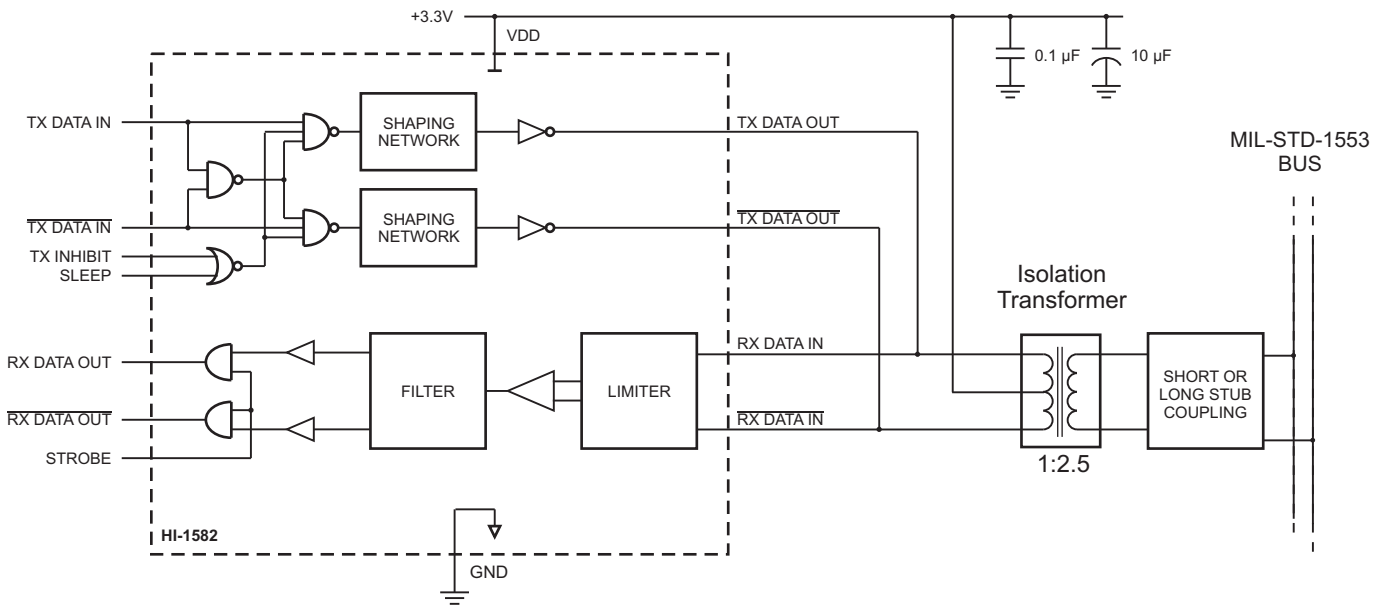


Figure 1. Block Diagram

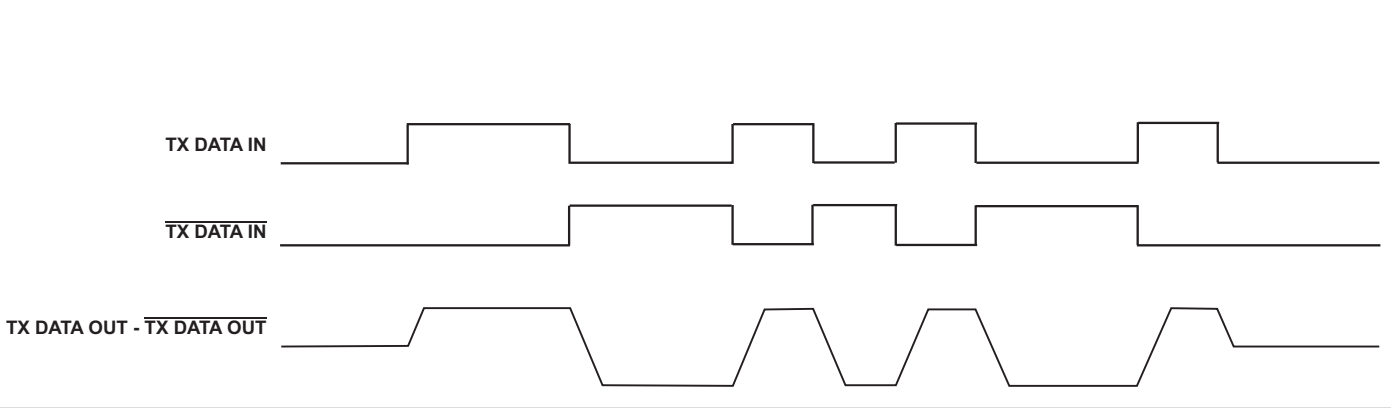


Figure 2. Transmit Waveform - Example Pattern

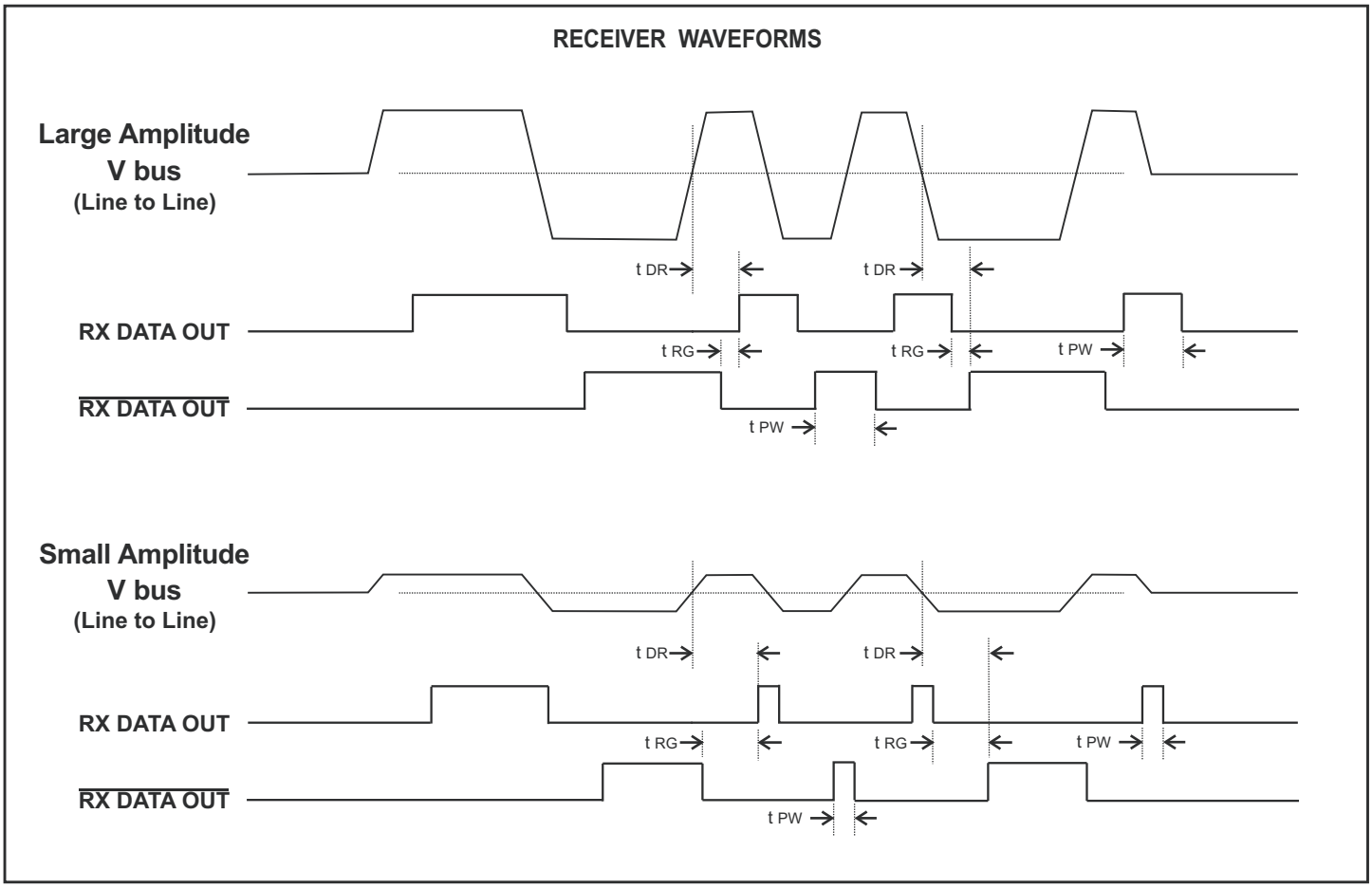


Figure 3. Receive Waveform - Example Pattern

ABSOLUTE MAXIMUM RATINGS

Supply voltage (V_{CC})	-0.3 V to +5 V
Logic input voltage range	-0.3 V dc to +3.6 V
Driver peak output current	+1.0 A
Power dissipation at 25°C derate 7mW/°C	1.5 W
Solder Temperature (reflow)	260°C
Junction Temperature	175°C
Storage Temperature	-65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

Supply Voltage VDD..... 3.3V... ±10%
Temperature Range Industrial Screening.....-40°C to +85°C Hi-Temp Screening.....-55°C to +125°C

NOTE: Stresses above absolute maximum ratings or outside recommended operating conditions may cause permanent damage to the device. These are stress ratings only. Operation at the limits is not recommended.

DC ELECTRICAL CHARACTERISTICS

VCC = 3.3 V, GND = 0V, T_A = Operating Temperature Range (unless otherwise specified).

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Operating Voltage	VDD		3.0	3.3	3.6	V
Total Supply Current	ICC1	Not Transmitting		4	10	mA
	ICC2	Transmit @ 100% duty cycle Transformer coupled 70 Ohm resistive load		800	900	mA
Power Dissipation	PD1	Not Transmitting		15	60	mW
	PD2	Transmit @ 100% duty cycle Transformer coupled 70 Ohm resistive load		0.3	0.5	W
Min. Input Voltage (Logic 1)	V_{IH}	Digital inputs	70%			V_{CC}
Max. Input Voltage (Logic 0)	V_{IL}	Digital inputs			30%	V_{CC}
Input Current (Logic 1)	I_{IH}	TX DATA IN, TX DATA IN, TX INHIBIT, SLEEP	20		100	µA
		STROBE			20	µA
Max. Input Current (Logic 0)	I_{IL}	TX DATA IN, TX DATA IN, TX INHIBIT, SLEEP	-20			µA
		STROBE	-100		-20	µA
Min. Output Voltage (Logic 1)	V_{OH}	I_{OUT} = -2.0mA, Digital outputs	V_{CC} - 0.4			V
Max. Output Voltage (Logic 0)	V_{IH}	I_{OUT} = 2.0mA, Digital outputs			0.4	V
RECEIVER (Measured at Point "A_D" in Figure 5 unless otherwise specified)						
Input resistance	R_{IN}	Differential (at chip pins)	20			Kohm
Input capacitance	C_{IN}	Differential			5	pF
Common mode rejection ratio	CMRR		40			dB
Input Level	V_{IN}	Differential			9	Vp-p
Input common mode voltage	V_{ICM}		-10.0		10.0	V-pk
Threshold Voltage - Direct-coupled Detect Measured at Point "A_D" in Figure 5 using 1 Mhz sinusoid across 35 Ohm load	V_{THD}	Pulse outputs present at RX DATA OUT / $\overline{\text{RX DATA OUT}}$	1.15			Vp-p
No Detect	V_{THND}	No pulse outputs at RX DATA OUT / $\overline{\text{RX DATA OUT}}$			0.28	Vp-p
Threshold Voltage - Transformer-coupled Detect Measured at Point "A_T" in Figure 6 using 1 Mhz sinusoid across 70 Ohm load	V_{THD}	Pulse outputs present at RX DATA OUT/$\overline{\text{RX DATA OUT}}$	0.86			Vp-p
No Detect	V_{THND}	No pulse outputs at RX DATA OUT / $\overline{\text{RX DATA OUT}}$			0.20	Vp-p

DC ELECTRICAL CHARACTERISTICS (cont.)

VCC = 3.3 V, GND = 0V, T_A =Operating Temperature Range (unless otherwise specified).

TRANSMITTER (Measured at Point "A_D" in Figure 5 unless otherwise specified)							
Output Voltage	Direct coupled	V_{OUT}	35 ohm load (Measured at Point "A_D" in Figure 5)	6.0		9.0	Vp-p
	Transformer coupled	V_{OUT}	70 ohm load (Measured at Point "A_T" in Figure 6)	20.0		27.0	Vp-p
Output Noise		V_{ON}	Differential, inhibited			10.0	mVp-p
Output Dynamic Offset Voltage	Direct coupled	V_{DYN}	35 ohm load (Measured at Point "A_D" in Figure 5)	-90		90	mV
	Transformer coupled	V_{DYN}	70 ohm load (Measured at Point "A_T" in Figure 6)	-250		250	mV
Output resistance		R_{OUT}	Differential, not transmitting	10			Kohm
Output Capacitance		C_{OUT}	1 MHz sine wave			15	pF

AC ELECTRICAL CHARACTERISTICS

VCC = 3.3 V, GND = 0V, T_A =Operating Temperature Range (unless otherwise specified).

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
RECEIVER (Measured at Point "A_T" in Figure 6)						
Receiver Delay (Note 1)	t_{DR}	From input signal zero crossing to corresponding zero crossing in RX DATA OUT or $\overline{\text{RX DATA OUT}}$			450 Note 4	ns
Receiver output pulse width (Note 1)	t_{PW}		70 Note 3			ns
Receiver gap time (Note 1)	t_{RG}	Spacing between RX DATA OUT and $\overline{\text{RX DATA OUT}}$ pulses	90 Note 2		430 Note 3	ns
Receiver Enable Delay	t_{REN}	From STROBE rising or falling edge to RX DATA OUT or $\overline{\text{RX DATA OUT}}$			40	ns

Note 1. This parameter varies with receive signal amplitude. See Receiver Waveforms, Figure 3.
Note 2. Measured using a 1 MHz sinusoid, 20 V peak to peak, line-to-line at Point "AT" (Guaranteed but not tested.)
Note 3. Measured transformer-coupled mode using a 1 MHz sinusoid, 860 mV peak to peak line-to-line at Point "AT" (100% tested).
Note 4. Measured transformer-coupled mode using a 1 MHz sinusoid 860 mV peak to peak, line-to-line at Point "AT".

TRANSMITTER (Measured at Point "A_T" in Figure 6)						
Driver Delay	t_{DT}	TX DATA IN, $\overline{\text{TX DATA IN}}$ to TX DATA OUT, $\overline{\text{TX DATA OUT}}$			150	ns
Rise time	tr	70 ohm resistive load	100		300	ns
Fall Time	tf	70 ohm resistive load	100		300	ns
Transmit Inhibit Delay	t_{DI-H}	Disable bus output			100	ns
	t_{DI-L}	Enable bus output			150	ns

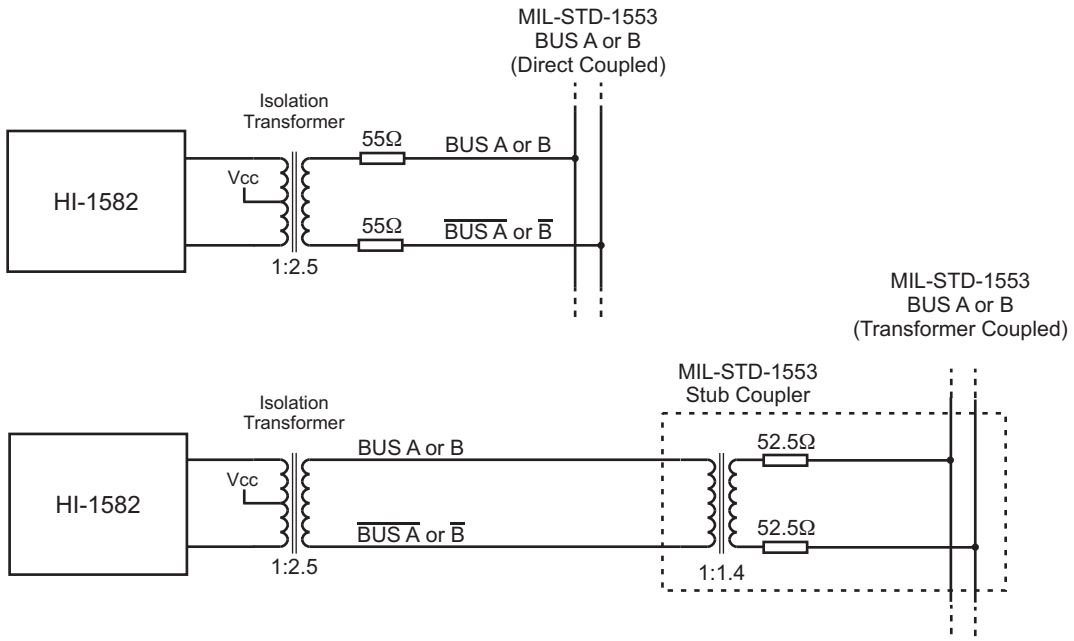


Figure 4. Bus Connection Examples using HI-1582

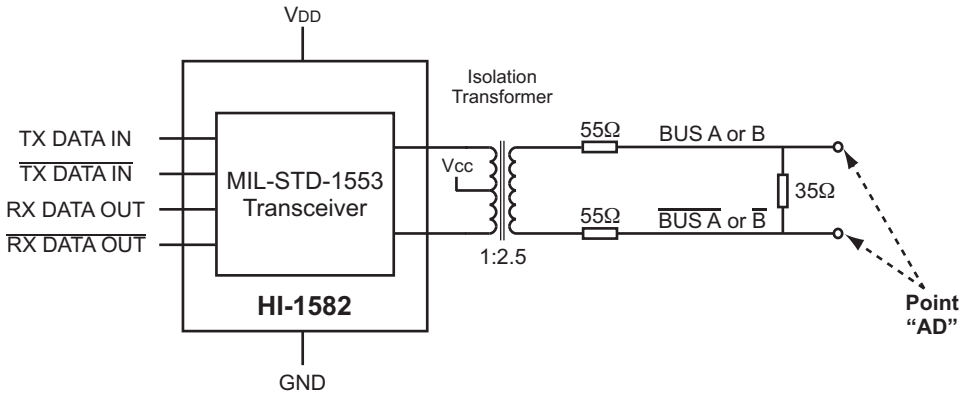


Figure 5. Direct Coupled Test Circuit

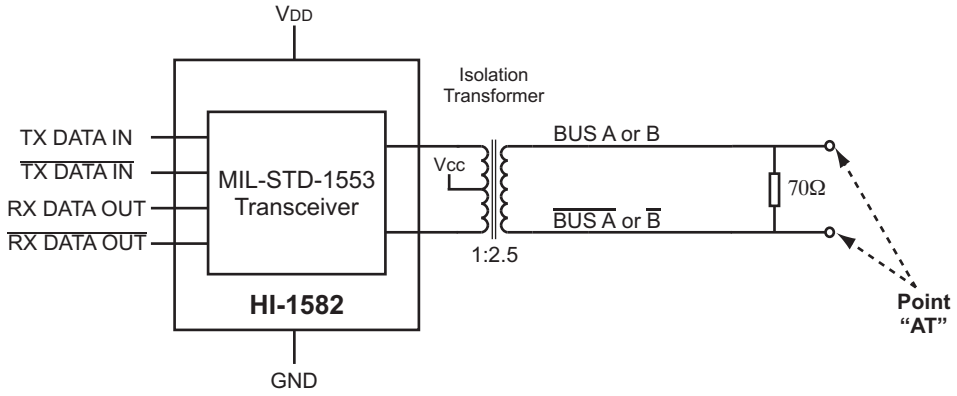


Figure 6. Transformer Coupled Test Circuit

HEAT SINK - CHIP-SCALE PACKAGE

The HI-1582PCI/T/M uses a 32-pin thermally enhanced QFN package. The package includes a metal heat sink located on the bottom surface of the device. This heat sink may be soldered down to the printed circuit board for optimum thermal dissipation. The heat sink is electrically isolated and may be soldered to any convenient power or ground plane.

APPLICATIONS NOTE

Holt Applications Note AN-500 provides circuit design notes regarding the use of Holt's family of MIL-STD-1553 transceivers. Layout considerations, as well as recommended interface and protection components are included.

THERMAL CHARACTERISTICS

PART NUMBER	PACKAGE STYLE	CONDITION	$Ø_{JA}$	JUNCTION TEMPERATURE		
				T_A=25°C	T_A=85°C	T_A=125°C
HI-1582PCI / T / M	32-pin Plastic chip-scale package	Heat sink unsoldered	49°C/W	50°C	110°C	150°C

Data taken at VDD=3.3V, continuous transmission at 1Mbit/s, single transmitter enabled.

RECOMMENDED TRANSFORMERS

The HI-1582 transceiver has been characterized for compliance with the electrical requirements of MIL-STD-1553 when used with the following transformers. Holt recommends the Premier Magnetics parts as offering the best combination of electrical performance, low cost and small footprint.

MANUFACTURER	PART NUMBER	APPLICATION	TURNS RATIO	DIMENSIONS
Premier Magnetics	PM-DB2791S	Isolation	Single 1:2.5	.400 x .400 x .185 inches
Premier Magnetics	PM-DB2756	Isolation	Dual 1:2.5	.930 x .575 x .185 inches
Premier Magnetics	PM-DB2702	Stub coupling	1:1.4	.625 x .500 x .250 inches

ORDERING INFORMATION

HI - 1582 PC x F

PART NUMBER	LEAD FINISH
F	NiPdAu (Pb-free RoHS compliant)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C TO +85°C	I	No
T	-55°C TO +125°C	T	No
M	-55°C TO +125°C	M	Yes

PART NUMBER	PACKAGE DESCRIPTION
PC	32 PIN PLASTIC CHIP-SCALE PACKAGE LPCC (32PCS7)

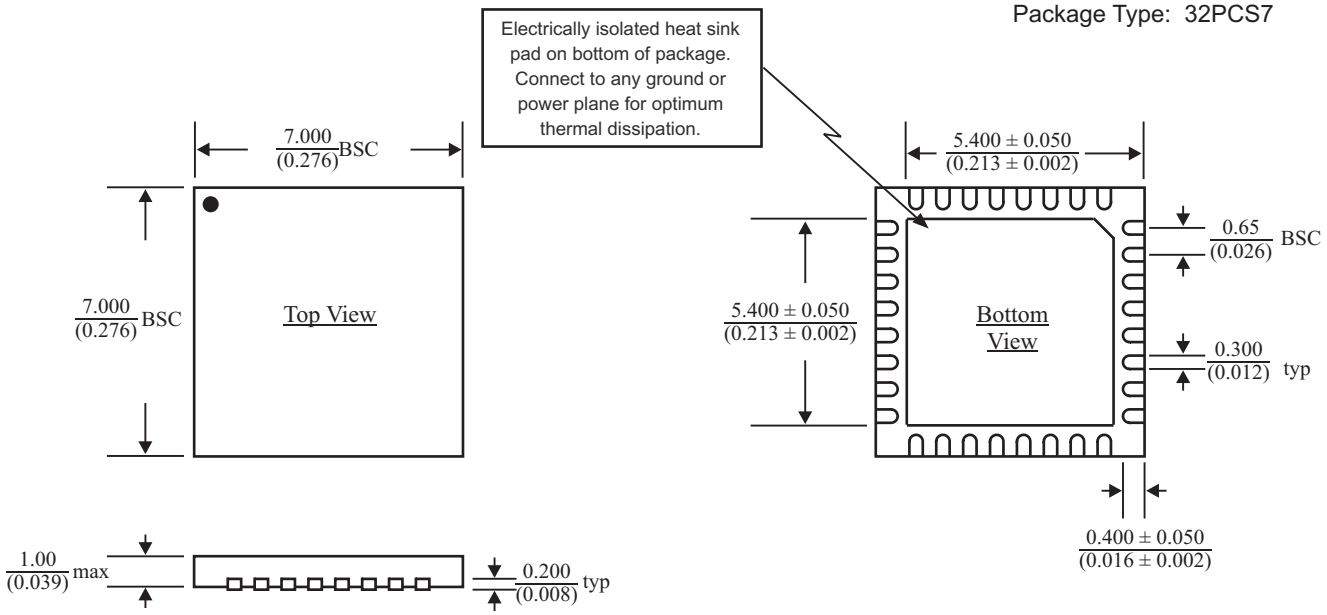
REVISION HISTORY

Document	Rev.	Date	Description of Change
DS1582	New.	05/23/14	Initial Release.
	A	03/12/15	Change internal pull-down on TX INHIBIT pin from 80kΩ pull-down to 80kΩ pull-up. Clarify Bus labels on Figures 4 and 5.

32-PIN PLASTIC CHIP-SCALE PACKAGE (QFN)

millimeters (inches)

Package Type: 32PCS7



BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)