VNQ860-E, VNQ860SP-E

Quad channel high-side driver

SO 20

PowerSO-10™

Features

Type	$R_{DS(on)}$[1]	I_{out}	V_{CC}
VNQ860-E VNQ860SP-E	270 mΩ	0.25 A	36 V

1. Per each channel

- CMOS compatible I/Os
- Undervoltage and overvoltage shutdown

- Shorted load protection
- Thermal shutdown
- Very low standby current
- Protection against loss of ground

Description

The VNQ860-E and the VNQ860SP-E are monolithic devices realized in STMicroelectronics VIPower M0-3 technology, intended to drive any kind of load with one side connected to ground. Active current limitation combined with thermal shutdown and automatic restart protect the device against overload. The device automatically turns OFF in case of ground pin disconnection. This device is especially suitable for IEC 61131 compliant industrial applications.
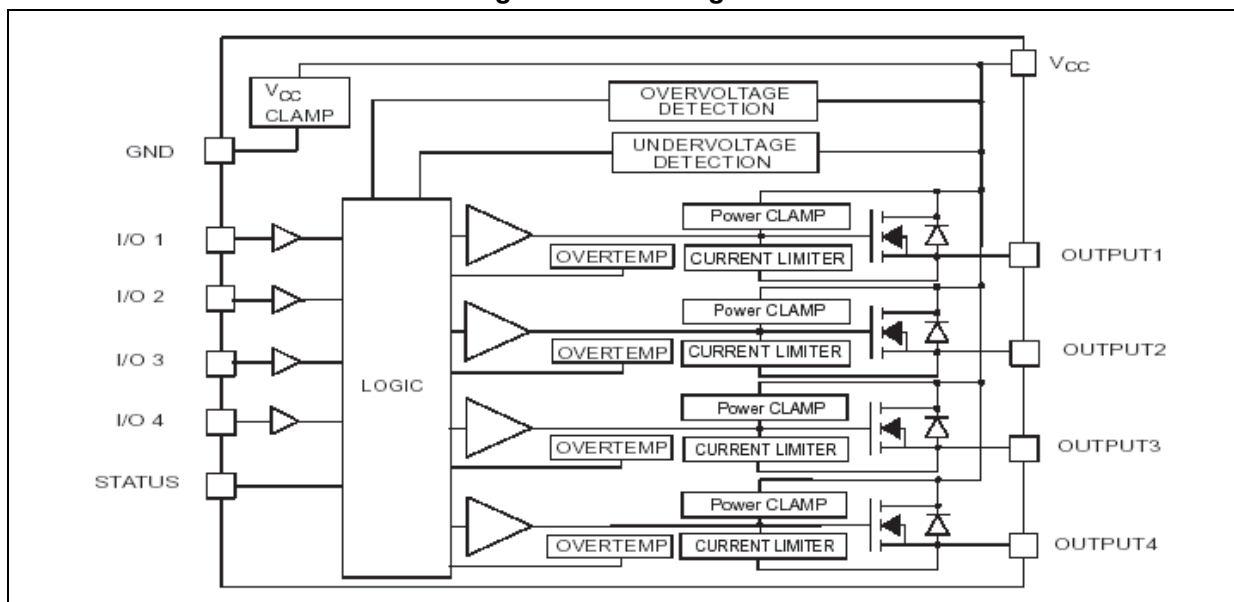
Figure 1. Block diagram

Contents

1 Maximum ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		SO20	**PowerSO-10**	
V_{CC}	DC supply voltage	41		V
$-V_{CC}$	Reverse DC supply voltage	-0.3		V
$-I_{GND}$	DC reverse ground pin	-200		mA
I_{OUT}	DC output current	Internally limited		A
$-I_{OUT}$	Reverse DC output current	-2		A
I_{IN}	DC input current	± 10		mA
V_{IN}	Input voltage range	$-3/+V_{CC}$		V
V_{STAT}	DC status voltage	$+ V_{CC}$		V
V_{ESD}	Electrostatic discharge (R = 1.5 kΩ, C = 100 pF)	2000		V
P_{tot}	Power dissipation at T_c <= 25 °C	16	90	W
T_J	Junction operating temperature	Internally limited		°C
T_c	Case operating temperature	-40 to 150		°C
T_{stg}	Storage temperature	-55 to 150		°C

Table 2. Thermal data

Symbol	Parameter		Values		Unit
			SO20	**PowerSO-10**	
$R_{th(JP)}$	Thermal resistance junction-pins	Max.	8	-	°C/W
$R_{th(JA)}$	Thermal resistance junction-ambient	Max.	58	52 [1]	°C/W
				37 [2]	
$R_{th(JC)}$	Thermal resistance junction-case	Max.	-	1.4	°C/W

1. When mounted on FR4 printed circuit board with 0.5 cm^2 of copper area (at least 35 μ thick) connected to all V_{CC} pins.

2. When mounted on FR4 printed circuit board with 6 cm^2 of copper area (at least 35 μ thick) connected to all V_{CC} pins.

2   Pin connection
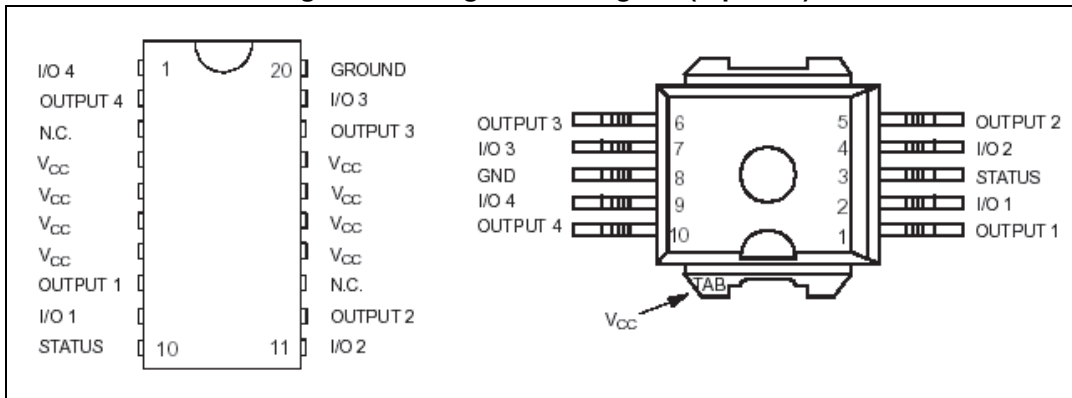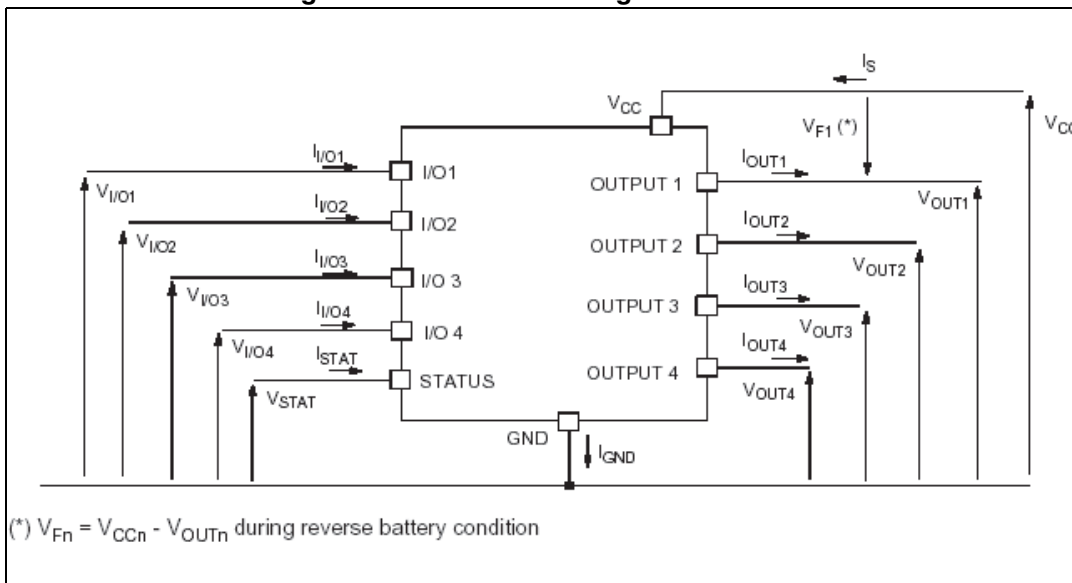
Figure 2. Configuration diagram (top view)

Table 3. Pin connection

Connection / pin	Status	N.C.	Output	Input
Floating	X	X	X	X
To ground		X		Through 10 kΩ resistor

Figure 3. Current and voltage conventions

$(*)\ V_{Fn} = V_{CCn} - V_{OUTn}$ during reverse battery condition

3   Electrical characteristics

$8\ V < V_{CC} < 36\ V$; $-40\ °C < T_J < 150\ °C$; unless otherwise specified.

Table 4. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		5.5		36	V
V_{USD}	Undervoltage shutdown		3	4	5.5	V
V_{OV}	Overvoltage shutdown		36	42	48	V
R_{ON}	On state resistance (per channel)	$I_{OUT} = 0.25\ A$; $T_J = 25\ °C$; $I_{OUT} = 0.25\ A$;			270 540	$m\Omega$
I_S	Supply current	OFF state; $V_{CC} = 24\ V$; $T_C = 25\ °C$ ON state (all channels ON)		70 5	120 10	μA mA
I_{LGND}	Output current	$V_{CC} - V_{STAT} = V_{IN} = V_{GND} = 24\ V$; $V_{OUT} = 0\ V$			1	mA
$I_{L(OFF)}$	OFF state output current	$V_{IN} = V_{OUT} = 0\ V$	0		10	μA
$I_{OUTleak}$	OFF state output leakage current	$V_{IN} = V_{GND} = 0\ V$; $V_{CC} = V_{OUT} = 24\ V$; $T_A = 25\ °C$			240	μA
$I_{OUTleak}$	OFF state output leakage current	$V_{IN} = V_{GND} = 0\ V$; $V_{CC} = 24\ V$; $V_{OUT} = 10\ V$; $T_A = 25\ °C$			100	μA

Table 5. Switching ($V_{CC} = 24\ V$)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{(ON)}$	Turn-on delay time of output current	$R_L = 96\ \Omega$ from V_{IN} rising edge to $V_{OUT} = 2.4\ V$	-	10	-	μs
$t_{(OFF)}$	Turn-off delay time of output current	$R_L = 96\ \Omega$ from V_{IN} rising edge to $V_{OUT} = 21.6\ V$	-	40	-	μs
$(dV_{OUT}/dt)_{on}$	Turn-on voltage slope	$R_L = 96\ \Omega$ from $V_{OUT} = 2.4\ V$ to 19.2 V	-	0.75	-	V/ μs
$(dV_{OUT}/dt)_{off}$	Turn-off voltage slope	$R_L = 96\ \Omega$ from $V_{OUT} = 21.6\ V$ to 2.4 V	-	0.25	-	V/ μs

Table 6. Protections (per channel)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{lim}	Current limitation		0.35	0.7	1.1	A
$T_{(hyst)}$	Thermal hysteresis		7	15		°C
T_{TSD}	Thermal shutdown temperature		150	175	200	°C
T_R	Reset temperature		135			°C
V_{demag}	Turn-off output clamp voltage	I_{OUT} = 0.25 A, V_{CC} = 24 V	V_{CC}-59	V_{CC}-52	V_{CC}-47	V

Table 7. Logic input (per channel)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Low level input voltage			-	1.25	V
I_{IL}	Low level input current	V_{IN} = 1.25 V	1	-		μA
V_{IH}	High level input voltage		3.25	-		V
I_{IH}	High level input current	V_{IN} = 3.25 V		-	10	μA
$V_{I(HYST)}$	Input hysteresis voltage		0.5	-		V
I_{IN}	Input current	V_{IN} = V_{CC} = 36 V		-	200	μA
VOL	I/O output voltage	I_{IN} = 5 mA (fault condition)		-	1	V

Table 8. Status pin

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
VSTAT	Status low output voltage	I_{STAT} = 5 mA (fault condition)	-	-	1	V
ILSTAT	Status leakage current	Normal operation; V_{STAT} = V_{CC} = 36 V	-	-	10	μA
C_{STAT}	Status pin input capacitance	Normal operation; V_{STAT} = 5 V	-	-	100	pF

Table 9. V_{CC} - output diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
VF	Forward on voltage	-I_{OUT} = 0.3 A; T_J = 150 °C	-	-	1	V

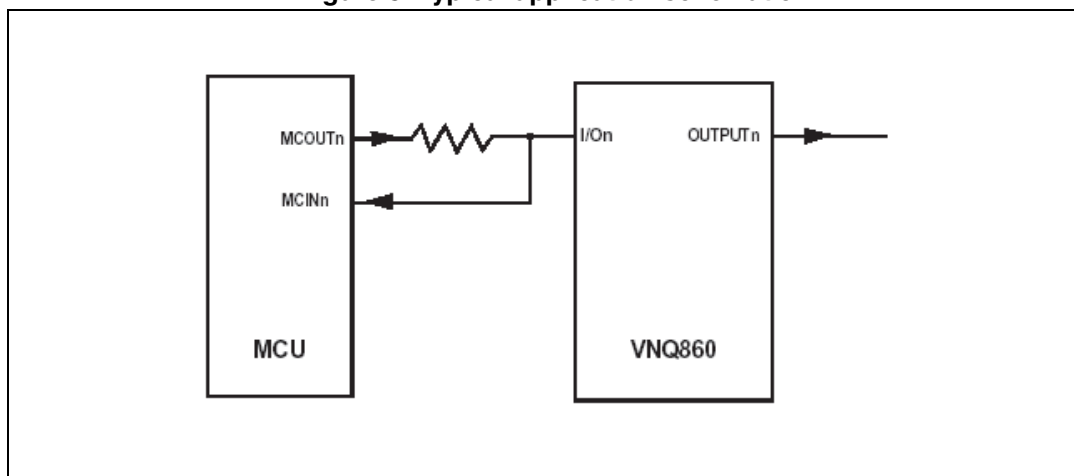# 4   Truth table and switching characteristics

Table 10. Truth table

Conditions	MCOUTn	I/On	OUTPUTn	STATUS
Normal operation	L H	L H	L H	H H
Current limitation	L H	L H	L X	H H
Overtemperature	L H	L Driven low	L L	L L
Undervoltage	L H	L H	L L	X X
Overvoltage	L H	L H	L L	H H

Figure 4. Switching characteristics
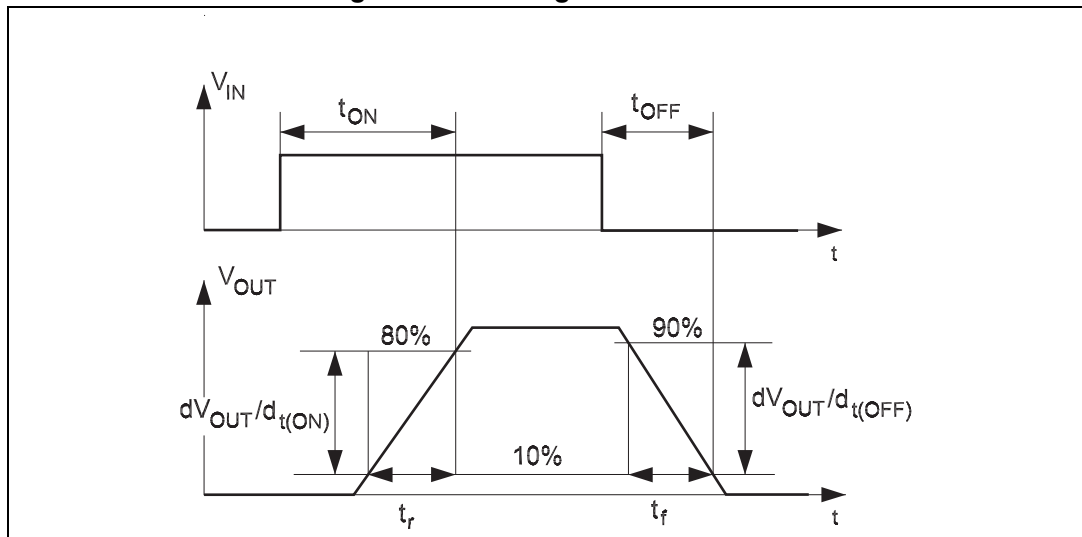
5 Typical application schematic

Figure 5. Typical application schematic

6   Waveforms

Figure 6. Waveforms
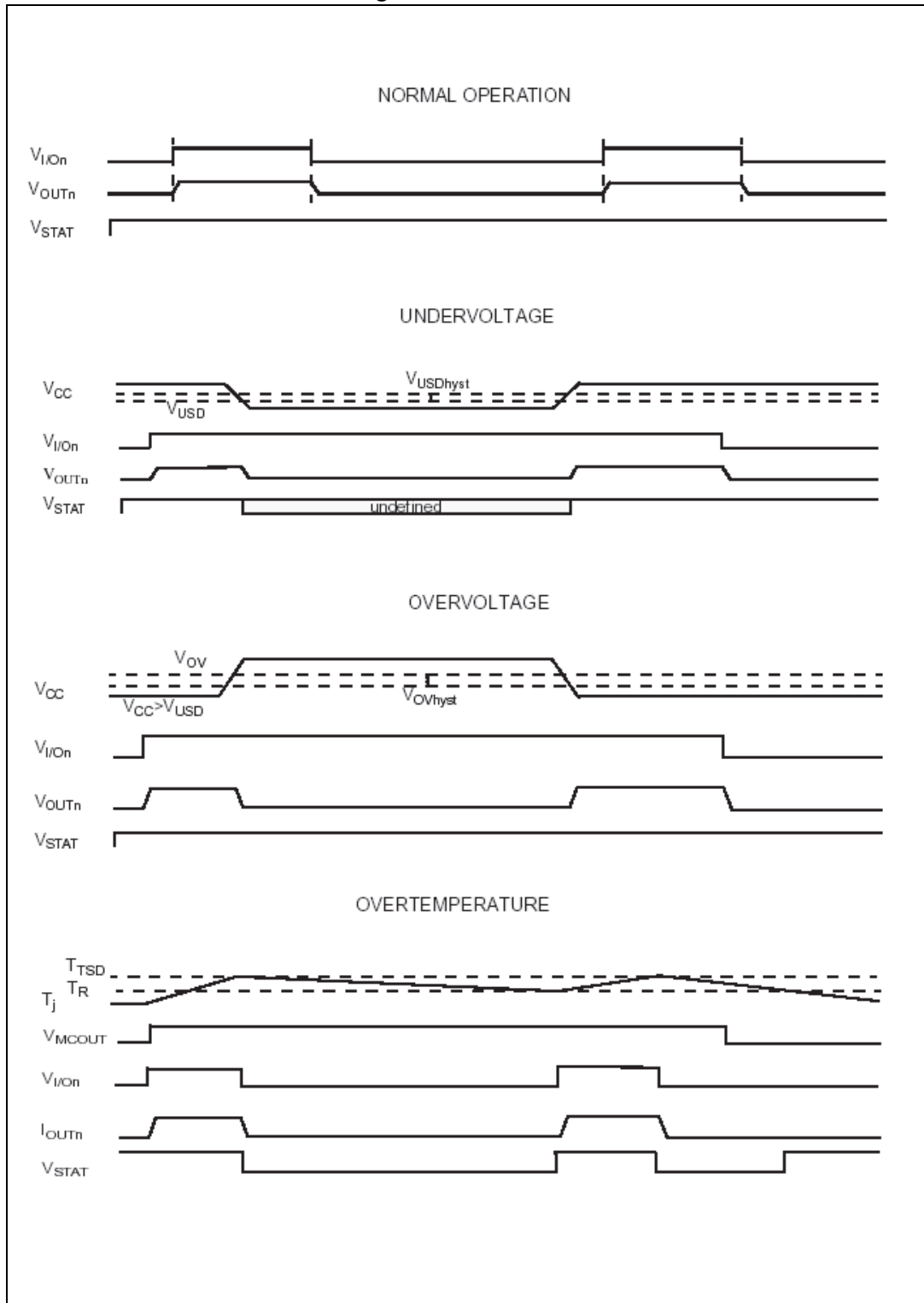
7   PowerSO-10™ thermal data

Figure 7. PowerSO-10™ PC board

Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area= 58mm x 58mm, PCB thickness=2mm, Cu thickness=35μm, Copper areas: from minimum pad lay-out to 8cm^2).
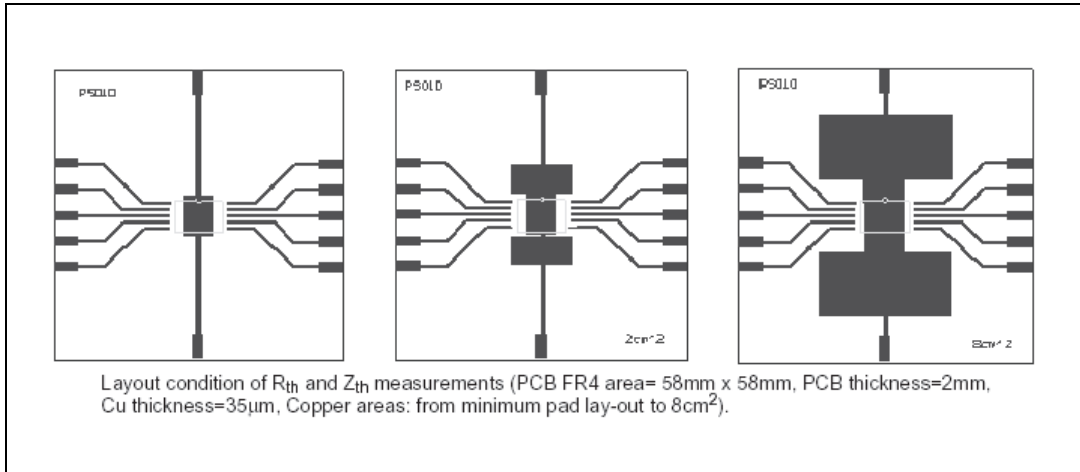
Figure 8. R$_{th(JA)}$ vs PBC copper area in open box free air condition
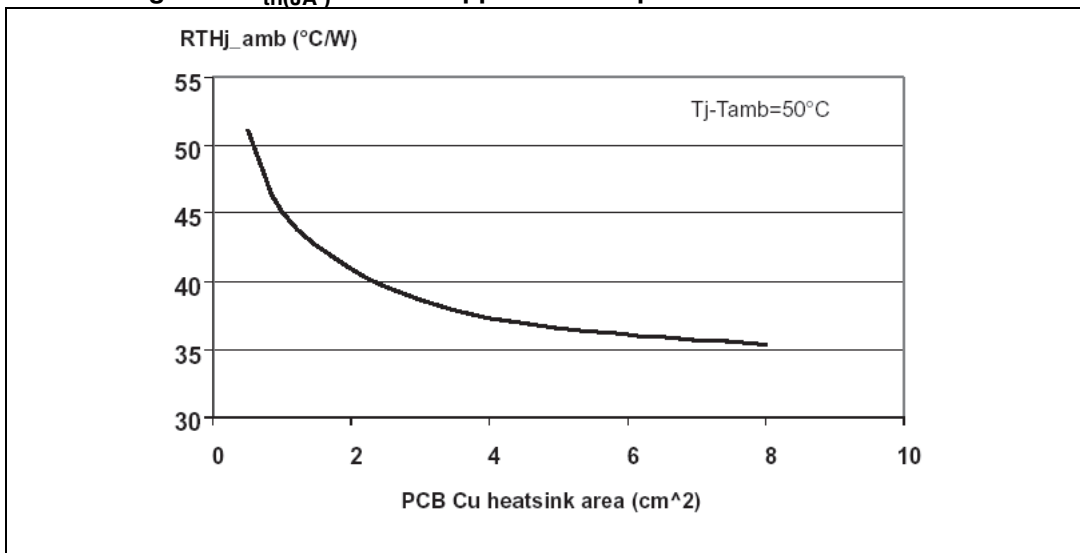
8 Reverse polarity protection

A solution to protect the IC against a reverse polarity condition is proposed in *Figure 9*.

This schematic is valid with any type of load connected to the outputs of the IC.

The R_{GND} resistor value can be selected according to the following conditions:

Equation 1

$R_{GND} \leq 600$ mV / (I_S in ON state max.).

Equation 2

$R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in *Table 1: Absolute maximum ratings*.

The power dissipation associated to R_{GND} during the reverse polarity condition is:

$PD = (-V_{CC})^2/R_{GND}$

This resistor can be shared by different ICs. In such case, I_S value, indicated in *Equation 1*, is the sum of the maximum ON-state currents of the different devices.

Please note that, if the microprocessor ground and the device ground are separated then the voltage drop across the R_{GND} (given by I_S in ON state max. * R_{GND}) produces a difference between the generated input level and the IC input signal level. This voltage drop varies depending on how many devices are ON in the case of several high-side switches sharing the same R_{GND}.

Figure 9. Reverse polarity protection
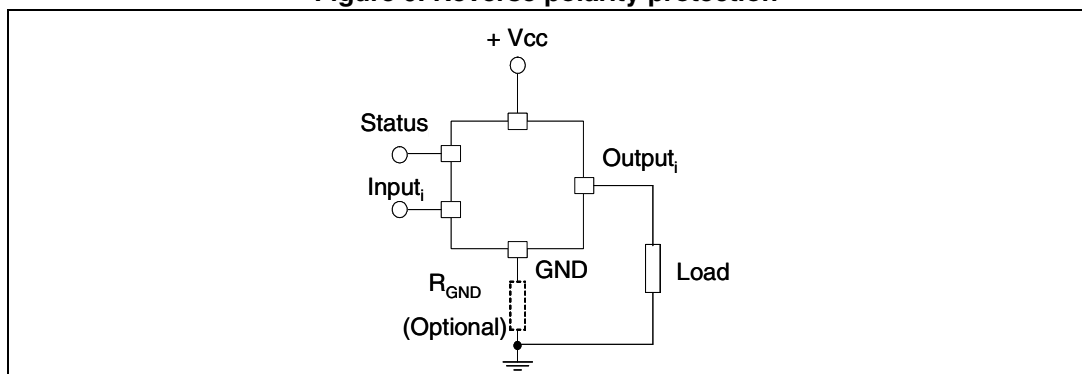
9 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 11. PowerSO-10™ mechanical data

Dim.	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	3.35		3.65	0.132		0.144
A1	0.00		0.10	0.000		0.004
B	0.40		0.60	0.016		0.024
c	0.35		0.55	0.013		0.022
D	9.40		9.60	0.370		0.378
D1	7.40		7.60	0.291		0.300
E	9.30		9.50	0.366		0.374
E1	7.20		7.40	0.283		0.291
E2	7.20		7.60	0.283		0.300
E3	6.10		6.35	0.240		0.250
E4	5.90		6.10	0.232		0.240
e		1.27			0.050	
F	1.25		1.35	0.049		0.053
H	13.80		14.40	0.543		0.567
h		0.50			0.002	
L	1.20		1.80	0.047		0.071
q		1.70			0.067	
a	0°		8°			

Figure 10. PowerSO-10™ package dimensions
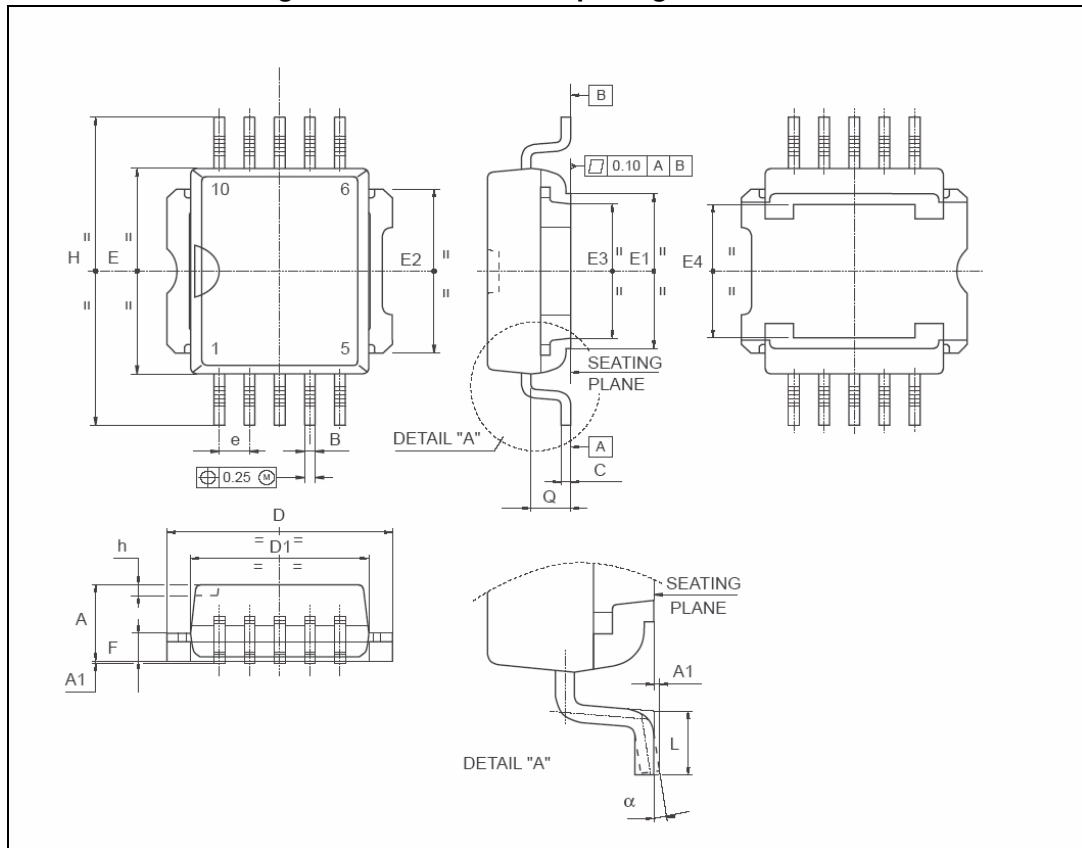
Figure 11. PowerSO-10™ suggested pad and tube shipment (no suffix)

	Base Q.ty	Bulk Q.ty	Tube length (± 0.5)	A	B	C (± 0.1)
Casablanca	50	1000	532	10.4	16.4	0.8
Muar	50	1000	532	4.9	17.2	0.8
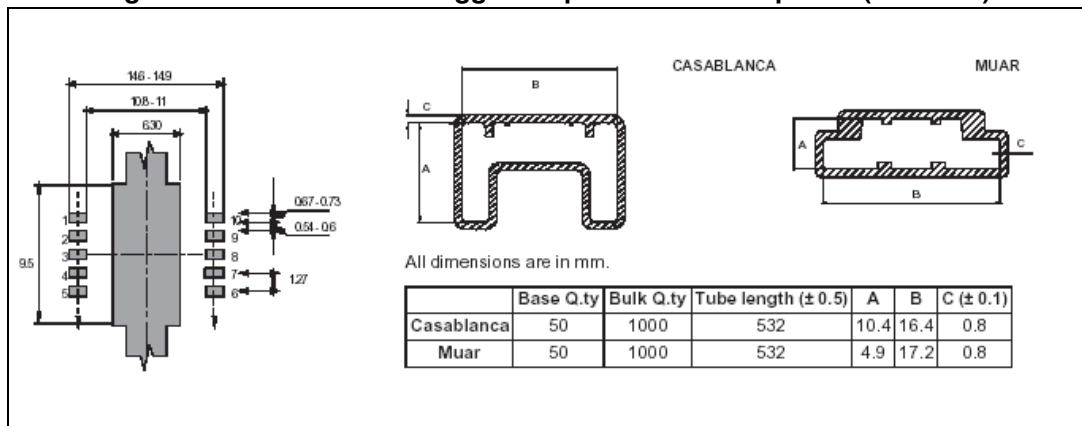
Figure 12. Tape and reel shipment (suffix "TR")

REEL DIMENSIONS

Base Q.ty	600
Bulk Q.ty	600
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	24.4
N (min)	60
T (max)	30.4

All dimensions are in mm.

TAPE DIMENSIONS

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	W	24
Tape Hole Spacing	P0 (± 0.1)	4
Component Spacing	P	24
Hole Diameter	D (± 0.1/-0)	1.5
Hole Diameter	D1 (min)	1.5
Hole Position	F (± 0.05)	11.5
Compartment Depth	K (max)	6.5
Hole Spacing	P1 (± 0.1)	2

All dimensions are in mm.

Figure 13. SO20 mechanical data and package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.35		2.65	0.093		0.104
A1	0.10		0.30	0.004		0.012
B	0.33		0.51	0.013		0.200
C	0.23		0.32	0.009		0.013
D [(1)]	12.60		13.00	0.496		0.512
E	7.40		7.60	0.291		0.299
e		1.27			0.050	
H	10.0		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

(1) "D" dimension does not include mold flash, protusions or gate burrs. Mold flash, protusions or gate burrs shall not exceed 0.15mm per side.

OUTLINE AND MECHANICAL DATA

SO20

0016022 D

Figure 14. SO20 tube shipment (no suffix)

Base Q.ty	40
Bulk Q.ty	800
Tube length (± 0.5)	532
A	3.5
B	13.8
C (± 0.1)	0.6

All dimensions are in mm.
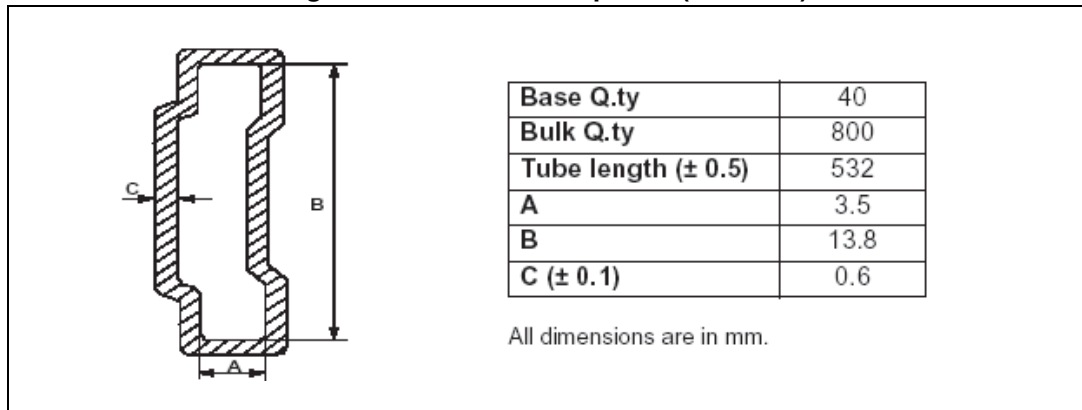
Figure 15. Tape and reel shipment (suffix "13TR")

REEL DIMENSIONS

Base Q.ty	1000
Bulk Q.ty	1000
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	24.4
N (min)	60
T (max)	30.4

TAPE DIMENSIONS

According to Electronic Industries Association
(EIA) Standard 481 rev. A, Feb 1986

Tape width	W	24
Tape Hole Spacing	P0 (± 0.1)	4
Component Spacing	P	12
Hole Diameter	D (± 0.1/-0)	1.5
Hole Diameter	D1 (min)	1.5
Hole Position	F (± 0.05)	11.5
Compartment Depth	K (max)	6.5
Hole Spacing	P1 (± 0.1)	2

All dimensions are in mm.

10 Ordering information

Table 12. Ordering information

Order codes	Package	Packaging
VNQ860-E	SO20	Tube
VNQ860SP-E	PowerSO-10™	
VNQ860TR-E	SO20	Tape and reel
VNQ860SPTR-E	PowerSO-10™	

11 Revision history

Table 13. Document revision history

Date	Revision	Changes
14-Jul-2005	1	Updates, new template
7-Nov-2005	2	Few updates
07-Jul-2008	3	Added *Section 8 on page 11*
28-Apr-2009	4	Updated *Figure 13 on page 15*
05-May-2010	5	Updated coverpage
31-Aug-2010	6	Updated *Table 10 on page 7*
15-Mar-2013	7	Updated *Table 1* and *Table 12*. Minor text changes.

Please Read Carefully: