

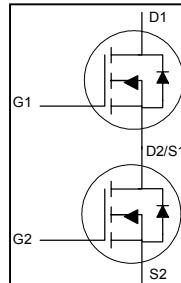


- ▼ Simple Drive Requirement
- ▼ Easy for Synchronous Buck Converter Application
- ▼ RoHS Compliant & Halogen-Free

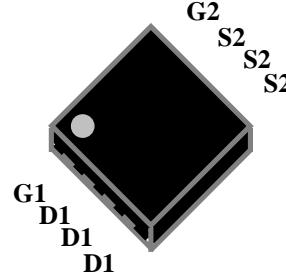
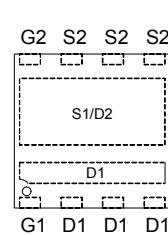
### Description

Advanced Power MOSFETs from APEC provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The control MOSFET (CH-1) and synchronous MOSFET (CH-2) co-package for synchronous buck converters.



CH-1	$BV_{DSS}$	30V
	$R_{DS(ON)}$	18mΩ
	$I_D$	21A
CH-2	$BV_{DSS}$	30V
	$R_{DS(ON)}$	10.5mΩ
	$I_D$	39A



PMPAK® 3 x 3

### Absolute Maximum Ratings@ $T_j=25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Rating		Units
		CH-1	CH-2	
$V_{DS}$	Drain-Source Voltage	30	30	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	$\pm 12$	V
$I_D @ T_c = 25^\circ\text{C}$	Drain Current (Chip Limited)	21	39	A
$I_D @ T_A = 25^\circ\text{C}$	Drain Current, $V_{GS} @ 10\text{V}^3$	8.3	11.8	A
$I_D @ T_A = 70^\circ\text{C}$	Drain Current, $V_{GS} @ 10\text{V}^3$	6.6	9.5	A
$I_{DM}$	Pulsed Drain Current <sup>1</sup>	40	40	A
$P_D @ T_A = 25^\circ\text{C}$	Total Power Dissipation <sup>3</sup>	1.9	2.2	W
$T_{STG}$	Storage Temperature Range	$-55$ to $150$		°C
$T_J$	Operating Junction Temperature Range	$-55$ to $150$		°C

### Thermal Data

Symbol	Parameter	Rating		Units
		CH-1	CH-2	
$R_{thj-c}$	Maximum Thermal Resistance, Junction-case	10	5	°C/W
$R_{thj-a}$	Maximum Thermal Resistance, Junction-ambient <sup>3</sup>	65	55	°C/W
$R_{thj-a}$	Maximum Thermal Resistance, Junction-ambient <sup>4</sup>	180	145	°C/W



# AP6950GYT-HF

## CH-1 Electrical Characteristics@ $T_j=25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$\text{BV}_{\text{DSS}}$	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=250\mu\text{A}$	30	-	-	V
$R_{\text{DS}(\text{ON})}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{\text{GS}}=10\text{V}, I_{\text{D}}=8\text{A}$	-	14	18	$\text{m}\Omega$
		$V_{\text{GS}}=4.5\text{V}, I_{\text{D}}=5\text{A}$	-	23.2	30	$\text{m}\Omega$
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=250\mu\text{A}$	1	1.4	3	V
$g_{\text{fs}}$	Forward Transconductance	$V_{\text{DS}}=10\text{V}, I_{\text{D}}=8\text{A}$	-	14	-	S
$I_{\text{DSS}}$	Drain-Source Leakage Current	$V_{\text{DS}}=24\text{V}, V_{\text{GS}}=0\text{V}$	-	-	10	$\text{uA}$
$I_{\text{GSS}}$	Gate-Source Leakage	$V_{\text{GS}}=+20\text{V}, V_{\text{DS}}=0\text{V}$	-	-	+100	nA
$Q_g$	Total Gate Charge	$I_{\text{D}}=8\text{A}$	-	4.2	6.7	nC
$Q_{\text{gs}}$	Gate-Source Charge	$V_{\text{DS}}=15\text{V}$	-	1.8	-	nC
$Q_{\text{gd}}$	Gate-Drain ("Miller") Charge	$V_{\text{GS}}=4.5\text{V}$	-	1.9	-	nC
$t_{\text{d}(\text{on})}$	Turn-on Delay Time	$V_{\text{DS}}=15\text{V}$	-	6.5	-	ns
$t_r$	Rise Time	$I_{\text{D}}=1\text{A}$	-	6	-	ns
$t_{\text{d}(\text{off})}$	Turn-off Delay Time	$R_{\text{G}}=3.3\Omega$	-	15	-	ns
$t_f$	Fall Time	$V_{\text{GS}}=10\text{V}$	-	3	-	ns
$C_{\text{iss}}$	Input Capacitance	$V_{\text{GS}}=0\text{V}$	-	450	720	pF
$C_{\text{oss}}$	Output Capacitance	$V_{\text{DS}}=15\text{V}$	-	70	-	pF
$C_{\text{rss}}$	Reverse Transfer Capacitance	$f=1.0\text{MHz}$	-	50	-	pF
$R_g$	Gate Resistance	$f=1.0\text{MHz}$	-	1.2	2.4	$\Omega$

## Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$V_{\text{SD}}$	Forward On Voltage <sup>2</sup>	$I_{\text{S}}=8\text{A}, V_{\text{GS}}=0\text{V}$	-	-	1.2	V
$t_{\text{rr}}$	Reverse Recovery Time	$I_{\text{S}}=8\text{A}, V_{\text{GS}}=0\text{V},$ $dI/dt=100\text{A}/\mu\text{s}$	-	13	-	ns
$Q_{\text{rr}}$	Reverse Recovery Charge		-	6	-	nC

**CH-2 Electrical Characteristics@ $T_j=25^\circ\text{C}$ (unless otherwise specified)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$\text{BV}_{\text{DSS}}$	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=250\mu\text{A}$	30	-	-	V
$R_{\text{DS(ON)}}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{\text{GS}}=10\text{V}, I_{\text{D}}=11\text{A}$	-	8	10.5	$\text{m}\Omega$
		$V_{\text{GS}}=4.5\text{V}, I_{\text{D}}=7\text{A}$	-	13.3	16.5	$\text{m}\Omega$
$V_{\text{GS(th)}}$	Gate Threshold Voltage	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=250\mu\text{A}$	1	1.4	3	V
$g_{\text{fs}}$	Forward Transconductance	$V_{\text{DS}}=10\text{V}, I_{\text{D}}=11\text{A}$	-	20	-	S
$I_{\text{DSS}}$	Drain-Source Leakage Current	$V_{\text{DS}}=24\text{V}, V_{\text{GS}}=0\text{V}$	-	-	10	$\text{uA}$
$I_{\text{GSS}}$	Gate-Source Leakage	$V_{\text{GS}}=\pm 12\text{V}, V_{\text{DS}}=0\text{V}$	-	-	$\pm 100$	nA
$Q_{\text{g}}$	Total Gate Charge	$I_{\text{D}}=11\text{A}$	-	7.5	12	nC
$Q_{\text{gs}}$	Gate-Source Charge	$V_{\text{DS}}=15\text{V}$	-	3	-	nC
$Q_{\text{gd}}$	Gate-Drain ("Miller") Charge	$V_{\text{GS}}=4.5\text{V}$	-	3	-	nC
$t_{\text{d(on)}}$	Turn-on Delay Time	$V_{\text{DS}}=15\text{V}$	-	9	-	ns
$t_{\text{r}}$	Rise Time	$I_{\text{D}}=1\text{A}$	-	5	-	ns
$t_{\text{d(off)}}$	Turn-off Delay Time	$R_{\text{G}}=3.3\Omega$	-	20	-	ns
$t_{\text{f}}$	Fall Time	$V_{\text{GS}}=10\text{V}$	-	4	-	ns
$C_{\text{iss}}$	Input Capacitance	$V_{\text{GS}}=0\text{V}$	-	970	1550	pF
$C_{\text{oss}}$	Output Capacitance	$V_{\text{DS}}=15\text{V}$	-	120	-	pF
$C_{\text{rss}}$	Reverse Transfer Capacitance	f=1.0MHz	-	80	-	pF
$R_{\text{g}}$	Gate Resistance	f=1.0MHz	-	1.2	2.4	$\Omega$

**Source-Drain Diode**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$V_{\text{SD}}$	Forward On Voltage <sup>2</sup>	$I_{\text{S}}=11\text{A}, V_{\text{GS}}=0\text{V}$	-	-	1.2	V
$t_{\text{rr}}$	Reverse Recovery Time	$I_{\text{S}}=11\text{A}, V_{\text{GS}}=0\text{V},$ $dI/dt=100\text{A}/\mu\text{s}$	-	16	-	ns
			-	10	-	nC

**Notes:**

- 1.Pulse width limited by Max. junction temperature.
- 2.Pulse test
- 3.Surface mounted on 1 in<sup>2</sup> copper pad of FR4 board, t  $\leq$ 10sec.
- 4.Surface mounted on min. copper pad of FR4 board, on steady-state

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

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## Channel-1

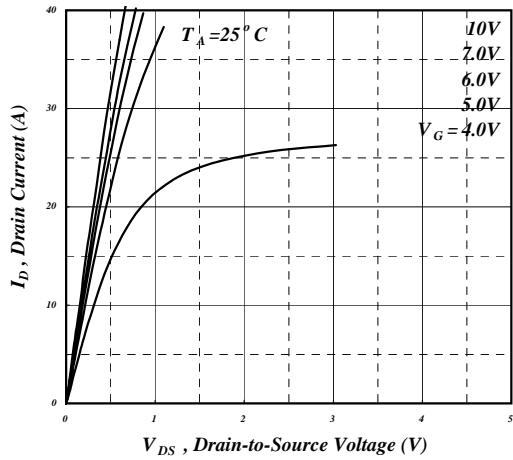


Fig 1. Typical Output Characteristics

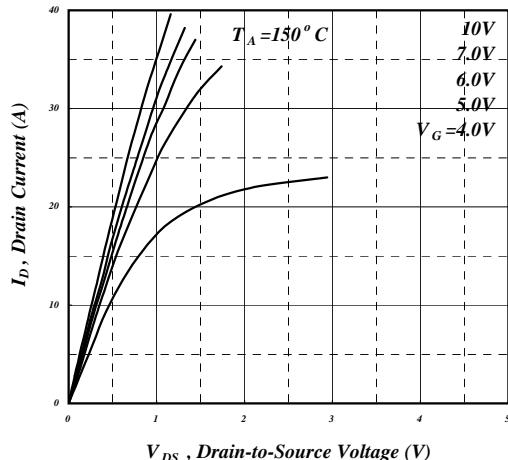


Fig 2. Typical Output Characteristics

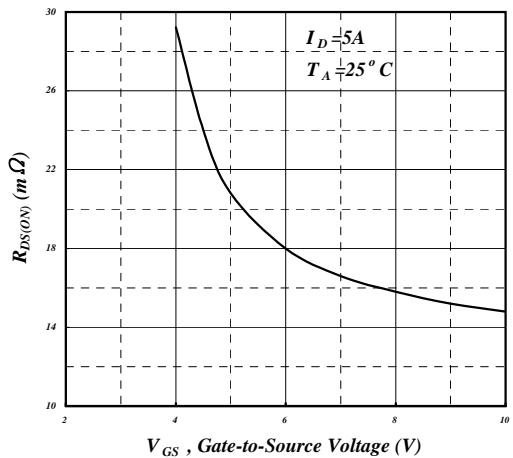


Fig 3. On-Resistance v.s. Gate Voltage

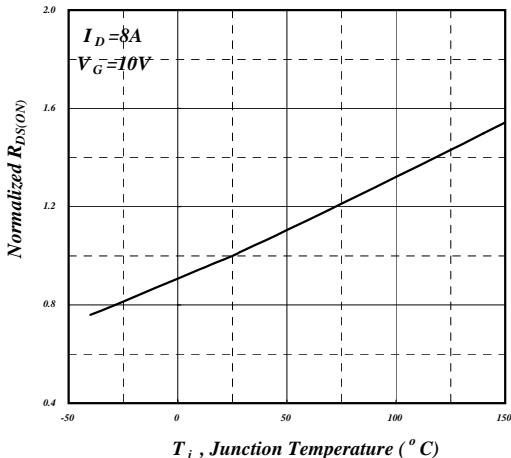


Fig 4. Normalized On-Resistance v.s. Junction Temperature

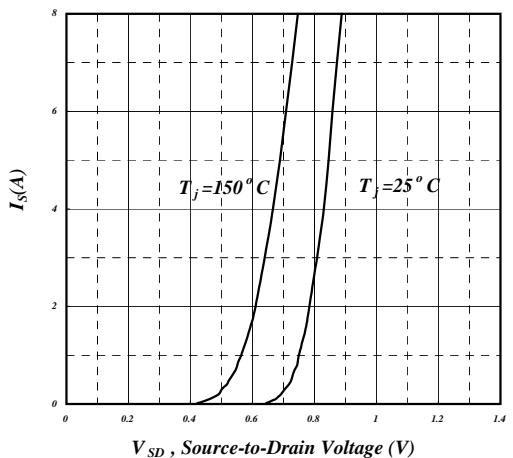


Fig 5. Forward Characteristic of Reverse Diode

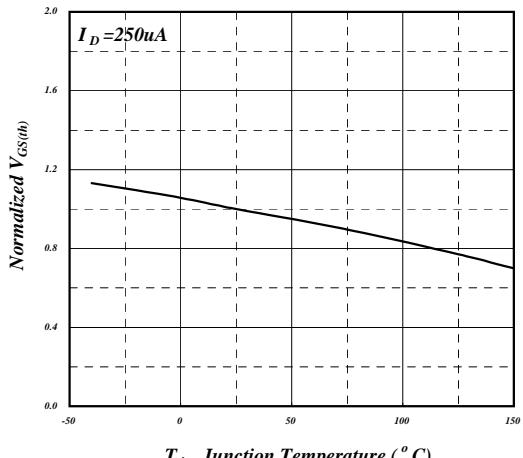


Fig 6. Gate Threshold Voltage v.s. Junction Temperature



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## Channel-1

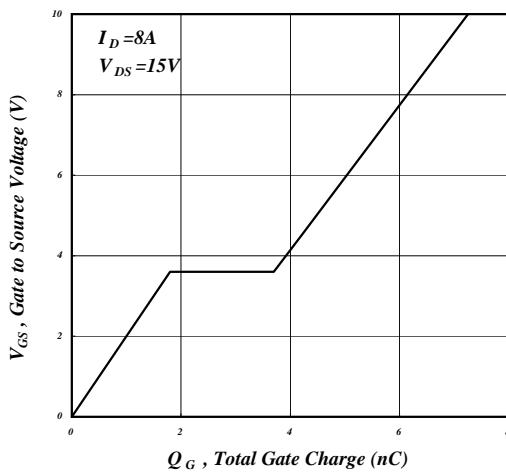


Fig 7. Gate Charge Characteristics

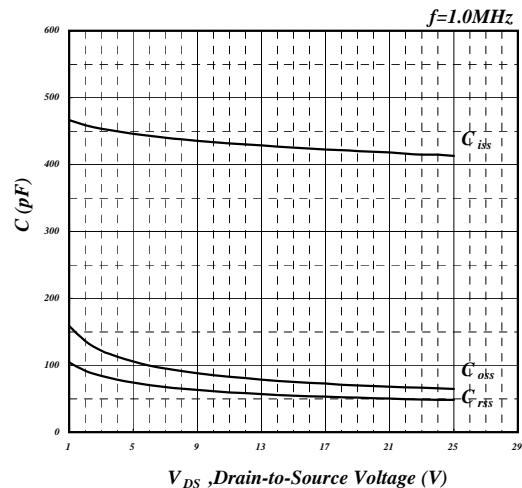


Fig 8. Typical Capacitance Characteristics

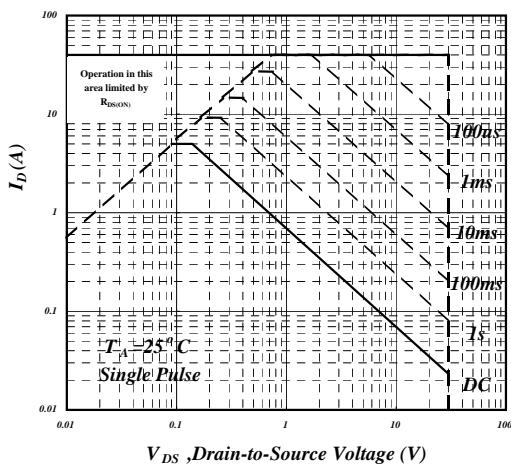


Fig 9. Maximum Safe Operating Area

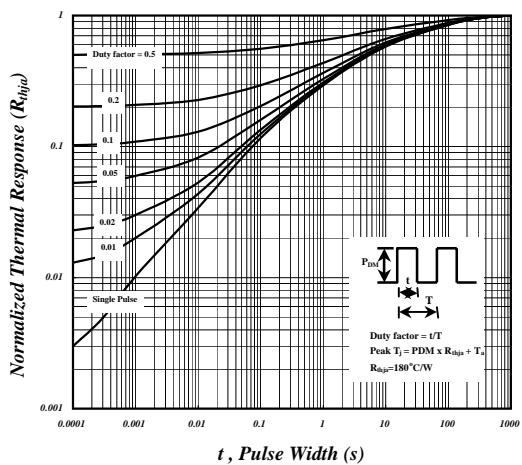


Fig 10. Effective Transient Thermal Impedance

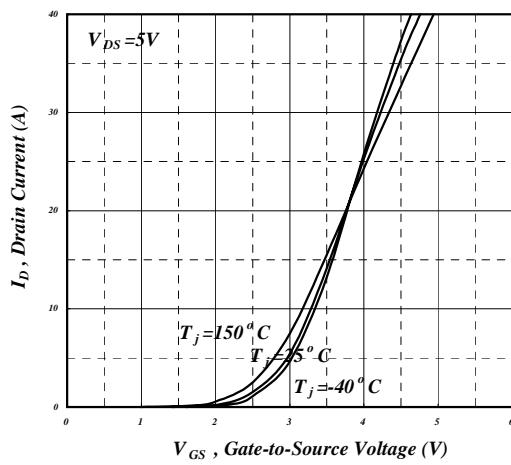


Fig 11. Transfer Characteristics

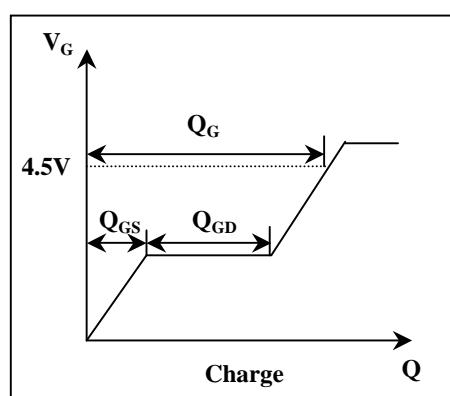


Fig 12. Gate Charge Waveform



## Channel-2

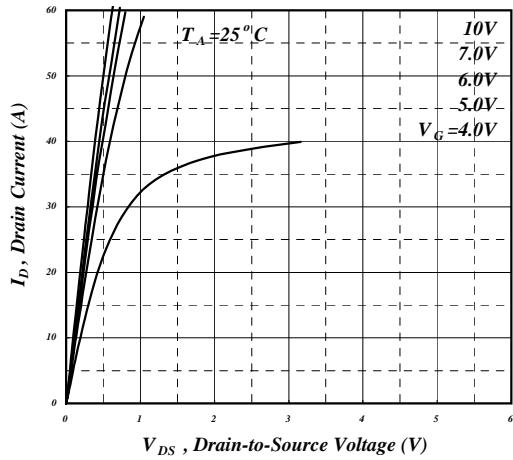


Fig 1. Typical Output Characteristics

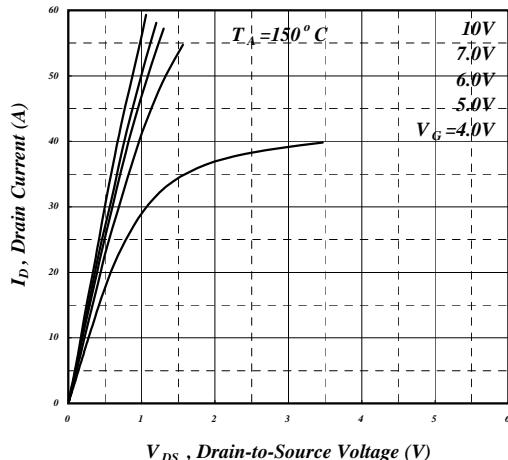


Fig 2. Typical Output Characteristics

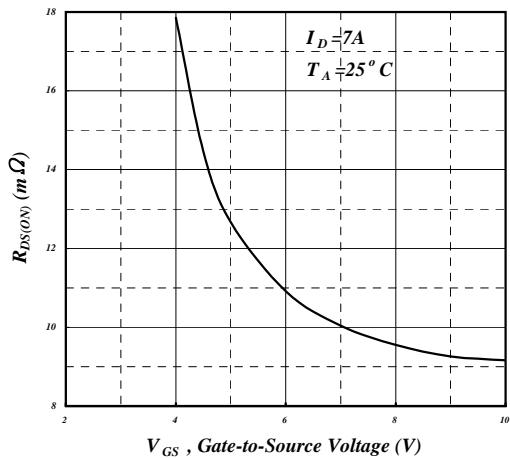


Fig 3. On-Resistance v.s. Gate Voltage

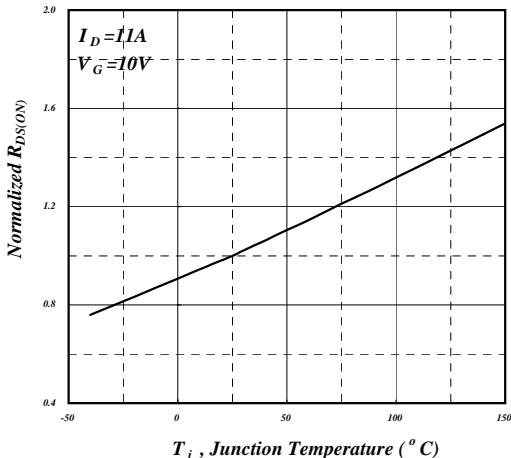


Fig 4. Normalized On-Resistance v.s. Junction Temperature

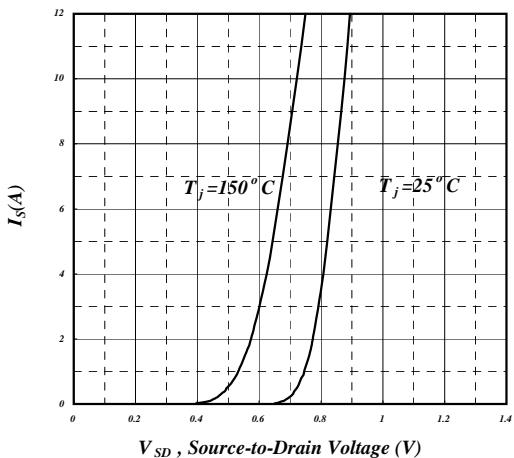


Fig 5. Forward Characteristic of Reverse Diode

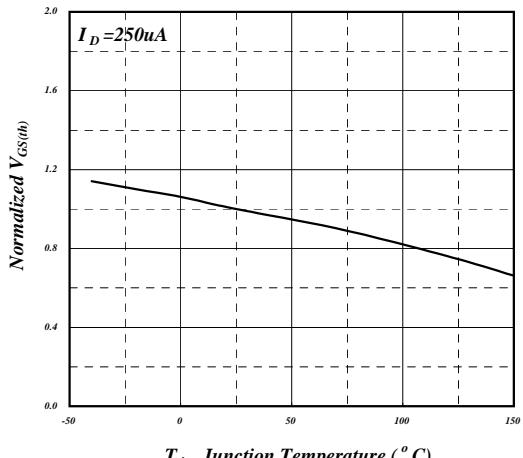
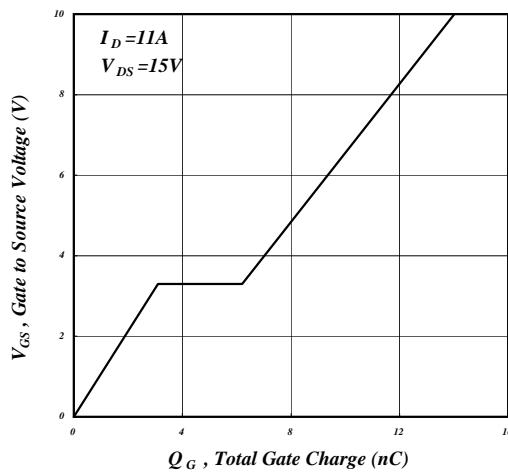


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

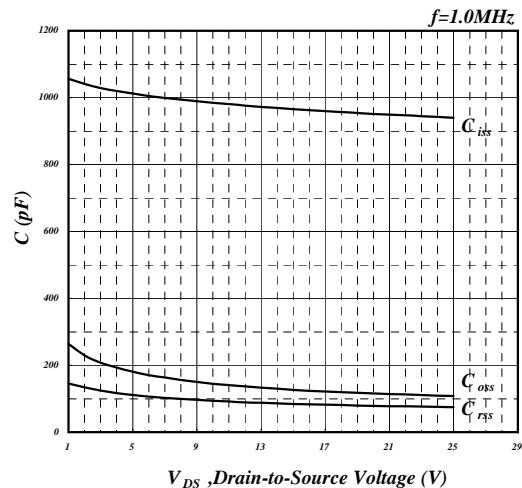


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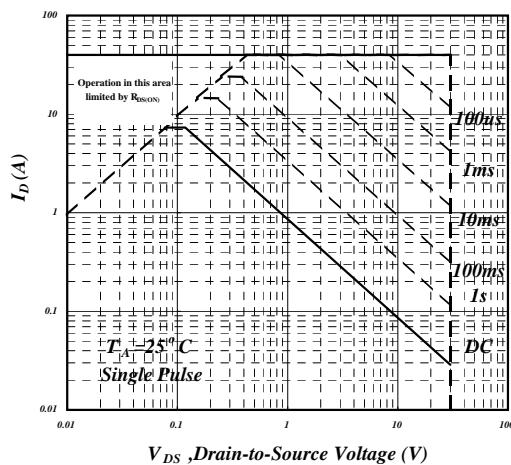
## Channel-2



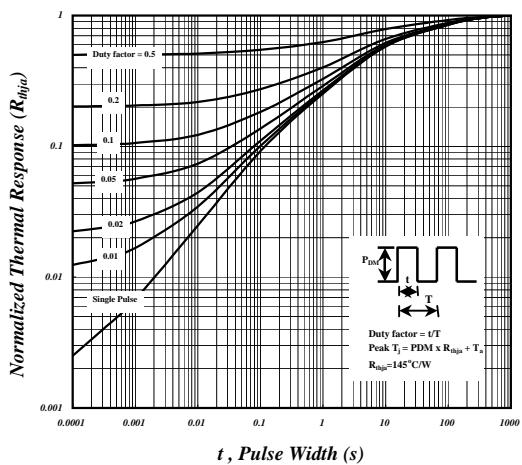
**Fig 7. Gate Charge Characteristics**



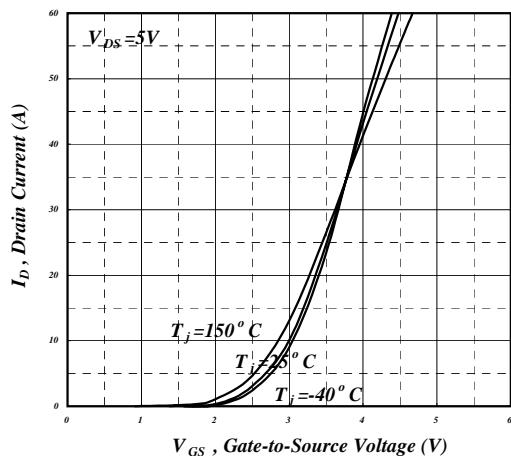
**Fig 8. Typical Capacitance Characteristics**



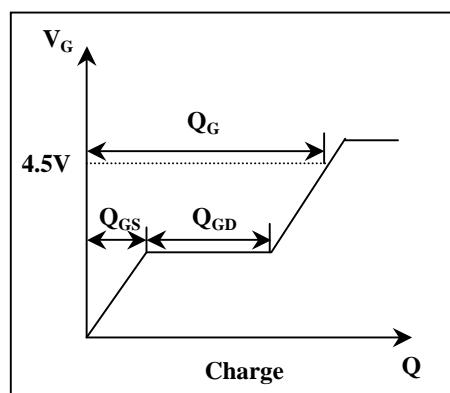
**Fig 9. Maximum Safe Operating Area**



**Fig 10. Effective Transient Thermal Impedance**



**Fig 11. Transfer Characteristics**



**Fig 12. Gate Charge Waveform**



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### MARKING INFORMATION

