

# MN83951

## TFT LCD Panel Controller

### ■ Overview

The MN83951 is a timing controller for displaying an analog video signal on a TFT color liquid crystal display panel in such applications as LCD television sets and video cameras.

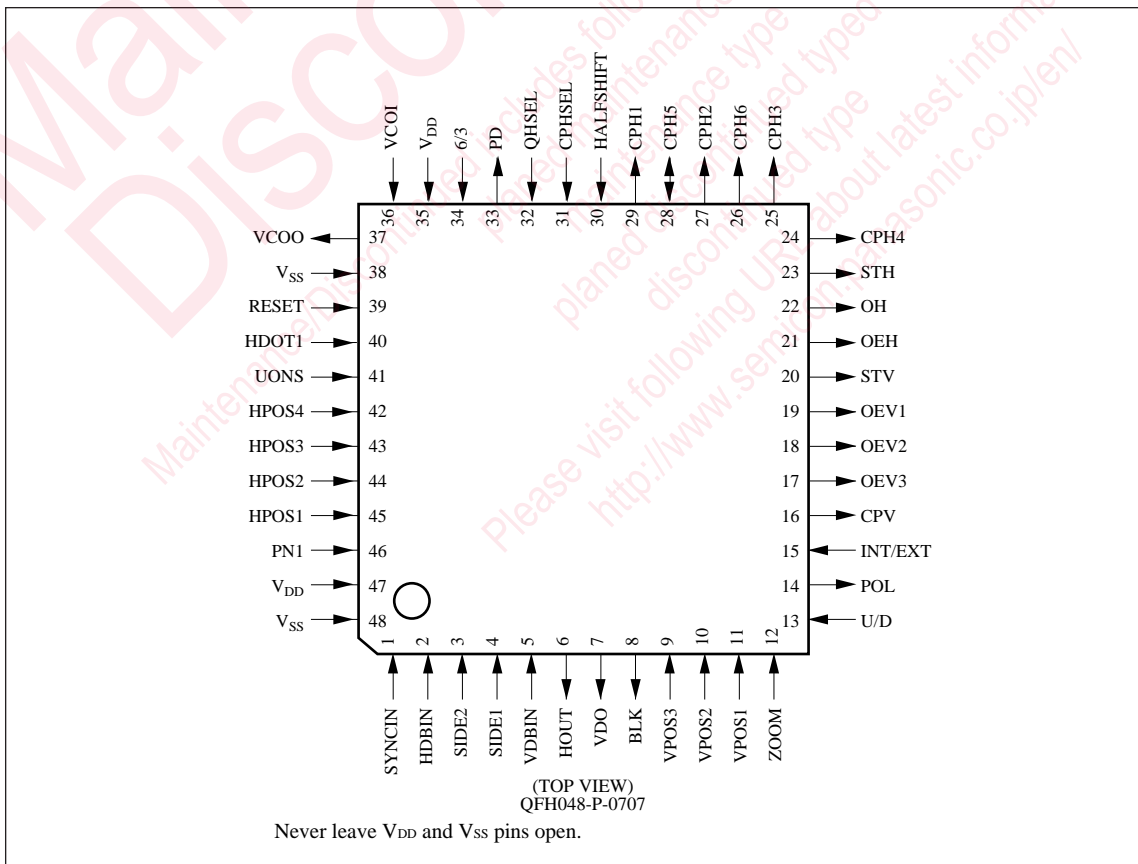
### ■ Features

- Support for both composite color sync input and separate color sync input
- Horizontal and vertical position adjustment functions
  - Horizontal: 4 bits (range: approximately 4  $\mu$ s)
  - Vertical: 3 bits (range: 7 H)
- Wide panel support
  - Three side blackout modes
  - Simple ZOOM mode (Support for both normal and reverse scans)
- Support for both single- and two-sided source driver configurations
- Support for both PAL and NTSC systems (decimation mode only for PAL)
- Support for underside on screen display(UONS)
- ON/OFF function for shifting output timing by half a pixel clock cycle

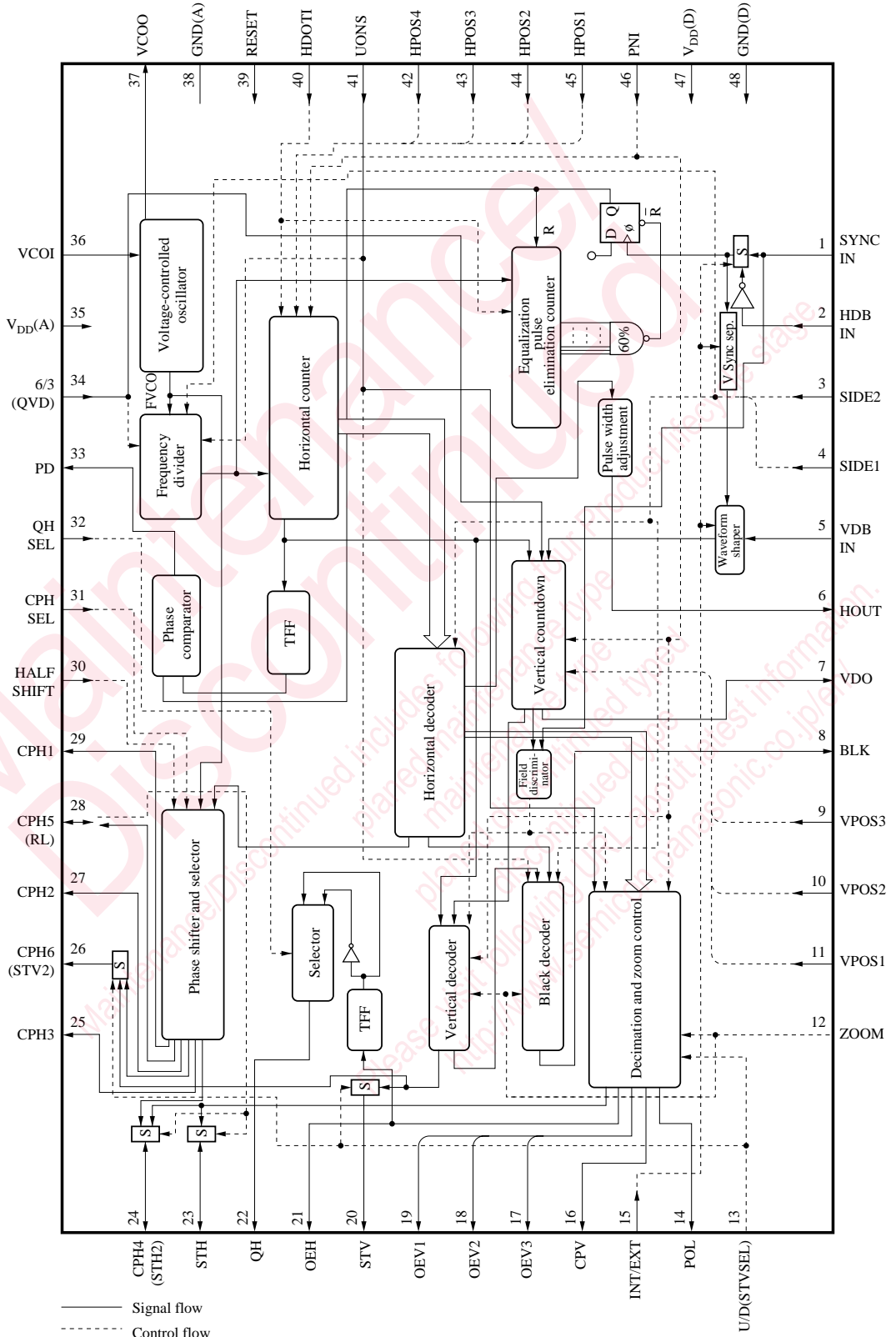
### ■ Applications

- LCD television sets and video cameras

### ■ Pin Assignment



■ Block Diagram



Note: The above is a bottom view.

### ■ Pin Descriptions

Pin No.	Internal Resistor	Symbol	Pin Name	I/O	Function Description									
1	None	SYNC IN	Composite color sync input	I	• Composite color sync signal (Sync "H" level)									
2	None	HDBIN	Horizontal sync input	I	• (Sync "L" level)									
3	PD	SIDE2	Side blackout control pins	I	<p>On-screen display or single-edge blackout</p> <p>SIDE ① Double-edged blackout</p> <p>SIDE ②</p> <p>SIDE ③</p>									
4	PD	SIDE1	<table border="0"> <tr> <td>SIDE2</td> <td>0</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>SIDE1</td> <td>0</td> <td>0</td> <td>1</td> <td>1</td> </tr> </table> <p>Normal ① ② ③</p>	SIDE2		0	1	0	1	SIDE1	0	0	1	1
SIDE2	0	1	0	1										
SIDE1	0	0	1	1										
5	None	VDB IN	Vertical sync input	I	• (Sync "L" level)									
6	—	HOUT	Horizontal sync output	O	• This pin provides the horizontal sync signal obtained by removing the equalization and the cut pulses for vertical synchronization from the composite color sync signal.									
7	—	VDO	Vertical sync output	O	• The pulse from this pin falls with the horizontal sync pulse of pin 6 following a falling edge of pin 5 pulse and rises after 3-H pulse width.									
8	—	BLK	Black signal output	O	• In the side blackout and underside on screen (UONS) modes, this pin provides "H" level pulses synchronized with the black and on-screen timing.									
9	PD	VPOS3	Vertical display position selection (These change the STV position.)	I	These pins control the position of the STV rising edge after the VDO falling edge. NTSC • $12H + (7 - VPOS1 - 2 \times VPOS2 - 4 \times VPOS3)H$ In the ZOOM mode, the interval is 31 H. PAL • $24H + (7 - VPOS1 - 2 \times VPOS2 - 4 \times VPOS3)H$ In the ZOOM mode, the interval is 35 H.									
10	PD	VPOS2		I										
11	PD	VPOS1		I										
12	PD	ZOOM	Zoom control ("H" level selects ZOOM mode.)	I	NTSC • The controller selects two scan lines every 3H. PAL • The controller deactivates decimation and simultaneously selects two scan lines at $(6n+1)H$ .									
13	PU	U/D	Scan direction control ("H" level selects normal scan.)	I	• In the ZOOM mode, the controller switches pulses of OEV1 - OEV3. • When HALFSHIFT is at "H" level, this pin functions as STVSEL.									

■ Pin Descriptions (continued)

Pin No.	Internal Resistor	Symbol	Pin Name	I/O	Function Description
14	—	POL	Pulses switching image polarity and opposing voltage	O	<ul style="list-style-type: none"> <li>• Pulses sent to chroma IC for controlling image polarity and opposing electrode. The level changes at the rising edge of OEH.</li> </ul>
15	PU	INT/EXT	Internal/external synchronization selection	I	<ul style="list-style-type: none"> <li>• "H" level selects composite color sync mode; "L" level, separate color sync mode.</li> </ul>
16	—	CPV	Gate driver clock pulses	O	<ul style="list-style-type: none"> <li>• Clock pulses for shift registers inside gate driver ICs</li> </ul>
17	—	OEV3	Gate driver output stage enable pulses (Selective stage output: "H" level for VgL; "L" level for VgH)	O	<ul style="list-style-type: none"> <li>• "H" level output from these pins forces the gate driver IC output buffers to VgL.</li> <li>• These pins are used during PAL decimation and in the ZOOM mode.</li> <li>• "L" level input from pin 39 (RESET) forces all three pins to "H" level.</li> </ul>
18	—	OEV2		O	
19	—	OEV1		O	
20	—	STV	Gate driver scan start pulses	O	<ul style="list-style-type: none"> <li>• These pulses start the shift registers inside the gate driver ICs. They are 1 H wide and change levels at the falling edge of CPV.</li> </ul>
21	—	OEH	Source driver output stage enable pulses	O	<ul style="list-style-type: none"> <li>• These pulses determine the timing with which the source drivers write image data to the LCD panel. The period is 1 H; the pulse width, 8 μs.</li> </ul>
22	—	QH	Color data switching pulses to source drivers	O	<ul style="list-style-type: none"> <li>• This pin controls switching of color data to source driver ICs. Pin 32 controls the order.</li> </ul>
23	—	STH	Source driver start pulses	O	<ul style="list-style-type: none"> <li>• These pulses start the shift registers inside the source driver ICs. They are 1 CPH wide and change levels at the falling edge of CPH1.</li> </ul>
24	—	CPH4	Source driver clock pulses 4/Source driver start pulses 2	O	<p>(1) When pins 30 and pins 34 are both "L" level, the controller delivers clock pulses only to CPH1 - CPH3 and drives CPH4 - CPH6 at "L" level.</p> <p>(2) When pins 30 and pins 34 are both "H" level, the controller alternates the CPH1 - CPH3 outputs between the CPH1 - CPH3 and CPH4 - CPH6 phase clock patterns every 1 H.</p>
25	—	CPH3	Source driver clock pulses 3	O	
26	—	CPH6	Source driver clock pulses 6/Source driver start pulses 2	O	
27	—	CPH2	Source driver clock pulses 2	O	
28	—	CPH5	Source driver clock pulses 5/STH switching signal	I/O	
29	—	CPH1	Source driver clock pulses 1	O	

### ■ Pin Descriptions (continued)

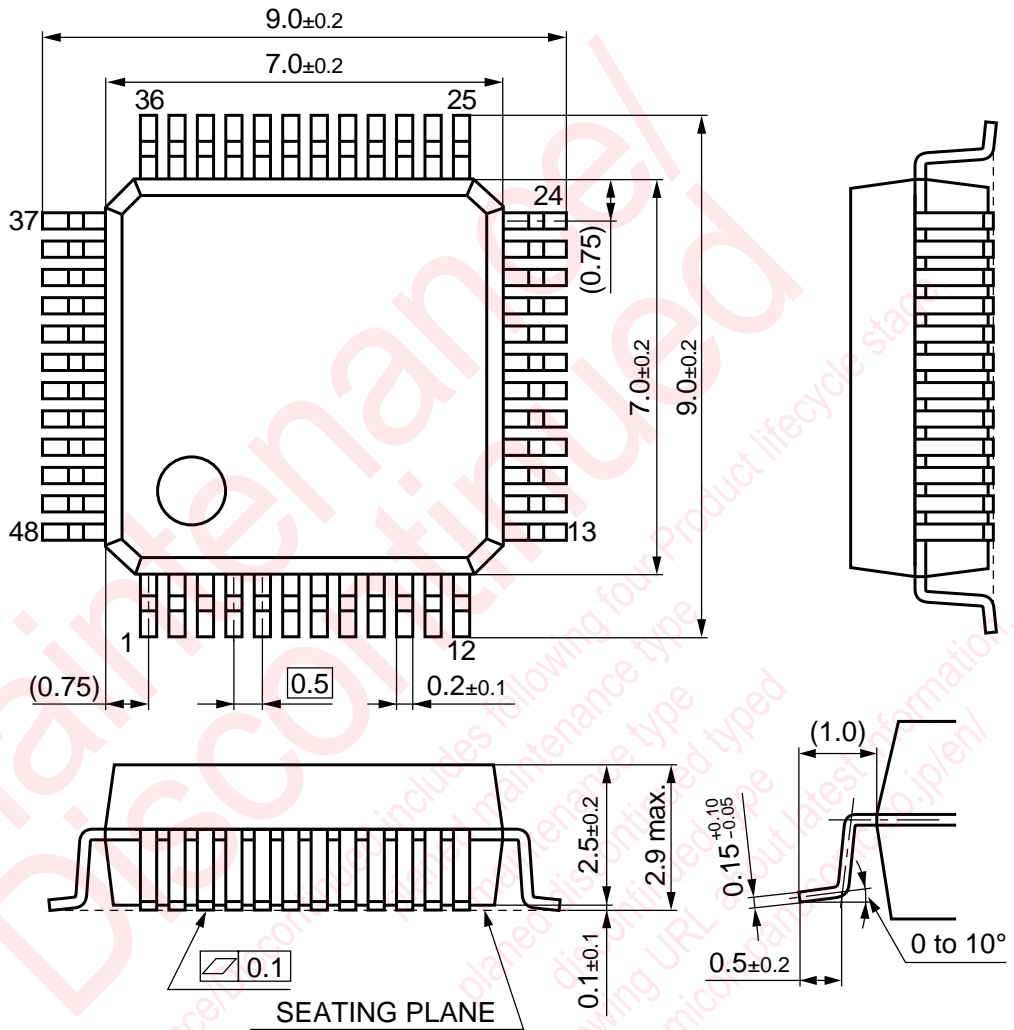
Pin No.	Internal Resistor	Symbol	Pin Name	I/O	Function Description
30	PD	HALF SHIFT	Controlling timing shift of half a pixel clock cycle ("H" level selects shifting.)	I	<ul style="list-style-type: none"> <li>The pin provides a means of shift output timing for alternate lines by half a pixel clock cycle to drive a delta panel layout.</li> </ul>
31	PD	CPH SEL	CPH pulse phase switching	I	<ul style="list-style-type: none"> <li>When the frequency divider is six—that is, pin 34 is at "H" level—this pin switches between the CPH1 - CPH3 and CPH4 - CPH6 phase clock patterns.</li> </ul>
32	PD	QH SEL	QH output switching	I	<ul style="list-style-type: none"> <li>This pin determines the order in which the color data switching pulses (QH from pin 22) to the source driver ICs.</li> </ul>
33	—	PD	Phase comparator output	O	<ul style="list-style-type: none"> <li>This pin provides output from the phase comparator using an edge trigger.</li> </ul>
34	None	6/3 (QVD)	Frequency divider doubler ("H" level input doubles the divider ratio from 3 to 6.)	I	<ul style="list-style-type: none"> <li>This pin determines the frequency divider ratio to CPH from FVCO, the fundamental frequency for the voltage-controlled oscillator: 6 for "H" level input and 3 for "L" level input.</li> <li>When pin 30 is at "H" level, this pin serves as the QVD input pin.</li> </ul>
35	—	V <sub>DD(A)</sub>	Power supply for analog circuits: 3 V	—	<ul style="list-style-type: none"> <li>This is the power supply for the voltage-controlled oscillator, clock frequency divider, and CPH generator.</li> </ul>
36	—	VCO I	VCO input	I	<ul style="list-style-type: none"> <li>Oscillator signal input for VCO</li> </ul>
37	—	VCO O	VCO output	O	<ul style="list-style-type: none"> <li>Oscillator signal output for VCO</li> </ul>
38	—	GND <sub>(A)</sub>	Ground for analog circuits	—	<ul style="list-style-type: none"> <li>This is the ground for the voltage-controlled oscillator, clock frequency divider, and CPH generator.</li> </ul>
39	PU	RESET	Reset ("L" level input selects RESET mode.)	I	<ul style="list-style-type: none"> <li>This signal resets internal counters, flip-flops, and other components. The pull-up resistance is between 50 kΩ and 500 kΩ.</li> </ul>
40	PU	HDOTI	Switching number of panel dots in the horizontal direction	I	<ul style="list-style-type: none"> <li>In combination with pins 30 and 34, this pin controls the horizontal frequency divider ratio to match the number of panel dots in the horizontal direction.</li> <li>For delta layouts, dot counts of 480, 600, 960, and 1200 are supported.</li> <li>For striped layouts, dot counts of 960 and 1200 are supported.</li> </ul>
41	PD	UONS	Controlling underside on screen (UONS) mode ("H" level selects UONS mode.)	I	<ul style="list-style-type: none"> <li>This mode switches the bottom 30 lines to an on-screen display mode.</li> </ul>

■ Pin Descriptions (continued)

Pin No.	Internal Resistor	Symbol	Pin Name	I/O	Function Description
42 to 45	PD	HPOS4 to HPOS1	Horizontal pixel position (STH position)	I	<p>These pins determine the lag between the rising edge of the SYNC IN signal and the STH rising edge: (assuming that the synchronization separation delay is 1.1 μs)</p> <ul style="list-style-type: none"> <li>• NTSC:  <math>7.3\mu\text{s} + (15 - \text{HPOS1} - 2 \times \text{HPOS2} - 4 \times \text{HPOS3} - 3 \times \text{HPOS4}) \times 0.3125\mu\text{s}</math> </li> <li>• PAL:  <math>8.0\mu\text{s} + (15 - \text{HPOS1} - 2 \times \text{HPOS2} - 4 \times \text{HPOS3} - 3 \times \text{HPOS4}) \times 0.3125\mu\text{s}</math> </li> </ul>
46	PD	PN1	PAL/NTSC switch ("L" level selects NTSC mode.)	I	<ul style="list-style-type: none"> <li>• "H" level input selects PAL mode with decimation at the rate of one line in eight. 1st: (8n+2) H, 2nd: (8n+5) H</li> </ul>
47	—	V <sub>DD</sub>	Power supply for digital circuits: 3 V	—	<ul style="list-style-type: none"> <li>• Power supply for digital circuits</li> </ul>
48	—	GND	Ground for digital circuits	—	<ul style="list-style-type: none"> <li>• Ground for digital circuits</li> </ul>

■ Package Dimensions (Unit:mm)

QFH048-P-0707



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