Optoelectronics Division
TRW Electronic Components Group

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January 1985

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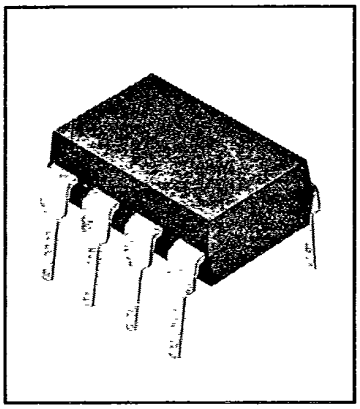
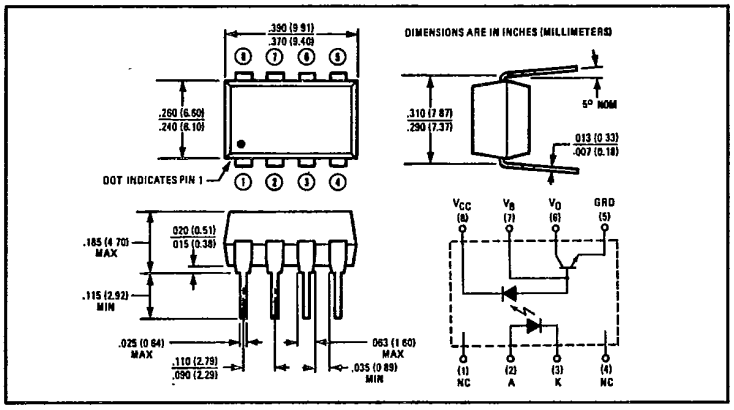
T-41-83

High Speed Optocouplers
Types 6N135, 6N136, OPI2502





Features
- High speed — 1 megabit/second
- TTL compatible
- High common mode transient immunity
- Wide bandwidth
- Open collector output
- U.L. Recognized, File No. E58730

Description
TRW's 6N135 and 6N136 JEDEC registered optocouplers are high speed devices consisting of GaAsP emitters and integrated photodetectors. The circuitry of each device consists of a photodiode driving an open collector transistor, inherently faster than a phototransistor. The OPI2502 is a high speed non-JEDEC part.

The 6N135 has a minimum current transfer ratio of 7% when driven with 16 mA and is compatible with TTL/CMOS or TTL/LSTTL as well as wide-band analog circuitry.

The 6N136, with a CTR of 19% minimum, can be driven from a TTL driver at 16 mA and will provide sufficient output to drive a single TTL load with a 5.6 kΩ pull-up resistor.

Pins 2 through 7 are compatible with the configuration of standard 6-pin DIP devices with phototransistor and photodarlington outputs. By supplying 1.5 to 15 volts bias to pin 8 the 6N135/6N136 optocouplers offer improved speed performance for existing circuits.

Absolute Maximum Ratings (No derating required up to 70°C)

Storage Temperature	−55°C to +125°C
Operating Temperature	−55°C to +100°C
Lead Soldering Temperature (1/16 inch [1.6 mm] from case for 10 seconds)	260°C
Average Input Current — I_F	25 mA(1)
Peak Input Current — I_F (50% duty cycle, 1 ms pulse width)	50 mA(2)
Peak Transient Input Current — I_F (≤ 1 μs pulse width, 300 pps)	1.0 A
Reverse Input Voltage — V_R	5.0 V
Input Power Dissipation	45 mW(3)
Average Output Current — I_O	8.0 mA
Peak Output Current	16.0 mA
Emitter-Base Reverse Voltage	5.0 V
Supply and Output Voltage — V_{CC}, V_O	−0.5 V to 15 V
Base Current — I_B	5.0 mA
Output Power Dissipation	100 mW(4)

Caution: This component is susceptible to damage from electrostatic discharge. Normal static prevention procedures should be used in handling.

Notes:
(1) Derate linearly above 70°C free-air temperature at a rate of 0.8 mA/°C.
(2) Derate linearly above 70°C free-air temperature at a rate of 1.6 mA/°C.
(3) Derate linearly above 70°C free-air temperature at a rate of 0.9 mA/°C.
(4) Derate linearly above 70°C free-air temperature at a rate of 2.0 mA/°C.
(5) CM_H is the maximum allowable dv/dt on the leading edge of a common mode pulse to assure that the output will not switch from high to low.
(6) CM_L is the maximum negative dv/dt allowable on the trailing edge of a common mode pulse to assure that the output will not switch from low to high.
(7) Test condition represents 1 TTL unit load with 5.6 kΩ pull-up rpsistor.
(8) Test condition represents 1 LSTTL unit load with a 6.1 kΩ pull-up resistor.
(9) Device considered a two-terminal device: pins 1, 2, 3 and 4 shorted together and pins 5, 6, 7 and 8 shorted together.

Applications
- Line receivers
- High speed logic isolation–TTL/TTL, TTL/LTTL, TTL/CMOS, TTL/LSTTL
- Improved speed as replacement for 6-pin DIP isolators
- Improved linearity in analog circuit ground isolation

Types 6N135, 6N136, OPI2502

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Electrical Characteristics Over recommended temperature (T_A = 0°C to 70°C), unless otherwise noted)

Symbol	Parameter	Device	Min.	Typ.**	Max.	Units	Test Conditions	Figure
CTR*	Current Transfer Ratio	6N135	7.0	19.0		%	I_F = 16.0 mA, V_O = 0.40 V, V_{CC} = 4.5 V, T_A = 25°C	1, 2
		6N136	19.0	25	*	%		
		OPI2502	15.0		22	%		
CTR		6N135	5.0	15.0		%	I_F = 16.0 mA, V_O = 0.50 V, V_{CC} = 4.5 V	
		6N136	15.0	23		%		
V_{OL}	Logic Low Output Voltage	6N135		0.100	0.40	V	I_F = 16.0 mA, I_O = 1.10 mA, V_{CC} = 4.5 V	
		6N136 OPI2502		0.100	0.40	V	I_F = 16.0 mA, I_O = 2.4 mA, V_{CC} = 4.5 V	
I_{OH}*	Logic High Output Current			3.0	500	nA	I_F = 0 mA, V_O = V_{CC} = 5.5 V, T_A = 25°C	6
				0.010	1.00	μA	I_F = 0 mA, V_O = V_{CC} = 15.0 V, T_A = 25°C.	
I_{OH}					50	μA	I_F = 0 mA, V_O = V_{CC} = 15.0 V	
I_{CCL}	Logic Low Supply Current			40		μA	I_F = 16.0 mA, V_O = Open, V_{CC} = 15.0 V	
I_{CCH}*	Logic High Supply Current			0.020	1.00	μA	I_F = 0 mA, V_O = Open, V_{CC} = 15.0 V, T_A = 25°C	
I_{CCH}					2.0	μA	I_F = 0 mA, V_O = Open, V_{CC} = 15.0 V,	
V_F*	Input Forward Voltage			1.50	1.70	V	I_F = 16.0 mA, T_A = 25°C	3
$\frac{\Delta V_F}{\Delta T_A}$	Temperature Coefficient of Forward Voltage			-1.80		mV/°C	I_F = 16.0 mA	
BV_R*	Input Reverse Breakdown Voltage		6.0			V	I_R = 10.0 μA, T_A = 25°C	
C_{IN}*	Input Capacitance			42		pF	f = 1.00 MHz, V_F = 0	
I_{IO}*	Input-Output Insulation Leakage Current				1.00	μA	45% Relative Humidity, t = 5.0 sec, V_{IO} = 3000 Vdc, T_A = 25°C (Note 9)	
R_{IO}	Input-Output Resistance			10^{12}		Ω	V_{IO} = 500 Vdc (Note 9)	
C_{IO}	Input-Output Capacitance			0.50		pF	f = 1.00 MHz (Note 9)	
h_{FE}	Transistor DC Current Gain			150		–	V_O = 5.0 V, I_O = 3.0 mA	

Switching Specifications (T_A = 25°C) V_{CC} = 5.0 V, I_F = 16.0 mA, unless otherwise specified

t_{PHL}	Propagation Delay Time to Logic Low at Output	6N135*		0.50	1.50	μs	R_L = 4.1 kΩ (Note 8)	5, 9
		6N136* OPI2502		0.20	0.80	μs	R_L = 1.90 kΩ (Note 7)	
t_{PLH}	Propagation Delay Time to Logic High at Output	6N135*		0.40	1.50	μs	R_L = 4.1 kΩ (Note 8)	5, 9
		6N136* OPI2502		0.30	0.80	μs	R_L = 1.90 kΩ (Note 7)	
CMH	Common Mode Transient Immunity at Logic High Level Output	6N135		1000		V/μs	I_F = 0 mA, V_{CM} = 10.0 V_{p-p}, R_L = 4.1 kΩ (Notes 6, 8)	10
		6N136 OPI2502		1000		V/μs	I_F = 0 mA, V_{CM} = 10.0 V_{p-p}, R_L = 1.90 kΩ (Notes 6, 7)	10
CML	Common Mode Transient Immunity at Logic Low Level Output	6N135		-1000		V/μs	V_{CM} = 10.0 V_{p-p}, R_L = 4.1 kΩ (Notes 5, 8)	10
		6N136 OPI2502		-1000		V/μs	V_{CM} = 10.0 V_{p-p}, R_L = 1.90 kΩ (Notes 5, 7)	10

*JEDEC Registered Data

**All typicals at T_A = 25°C and V_{CC} = 5.0 V, unless otherwise noted.

Typical Performance Curves

Figure 1. Output Current vs Output Voltage

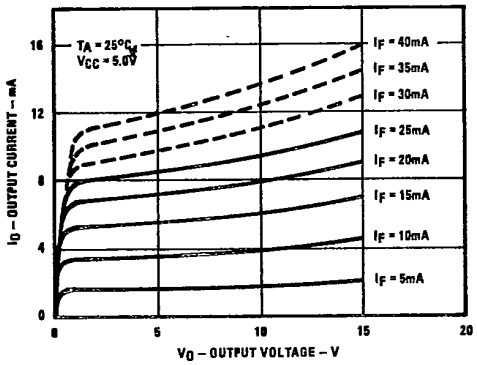


Figure 2. Current Transfer Ratio vs Forward Current

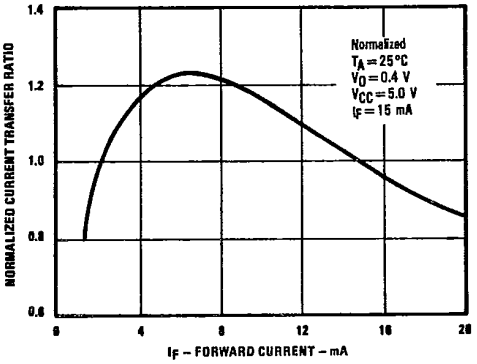


Figure 3. Forward Current vs Forward Voltage

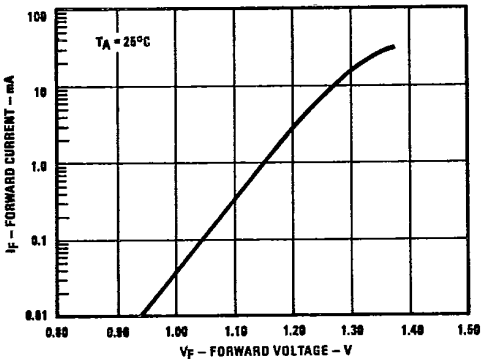


Figure 4. Current Transfer Ratio vs Temperature

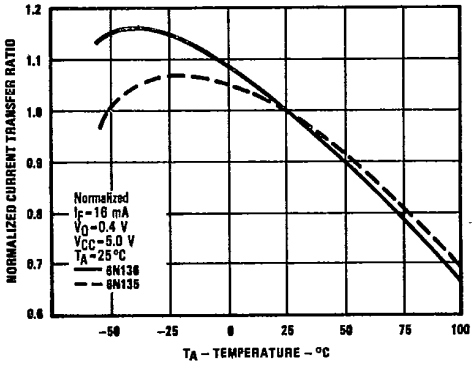


Figure 5. Propagation Delay vs Temperature

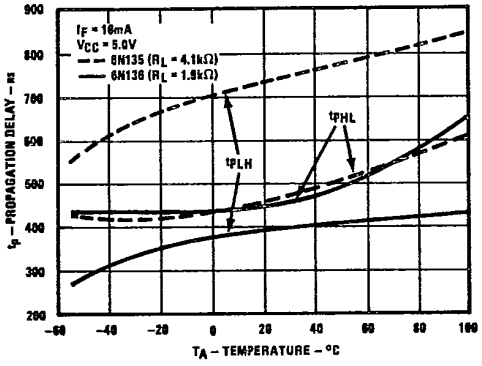


Figure 6. Logic High Output Current vs Temperature

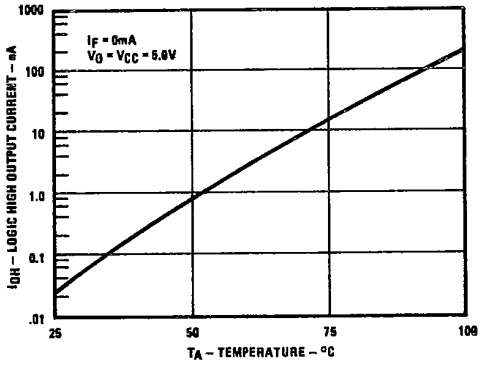


Figure 7. Small Signal Current Transfer Ratio vs Quiescent Input Current

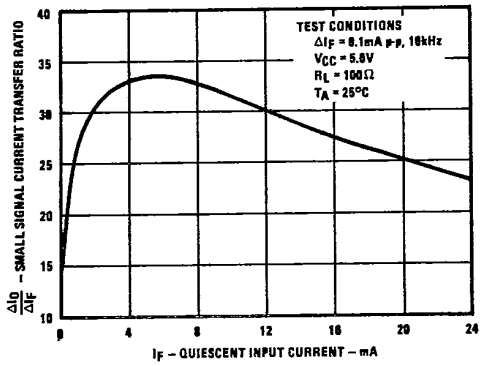


Figure 8. Frequency Response

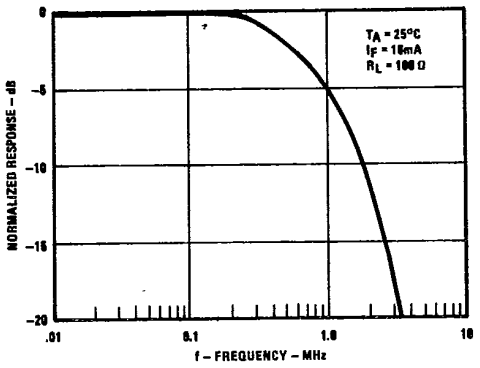
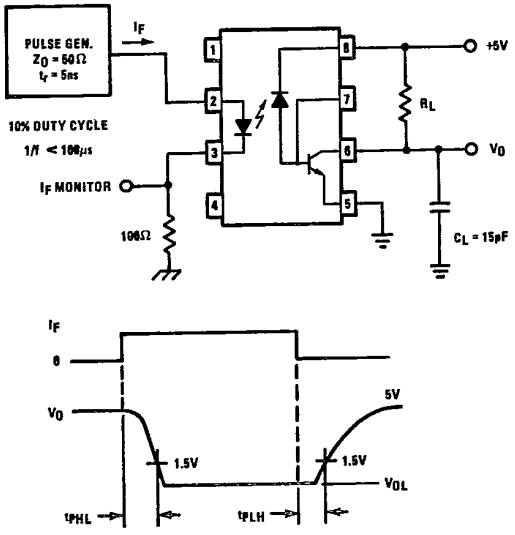


Figure 9. Switching Test Circuit*



*JEDEC Registered Data.

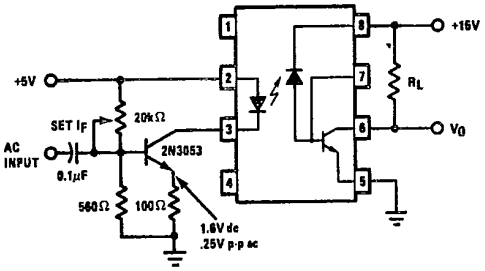
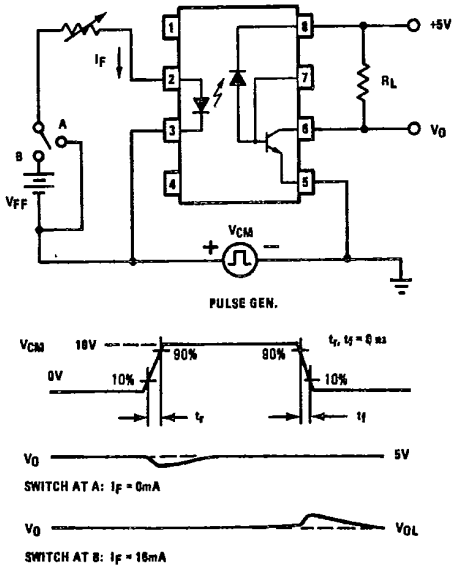


Figure 10. Test Circuit for Transient Immunity and Typical Waveforms



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