



Simplifying System Integration™

78Q8430 ARM9(920T) Embest Evaluation Board User Manual

**May, 2008
Rev. 1.0
UM_8430_007**

© 2008 Teridian Semiconductor Corporation. All rights reserved.

Teridian Semiconductor Corporation is a registered trademark of Teridian Semiconductor Corporation.

Simplifying System Integration is a trademark of Teridian Semiconductor Corporation.

ARM9 is a trademark of ARM Limited.

Linux is the registered trademark of Linus Torvalds.

Pentium is a registered trademark of Intel Corporation.

All other trademarks are the property of their respective owners.

Teridian Semiconductor Corporation makes no warranty for the use of its products, other than expressly contained in the Company's warranty detailed in the Teridian Semiconductor Corporation standard Terms and Conditions. The company assumes no responsibility for any errors which may appear in this document, reserves the right to change devices or specifications detailed herein at any time without notice and does not make any commitment to update the information contained herein. Accordingly, the reader is cautioned to verify that this document is current by comparing it to the latest version on <http://www.teridian.com> or by checking with your sales representative.

Teridian Semiconductor Corp., 6440 Oak Canyon, Suite 100, Irvine, CA 92618
TEL (714) 508-8800, FAX (714) 508-8877, <http://www.teridian.com>

Table of Contents

1	Introduction	5
1.1	Package Contents.....	6
1.2	Safety and ESD Notes	7
1.3	System Hardware Requirements.....	7
1.4	System Software Requirements	7
2	System Setup	8
2.1	Jumper and Dip Switch Settings.....	8
2.2	Connections	9
2.3	System Startup	10
3	78Q8430 Embest Evaluation Board Schematic, BOM and PCB Layout	11
4	Ordering Information	20
5	Related Documentation	20
6	Contact Information.....	20

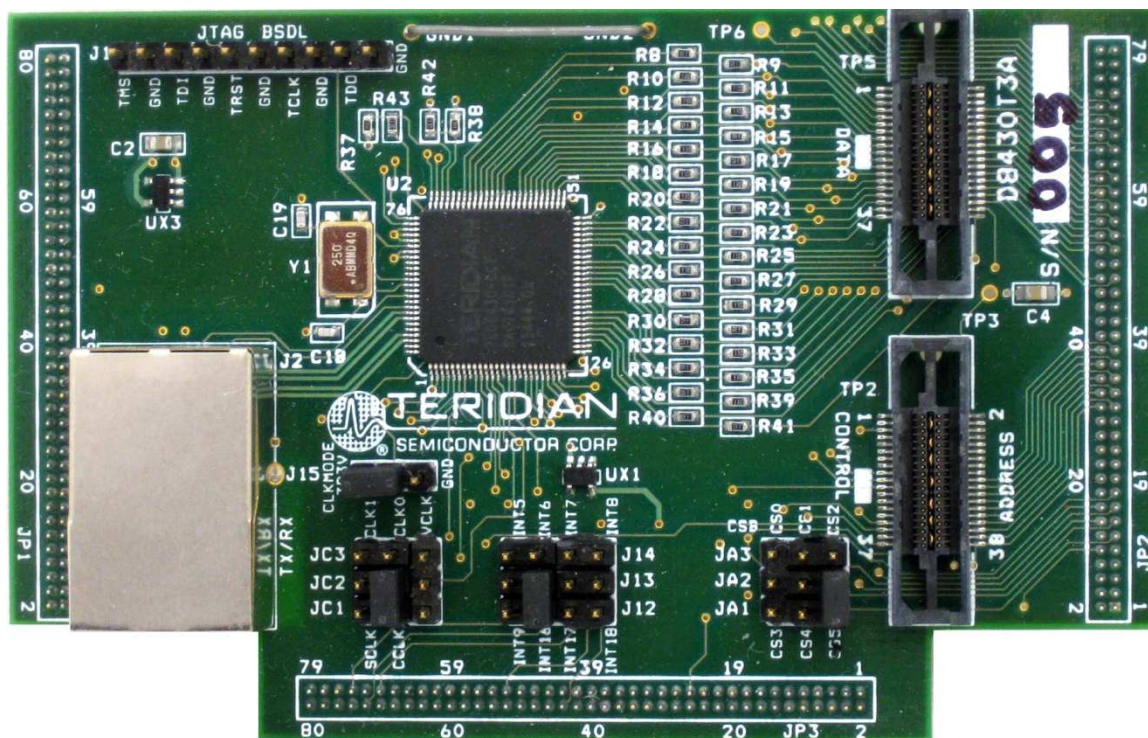
Figures

Figure 1: 78Q8430 System Interface Diagram	6
Figure 2: 78Q8430 Embest Evaluation Board Jumper Locations	8
Figure 3: 78Q8430 Embest Evaluation System Hardware Connections	9
Figure 4: Bus Interface Block Diagram	11
Figure 5: Bus Interface Schematic	12
Figure 6: MICTOR Diagnostic Connectors Schematic	13
Figure 7: MAC Interface Schematic	14
Figure 8: PHY Interface Schematic	15
Figure 9: Top Silkscreen Layout	17
Figure 10: Top Layer Layout	17
Figure 11: VCC Layer Layout	18
Figure 12: Ground Layer Layout	18
Figure 13: Bottom Layer Layout	19
Figure 14: Bottom Silkscreen Layout	19

Tables

Table 1: 78Q8430 Embest Evaluation Board Jumper Settings	8
Table 2: 78Q8430 Embest Evaluation Board Bill of Materials	16
Table 3: Order Number and Part Description	20

1 Introduction



The 78Q8430 Embest Evaluation Board (D8430T3A_EB) is a design example for a 10/100BASE-TX MAC+PHY Embest S3CEB2410 daughter card. The D8430T3A_EB plugs directly into the Embest S3CEB2410 (ARM9™ based) motherboard. The network connection is provided by the 78Q8430 which is a single chip auto-sensing, auto-switching (auto-negotiation or parallel detect modes and auto-MDIX) 10/100BASE-TX Fast Ethernet transceiver with full duplex operation capability. The device is designed specifically for the Audio/Visual (A/V) and Set Top Box (STB) markets and is easily interfaced to available A/V and STB core processors.

The 78Q8430 is compliant with applicable IEEE-802.3 standards. MAC and PHY configuration and status registers are provided as specified by IEEE802.3u. The integrated MAC is supported by an internal 32KByte transmit and receive SRAM FIFO. The partition of transmit and receive queues is configurable through software, allowing the 78Q8430 to be tuned for specific applications. The device contains hardware support for TCP-IP checksum and ARC address recognition.

The D8430T3A_EB provides support for the following 78Q8430 hardware interface features:

- The system bus interface operates like external memory with an active low chip select.
- Supports asynchronous big endian bus format.
- Supports asynchronous 100 MHz operation.
- Supports 32-bit wide data bus.
- Optional EEPROM interface for configuration data.
- Two programmable LED outputs for PHY status.
- Single +3.3V power supply voltage with a common ground plane.

A host processor interfaces directly to the FIFO via the Global Bus Interface (GBI). The D8430T3A_EB is configured for 32-bit big endian bus format. [Figure 1](#) shows the 78Q8430 system interfaces.

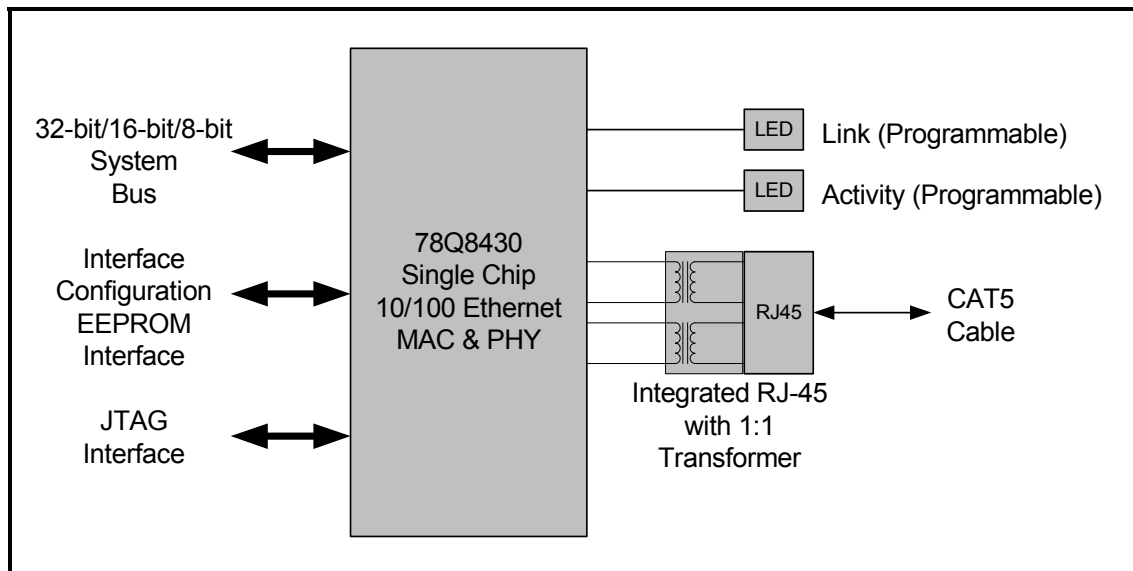


Figure 1: 78Q8430 System Interface Diagram

This document describes the setup and configuration of the 78Q8430 Embest Evaluation Board. The evaluation board requires operation with a +3.3 V power supply sourced from the Embest bus interface on the S3CEB2410 evaluation board. The 78Q8430 PHY interfaces to a CAT5 UTP cable via a 1:1 transformer.

The supplied software driver includes support for the Linux[®] operating system. The included *78Q8430 Software Driver Development Guidelines* and *78Q8430 ARM9 Linux Driver User and Test Guide* documents describe the software interfacing requirements for quick driver integration and prompt system evaluation of the 78Q8430.

Use this document with those listed in the [Related Documentation](#) section.

1.1 Package Contents

The 78Q8430 Embest Evaluation Board kit includes:

- A 78Q8430 Embest Evaluation Board (D8430T3A_EB).
- The Embest ARM9 S3CEB2410 evaluation platform.
- A memory card containing the 78Q8430 Linux software device driver and supporting tools.
- The following documents on CD:
 - *78Q8430 ARM9(920T) Embest Evaluation Board User Manual (this document)*
 - *78Q8430 Preliminary Data Sheet*
 - *78Q8430 Layout Guidelines*
 - *78Q8430 Software Driver Development Guidelines*
 - *78Q8430 78Q8430 Driver Guide for ARM920T Linux*
 - *78Q8430 ARM9(920T) Linux Driver Diagnostic Guide*

The printed circuit board Gerber files are available upon request.

1.2 Safety and ESD Notes

Connecting live voltages to the evaluation system will result in potentially hazardous voltages on the boards.



The evaluation boards are ESD sensitive! ESD precautions must be taken when handling these boards!

1.3 System Hardware Requirements

The following describes the minimum hardware requirements for the 78Q8430 Embest Evaluation Board system:

- The 78Q8430 Embest Evaluation Board (D8430T3A_EB).
- The Embest ARM9 S3CEB2410 evaluation platform.
- A PC to serve as the Linux host and control the ARM9 S3CEB2410 platform.

1.4 System Software Requirements

The following describes the minimum software requirements for evaluating the 78Q8430 Embest Evaluation Board:

- 78Q8430 ARM Linux 2.6.13 driver, version 1.1.
- Linux operating system supporting kernel 2.6.13.

2 System Setup

2.1 Jumper and Dip Switch Settings

The 78Q8430 Embest Evaluation Board utilizes several jumpers (JA, JC and J12 through J15) for establishing the startup configuration of the 78Q8430 device. Figure 2 shows the location of the jumpers. Table 1 describes the jumper options. The jumper numbers and settings are printed on the board.

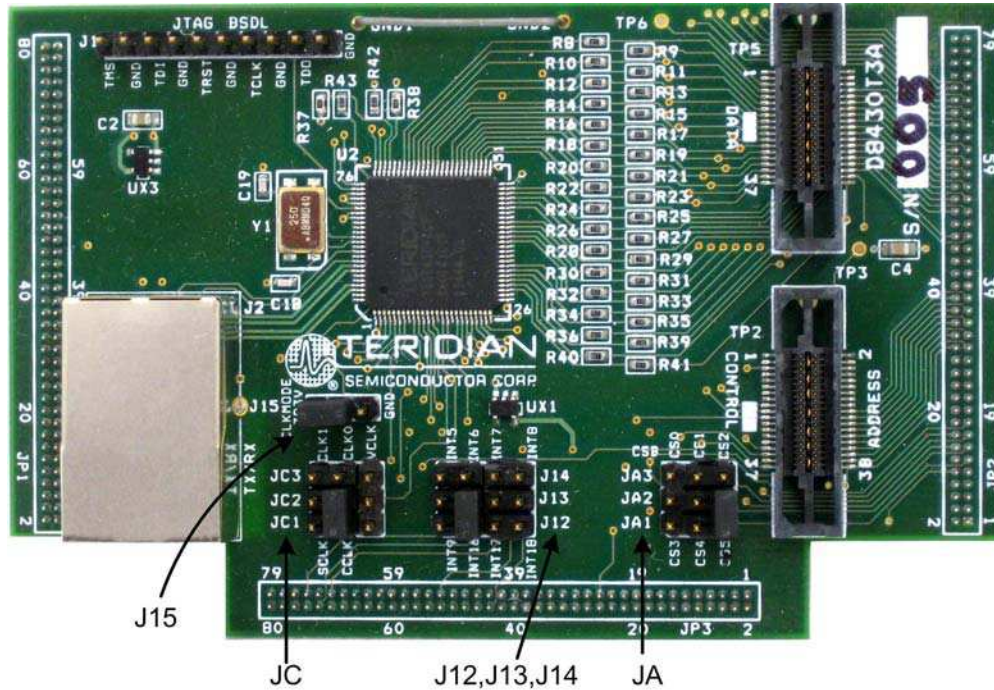


Figure 2: 78Q8430 Embest Evaluation Board Jumper Locations

Table 1: 78Q8430 Embest Evaluation Board Jumper Settings

Jumper	Name	Setting	Description
J15	CLKMODE Selection	GND	Internal clock.
		3P3V	External clock (default).
JA	Chip Select Source	CS0	Selects the source for the 78Q8430 chip select signal. The default setting is CS5.
		CS1	
		CS2	
		CS3	
		CS4	
J12 J13 J14	Interrupt Selection	INT5	Selects the destination for the 78Q8430 Interrupt signal. The default setting is INT16.
		INT6	
		INT7	
		INT8	
		INT9	
		INT16	
		INT17	
INT18			

Jumper	Name	Setting	Description
JC	Clock Source	CLK1	Selects the source for the 78Q8430 clock. The default setting is CCLK.
		CLK0	
		VCLK	
		SCLK	
		CCLK	

2.2 Connections

Connect the system components as shown in [Figure 3](#). Refer to the Embest S3CEB2410 documentation for additional information on the connections for that platform.

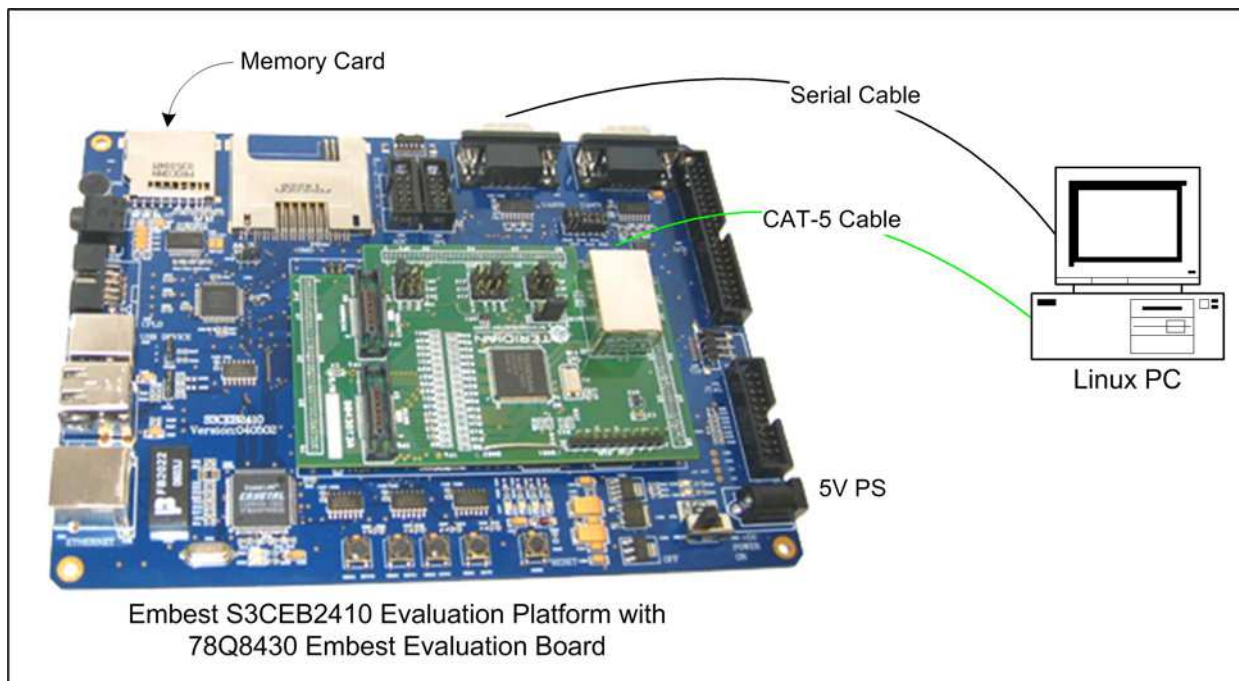


Figure 3: 78Q8430 Embest Evaluation System Hardware Connections

STEP 1: Attach the 78Q8430 Embest Evaluation Board to the S3CEB2410 Evaluation Board via the three connectors on the bottom of the 78Q8430 evaluation board.

STEP 2: Connect the 78Q8430 Embest Evaluation Board Ethernet port to the Linux PC using a CAT-5 cable.

STEP 3: Connect a serial console cable from the Linux Host PC serial port to the S3CEB2410 board serial port.

STEP 4: Insert the memory card containing the 78Q8430 Linux software device driver into the memory card slot on the S3CEB2410 board.

2.3 System Startup

STEP 1: On the Linux Host, set the testing port IP address to 192.168.10.100 (the S3CEB2410 platform boots with IP address 192.168.10.99).

STEP 2: Open a full height xterm or kconsole window on the Linux Host.

STEP 3: Start minicom on the Linux Host at the xterm/kconsole command prompt:

```
~# minicom
```

STEP 4: Turn on the S3CEB2410 board power. Refer to the S3CEB2410 documentation for additional information. The 78Q8430 Embest Evaluation Board receives its power through the Embest bus interface on the S3CEB2410 Evaluation Board.

STEP 5: Boot the S3CEB2410 Board. Console messages must appear in the minicom window after power on.

- Hit the space bar at the first boot prompt
- Respond with: **cpu set 200 2**
- On the next prompt, respond: **boot**

STEP 6: When boot up completes, enter the following at the prompt:

```
arp -s 192.168.10.100 00:0E:2E:5B:25:86
```

STEP 7: On the Linux Host, issue the following ping command to verify the connection to the target:

```
ping 192.168.10.99
```

3 78Q8430 Embest Evaluation Board Schematic, BOM and PCB Layout

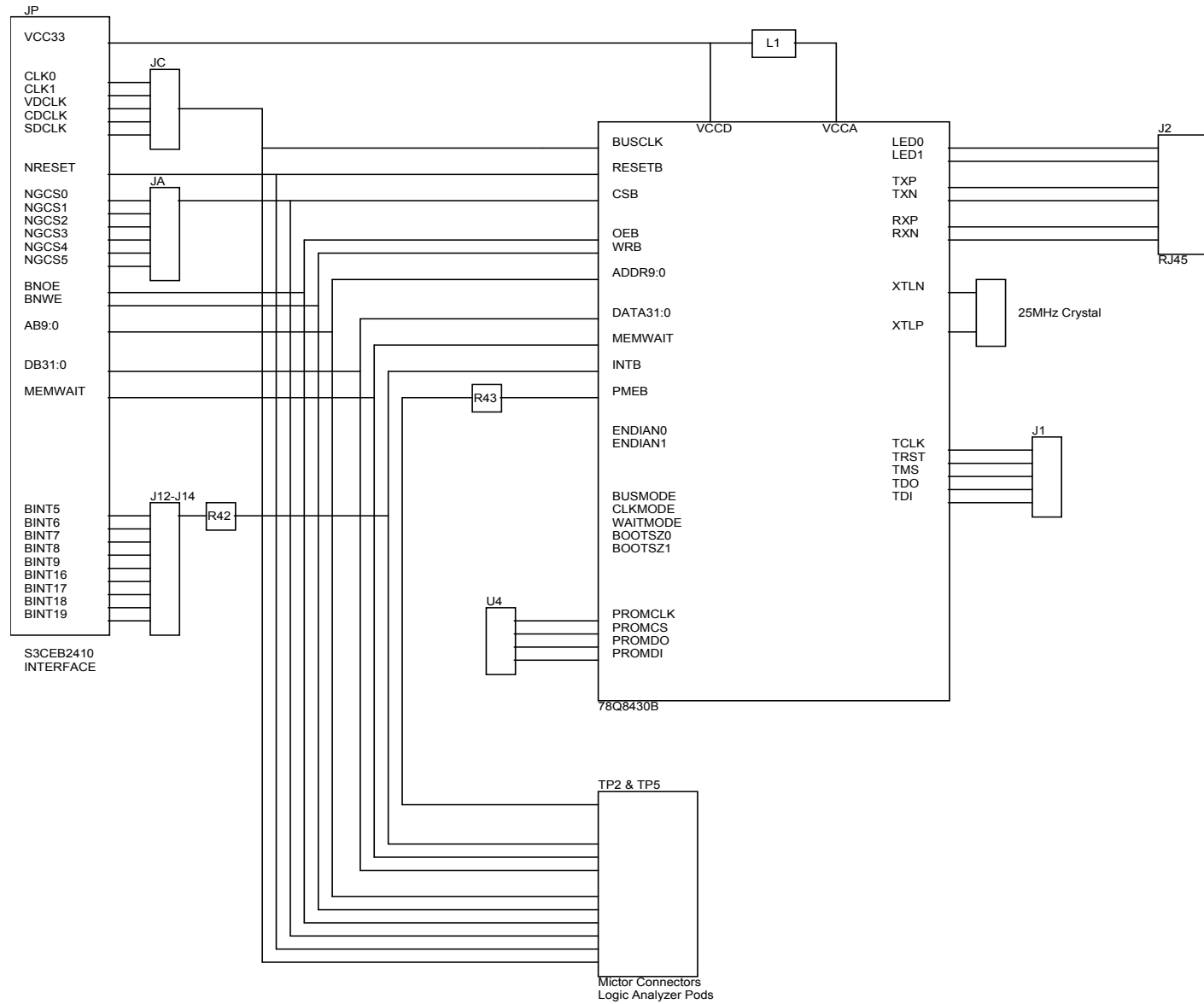


Figure 4: Bus Interface Block Diagram

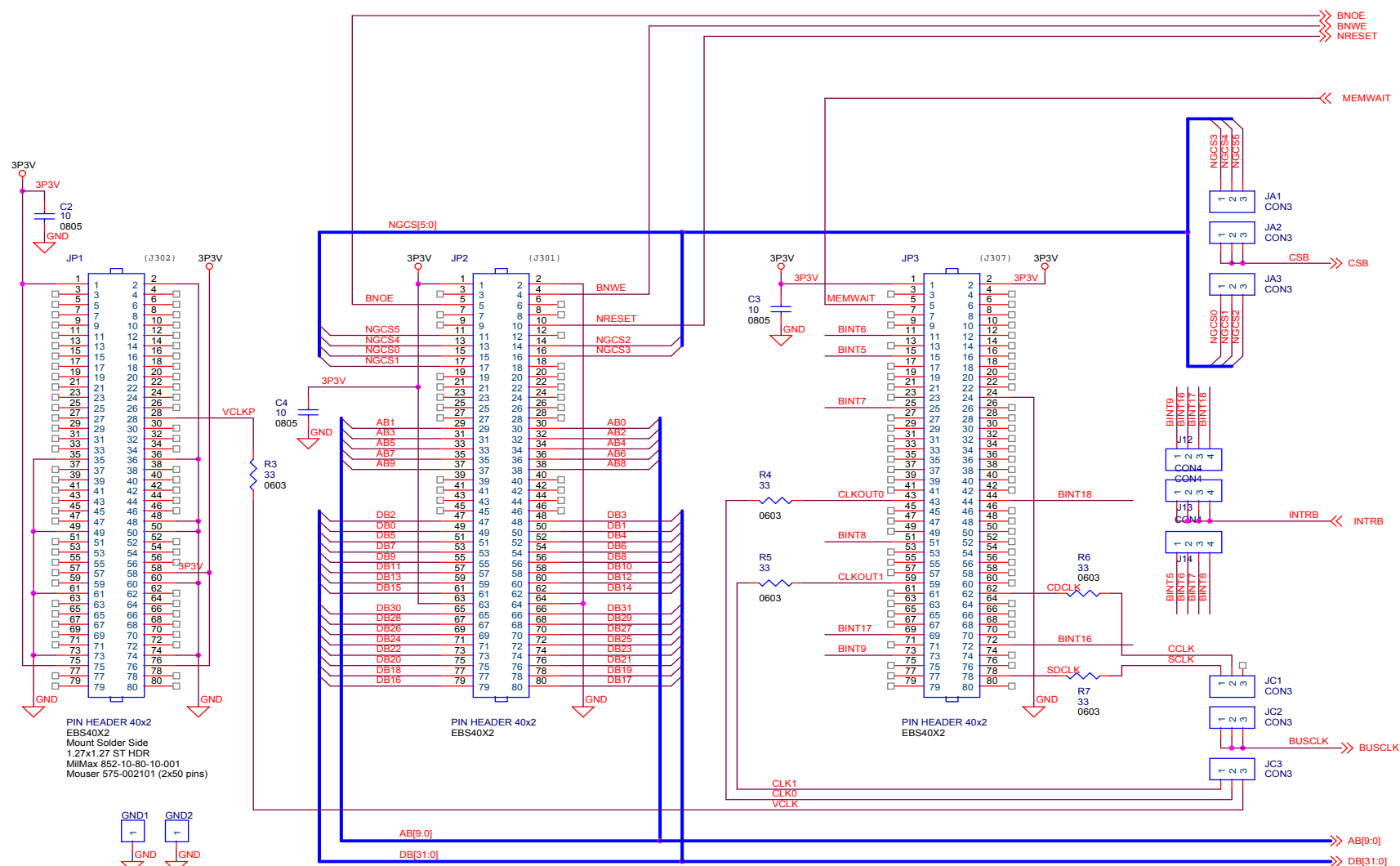


Figure 5: Bus Interface Schematic

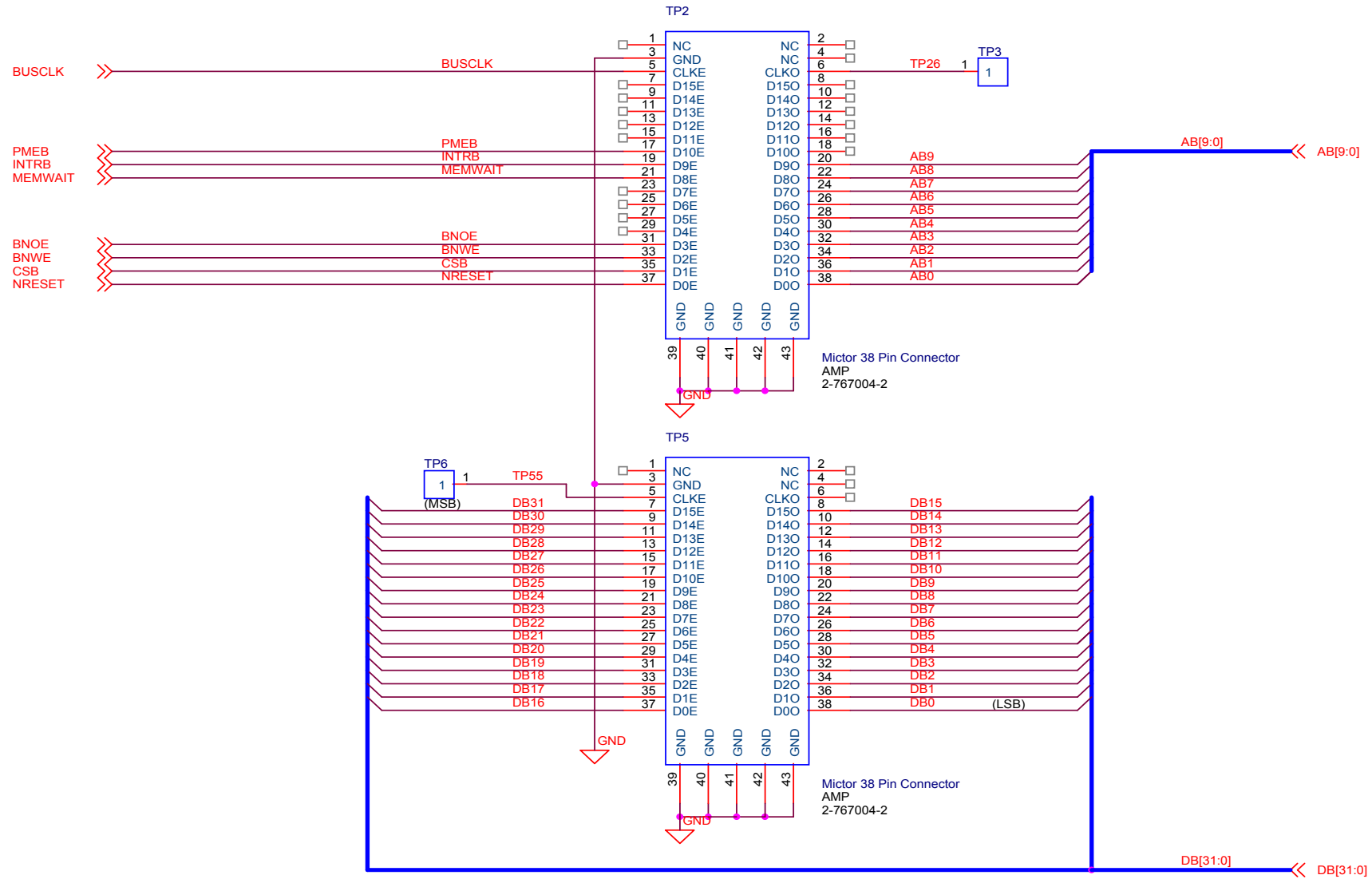


Figure 6: MICTOR Diagnostic Connectors Schematic

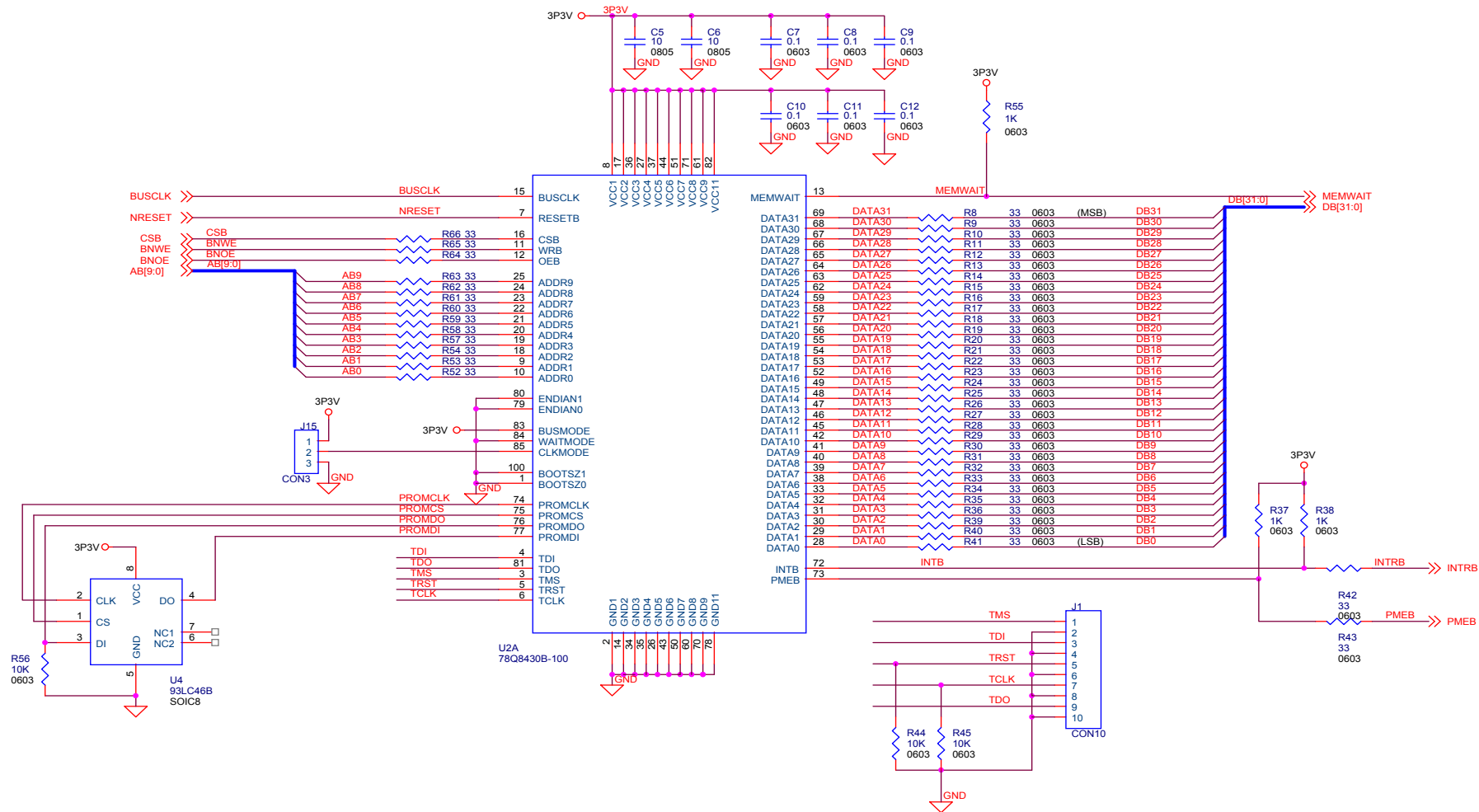


Figure 7: MAC Interface Schematic

Downloaded from: http://www.datasheetcatalog.com/

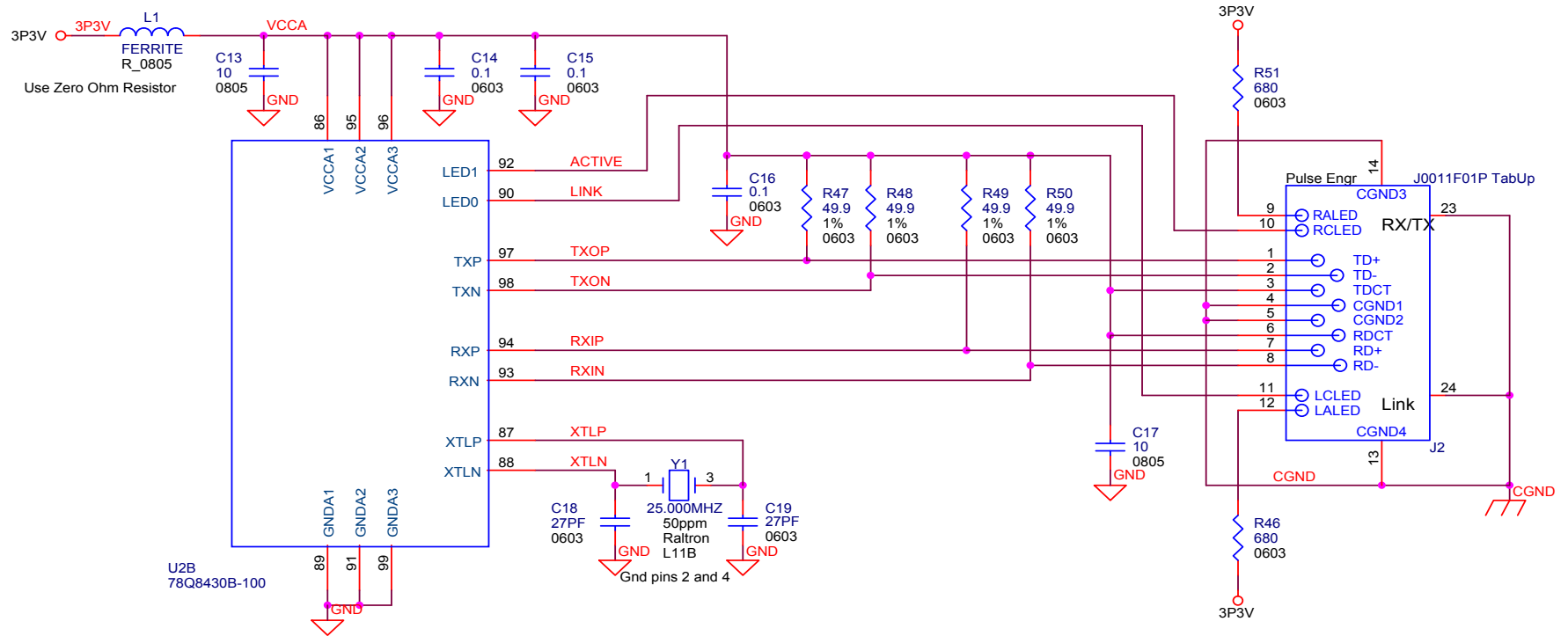


Figure 8: PHY Interface Schematic

Table 2: 78Q8430 Embest Evaluation Board Bill of Materials

Item	Quantity	Reference	Part	PCB Footprint	Part Number	Vendor
1	2	C18,C19	CAP., 27pF, 50V	C_0603	C1608C0G1H270J	TDK
2	9	C7-C12,C14-C16	CAP., 0.1uF,16V	C_0603	ECJ-1VB1E104K	Panasonic
3	7	C2-C6,C13,C17	CAP.,10uF,10V	C_0805	GRM21BR61A106KE19L	Murata
4	2	TP3,TP6	CON1	Testpoint	5011	Keystone
5	7	JA1-JA3,JC1-JC3, J15	SIP3	SIP\3P	PBC03SAAN	Sullins Electronics Corp
6	3	J12,J13,J14	SIP4	SIP\4P	PBC04SAAN	Sullins Electronics Corp
7	1	J1	CON10	SIP\10P	PBC10SAAN	Sullins Electronics Corp
8	3	JP1-JP3	40-Pin Header	EBS40X2	852-10-100-10-001000	Mill Max
9	1	J2	Integrated RJ45	RJ45-INT	J1011F01P	Pulse Eng
10	1	Y1	25MHz Crystal	XTAL-SMD	ABMM-25MHz	Abrakon
11	1	L1	Ferrite Bead	L_0805	MMZ2012S181A	TDK
12	3	R44,R45,R56	RES, 10k, 5%	R_0603	ERJ-3GEYJ103V	Panasonic
13	3	R37,R38,R55	RES, 1k, 1%	R_0603	ERJ-EEKF1001V	Panasonic
14	4	R47-R50	RES, 49.9, 1%	R_0603	ERJ-3EKF49R9V	Panasonic
15	52	R3-R36,R39-R43, R52,R53,R54, R57-R66	RES, 33, 5%	R_0603	ERJ-3GEYJ330V	Panasonic
16	2	R46,R51	RES, 680, 5%	R_0603	ERJ-3GEYJ681V	Panasonic
17	2	TP2,TP5	Mictor 38-pin	MICTOR	2-767004-2	Tyco
18	1	L1	Ferrite Bead	L_0805	MMZ2012S181A	TDK
19	1	U2	78Q8430	100 LQFP	78Q8430	Teridian Semiconductor
20	1	U4	93LC46	SOIC8	93LC46BT-I/SN	Microchip

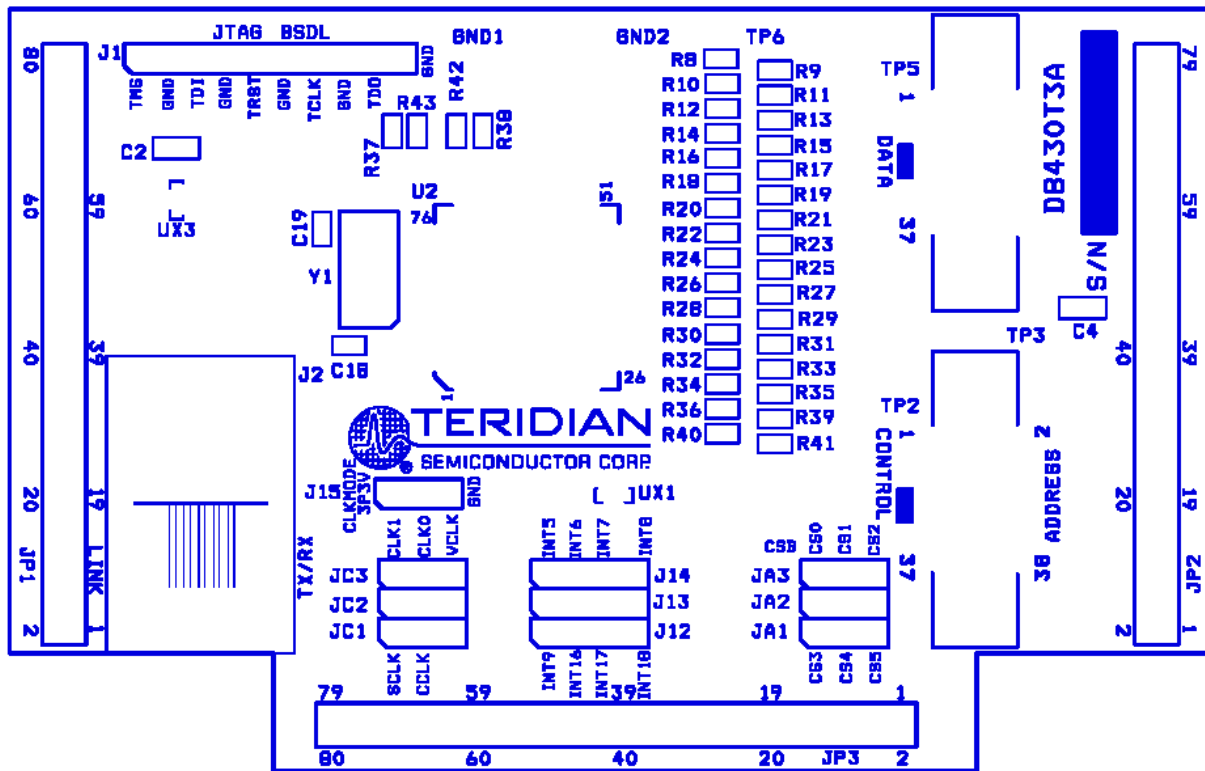


Figure 9: Top Silkscreen Layout

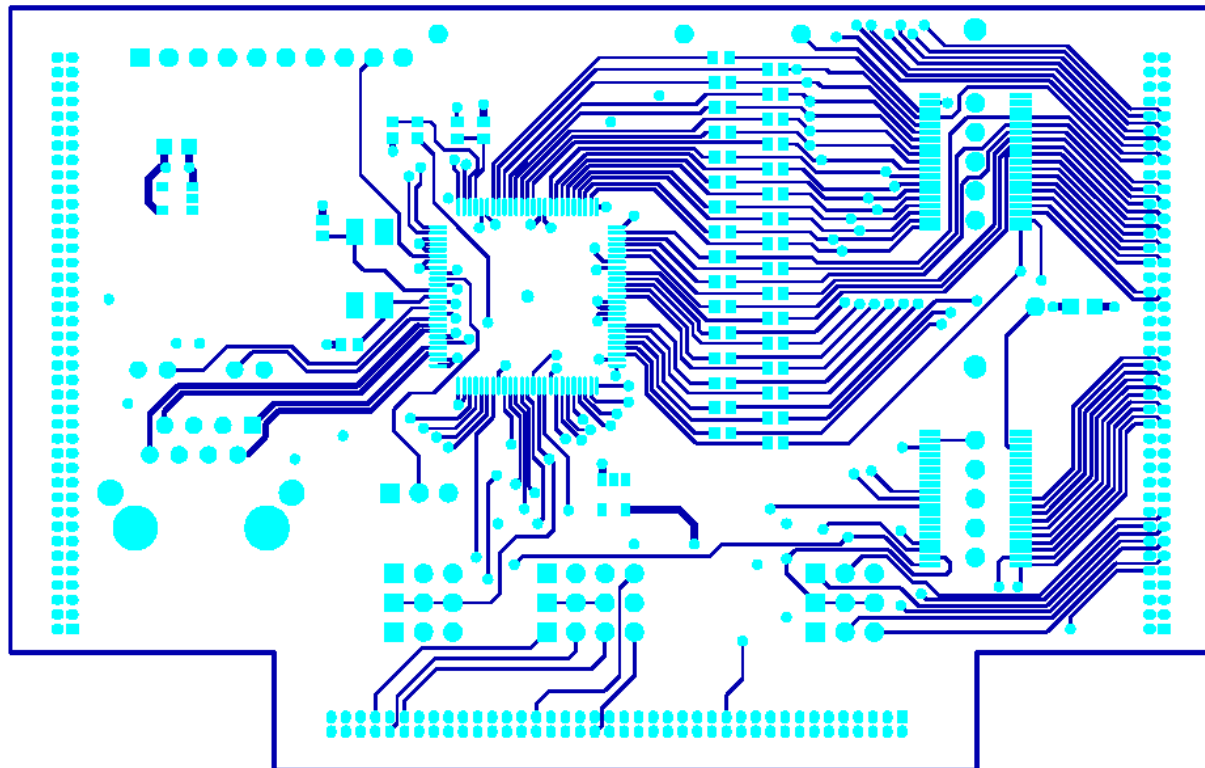


Figure 10: Top Layer Layout

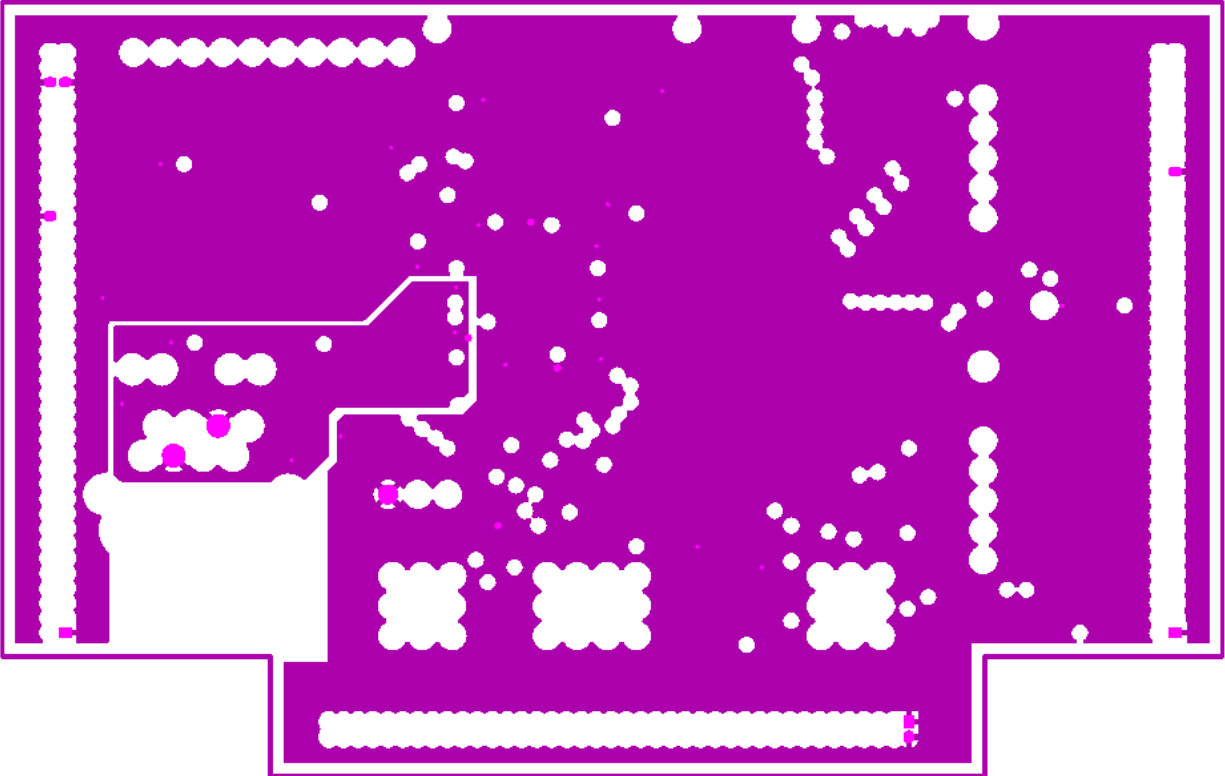


Figure 11: VCC Layer Layout

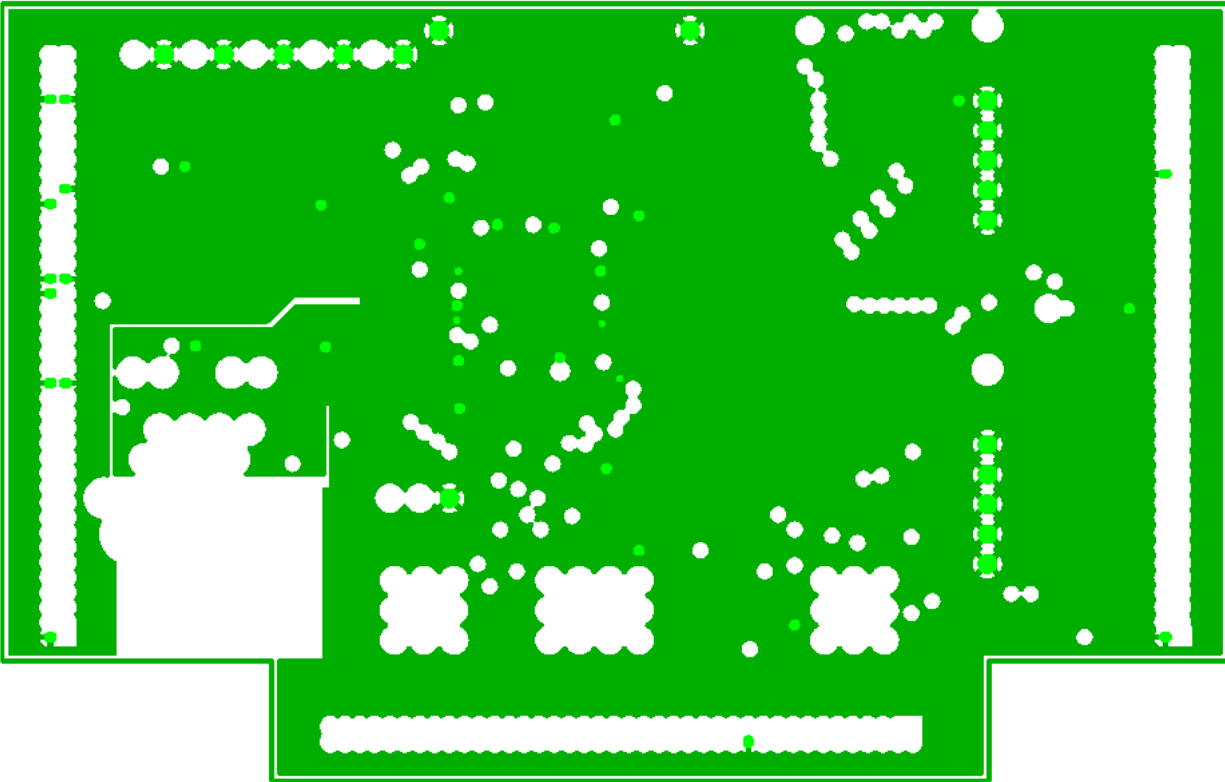


Figure 12: Ground Layer Layout

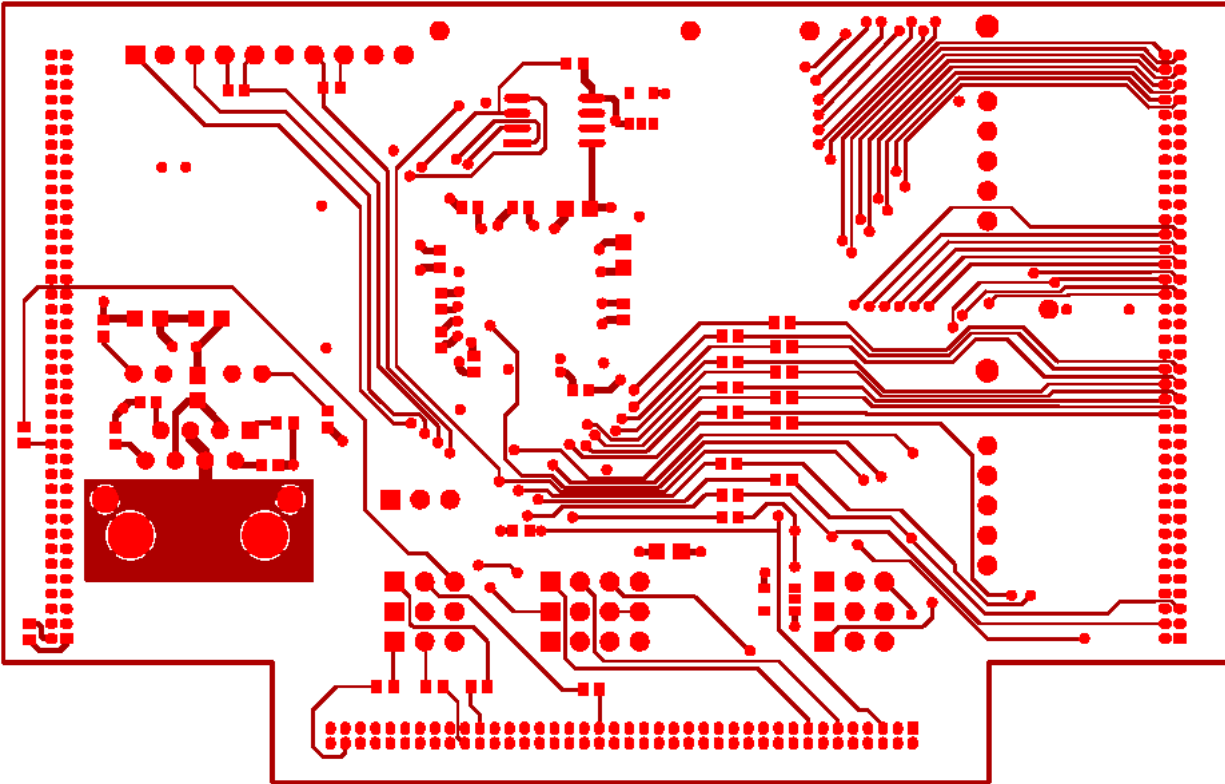


Figure 13: Bottom Layer Layout

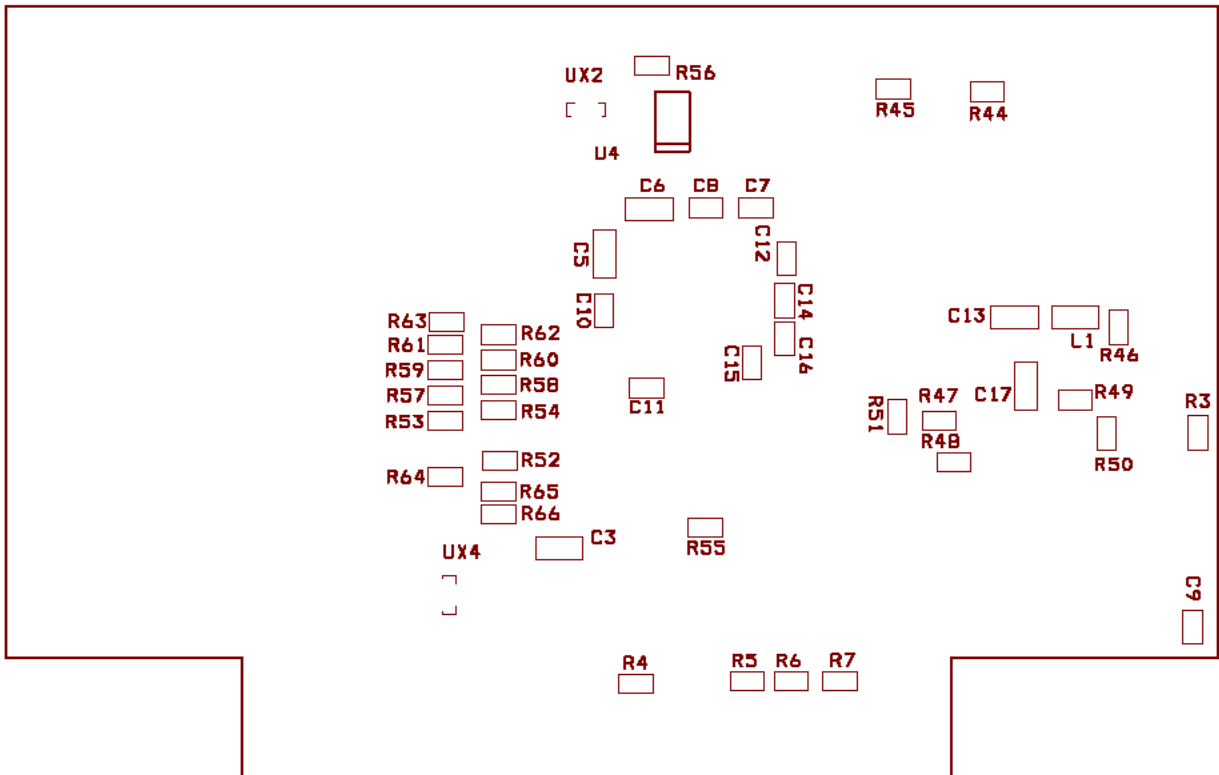


Figure 14: Bottom Silkscreen Layout

4 Ordering Information

Table 3 lists the order number for the 78Q8430 Embest Evaluation Board.

Table 3: Order Number and Part Description

Part Description	Order Number
78Q8430 Embest Evaluation Board (D8430T3A_EB)	EVM8430-ARM9

5 Related Documentation

The following 78Q8430 documents are available from Teridian Semiconductor Corporation:

78Q8430 Preliminary Data Sheet

78Q8430 Layout Guidelines

78Q8430 Software Driver Development Guidelines

78Q8430 Driver Guide for ST 5100/OS-20 with NexGen TCP/IP Stack

78Q8430 STEM Demo Board User Manual

78Q8430 Driver Guide for ARM920T Linux

78Q8430 ARM9(920T) Embest Evaluation Board User Manual

78Q8430 ARM9(920T) Linux Driver Diagnostic Guide

6 Contact Information

For more information about Teridian Semiconductor products or to check the availability of the 78Q8430, contact us at:

6440 Oak Canyon Road
Suite 100
Irvine, CA 92618-5201

Telephone: (714) 508-8800
FAX: (714) 508-8878
Email: lan.support@teridian.com

For a complete list of worldwide sales offices, go to <http://www.teridian.com>.

Revision History

Revision	Date	Description
1.0	May 6, 2008	First Publication