

**IRHG567110**

**RADIATION HARDENED 100V, Combination 2N-2P-CHANNEL  
 POWER MOSFET  
 THRU-HOLE (MO-036AB)**

**RAD-Hard™ HEXFET®  
 TECHNOLOGY**

**Product Summary**

Part Number	Radiation Level	RDS(on)	ID	CHANNEL
IRHG567110	100K Rads (Si)	0.29Ω	1.6A	N
IRHG563110	300K Rads (Si)	0.29Ω	1.6A	N
IRHG567110	100K Rads (Si)	0.96Ω	-0.96A	P
IRHG563110	300K Rads (Si)	0.96Ω	-0.96A	P



International Rectifier's RAD-Hard™ HEXFET® MOSFET Technology provides high performance power MOSFETs for space applications. This technology has over a decade of proven performance and reliability in satellite applications. These devices have been characterized for both Total Dose and Single Event Effects (SEE). The combination of low RDS(on) and low gate charge reduces the power losses in switching applications such as DC to DC converters and motor control. These devices retain all of the well established advantages of MOSFETs such as voltage control, fast switching, ease of paralleling and temperature stability of electrical parameters.

**Features:**

- Single Event Effect (SEE) Hardened
- Low RDS(on)
- Low Total Gate Charge
- Proton Tolerant
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Ceramic Package
- Light Weight
- ESD Rating: Class 1A per MIL-STD-750, Method 1020

**Absolute Maximum Ratings (Per Die)**

**Pre-Irradiation**

	Parameter	N-Channel	P-Channel	Units
ID @ VGS = ± 12V, TC = 25°C	Continuous Drain Current	1.6	-0.96	A
ID @ VGS = ± 12V, TC = 100°C	Continuous Drain Current	1.0	-0.6	
IDM	Pulsed Drain Current ①	6.4	-3.84	
PD @ TC = 25°C	Max. Power Dissipation	1.4	1.4	W
	Linear Derating Factor	0.011	0.011	W/°C
VGS	Gate-to-Source Voltage	± 20	± 20	V
EAS	Single Pulse Avalanche Energy	130 ②	200 ⑦	mJ
IAR	Avalanche Current ①	1.6	-0.96	A
EAR	Repetitive Avalanche Energy ①	0.14	0.14	mJ
dv/dt	Peak Diode Recovery dv/dt	6.5 ③	7.1 ⑧	V/ns
TJ	Operating Junction	-55 to 150		°C
TSTG	Storage Temperature Range			
	Lead Temperature	300 (0.63 in./1.6 mm from case for 10s)		
	Weight	1.3 (Typical)		g

For footnotes refer to the last page

**Electrical Characteristics For Each N-Channel Device @ T<sub>j</sub> = 25°C (Unless Otherwise Specified)**

	Parameter	Min	Typ	Max	Units	Test Conditions
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	100	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 1.0mA
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Temperature Coefficient of Breakdown Voltage	—	0.14	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1.0mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-State Resistance	—	—	0.29	Ω	V <sub>GS</sub> = 12V, I <sub>D</sub> = 1.0A ④
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	—	4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 1.0mA
g <sub>fs</sub>	Forward Transconductance	1.0	—	—	S	V <sub>DS</sub> = 15V, I <sub>DS</sub> = 1.0A ④
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	—	—	10	μA	V <sub>DS</sub> = 80V, V <sub>GS</sub> = 0V
		—	—	25		V <sub>DS</sub> = 80V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Leakage Forward	—	—	100	nA	V <sub>GS</sub> = 20V
I <sub>GSS</sub>	Gate-to-Source Leakage Reverse	—	—	-100		V <sub>GS</sub> = -20V
Q <sub>g</sub>	Total Gate Charge	—	—	17	nC	V <sub>GS</sub> = 12V, I <sub>D</sub> = 1.6A, V <sub>DS</sub> = 50V
Q <sub>gs</sub>	Gate-to-Source Charge	—	—	4.4		
Q <sub>gd</sub>	Gate-to-Drain ('Miller') Charge	—	—	3.9		
t <sub>d(on)</sub>	Turn-On Delay Time	—	—	21	ns	V <sub>DD</sub> = 50V, I <sub>D</sub> = 1.6A, V <sub>GS</sub> = 12V, R <sub>G</sub> = 7.5Ω
t <sub>r</sub>	Rise Time	—	—	16		
t <sub>d(off)</sub>	Turn-Off Delay Time	—	—	30		
t <sub>f</sub>	Fall Time	—	—	15		
LS + LD	Total Inductance	—	10	—	nH	Measured from Drain lead (6mm /0.25in. from package) to Source lead (6mm /0.25in from package) with Source wires internally bonded from Source Pin to Drain Pad
C <sub>iss</sub>	Input Capacitance	—	370	—	pF	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 25V f = 1.0MHz
C <sub>oss</sub>	Output Capacitance	—	110	—		
C <sub>rss</sub>	Reverse Transfer Capacitance	—	3.4	—		

**Source-Drain Diode Ratings and Characteristics (Per Die)**

	Parameter	Min	Typ	Max	Units	Test Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	1.6	A	T <sub>j</sub> = 25°C, I <sub>S</sub> = 1.6A, V <sub>GS</sub> = 0V ④
I <sub>SM</sub>	Pulse Source Current (Body Diode) ①	—	—	6.4		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.2	V	T <sub>j</sub> = 25°C, I <sub>F</sub> = 1.6A, di/dt ≤ 100A/μs
t <sub>rr</sub>	Reverse Recovery Time	—	—	110	ns	V <sub>DD</sub> ≤ 25V ④
Q <sub>RR</sub>	Reverse Recovery Charge	—	—	380	nC	
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by LS + LD.				

**Thermal Resistance (Per Die)**

	Parameter	Min	Typ	Max	Units	Test Conditions
R <sub>thJA</sub>	Junction-to-Ambient	—	—	90	°C/W	Typical socket mount

**Note:** Corresponding Spice and Saber models are available on International Rectifier Website.

For footnotes refer to the last page

Electrical Characteristics For Each P-Channel Device @ T<sub>j</sub> = 25°C (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BVDSS	Drain-to-Source Breakdown Voltage	-100	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = -1.0mA
ΔBVDSS/ΔT <sub>J</sub>	Temperature Coefficient of Breakdown Voltage	—	-0.14	—	V/°C	Reference to 25°C, I <sub>D</sub> = -1.0mA
RDS(on)	Static Drain-to-Source On-State Resistance	—	—	0.96	Ω	V <sub>GS</sub> = -12V, I <sub>D</sub> = -0.6A ④
VGS(th)	Gate Threshold Voltage	-2.0	—	-4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -1.0mA
gfs	Forward Transconductance	1.1	—	—	S	V <sub>DS</sub> = -15V, I <sub>DS</sub> = -0.6A ④
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	—	—	-10	μA	V <sub>DS</sub> = -80V, V <sub>GS</sub> = 0V
		—	—	-25		V <sub>DS</sub> = -80V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Leakage Forward	—	—	-100	nA	V <sub>GS</sub> = -20V
I <sub>GSS</sub>	Gate-to-Source Leakage Reverse	—	—	100		V <sub>GS</sub> = 20V
Q <sub>g</sub>	Total Gate Charge	—	—	13.4	nC	V <sub>GS</sub> = -12V, I <sub>D</sub> = -0.96A, V <sub>DS</sub> = -50V
Q <sub>gs</sub>	Gate-to-Source Charge	—	—	3.7		
Q <sub>gd</sub>	Gate-to-Drain ('Miller') Charge	—	—	3.0		
t <sub>d(on)</sub>	Turn-On Delay Time	—	—	21	ns	V <sub>DD</sub> = -50V, I <sub>D</sub> = -0.96A, V <sub>GS</sub> = -12V, R <sub>G</sub> = 7.5Ω
t <sub>r</sub>	Rise Time	—	—	17		
t <sub>d(off)</sub>	Turn-Off Delay Time	—	—	40		
t <sub>f</sub>	Fall Time	—	—	90		
LS + LD	Total Inductance	—	10	—	nH	Measured from Drain lead (6mm /0.25in. from package) to Source lead (6mm /0.25in. from package) with Source wires internally bonded from Source Pin to Drain Pad
C <sub>iss</sub>	Input Capacitance	—	390	—	pF	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 25V f = 1.0MHz
C <sub>oss</sub>	Output Capacitance	—	100	—		
C <sub>rss</sub>	Reverse Transfer Capacitance	—	7.0	—		

## Source-Drain Diode Ratings and Characteristics (Per Die)

	Parameter	Min	Typ	Max	Units	Test Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	-0.96	A	T <sub>J</sub> = 25°C, I <sub>S</sub> = -0.96A, V <sub>GS</sub> = 0V ④
I <sub>SM</sub>	Pulse Source Current (Body Diode) ①	—	—	-3.84		
V <sub>SD</sub>	Diode Forward Voltage	—	—	-5.0	V	T <sub>J</sub> = 25°C, I <sub>F</sub> = -0.96A, di/dt ≤ -100A/μs
t <sub>rr</sub>	Reverse Recovery Time	—	—	86	ns	V <sub>DD</sub> ≤ -25V ④
Q <sub>RR</sub>	Reverse Recovery Charge	—	—	240	nC	
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by LS + LD.				

## Thermal Resistance (Per Die)

	Parameter	Min	Typ	Max	Units	Test Conditions
R <sub>thJA</sub>	Junction-to-Ambient	—	—	90	°C/W	Typical socket mount

Note: Corresponding Spice and Saber models are available on International Rectifier Website.

For footnotes refer to the last page

International Rectifier Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at International Rectifier is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-39 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

**Table 1. Electrical Characteristics For Each N-Channel Device @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥**

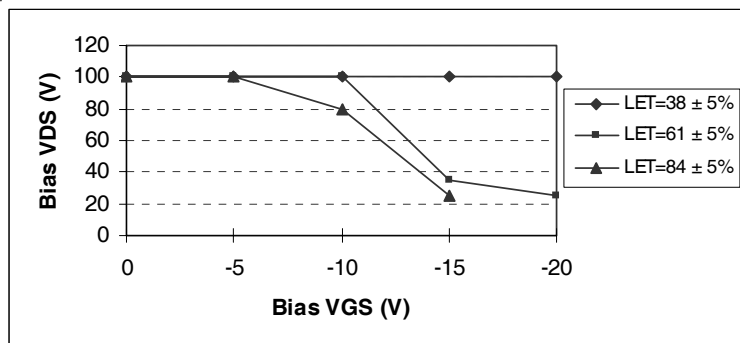
	Parameter	100K Rads(Si) <sup>1</sup>		300K Rads (Si) <sup>2</sup>		Units	Test Conditions
		Min	Max	Min	Max		
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	100	—	100	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 1.0mA
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	4.0	2.0	4.0		V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 1.0mA
I <sub>GSS</sub>	Gate-to-Source Leakage Forward	—	100	—	100	nA	V <sub>GS</sub> = 20V
I <sub>GSS</sub>	Gate-to-Source Leakage Reverse	—	-100	—	-100		V <sub>GS</sub> = -20V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	—	10	—	10	μA	V <sub>DS</sub> = 80V, V <sub>GS</sub> = 0V
R <sub>DS(on)</sub>	Static Drain-to-Source ④ On-State Resistance (TO-39)	—	0.226	—	0.246	Ω	V <sub>GS</sub> = 12V, I <sub>D</sub> = 1.0A
R <sub>DS(on)</sub>	Static Drain-to-Source ④ On-State Resistance (MO-036AB)	—	0.29	—	0.31	Ω	V <sub>GS</sub> = 12V, I <sub>D</sub> = 1.0A
V <sub>SD</sub>	Diode Forward Voltage ④	—	1.2	—	1.2	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = 1.6A

1. Part number IRHG567110
2. Part number IRHG563110

International Rectifier radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

**Table 2. Typical Single Event Effect Safe Operating Area (Per Die)**

LET (MeV/(mg/cm <sup>2</sup> ))	Energy (MeV)	Range (μm)	VDS (V)				
			@VGS = 0V	@VGS = -5V	@VGS = -10V	@VGS = -15V	@VGS = -20V
38 ± 5%	300 ± 7.5%	38 ± 7.5%	100	100	100	100	100
61 ± 5%	330 ± 7.5%	31 ± 10%	100	100	100	35	25
84 ± 5%	350 ± 10%	28 ± 7.5%	100	100	80	25	-



**Fig a. Typical Single Event Effect, Safe Operating Area**

For footnotes refer to the last page

## Radiation Characteristics

IRHG567110

International Rectifier Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at International Rectifier is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-39 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

**Table 1. Electrical Characteristics For Each P-Channel Device @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥**

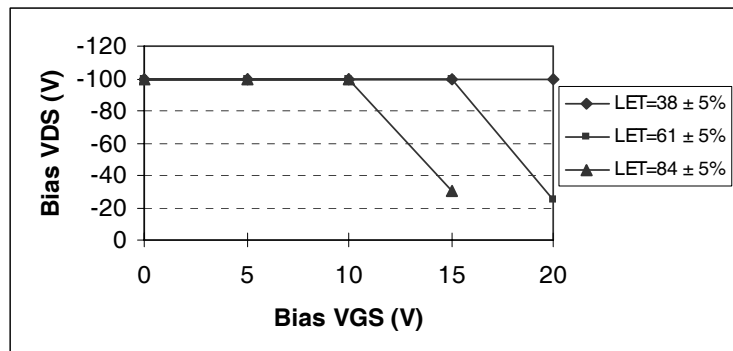
	Parameter	100K Rads (Si) <sup>1</sup>		300K Rads (Si) <sup>2</sup>		Units	Test Conditions
		Min	Max	Min	Max		
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	-100	—	-100	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = -1.0mA
V <sub>GS(th)</sub>	Gate Threshold Voltage	-2.0	-4.0	-2.0	-4.0		V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = -1.0mA
I <sub>GSS</sub>	Gate-to-Source Leakage Forward	—	-100	—	-100	nA	V <sub>GS</sub> = -20V
I <sub>GSS</sub>	Gate-to-Source Leakage Reverse	—	100	—	100		V <sub>GS</sub> = 20 V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	—	-10	—	-10	μA	V <sub>DS</sub> = -80V, V <sub>GS</sub> = 0V
R <sub>DS(on)</sub>	Static Drain-to-Source ④ On-State Resistance (TO-39)	—	0.916	—	0.936	Ω	V <sub>GS</sub> = -12V, I <sub>D</sub> = -0.6A
R <sub>DS(on)</sub>	Static Drain-to-Source ④ On-State Resistance (MO-036AB)	—	0.96	—	0.98	Ω	V <sub>GS</sub> = -12V, I <sub>D</sub> = -0.6A
V <sub>SD</sub>	Diode Forward Voltage ④	—	-3.5	—	-3.5	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = -0.96A

1. Part number IRHG567110
2. Part number IRHG563110

International Rectifier radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

**Table 2. Typical Single Event Effect Safe Operating Area (Per Die)**

LET (MeV/(mg/cm <sup>2</sup> ))	Energy (MeV)	Range (μm)	VDS (V)				
			@VGS = 0V	@VGS = 5V	@VGS = 10V	@VGS = 15V	@VGS = 20V
38 ± 5%	270 ± 7.5%	35 ± 7.5%	-100	-100	-100	-100	-100
61 ± 5%	330 ± 7.5%	30 ± 7.5%	-100	-100	-100	-100	-25
84 ± 5%	350 ± 7.5%	28 ± 7.5%	-100	-100	-100	-30	-



**Fig a. Typical Single Event Effect, Safe Operating Area**

For footnotes refer to the last page

N-Channel  
Q1,Q3

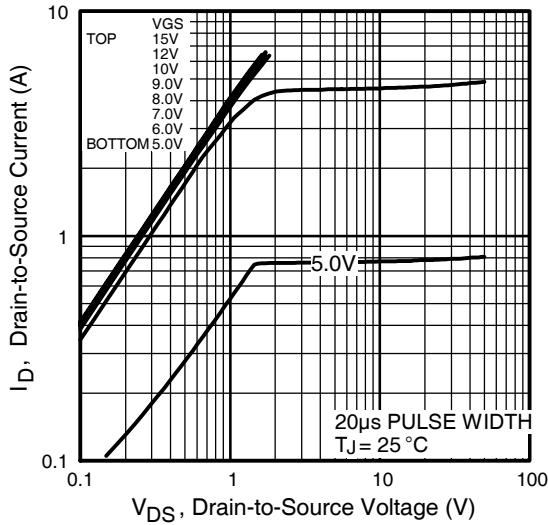


Fig 1. Typical Output Characteristics

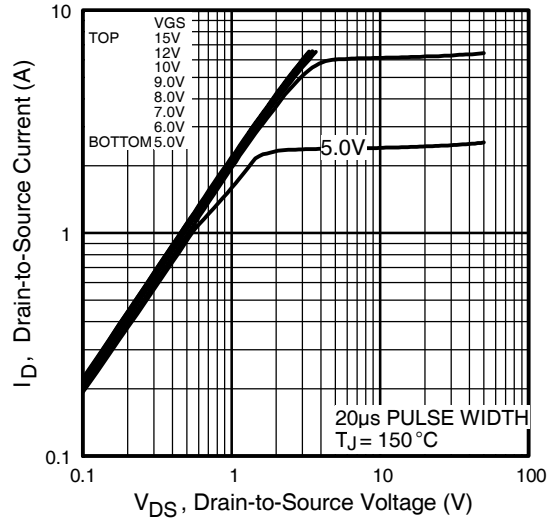


Fig 2. Typical Output Characteristics

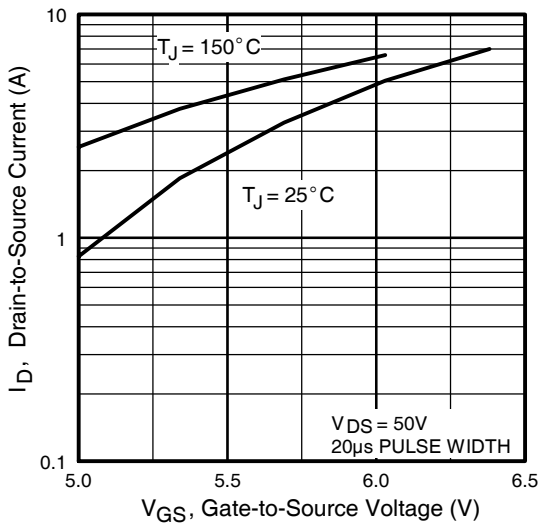


Fig 3. Typical Transfer Characteristics

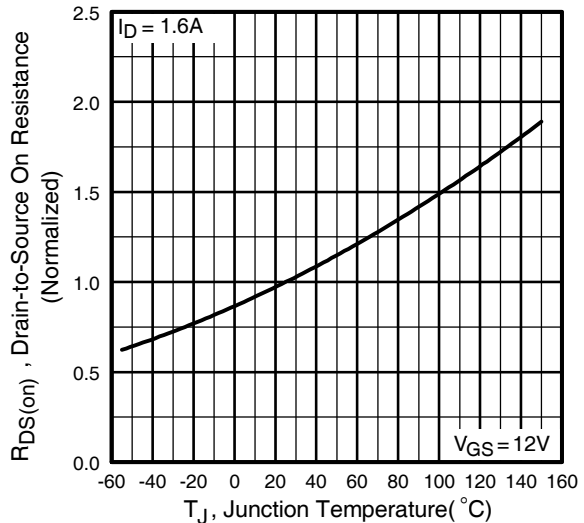


Fig 4. Normalized On-Resistance Vs. Temperature

N-Channel  
Q1,Q3

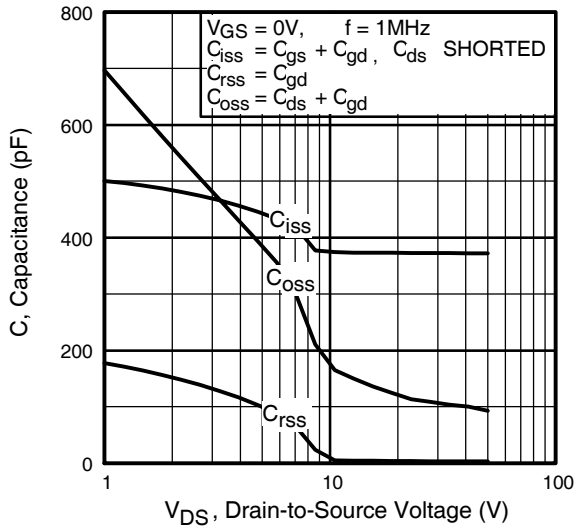


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

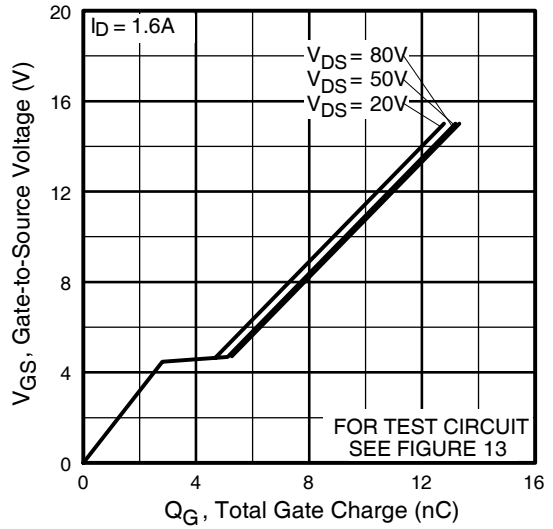


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

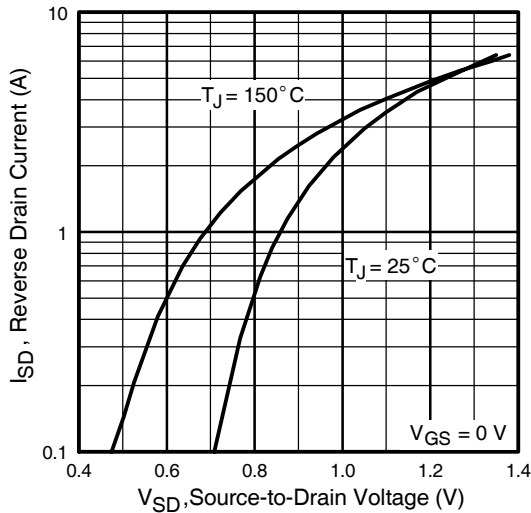


Fig 7. Typical Source-Drain Diode Forward Voltage

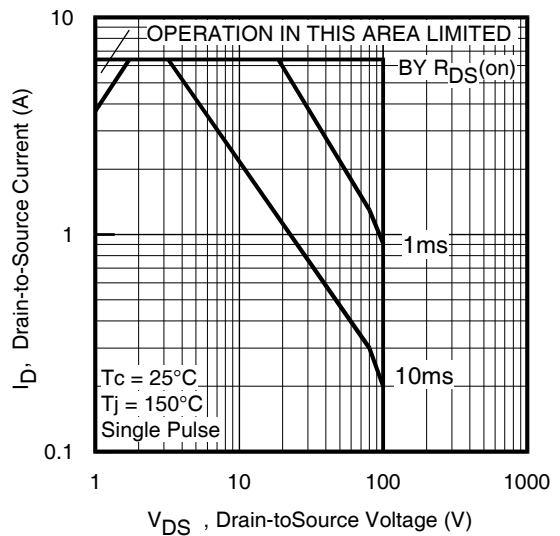


Fig 8. Maximum Safe Operating Area

N-Channel  
Q1,Q3

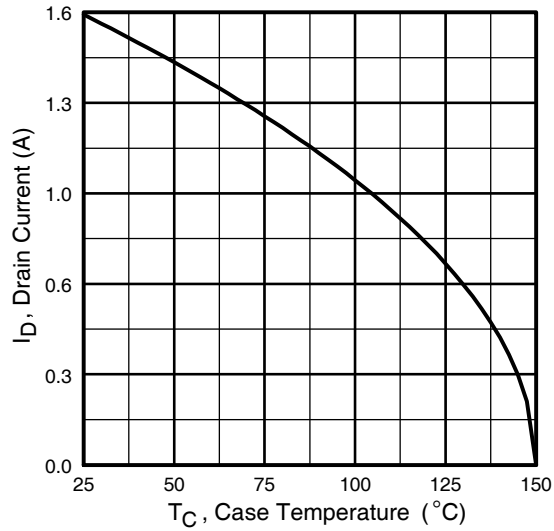


Fig 9. Maximum Drain Current Vs. Case Temperature

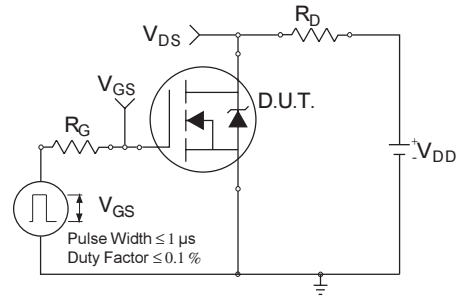


Fig 10a. Switching Time Test Circuit

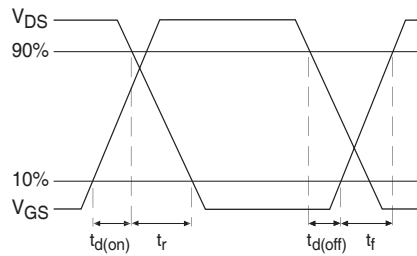


Fig 10b. Switching Time Waveforms

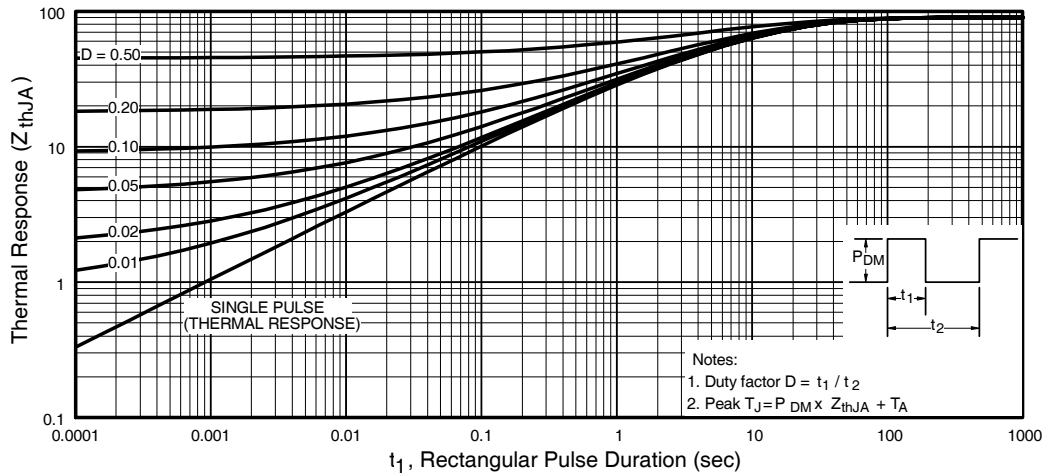


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient



N-Channel  
Q1,Q3

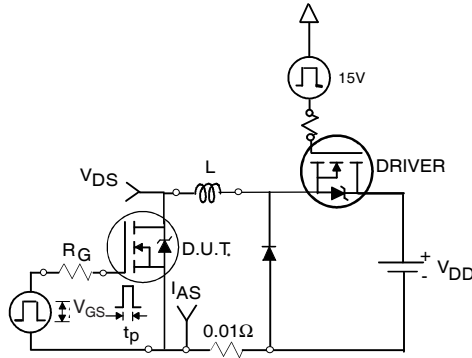


Fig 12a. Unclamped Inductive Test Circuit

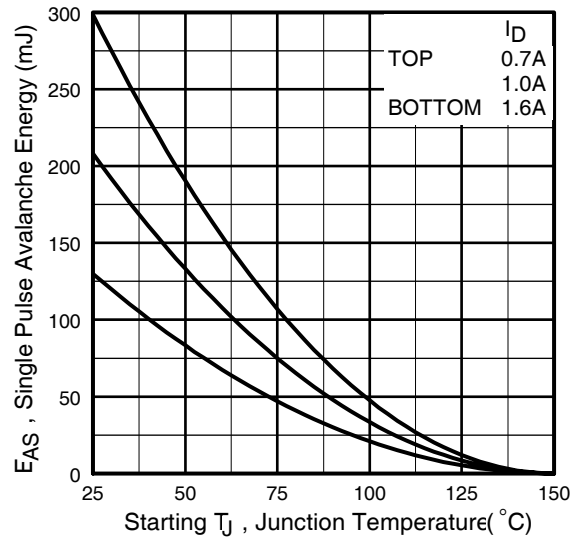


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

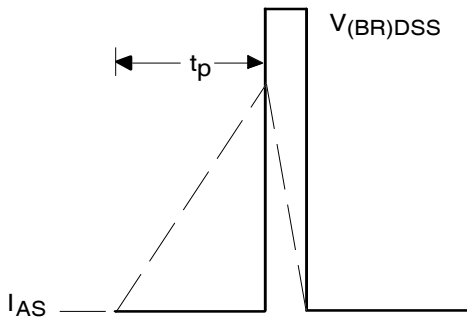


Fig 12b. Unclamped Inductive Waveforms

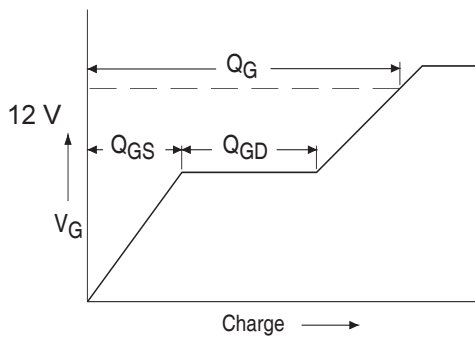


Fig 13a. Basic Gate Charge Waveform

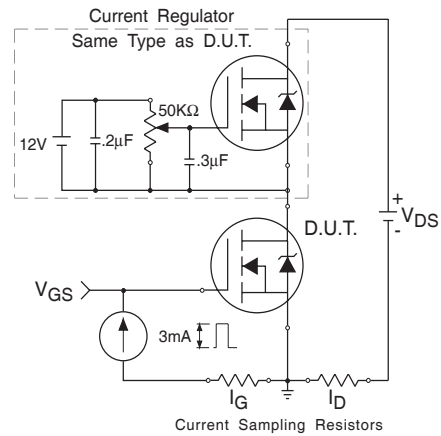


Fig 13b. Gate Charge Test Circuit

P-Channel  
Q2,Q4

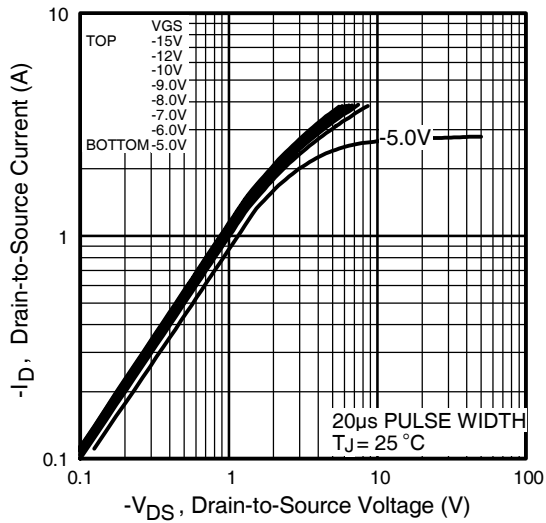


Fig 1. Typical Output Characteristics

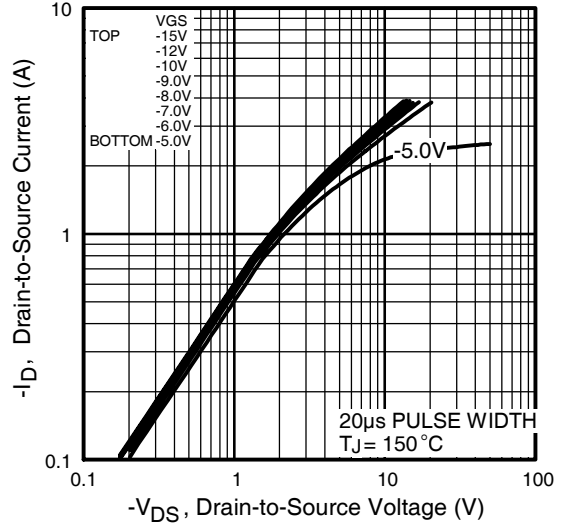


Fig 2. Typical Output Characteristics

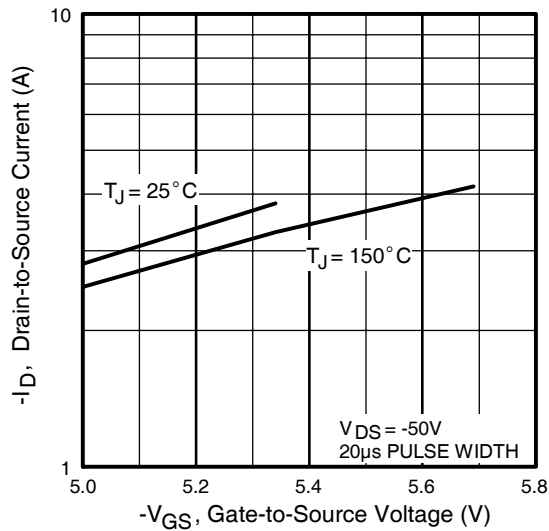


Fig 3. Typical Transfer Characteristics

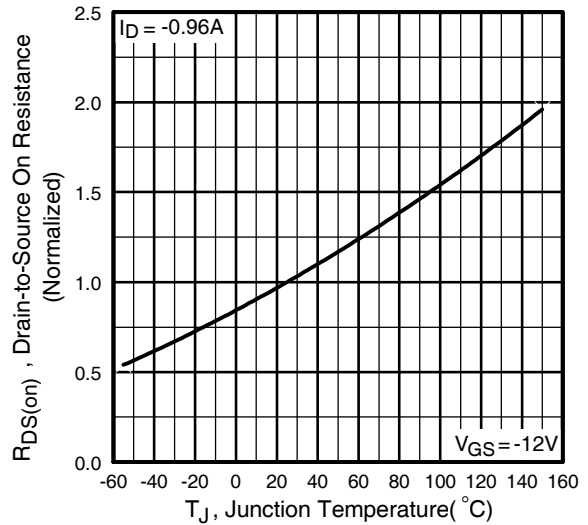
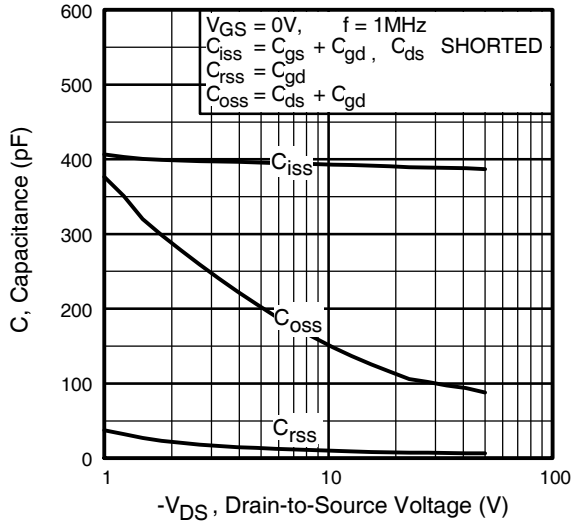
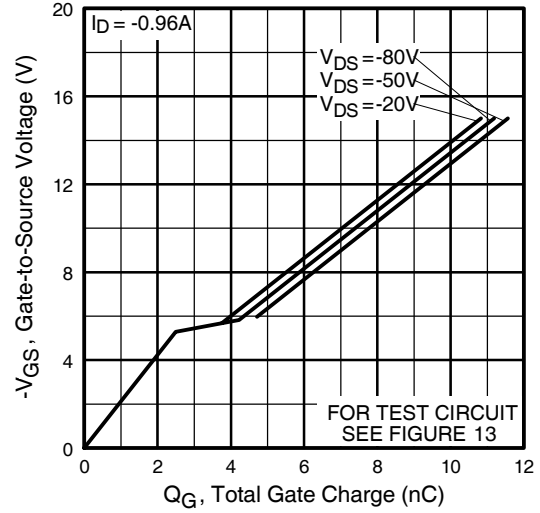


Fig 4. Normalized On-Resistance Vs. Temperature

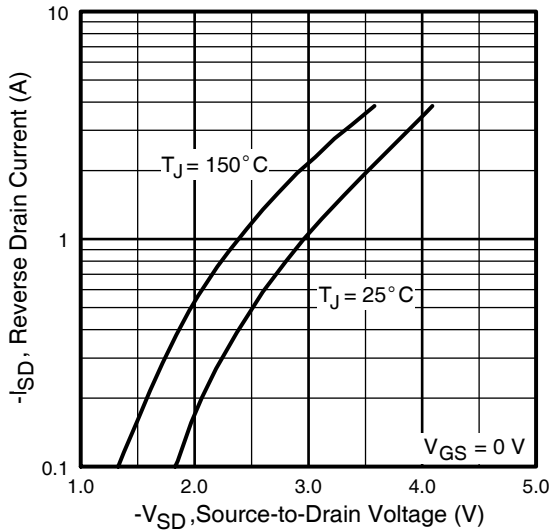
**P-Channel  
Q2,Q4**



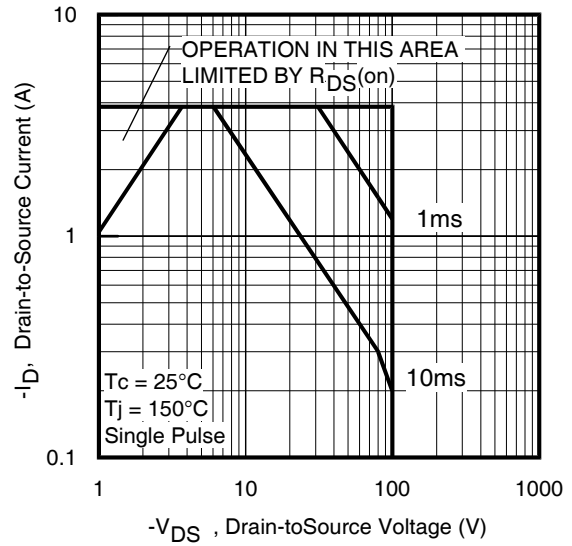
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



**Fig 7.** Typical Source-Drain Diode Forward Voltage



**Fig 8.** Maximum Safe Operating Area

P-Channel  
Q2,Q4

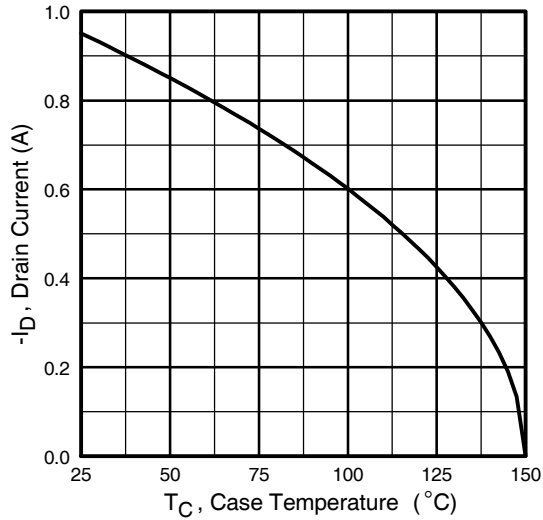


Fig 9. Maximum Drain Current Vs. Case Temperature

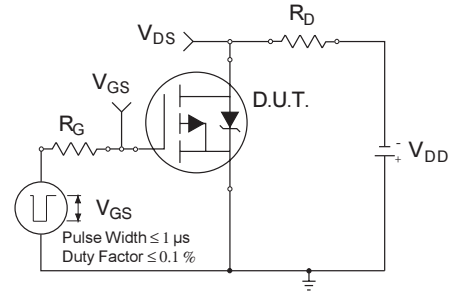


Fig 10a. Switching Time Test Circuit

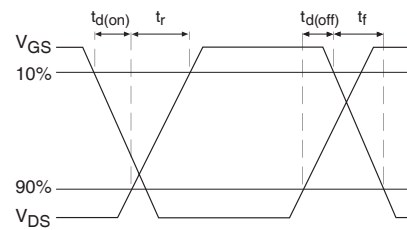


Fig 10b. Switching Time Waveforms

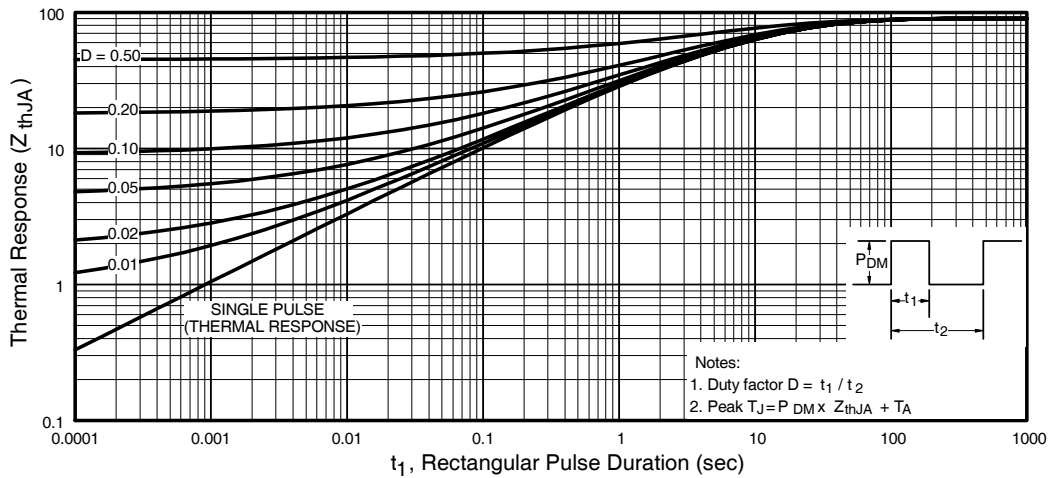
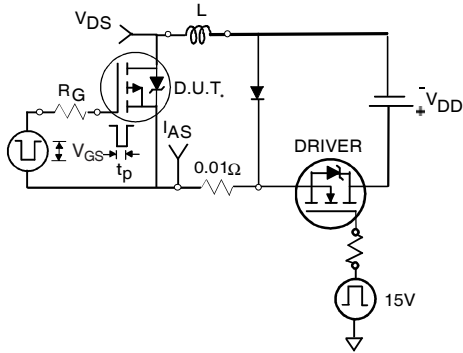
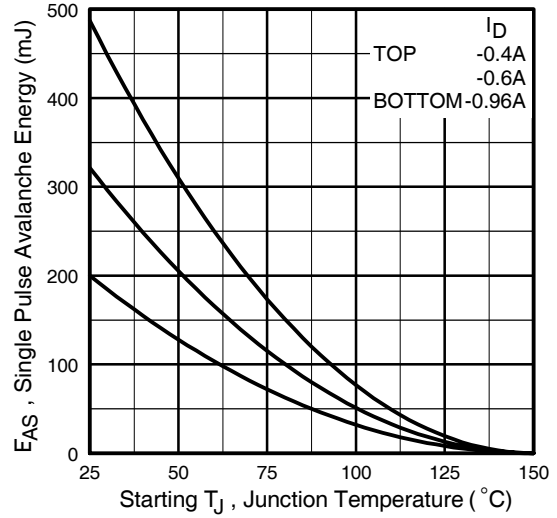


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

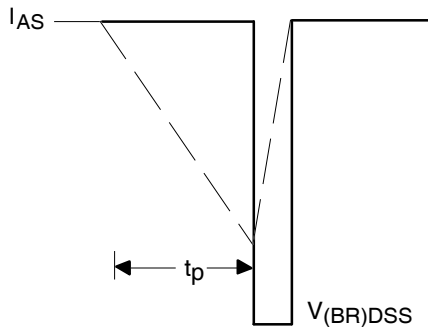
**P-Channel  
Q2,Q4**



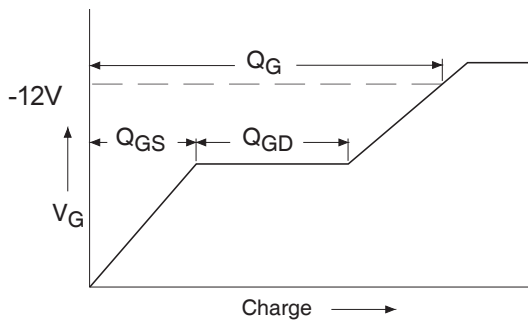
**Fig 12a.** Unclamped Inductive Test Circuit



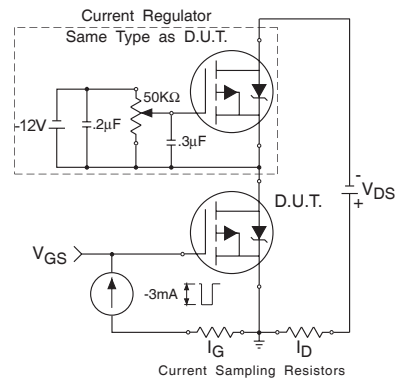
**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current



**Fig 12b.** Unclamped Inductive Waveforms



**Fig 13a.** Basic Gate Charge Waveform

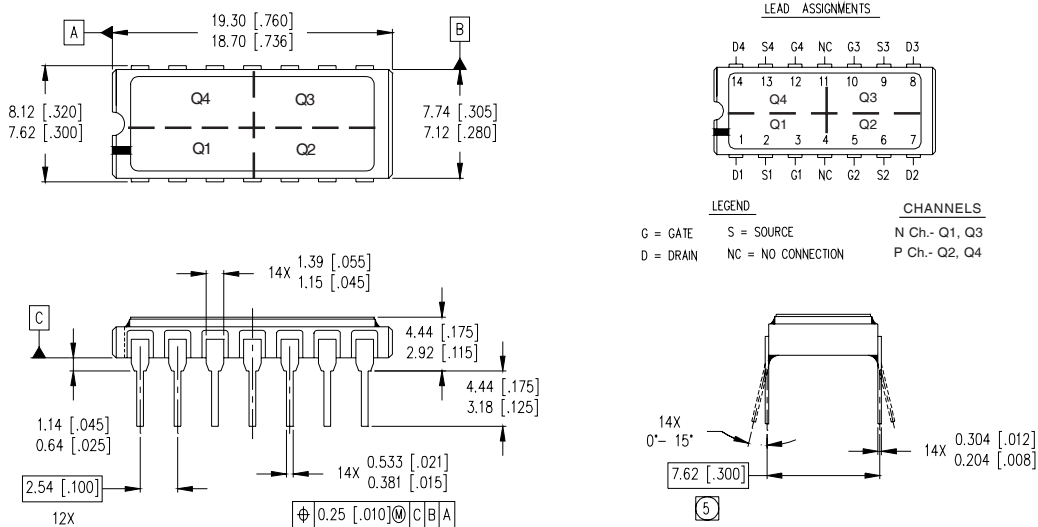


**Fig 13b.** Gate Charge Test Circuit

**Footnotes:**

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ②  $V_{DD} = 25V$ , starting  $T_J = 25^\circ C$ ,  $L = 100mH$ , Peak  $I_L = 1.6A$ ,  $V_{GS} = 12V$
- ③  $I_{SD} \leq 1.6A$ ,  $di/dt \leq 340A/\mu s$ ,  $V_{DD} \leq 100V$ ,  $T_J \leq 150^\circ C$
- ④ Pulse width  $\leq 300 \mu s$ ; Duty Cycle  $\leq 2\%$
- ⑤ **Total Dose Irradiation with  $V_{GS}$  Bias.**  
12 volt  $V_{GS}$  applied and  $V_{DS} = 0$  during irradiation per MIL-STD-750, method 1019, condition A
- ⑥ **Total Dose Irradiation with  $V_{DS}$  Bias.**  
80 volt  $V_{DS}$  applied and  $V_{GS} = 0$  during irradiation per MIL-STD-750, method 1019, condition A
- ⑦  $V_{DD} = -25V$ , starting  $T_J = 25^\circ C$ ,  $L = 430mH$ , Peak  $I_L = -0.96A$ ,  $V_{GS} = -12V$
- ⑧  $I_{SD} \leq -0.96A$ ,  $di/dt \leq -290A/\mu s$ ,  $V_{DD} \leq -100V$ ,  $T_J \leq 150^\circ C$

**Case Outline and Dimensions — MO-036AB**



**NOTES:**

- 1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
- 2. CONTROLLING DIMENSION: INCH.
- 3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- 4. OUTLINE CONFORMS TO JEDEC OUTLINE MO-036AB.
- ⑤ MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.

International  
**IR** Rectifier

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Data and specifications subject to change without notice. 07/2015