NEC Electronics Inc.

μPB100474E
1024 x 4-Bit
100K ECL RAM

T-46-23-08

Description

The μPB100474E is a very-high-speed 100K interface ECL RAM organized as 1024 words by 4 bits and designed with noninverted, open-emitter outputs and low power consumption.

Features

- 1024-word x 4-bit organization
- 100K ECL interface
- Noninverted, open-emitter outputs
- Fast access times
- Full voltage and temperature compensation
- 24-pin ceramic package, DIP or flatpack

Ordering Information

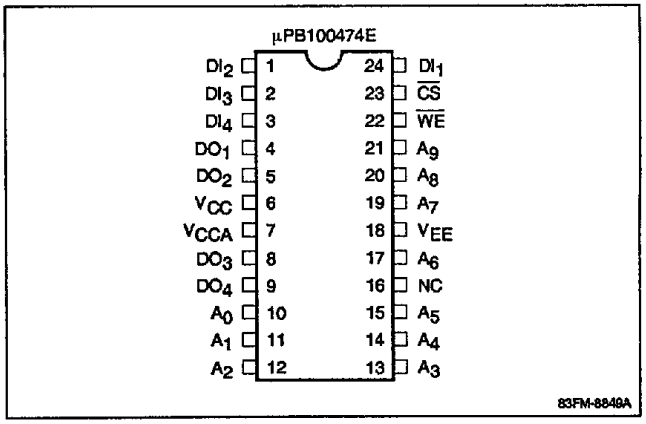
Part Number	Access Time (max)	Package
μPB100474EDH-3	3 ns	24-pin cerdip
DH-4	4 ns	
μPB100474EBH-3	3 ns	24-pin ceramic flatpack
BH-4	4 ns	

Pin Identification

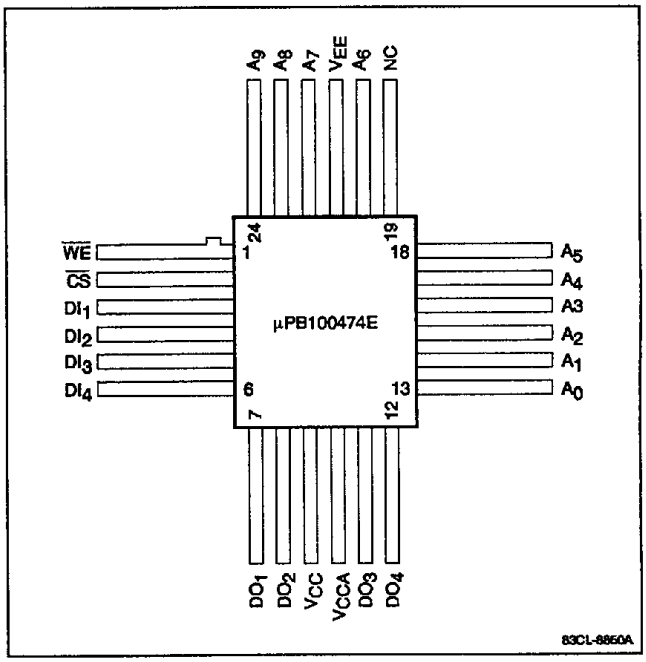
Symbol	Function
A_0 - A_9	Address inputs
DI_1 - DI_4	Data inputs
DO_1 - DO_4	Data outputs
$\overline{WE}$	Write enable input
$\overline{CS}$	Chip select input
V_{CC}	Power supply ground (current switches and bias driver)
V_{CCA}	Power supply ground (output devices)
V_{EE}	Power supply (–5.2 volts)
NC	No connection

Pin Configurations

24-Pin Cerdip



24-Pin Ceramic Flatpack



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Absolute Maximum Ratings

Supply voltage, V_{EE} to V_{CC}	−7.0 to +0.5 V
Input voltage, V_{IN}	V_{EE} to +0.5 V
Output current, I_{OUT}	−30 to +0.1 mA
Storage temperature, T_{STG}	−65 to +150°C
Storage temperature under bias, T_{STG} (bias)	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

f = 1 MHz

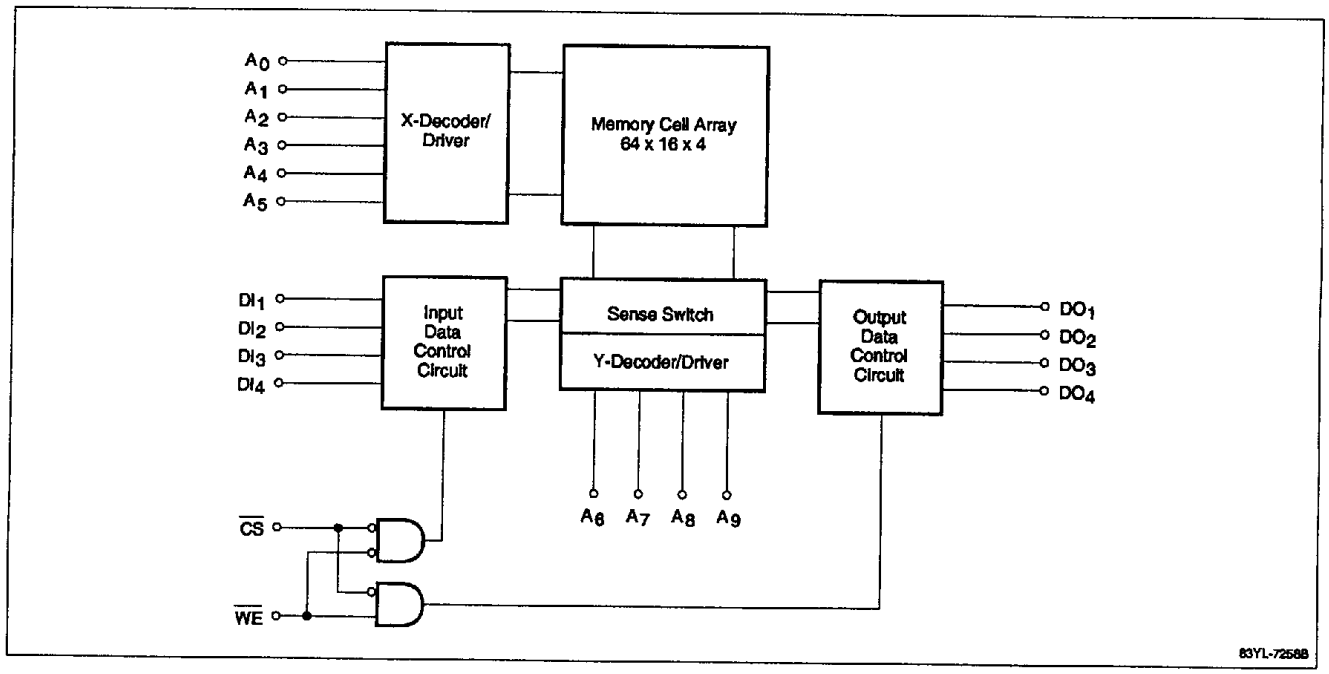
Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}		4		pF
Output capacitance	C_{OUT}		5		pF

Truth Table

$\overline{CS}$	$\overline{WE}$	D_{IN}	Output	Mode
H	X	X	L	Not selected
L	L	L	L	Write 0
L	L	H	L	Write 1
L	H	X	D_{OUT}	Read

X = don't care.

Block Diagram



DC Characteristics

T_A = 0 to +85°C; V_{CC} = V_{CCA} = 0 V; V_{EE} = −4.5 V; output load = 50 Ω to −2.0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1025		−880	mV	V_{IN} = V_{IH} max or V_{IL} min;
Output voltage, low	V_{OL}	−1810		−1620	mV	V_{IN} = V_{IH} max or V_{IL} min;
Output threshold voltage, high	V_{OHC}	−1035			mV	V_{IN} = V_{IH} min or V_{IL} max;
Output threshold voltage, low	V_{OLC}			−1610	mV	V_{IN} = V_{IH} min or V_{IL} max;
Input voltage, high	V_{IH}	−1165		−880	mV	For all inputs: T_A = 0°C
Input voltage, low	V_{IL}	−1810		−1475	mV	For all inputs: T_A = 0°C
Input current, high	I_{IH}			220	μA	V_{IN} = V_{IH} max
Input current, low	I_{IL}	0.5		170	μA	For $\overline{CS}$: V_{IN} = V_{IL} min
		−50			μA	For all others: V_{IN} = V_{IL} min
Supply current	I_{EE}	−330			mA	All inputs and outputs open

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

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AC Characteristics

T_A = 0 to +85°C; V_{EE} = −4.5 V ± 5%; output load = 50 Ω to −2.0 V

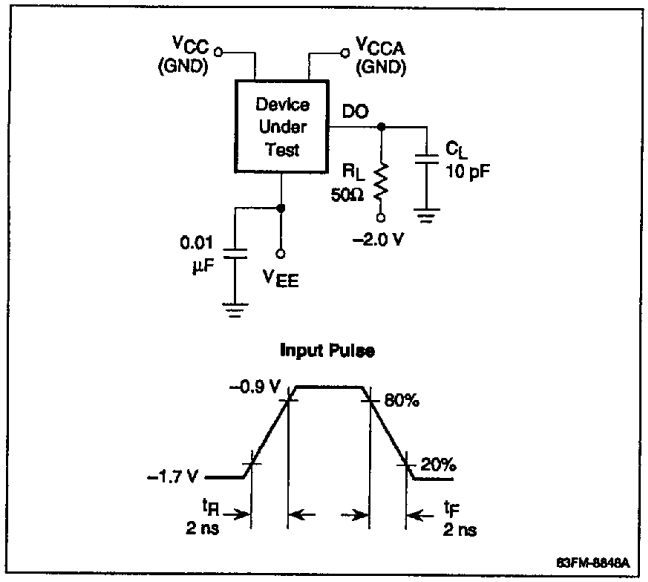
		μPB100474E-3			μPB100474E-4				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions
Read Operation									
Address access time	t_{AA}			3			4	ns	
Chip select access time	t_{ACS}			2			3	ns	
Chip select recovery time	t_{RCS}			2			3	ns	
Write Operation									
Write pulse width	t_W	5			6			ns	
Address hold time	t_{WHA}	0.5			0.5			ns	
Chip select hold time	t_{WHCS}	0.5			0.5			ns	
Data hold time	t_{WHD}	0.5			0.5			ns	
Write recovery time	t_{WR}			4			5	ns	
Write disable time	t_{WS}			2			3	ns	
Address setup time	t_{WSA}	0.5			0.5			ns	
Chip select setup time	t_{WSCS}	0.5			0.5			ns	
Data setup time	t_{WSD}	0.5			0.5			ns	

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

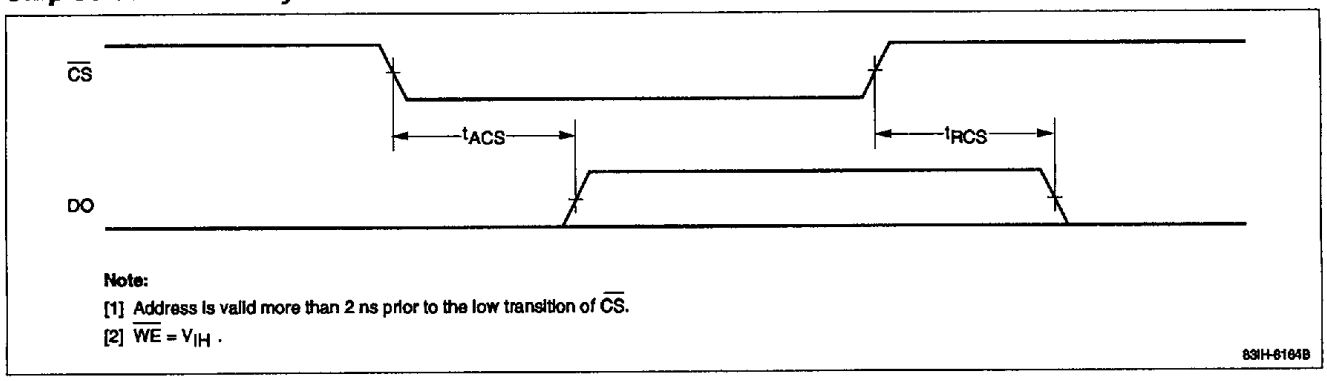
(2) See figure 1 for loading conditions and input pulse shape.

Figure 1. Test Circuit



Timing Waveforms

Chip Select Access Cycle



Note:
[1] Address is valid more than 2 ns prior to the low transition of $\overline{CS}$.
[2] $\overline{WE} = V_{IH}$.

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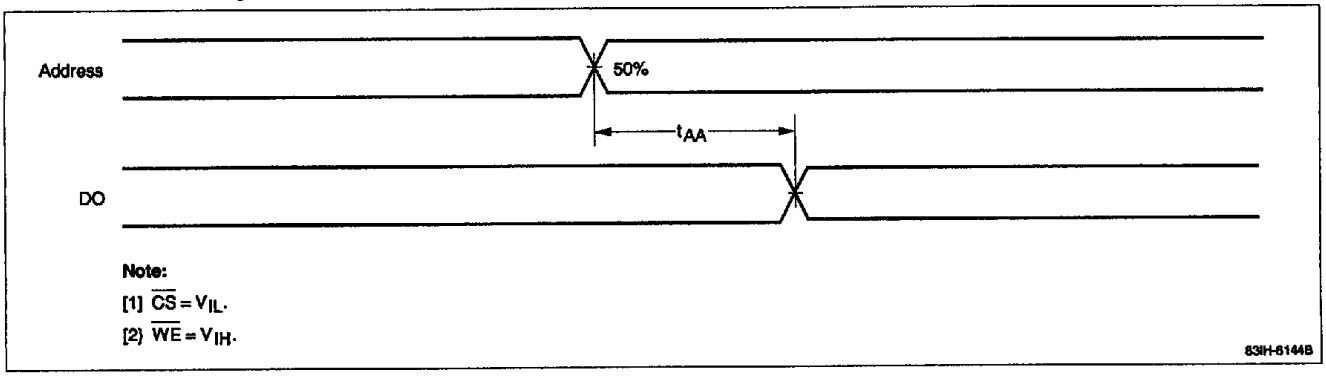
Address Access Cycle



Note:
[1] $\overline{CS} = V_{IL}$.
[2] $\overline{WE} = V_{IH}$.

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Timing Waveforms (cont)

Write Cycle