Elektronische Bauelemente

SGE2329S

-1.5A, -100V, $R_{DS(ON)}$ 650mΩ
P-Channel Enhancement Mode Power MOSFET

RoHS Compliant Product
A suffix of "-C" specifies halogen free

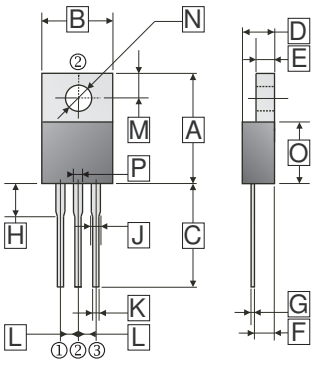
DESCRIPTION

The SGE2329S uses advanced trench technology to provide excellent on-resistance extremely efficient and cost-effectiveness device. The through-hole version is available for low-profile applications and suited for low voltage applications such as DC/DC converters.

FEATURES

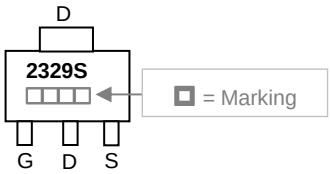
- High Density Cell Design for Ultra Low On-Resistance
- High power and Current handling capability
- Excellent CdV/dt effect decline
- 100% EAS and 100% Rg Guaranteed
- Green Device Available

TO-220

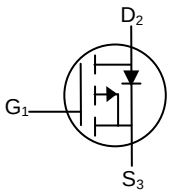


REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	14.22	16.51	J	0.7	1.78
B	9.65	10.67	K	0.38	1.02
C	12.50	14.75	L	2.39	2.69
D	3.56	4.90	M	2.50	3.43
E	0.51	1.45	N	3.10	4.09
F	2.03	2.92	O	8.38	9.65
G	0.31	0.76	P	0.89	1.47
H	3.5	4.5			

PACKAGE CODE



P-Channel



ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DS}	-100	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current, V_{GS}@10V[1]	T_A=25℃	I_D	-1.5	A
	T_A=70℃		-1.2	A
Pulsed Drain Current[2]		I_{DM}	-5.5	A
Total Power Dissipation[3]	T_A=25℃	P_D	2	W
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 ~ +150	℃
Thermal Resistance Ratings				
Thermal Resistance Junction-ambient[1]	Max.	$R_{\theta JA}$	62.5	℃/W

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ELECTRICAL CHARACTERISTICS (T_J= 25°C unless otherwise specified)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test condition
Drain-Source Breakdown Voltage		BV_{DSS}	-100	-	-	V	V_{GS}=0, I_D= -250uA
Gate Threshold Voltage		$V_{GS(th)}$	-1	-	-2.5	V	V_{DS}=V_{GS}, I_D= -250uA
Forward Transconductance		g_{fs}	-	3	-	S	V_{DS}= -5V, I_D= -1A
Gate-Source Leakage Current		I_{GSS}	-	-	±100	nA	V_{GS}= ±20V
Drain-Source Leakage Current	T_J=25℃	I_{DSS}	-	-	-1	μA	V_{DS}= -80V, V_{GS}=0
	T_J=55℃		-	-	-5	μA	
Static Drain-Source On-Resistance		$R_{DS(ON)}$	-	-	650	mΩ	V_{GS}= -10V, I_D= -1A
			-	-	700		V_{GS}= -4.5V, I_D= -0.5A
Total Gate Charge[2]		Q_g	-	9.3	-	nC	I_D= -1A V_{DS}= -50V V_{GS}= -10V
Gate-Source Charge		Q_{gs}	-	1.75	-		
Gate-Drain (“Miller”) Change		Q_{gd}	-	1.25	-		
Turn-on Delay Time[2]		$T_{d(on)}$	-	2	-	ns	V_{DD}= -50V I_D= -0.5A V_{GS}= -10V R_G=3.3Ω R_L=30Ω
Rise Time		T_r	-	18.4	-		
Turn-off Delay Time		$T_{d(off)}$	-	19.6	-		
Fall Time		T_f	-	19.6	-		
Input Capacitance		C_{iss}	-	513	-	pF	V_{GS}=0V V_{DS}= -15V f=1.0MHz
Output Capacitance		C_{oss}	-	29	-		
Reverse Transfer Capacitance		C_{rss}	-	17	-		
Source-Drain Diode							
Forward On Voltage[2]		V_{SD}	-	-	-1.2	V	I_S= -1A, V_{GS}=0V, Tj=25℃
Continuous Source Current[1,4]		I_S	-	-	-1.5	A	V_D= V_G=0V, Force Current
Pulsed Source Current[2,4]		I_{SM}	-	-	-5	V	
Reverse Recovery Time		T_{rr}	-	27	-	nS	I_F= -1A, Tj=25℃ dI/dt=100A/μs
Reverse Recovery Charge		Q_{rr}	-	36	-	nC	

Notes:

1. The data tested by surface mounted on a inch^2 FR-4 board with 2OZ copper.
2. The data tested by pulse width≦300us, duty cycle≦2%.
3. The power dissipation is limited by 150℃ jun ction temperature.
4. The data is theoretically the same as ID and IDM, In real applications, should by limited by total power dissipation.

CHARACTERISTICS CURVE

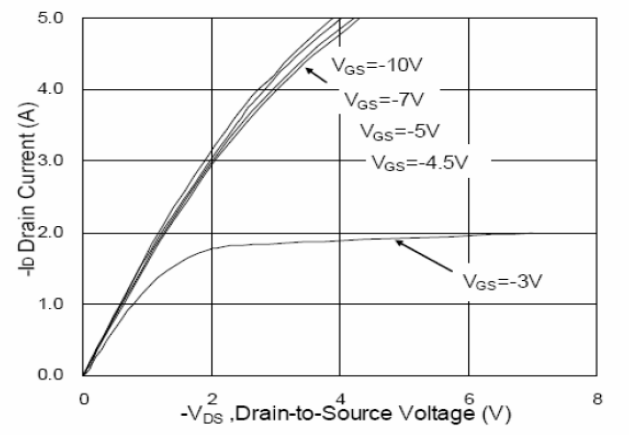

Fig.1 Typical Output Characteristics

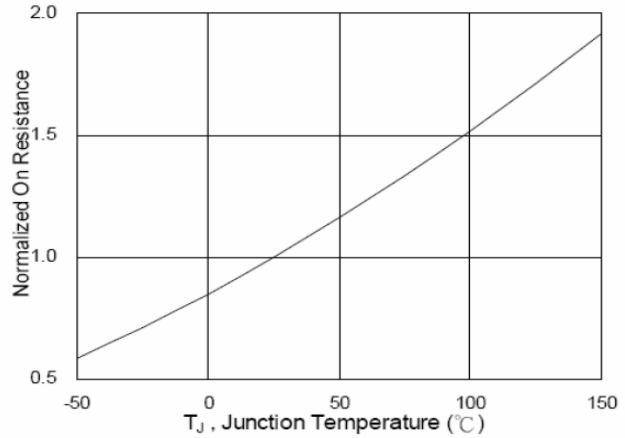

Fig.2 Normalized R_{DSON} vs. T_J

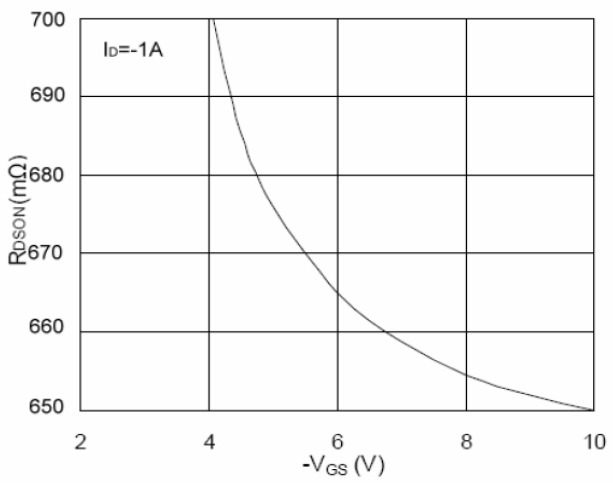

Fig.3 On-Resistance vs. G-S Voltage

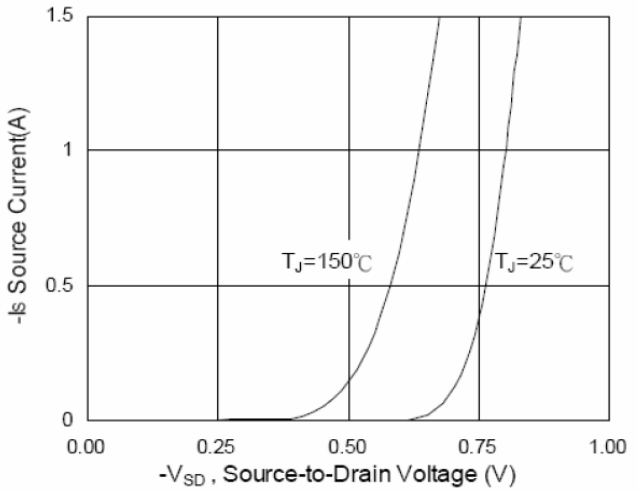

Fig.4 Forward Characteristics of Reverse

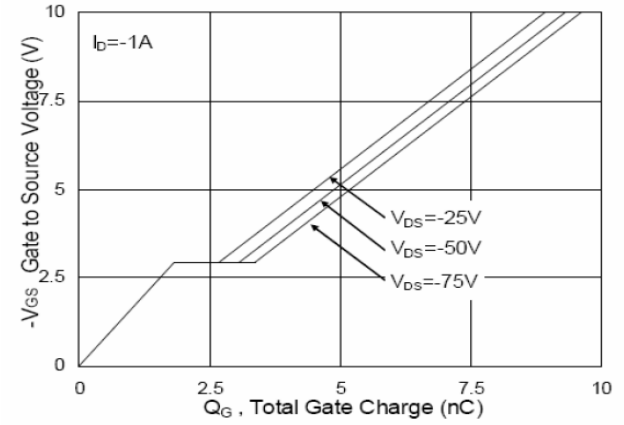

Fig.5 Gate-Charge Characteristics

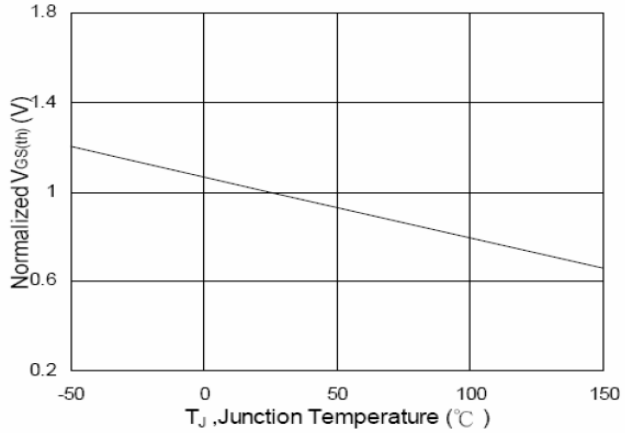

Fig.6 Normalized $V_{GS(th)}$ vs. T_J

CHARACTERISTIC CURVE

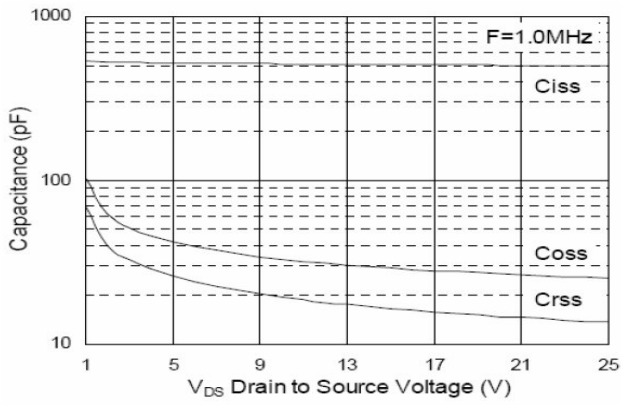

Fig.7 Capacitance

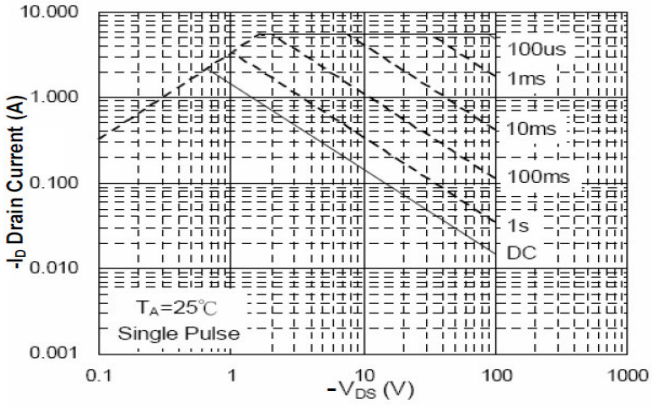

Fig.8 Safe Operating Area

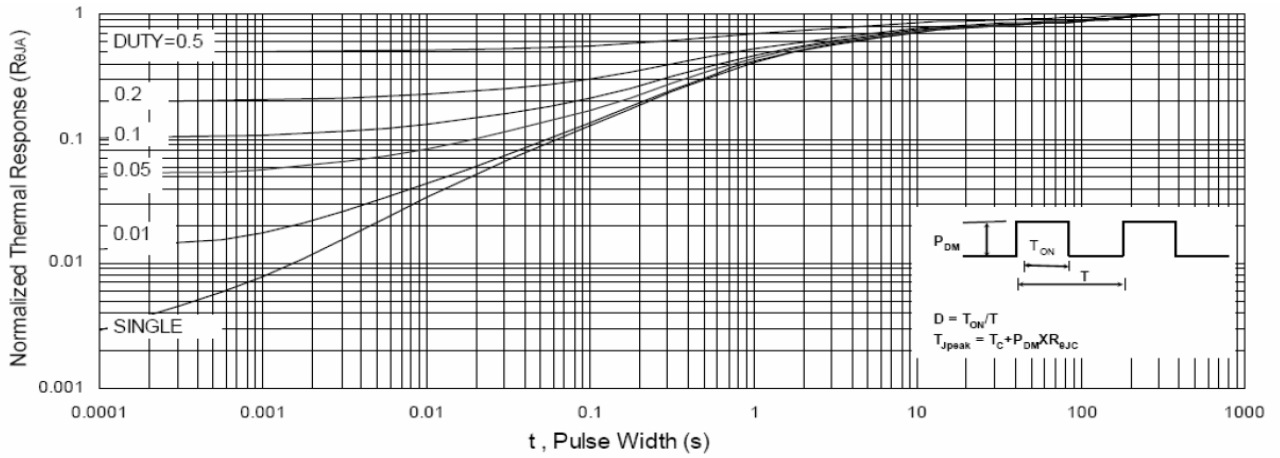

Fig.9 Normalized Maximum Transient Thermal Impedance

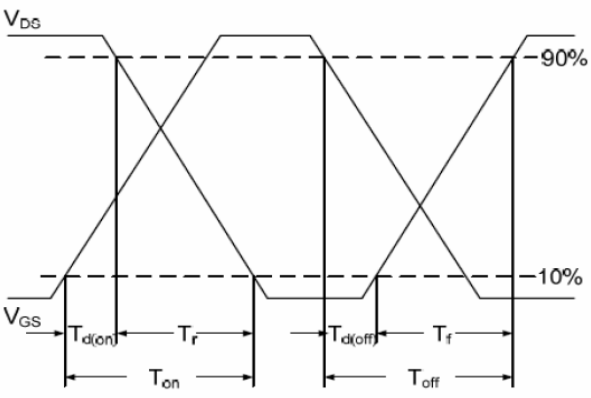

Fig.10 Switching Time Waveform

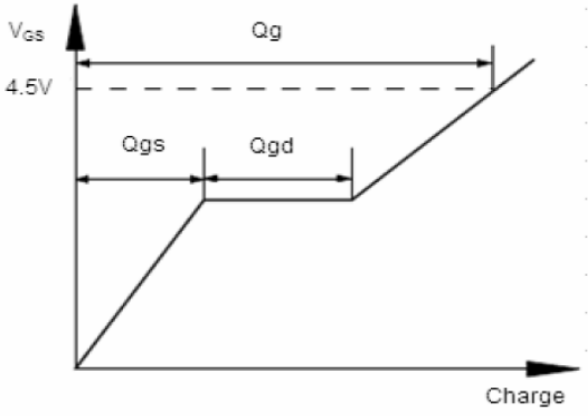

Fig.11 Gate Charge Waveform