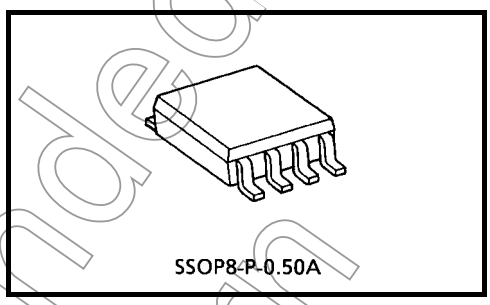
TOSHIBA CMOS Digital Integrated Circuits Silicon Monolithic

TC9WMA2FK

2,048-Bit (256 × 8 Bit) Serial E^2PROM

The TC9WMA2FK is electrically erasable/programmable nonvolatile memory (E^2PROM).

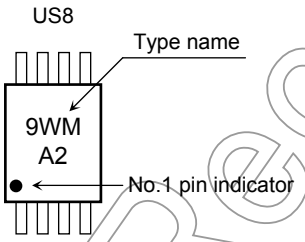


Weight: 0.01 g (typ.)

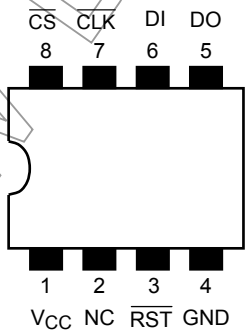
Features

- Serial data input/output
- Programmable in units of one word and collectively erasable in one operation
- Automatically set programming time (built-in timer)
- Programming time: 10 ms (max) (V_{CC} = 3.0 to 5.5 V)
  12 ms (max) (V_{CC} = 2.3 to 2.7 V)
- Overwrite enabled or disabled by software
- Single power supply and low power consumption
- Operating voltage range for reading: V_{CC} = 1.8 to 5.5 V
- Operating voltage range for writing: V_{CC} = 2.3 to 5.5 V
- Wide operating temperature range (−40 to 85°C)

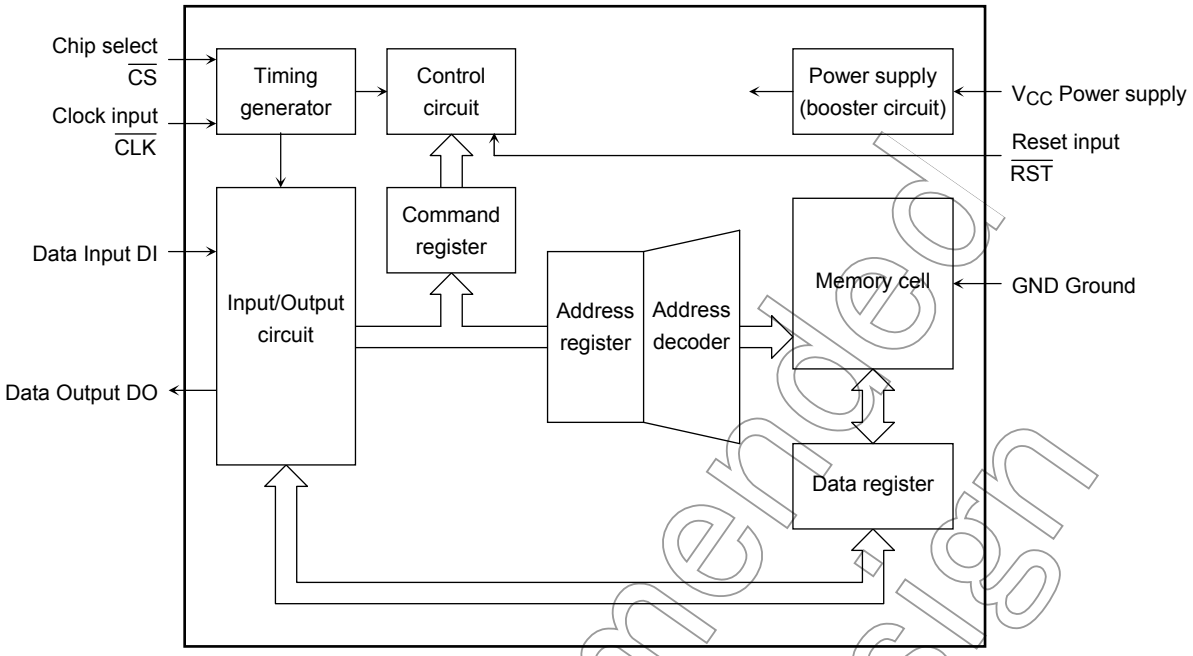
Product Marking



Pin Assignment (top view)



Block Diagram



Pin Function

Pin Name	Input/Output	Function
$\overline{CS}$	Input	Chip select A low on $\overline{CS}$ selects the chip. Always return $\overline{CS}$ high temporarily before executing instructions.
$\overline{CLK}$	Input	Clock input The data on DI is latched by a rising edge of $\overline{CLK}$. Data is output to DO by a falling edge of $\overline{CLK}$. $\overline{CLK}$ is effective when $\overline{CS}$ is low.
DI	Input	Serial data input This pin is used to enter addresses, commands, and data into the chip.
DO	Output	Serial data output This pin outputs data from the chip.
$\overline{RST}$	Input	Reset input A low on this input resets the chip.
NC	—	No connection (not connected internally)
V_{CC}	Power supply	1.8 V~5.5 V (for reading) 2.3~5.5 V (for writing)
GND		0 V (GND)

Functional Description

1. Types of Instructions

Operation	Address	Command								Data
		C0	C1	C2	C3					
Read	A0~A7	1	0	0	0	0	0	0	0	
Program	A0~A7	0	1	1	0	0	0	0	0	D0~D7
All erase	********	0	0	1	1	0	0	0	0	
Busy monitor	********	1	0	1	1	0	0	0	0	
Overwrite enable	********	1	0	0	1	0	0	0	0	
Overwrite disable	********	1	1	0	1	0	0	0	0	
Read Auto-incremented	A0~A7	1	0	0	0	1	0	0	0	

*: Don't care

2. Operation Method

Be sure to drive $\overline{CS}$ and $\overline{CLK}$ high temporarily before entering an instruction. After $\overline{CS}$ is asserted low, $\overline{CLK}$ becomes effective, acting as a serial transfer synchronizing signal. The data on DI is latched on a rising edge of $\overline{CLK}$, while data is output to DO on a falling edge of $\overline{CLK}$.

Instructions can only be executed when the chip is not being programmed or collectively erased (i.e., when the ready/busy status signal is high). However, the Monitor Busy instruction can be entered at any time.

Only the commands listed in the above table can be used. Do not use any other command.

- Read

  Entering the Read instruction causes memory data at the specified address to be read out and serially output from the DO pin.

- Program

  Entering the Program instruction causes overwrite operation to automatically start within the chip, overwriting memory data at the specified address with the input data.

  After the instruction is entered, $\overline{CS}$ can be driven high even while overwrite operation is still in progress internally.

- All Erase

  Entering the Erase All instruction causes erase operation to automatically start within the chip, erasing memory data at all addresses.

  After the instruction is entered, $\overline{CS}$ can be driven high even while erase operation is still in progress internally.

  This command clears the memory data to 0.

- Busy Monitor

  Entering the Monitor Busy instruction causes a ready/busy status signal to be output from the DO pin.

  This output signal is low while the chip is being programmed or collectively erased, and is high after programming or collective erase operation is completed.

  The ready/busy status signal is output continuously until $\overline{CS}$ is driven high.

- Overwrite Enable/Disable

  Entering the Enable Overwrite instruction places the chip in overwrite enabled mode, where the Program and Erase All instructions can be entered.

  Entering the Disable Overwrite instruction places the chip in overwrite disabled mode, where the Program and Erase All instructions cannot be entered.

  Once the chip is placed in overwrite disabled mode, it remains disabled against overwriting until the Enable Overwrite instruction is entered.

- Read Auto-incremented

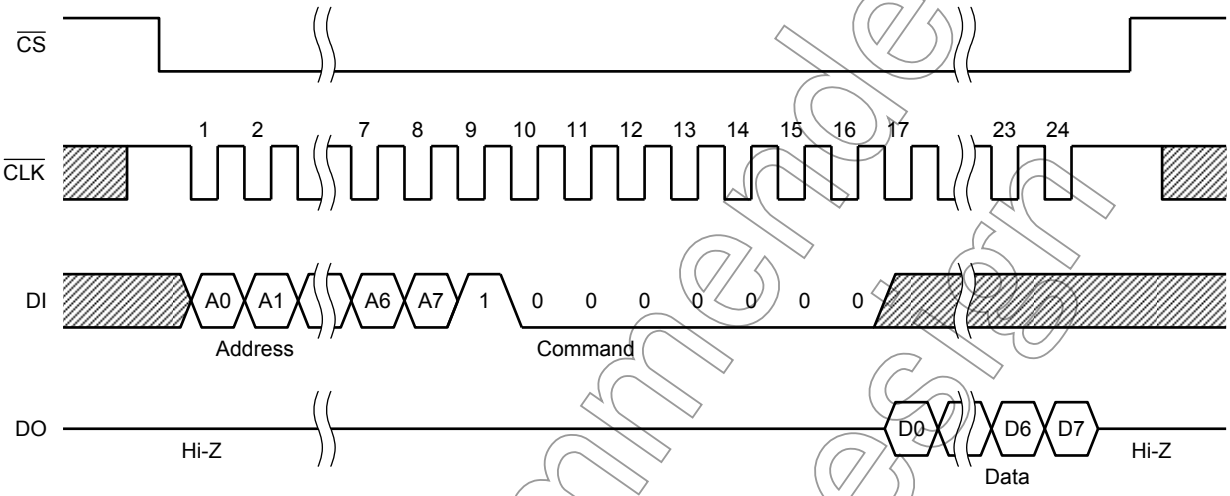
  After the data at the specified address is output, the subsequent $\overline{CLK}$ pulse causes the address to be incremented so that the data at the next address is output automatically. After the data at the last address is output, that at the first address will be read and output.

3. Precautions on Powering Up or Down the Chip

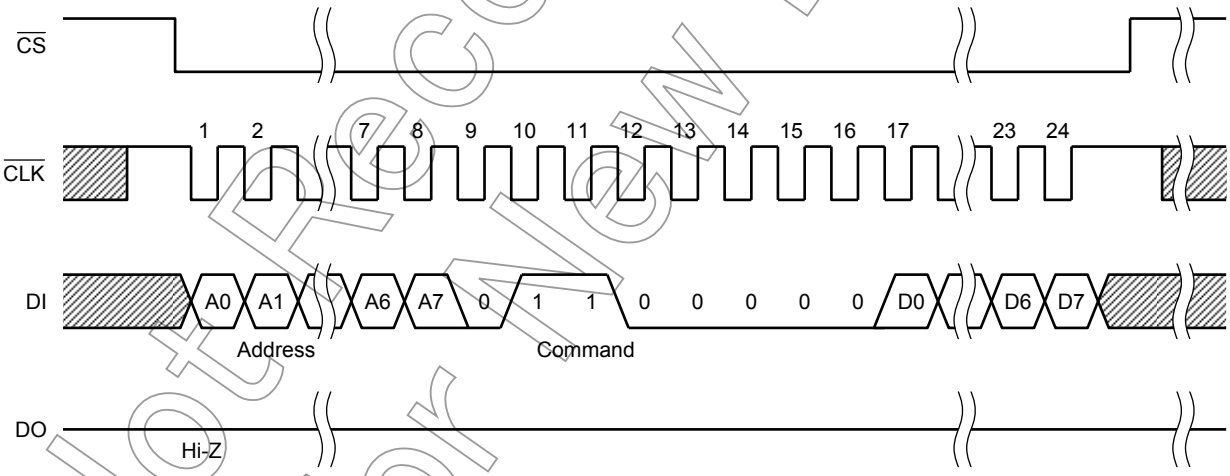
(1) A wait time of 1 ms is required before the chip can start operation after it is powered up.
(2) Ensure that $\overline{RST}$ is low when powering up or down the chip.
(3) Resetting the chip places it in overwrite disabled mode.

4. Timing Chart

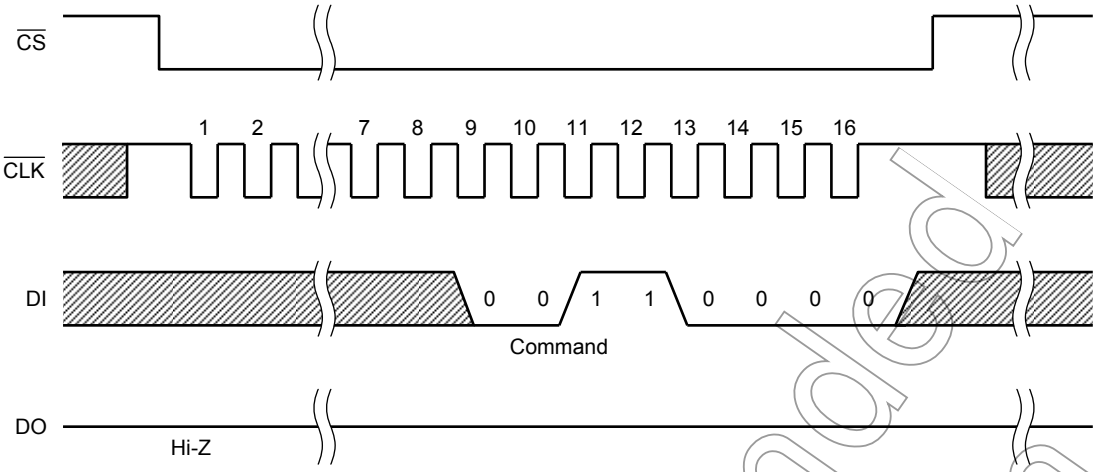
(1) Read



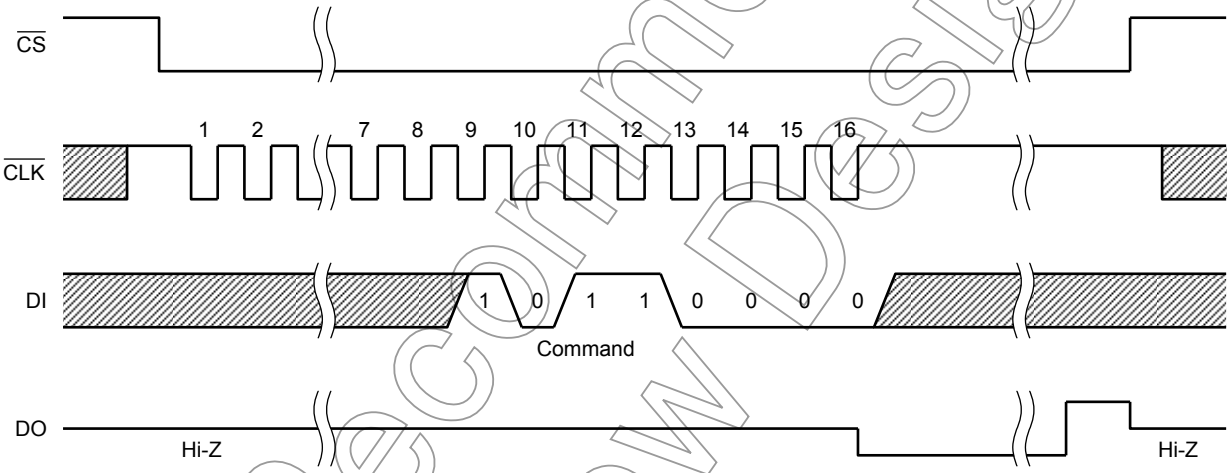
(2) Program



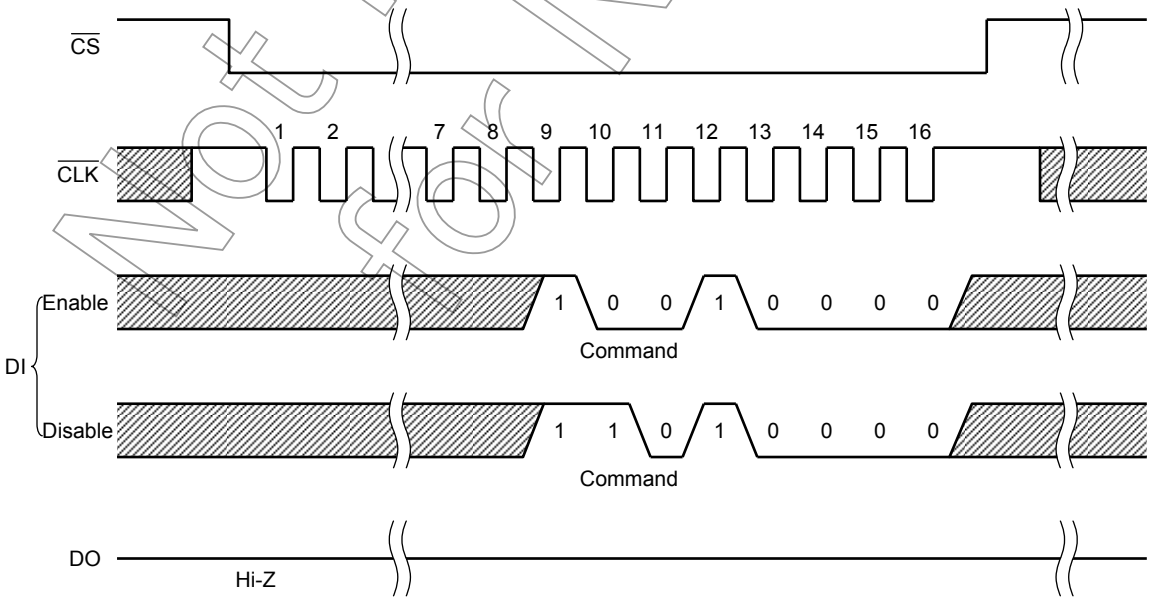
(3) All Erase



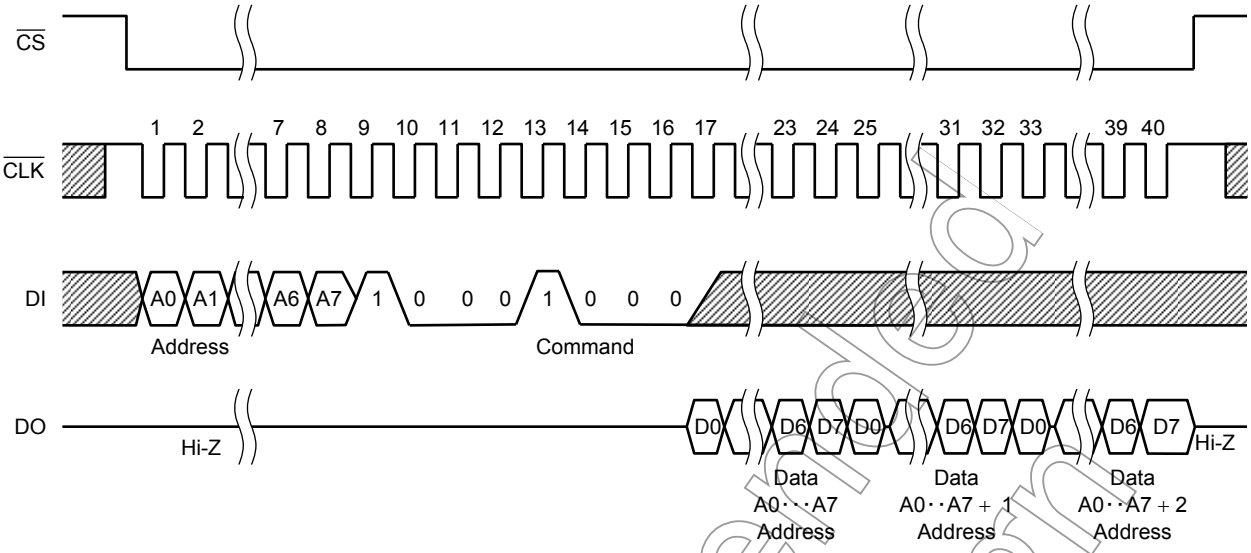
(4) Busy Monitor



(5) Overwrite Enable/Disable



(6) Read Auto-incremented



Absolute Maximum Ratings (Note) (GND = 0 V)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{CC}	−0.3~7.0	V
Input voltage	V_{IN}	−0.3~V_{CC} + 0.3	V
Output voltage	V_{OUT}	−0.3~V_{CC} + 0.3	V
Power dissipation	P_D	200 (25°C)	mW
Soldering temperature (in time)	T_{sld}	260 (10 s)	°C
Storage temperature	T_{stg}	−55~125	°C
Operating temperature	T_{opr}	−40~85	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ranges (Note 1) (GND = 0 V, T_{opr} = −40 to 85°C)

Characteristics	Symbol	Test Condition	Min	Max	Unit
Supply voltage (for reading)	V_{CC}		1.8	5.5	V
Supply voltage (for writing)	V_{CC}		2.3	5.5	V

Operating Ranges (Note 1) (V_{CC} = 1.8 to 2.7 V, GND = 0 V, T_{opr} = −40 to 85°C)

Characteristics	Symbol	1.8 V ≦ V_{CC} < 2.3 V		2.3 V ≦ V_{CC} < 2.7 V		Unit
		Min	Max	Min	Max	
Low level input voltage	V_{IL}	0	0.15 × V_{CC}	0	0.35	V
High level input voltage	V_{IH1} (Note 1)	0.7 × V_{CC}	V_{CC}	1.6	V_{CC}	V
	V_{IH2} (Note 2)	0.8 × V_{CC}	V_{CC}	1.8	V_{CC}	
Operating frequency	f_{CLK}	0	0.25	0	0.5	MHz

Operating Ranges (Note 1) (V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_{opr} = −40 to 85°C)

Characteristics	Symbol	2.7 V ≦ V_{CC} ≦ 3.6 V		4.5 V ≦ V_{CC} ≦ 5.5 V		Unit
		Min	Max	Min	Max	
Low level input voltage	V_{IL}	0	0.45	0	0.7	V
High level input voltage	V_{IH1} (Note 2)	1.6	V_{CC}	2.0	V_{CC}	V
	V_{IH2} (Note 3)	2.2	V_{CC}	3.0	V_{CC}	
Operating frequency	f_{CLK}	0	1	0	1	MHz

Note 1: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either VCC or GND.

Note 2: $\overline{CS}$, DI, $\overline{RST}$

Note 3: $\overline{CLK}$

Electrical Characteristics

D.C. Characteristics (V_{CC} = 1.8 to 2.7 V, GND = 0 V, T_{opr} = −40 to 85°C)

Characteristics	Symbol	Test Condition	1.8 V ≦ V_{CC} < 2.3 V		2.3 V ≦ V_{CC} < 2.7 V		Unit
			Min	Max	Min	Max	
Input current	I_{LI}		—	±1	—	±1	μA
Output leakage current	I_{LO}		—	±1	—	±1	μA
High level output voltage	V_{OH}	I_{OH} = −1 mA	—	—	—	—	V
		I_{OH} = −500 μA	—	—	V_{CC} − 0.4	—	
		I_{OH} = −100 μA	V_{CC} − 0.2	—	—	—	
Low level output voltage	V_{OL}	I_{OL} = 2 mA	—	—	—	—	V
		I_{OL} = 500 μA	—	—	0.4	—	
		I_{OL} = 100 μA	0.2	—	—	—	
Quiescent supply current	I_{CC1} (Note 1)		—	5	—	5	μA
Supply current during read	I_{CC2} (Note 2)		—	0.5	—	1.0	mA
Supply current during all erase/program	I_{CC3} (Note 3)		—	—	—	1.0	mA

D.C. Characteristics (V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_{opr} = −40 to 85°C)

Characteristics	Symbol	Test Condition	2.7 V ≦ V_{CC} < 3.6 V		4.5 V ≦ V_{CC} ≦ 5.5 V		Unit
			Min	Max	Min	Max	
Input current	I_{LI}		—	±1	—	±1	μA
Output leakage current	I_{LO}		—	±1	—	±1	μA
High level output voltage	V_{OH}	I_{OH} = −1 mA	V_{CC} − 0.4	—	V_{CC} − 0.4	—	V
		I_{OH} = −500 μA	—	—	—	—	
		I_{OH} = −100 μA	—	—	—	—	
Low level output voltage	V_{OL}	I_{OL} = 2 mA	0.4	—	0.4	—	V
		I_{OL} = 500 μA	—	—	—	—	
		I_{OL} = 100 μA	—	—	—	—	
Quiescent supply current	I_{CC1} (Note 1)		—	5	—	5	μA
Supply current during read	I_{CC2} (Note 2)		—	1.5	—	2.5	mA
Supply current during all erase/program	I_{CC3} (Note 3)		—	1.0	—	2.0	mA

Note 1: $\overline{CS}$ = 1 (except when busy, however)

Note 2: Current that flows for a period between a fall of the 14th $\overline{CLK}$ pulse and a rise of the 16th $\overline{CLK}$ pulse when executing the Read instruction.

Note 3: Current that flows while executing the Erase All or Program instruction.

A.C. Characteristics (V_{CC} = 1.8 to 2.7 V, GND = 0 V, T_{opr} = −40 to 85°C)

Characteristics	Symbol	Test Condition	1.8 V ≦ V_{CC} < 2.3 V		2.3 V ≦ V_{CC} < 2.7 V		Unit
			Min	Max	Min	Max	
Maximum clock frequency	f_{MAX}		0	0.25	0	0.5	MHz
Minimum clock pulse width	twCLK (L)		1.0	—	1.0	—	μs
	twCLK (H)						
Minimum reset pulse width	t_{WRST}		1	—	1	—	μs
Minimum chip select pulse width	t_{WCS}		1	—	1	—	μs
Reset setup time	t_{RSS}	$\overline{RST}$ setup time when $\overline{CS}$ is switched over	1	—	1	—	μs
Clock setup time	t_{CKS}	$\overline{CLK}$ setup time when $\overline{CS}$ is switched over	500	—	500	—	ns
$\overline{CS}$ setup time	t_{CSS}	$\overline{CS}$ setup time when $\overline{CLK}$ is switched over	500	—	500	—	ns
Propagation delay time (Note)	t_{pLH} t_{pHL} t_{pZH} t_{pZL}	Time from $\overline{CLK}$ switchover until valid data is output	—	2.0	—	1.0	μs
	t_{pLZ} t_{pHZ}	Time from $\overline{CS}$ switchover until output data goes Hi-Z	—	2.0	—	1.0	
Input data setup time	t_s	Input data setup time when $\overline{CLK}$ is switched over	500	—	500	—	ns
Input data hold time	t_h	Input data hold time when $\overline{CLK}$ is switched over	500	—	500	—	ns

Note: C_L = 100 pF, R_L = 1 kΩ

A.C. Characteristics (V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_{opr} = −40 to 85°C)

Characteristics	Symbol	Test Condition	2.7 V ≦ V_{CC} ≦ 3.6 V		4.5 V ≦ V_{CC} ≦ 5.5 V		Unit
			Min	Max	Min	Max	
Maximum clock frequency	f_{MAX}		0	1	0	1	MHz
Minimum clock pulse width	twCLK (L)		0.4	—	0.4	—	μs
	twCLK (H)						
Minimum reset pulse width	t_{WRST}		1	—	1	—	μs
Minimum chip select pulse width	t_{WCS}		1	—	1	—	μs
Reset setup time	t_{RSS}	$\overline{RST}$ setup time when $\overline{CS}$ is switched over	1	—	1	—	μs
Clock setup time	t_{CKS}	$\overline{CLK}$ setup time when $\overline{CS}$ is switched over	250	—	250	—	ns
$\overline{CS}$ setup time	t_{CSS}	$\overline{CS}$ setup time when $\overline{CLK}$ is switched over	250	—	250	—	ns
Propagation delay time (Note)	t_{pLH} t_{pHL} t_{pZH} t_{pZL}	Time from $\overline{CLK}$ switchover until valid data is output	—	0.25	—	0.25	μs
	t_{pLZ} t_{pHZ}	Time from $\overline{CS}$ switchover until output data goes Hi-Z	—	0.5	—	0.5	
Input data setup time	t_s	Input data setup time when $\overline{CLK}$ is switched over	250	—	250	—	ns
Input data hold time	t_h	Input data hold time when $\overline{CLK}$ is switched over	250	—	250	—	ns

Note: C_L = 100 pF, R_L = 1 kΩ

E^2PROM Characteristics (GND = 0 V, 2.3 V ≦ V_{CC} ≦ 2.7 V, T_{opr} = −40 to 85°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
All erase time	t_E		—		12	ms
Program time	t_P		—		12	ms
Endurance	N_{EW}		1×10^5	—	—	Times
Data retention time	t_{RET}		10	—	—	Year

E^2PROM Characteristics (GND = 0 V, 3.0 V ≦ V_{CC} ≦ 5.5 V, T_{opr} = −40 to 85°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
All erase time	t_E		—		10	ms
Program time	t_P		—		10	ms
Endurance	N_{EW}		1×10^5	—	—	Times
Data retention time	t_{RET}		10	—	—	Year

Capacitance Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Typ.	Unit
Input capacitance	C_{IN}		3.3	4	pF
Output capacitance	C_O		3.3	3	pF
Equivalent Internal capacitance	C_{PD}	f_{IN} = 1 MHz (Note)	3.3	8.5	pF

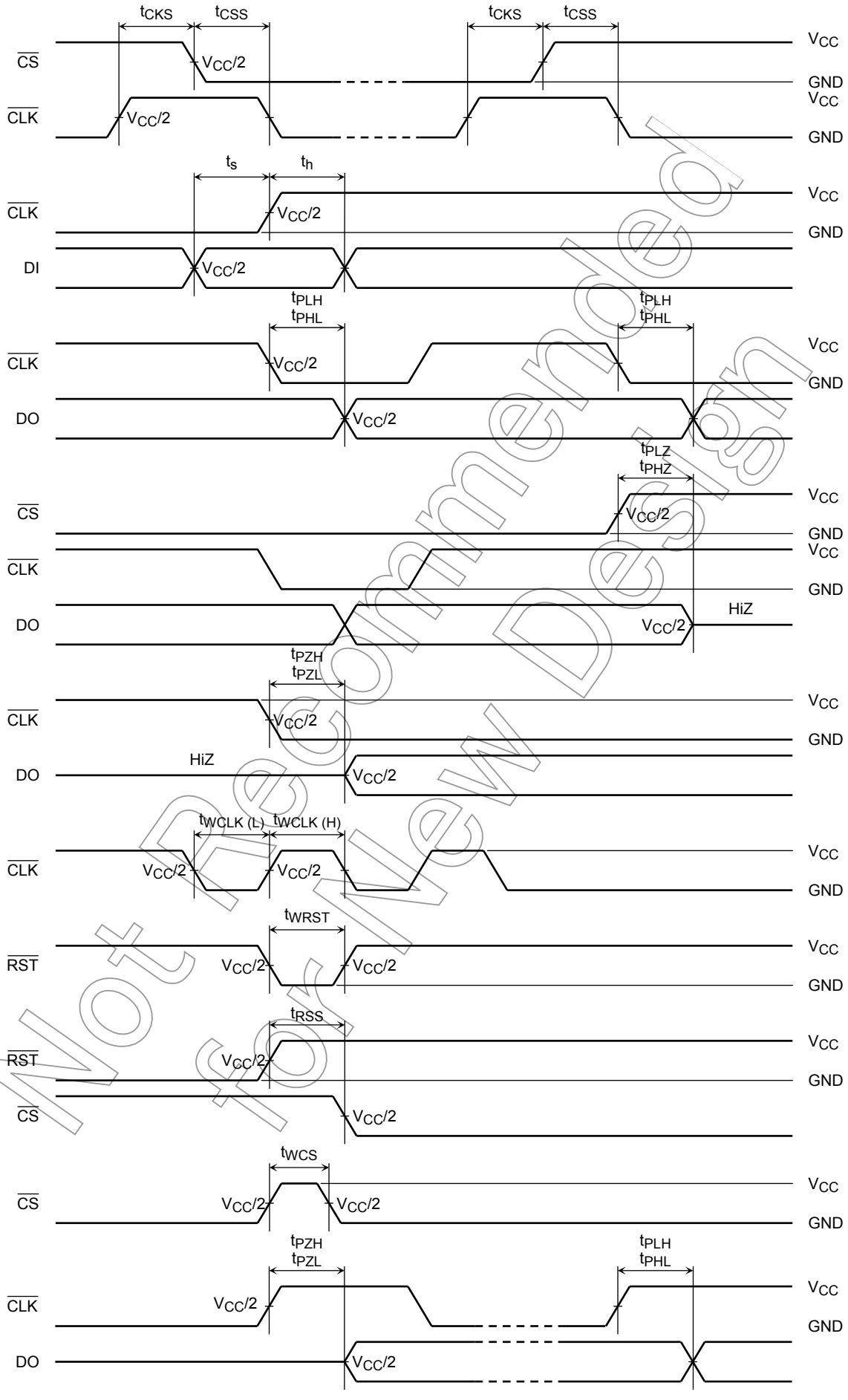
Note: C_{PD} denotes the IC's internal equivalent capacitance calculated from the amount of current it consumes while operating.

The average current consumption during non-loaded operation is obtained from the equations below.

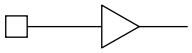
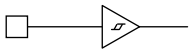
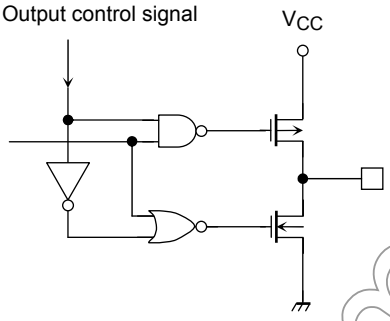
$I_{CC\ (Read)} = f_{CLK} \cdot C_{PD} \cdot V_{CC} + I_{CC1} + I_{CC2} \cdot 3/24$

$I_{CC\ (Prog)} = f_{CLK} \cdot C_{PD} \cdot V_{CC} + I_{CC1} + I_{CC3}$

A.C. Characteristics Timing Chart

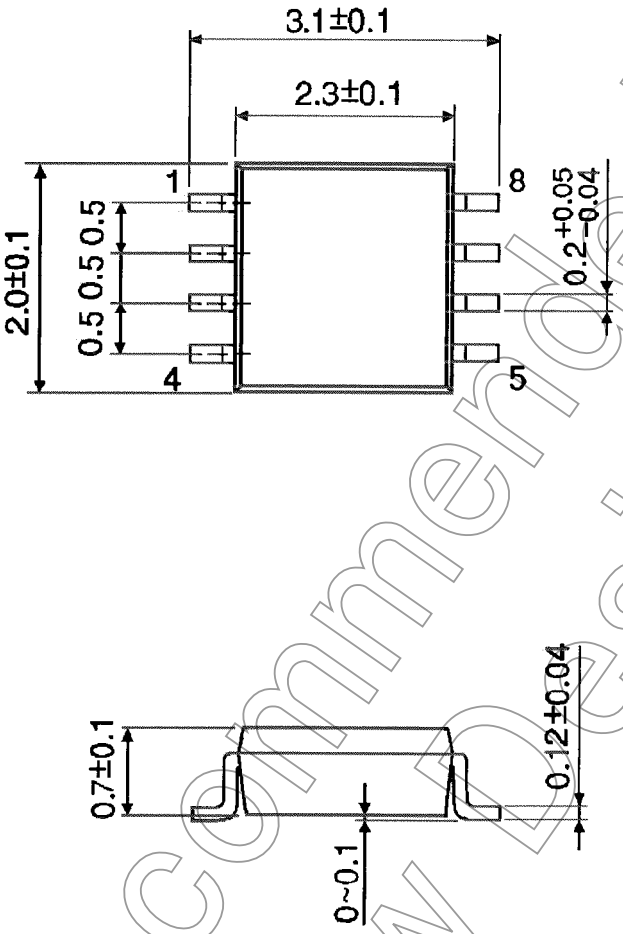


Input/Output Circuits of Pins

Pin Name	Type	Input/Output Circuit	Remarks
$\overline{CS}$ DI $\overline{RST}$	Input		
$\overline{CLK}$	Input		Hysteresis input
DO	Output		Initial “HiZ”

Package Dimensions

SSOP8-P-0.50A Unit : mm



Weight: 0.01 g (typ.)

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