# **AN6367NK, AN6367NS**

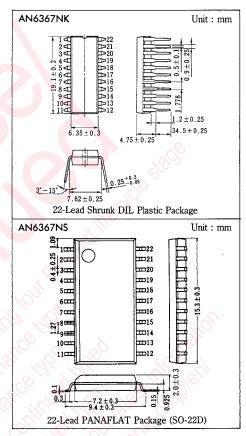
# VTR Color Signal Processing Circuits for 3 Systems

### Outline

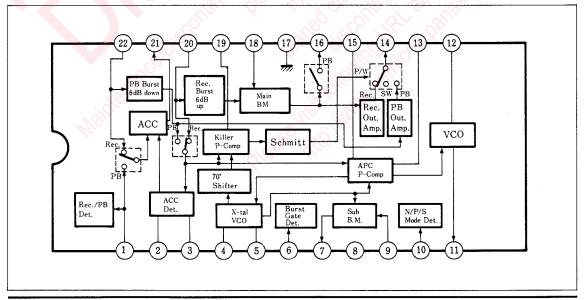
The AN6367NK and The AN6367NS are integrated circuits provided with color signal processing function which can cope with 3 VTR systems, such as PAL, pseudo NTSC and pseudo SECAM, by combining with the AN6163A.

#### Features

- Operated by low supply voltage: Vcc = 5 V
- Low power consumption (110mV)
- AFC+APC system during recording mode
   Only APC system during playback mode
- Requires only one crystal for PAL system



## Block Diagram



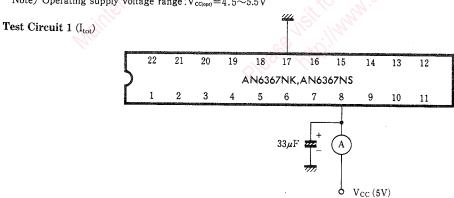
## ■ Absolute Maximum Ratings (T<sub>a</sub>=25°C)

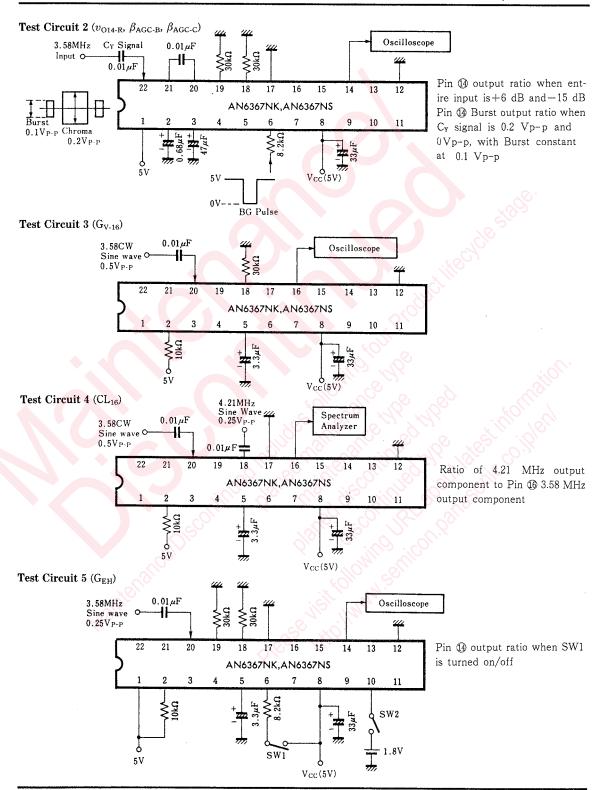
Item	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	6	V
Power dissipation (Ta=70℃)	$P_{\mathrm{D}}$	250	mW
Operating ambient temperature	$T_{opr}$	<del>-20~+70</del>	°C
Storage temperature	$T_{\rm stg}$	<del>-55~+150</del>	°C

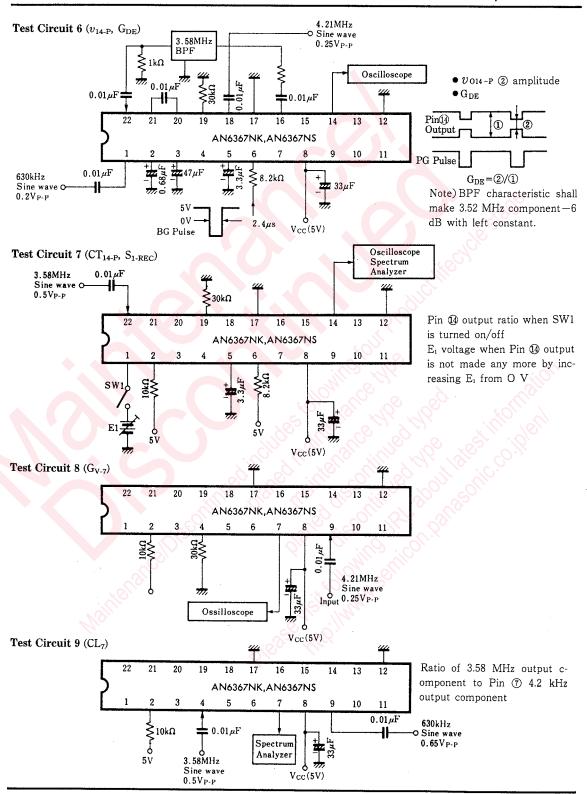
## ■ Electrical Characteristics (T<sub>a</sub>=25°C)

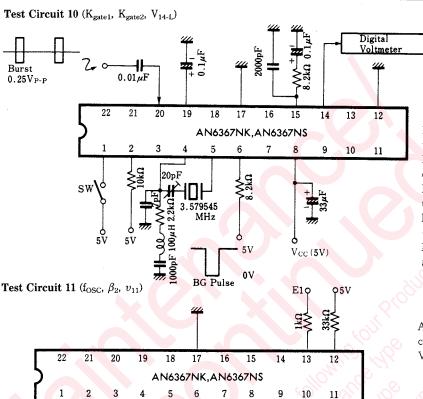
Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
$I_{tot}$	1	V <sub>CC</sub> =5V	15		32	mA
$v_{ m O14-R}$	2	V <sub>CC</sub> =5V, Pin ② Input, Burst 0.1V <sub>P-P</sub>	0.5		0,	V <sub>P-P</sub>
$\beta_{\text{AGC-B}}$	2	V <sub>CC</sub> =5V, +6dB~-15dB		76	3	dB
$\beta_{\text{AGC-C}}$	2	V <sub>CC</sub> =5V	0.5	(C)	4.5	dB
G <sub>V-16</sub>	3	V <sub>CC</sub> =5V, Pin 20 Input 0.5V <sub>P-P</sub>	4	<u>~ </u>		dB
CL <sub>16</sub>	4	V <sub>CC</sub> =5V	10			dB
G <sub>(EH)</sub>	5	V <sub>CC</sub> =5V, Pin @Input 0.25V <sub>P-P</sub>	5		7	dB
$v_{ m O14-P}$	6	$V_{CC}=5V$	0.2		0.55	V <sub>P-P</sub>
G <sub>(DE)</sub>	6	V <sub>CC</sub> =5V	-6.5			dB
CT <sub>14-P</sub>	.7	V <sub>CC</sub> =5V			<u> </u>	dB
S <sub>1-REC</sub>	7	$V_{CC}=5V$	4.6			V
G <sub>V-7</sub>	8	V <sub>CC</sub> =5V, Pin (9) Input 0.65V <sub>P-P</sub>	1		5	dB
CL <sub>7</sub>	9	V <sub>CC</sub> =5V				dB
$K_{gate1}$	10	V <sub>CC</sub> =5V, Pin @ Input 0dB=0.25V <sub>P-P</sub>	-22		all a	dB
K <sub>gate2</sub>	10	V <sub>CC</sub> =5V, Pin (9) Input 0dB=0.25V <sub>P-P</sub>	-		-10	dB
V <sub>14-L</sub>	10	V <sub>CC</sub> =5V	<b>7</b> .		<u> </u>	v
f <sub>OSC</sub>	11	V <sub>CC</sub> =5V	3			MHz
$eta_2$	11	V <sub>CC</sub> =5V	1.5	·0.1		kHz/mV
$v_{ m O11}$	11	V <sub>CC</sub> =5V	1	U.		V <sub>P-P</sub>
f <sub>APC-H</sub>	12	V <sub>CC</sub> =5V				Hz
	12	V <sub>cc</sub> =5V	10/2		- 500	Hz
S <sub>10-1</sub>	13	V <sub>CC</sub> =5V	7			
S <sub>10-2</sub>	13	V <sub>CC</sub> =5V	1.6			$\frac{}{v}$
	13	V <sub>CC</sub> =5V				$\frac{}{v}$
	Itot  VO14-R  βAGC-B  βAGC-C  GV-16  CL16  G(EH)  VO14-P  G(DE)  CT14-P  S1-REC  GV-7  CL7  Kgate1  Kgate2  V14-L  fOSC  β2  V011  fAPC-H  fAPC-L	Symbol         Circuit           I <sub>tot</sub> 1           ν <sub>014-R</sub> 2           β <sub>AGC-B</sub> 2           β <sub>AGC-C</sub> 2           G <sub>V-16</sub> 3           CL <sub>16</sub> 4           G <sub>(EH)</sub> 5           ν <sub>014-P</sub> 6           G <sub>(DE)</sub> 6           CT <sub>14-P</sub> .7           S <sub>1-REC</sub> .7           G <sub>V-7</sub> .8           CL <sub>7</sub> 9           K <sub>gate1</sub> 10           K <sub>gate2</sub> 10           V <sub>14-L</sub> 10           f <sub>0SC</sub> 11           β <sub>2</sub> 11           ν <sub>011</sub> 11           f <sub>APC-H</sub> 12           f <sub>APC-L</sub> 12           S <sub>10-1</sub> 13           S <sub>10-2</sub> 13	Symbol         Circuit         Condition           I <sub>tot</sub> 1         V <sub>CC</sub> =5V           ν <sub>O14-R</sub> 2         V <sub>CC</sub> =5V, Pin @ Input, Burst 0.1V <sub>P-P</sub> β <sub>AGC-B</sub> 2         V <sub>CC</sub> =5V, +6dB~-15dB           β <sub>AGC-C</sub> 2         V <sub>CC</sub> =5V           G <sub>V-16</sub> 3         V <sub>CC</sub> =5V, Pin @ Input 0.5V <sub>P-P</sub> CL <sub>16</sub> 4         V <sub>CC</sub> =5V           G <sub>(EH)</sub> 5         V <sub>CC</sub> =5V, Pin @ Input 0.25V <sub>P-P</sub> ν <sub>O14-P</sub> 6         V <sub>CC</sub> =5V           G <sub>(DE)</sub> 6         V <sub>CC</sub> =5V           CT <sub>14-P</sub> 7         V <sub>CC</sub> =5V           G <sub>V-7</sub> 8         V <sub>CC</sub> =5V           G <sub>V-7</sub> 8         V <sub>CC</sub> =5V, Pin @ Input 0.65V <sub>P-P</sub> CL <sub>7</sub> 9         V <sub>CC</sub> =5V           K <sub>gate1</sub> 10         V <sub>CC</sub> =5V, Pin @ Input 0dB=0.25V <sub>P-P</sub> V <sub>14-L</sub> 10         V <sub>CC</sub> =5V           f <sub>OSC</sub> 11         V <sub>CC</sub> =5V           β <sub>2</sub> 11         V <sub>CC</sub> =5V           ν <sub>011</sub> 11         V <sub>CC</sub> =5V           f <sub>APC-H</sub> 12         V <sub>CC</sub> =5V           f <sub>APC-L</sub> 12         V <sub>CC</sub> =5V           S	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Symbol         Circuit         Condition         min.         typ.           I tot         1         V <sub>CC</sub> =5V         15           ν <sub>O14-R</sub> 2         V <sub>CC</sub> =5V, Pin @ Input, Burst 0.1V <sub>P-P</sub> 0.5           β <sub>AGC-B</sub> 2         V <sub>CC</sub> =5V, +6dB~-15dB         0.5           β <sub>AGC-C</sub> 2         V <sub>CC</sub> =5V         0.5           G <sub>V-16</sub> 3         V <sub>CC</sub> =5V         0.5           G <sub>CH</sub> 5         V <sub>CC</sub> =5V         0.2           G <sub>CH</sub> 5         V <sub>CC</sub> =5V         0.2           G <sub>OB</sub> 6         V <sub>CC</sub> =5V         0.2           G <sub>OB</sub> 6         V <sub>CC</sub> =5V         0.2           G <sub>V-7</sub> 8         V <sub>CC</sub> =5V         4.6           G <sub>V-7</sub> 8         V <sub>CC</sub> =5V, Pin @ Input 0.65V <sub>P-P</sub> 1           CL <sub>7</sub> 9         V <sub>CC</sub> =5V, Pin @ Input 0dB=0.25V <sub>P-P</sub> -22           K <sub>gate1</sub> 10         V <sub>CC</sub> =5V, Pin @ Input 0dB=0.25V <sub>P-P</sub> -22           K <sub>gate2</sub> 10         V <sub>CC</sub> =5V         3           β <sub>2</sub> 11         V <sub>CC</sub> =5V         3           β <sub>2</sub> 11         V <sub>CC</sub> =5V         500           f <sub>APC-H</sub>	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$

Note) Operating supply voltage range:  $V_{\text{CC(opt)}} = 4.5 \sim 5.5 \text{V}$ 









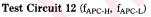
Pin @ Burst input level when the Pin @ is turned from H to L by lowering the Pin @ level(0.25 Vp-p=O dB)

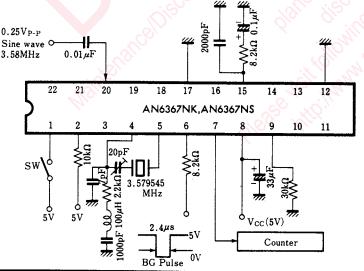
Pin @ Burst input level when the Pin @ is turned from L to H by raising the Pin @ level (0.25 Vp-p=O dB)

Pin 4 voltage in case of K gate2

Assuming that output frequencies are  $f_1$  and  $f_2$  when  $E_1$  is 2.4 V, respectively;

Counter Oscilloscope





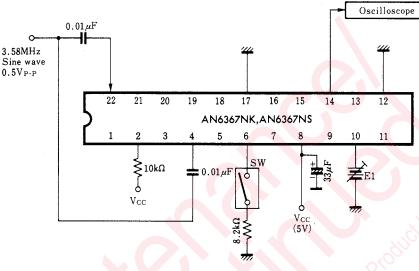
 $V_{CC}(5V)$ 

Frequency difference between a Pin @ input frequency and 3.57945 MHz when the former is lowered from 3.581 MHz and a Pin @ output frequency coincides with the former. fapc-H= Pin @ frequency-

 $f_{\text{APC-H}} = \text{Pin}$  @ frequency-3.579545 MHz

Frequency difference between the Pin @ input frequency and 3.579545 MHz when the former is increased from 3.578 MHz 3.578 MHz and the Pin @ output frequency coincides with the former.fapc\_l=Pin @ frequency-3.579545 MHz

**Test Circuit 13** (S<sub>10-1</sub>, S<sub>10-2</sub>, S<sub>10-3</sub>)

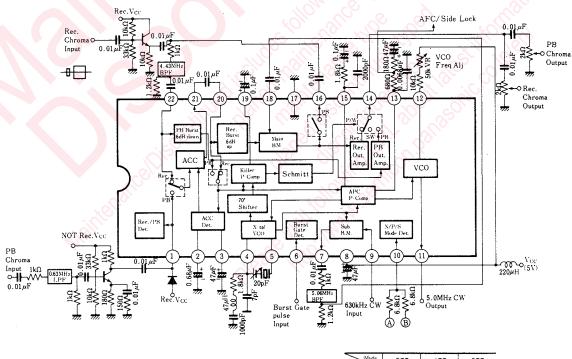


Pin 0 voltage range within which a Pin 0 output level is raised by about 6 dB by increasing  $E_1$  from O V

Pin (1) voltage range within a Pin (2) output DC voltage is turned to a phase comparator error voltage, with E<sub>1</sub> further increased. waveform

Pin ① voltage range when the Pin ⑤ voltage maintains the phase comparator error voltage, with E further increased For 7pF between the Pin ⑥ and GND, select taking into account an optimum capacity on the PCB, etc.

## Application Circuit

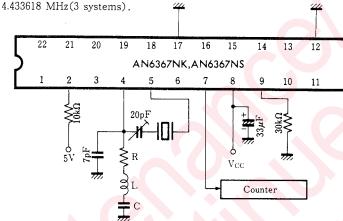


Output Mode	2H	4H	6 <b>H</b>	
A	L	H	H	
В	L	L	Н	

## Precautions for Use

- (i) Allowable power supply range: 4.5 V to 5.5 V
- (ii) Adjusting X-tal VCO

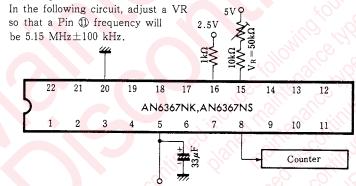
In the PB mode, connect 30 k $\Omega$  between the Pin 9 and GND, and adjust a trimmer so that a 7 output frequency will be 3.579545 MHz(for NTSC)or



	NTSC	3 Systems
R	2.2kΩ	1.8kΩ
L	100µF	<b>47,</b> μ <b>F</b>
С	1000pF	1000pF

For 7pF between the Pin (4) and GND, select taking into account an optimum capacity on the PCB, etc.

#### (iii) Adjusting VCO



 $$V{\rm cc}$$  (iv)For forced burst ACC, connect 100  $k\Omega$  between the Pin 3 and GND.

#### Pin

Pin No.	Pin Name	Pin No.	Pin Name
1	PB Chroma Input Rec. Changeover Input	12	VCO Frequency Adjustment
2	ACC Burst Det.	13	VCO Control Terminal
3	ACC Ref. Level	14	Chroma Output
4	X'tal Osc. Input	15	X'tal APC Control Terminal
5	X'tal Osc. Output	16	PB Main BM Output
6	Burst Gate Pulse Input	17	GND
7	Sub BM Output	18	Main BM Input
8	V <sub>cc</sub>	19	Killer Control Terminal
9	Sub BM Input	20	ACC Input
10	NTSC/PAL/SECAM Mode Changeover Input	21	ACC Output
11	VCO Output	22	3.58MHz Chroma Input

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