Dual 3A Boost/Inverting/SEPIC DC/DC Converter with Fault Protection

FEATURES

- **Dual 42V, 3A Combined Power Switch**
- **Master/Slave (1.7A/1.3A) Switch Design**
- **Wide Input Range: 2.5V to 22V Operating, 40V Maximum Transient**
- **Power Good Pin for Event Based Sequencing**
- Switching Frequency Up to 2.5MHz
- Each Channel Easily Configurable as a Boost, SEPIC, Inverting or Flyback Converter
- Low V_{CESAT} Switch: 270mV at 2.75A (Typical)
- Can be Synchronized to an External Clock
- Output Short-Circuit Protection
- High Gain $\overline{SHDN}$ Pin Accepts Slowly Varying Input Signals
- 24-Pin 7mm × 4mm DFN Package

APPLICATIONS

- Local Power Supply
- Vacuum Fluorescent Display (VFD) Bias Supplies
- TFT-LCD Bias Supplies
- Automotive Engine Control Unit (ECU) Power

DESCRIPTION

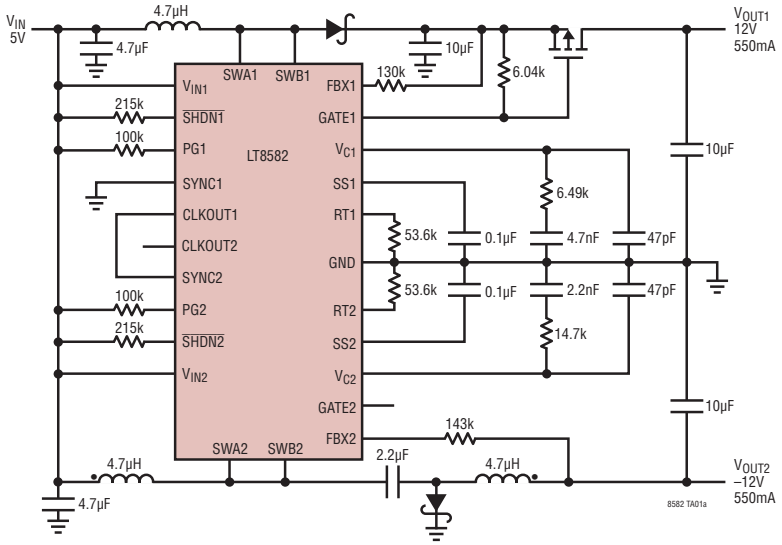
The LT®8582 is a dual independent channel PWM DC/DC converter with a power good pin and built-in fault protection to help guard against input overvoltage and overtemperature conditions. Each channel consists of a 42V master switch and a 42V slave switch that can be tied together for a total current limit of 3A.

The LT8582 is ideal for many local power supply designs. Each channel can be easily configured in boost, SEPIC, inverting, or flyback configurations. Together, the two channels can produce a 12V and a –12V output with 14.4W of combined output power from a 5V input. In addition, the LT8582's slave switch allows the part to be configured in high voltage, high power charge pump topologies that are more efficient and require fewer components than traditional circuits.

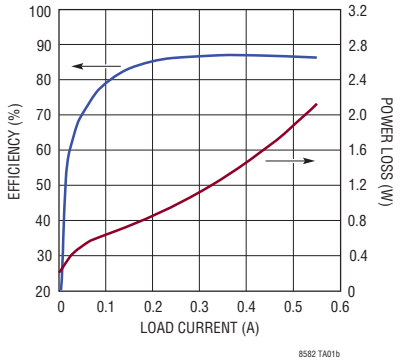
The LT8582 also features innovative $\overline{SHDN}$ pin circuitry that allows for slowly varying input signals and an adjustable undervoltage lockout function. Additional features such as output short protection, frequency foldback and soft-start are integrated. The LT8582 is available in a 24-pin 7mm × 4mm DFN package.

TYPICAL APPLICATION

1.5MHz, 5V to ±12V



Efficiency and Power Loss (Load Between 12V and –12V Outputs)



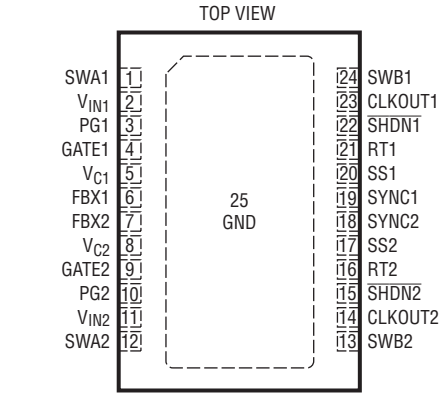
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN1} Voltage ..... –0.3V to 40V
SWA1/SWB1 Voltage..... –0.4V to 42V
RT1 Voltage ..... –0.3V to 5V
SS1 Voltage ..... –0.3V to 2.5V
FBX1 Voltage..... –0.3V to 5V
V_{C1} Voltage ..... –0.3V to 2V
$\overline{SHDN1}$ Voltage 40V
$\overline{SHDN1}$ Current .....–1mA
SYNC1 Voltage..... –0.3V to 5.5V
GATE1 Voltage ..... –0.3V to 60V
PG1 Voltage ..... –0.3V to 40V
PG1 Current .....±0.5mA
CLKOUT1 ..... (Note 5)
Operating Junction Temperature Range
LT8582E ..... –40°C to 125°C
LT8582I ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C

Note: Absolute maximum ratings are shown for channel 1 only. Channel 2 ratings are identical.

PIN CONFIGURATION



DKD PACKAGE
24-LEAD (7mm × 4mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 34°C/W, θ_{JC} = 7°C/W
EXPOSED PAD (PIN 25) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT8582EDKD#PBF	LT8582EDKD#TRPBF	8582	24-Pin (7mm × 4mm) Plastic DFN	–40°C to 125°C
LT8582IDKD#PBF	LT8582IDKD#TRPBF	8582	24-Pin (7mm × 4mm) Plastic DFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 5V, $V_{\overline{SHDN}}$ = V_{IN}, unless otherwise noted (Note 2). Specifications are identical for both channels unless noted otherwise.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Input Voltage V_{IN}		●		2.3	2.5	V
V_{IN} Overvoltage Lockout			22.2	24.5	27	V
Positive Feedback Voltage		●	1.185	1.204	1.220	V
Negative Feedback Voltage		●	2	7	16	mV
Positive FBX Pin Bias Current	V_{FBX} = Positive Feedback Voltage, Current into Pin	●	81	83.3	85	µA
Negative FBX Pin Bias Current	V_{FBX} = Negative Feedback Voltage, Current out of Pin	●	81	83.3	85.5	µA
Error Amp Transconductance	ΔI = 10µA			280		µmhos
Error Amp Voltage Gain				80		V/V
Quiescent Current	$V_{\overline{SHDN}}$ = 2.5V, Not Switching			2.1	2.5	mA
Quiescent Current in Shutdown	$V_{\overline{SHDN}}$ = 0			0	1	µA
Reference Line Regulation	2.5V ≤ V_{IN} ≤ 20V			0.01	0.05	%/V
Switching Frequency, f_{OSC}	R_T = 31.6kΩ R_T = 407kΩ	● ●	2.125 170	2.5 200	2.875 230	MHz kHz
Switching Frequency in Foldback	Compared to Normal f_{OSC}			1/6		ratio
Switching Frequency Range	Free-Running or Synchronizing	●	200		2500	kHz
SYNC High Level for Sync		●	1.3			V
SYNC Low Level for Sync		●			0.4	V
SYNC Clock Pulse Duty Cycle	V_{SYNC} = 0V to 2V		20		80	%
Recommended Min SYNC Ratio f_{SYNC}/f_{OSC}				3/4		ratio
Minimum Off-Time				45		ns
Minimum On-Time				55		ns
SWA Current Limit	Minimum Duty Cycle Maximum Duty Cycle	● ●	1.8 1.3	2.4 1.8	3 2.5	A A
SWA FAULT Current Limit	Minimum Duty Cycle Maximum Duty Cycle	● ●	2.2 1.6	2.8 2.3	3.5 3.0	A A
SW Current Sharing, I_{SWB}/I_{SWA}	SWA and SWB Tied Together			0.79		A/A
SWA + SWB Current Limit	Minimum Duty Cycle, I_{SWB}/I_{SWA} = 0.79 Maximum Duty Cycle, I_{SWB}/I_{SWA} = 0.79	● ●	3.3 2.3	4.3 4.1	5.4 4.5	A A
SWA + SWB FAULT Current Limit	Minimum Duty Cycle, I_{SWB}/I_{SWA} = 0.79 Maximum Duty Cycle, I_{SWB}/I_{SWA} = 0.79	● ●	4 2.8	5 4	6.3 5.4	A A
Switch V_{CESAT}	I_{SWA} + I_{SWB} = 2.75A			270		mV
SWA Leakage Current	V_{SWA} = 5V, $V_{\overline{SHDN}}$ = 0			0.01	1	µA
SWB Leakage Current	V_{SWB} = 5V, $V_{\overline{SHDN}}$ = 0			0.01	1	µA
SS Charge Current	V_{SS} = 30mV, Current Flows out of SS Pin	●	5.7	8.8	11.7	µA
SS Discharge Current	Part in FAULT, V_{SS} = 2.1V, Current Flows into SS Pin	●	5.7	8.8	11.7	µA
SS High Detection Voltage	Part in FAULT	●	1.65	1.84	2	V
SS Low Detection Voltage	Part Exiting FAULT	●	15	55	100	mV
$\overline{SHDN}$ Minimum Input Voltage High	Active Mode, $\overline{SHDN}$ Rising Active Mode, $\overline{SHDN}$ Falling	● ●	1.26 1.21	1.31 1.27	1.4 1.35	V V
$\overline{SHDN}$ Input Voltage Low	Shutdown Mode	●			0.3	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 5V, $V_{\overline{SHDN}}$ = V_{IN}, unless otherwise noted (Note 2). Specifications are identical for both channels unless noted otherwise.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$\overline{SHDN}$ Pin Bias Current	$V_{\overline{SHDN}}$ = 3V $V_{\overline{SHDN}}$ = 1.3V $V_{\overline{SHDN}}$ = 0V		 10.1	45 12.1 0	65 14.1 0.1	µA µA µA
CLKOUT Output Voltage High	1mA out of CLKOUT Pin		1.9	2.1	2.3	V
CLKOUT Output Voltage Low	1mA into CLKOUT Pin			30	200	mV
CLKOUT1 Duty Cycle	All T_J			50		%
CLKOUT2 Duty Cycle	T_J = –40°C T_J = 25°C T_J = 125°C			22.5 42 72		% % %
CLKOUT Rise Time	C_{CLKOUT} = 120pF			25		ns
CLKOUT Fall Time	C_{CLKOUT} = 120pF			15		ns
GATE Pull-Down Current	V_{GATE} = 3V V_{GATE} = 20V	● ●	0.8 0.8	1 1	1.2 1.2	mA mA
GATE Leakage Current	V_{GATE} = 50V, GATE Off			0.01	1	µA
PG Threshold for Positive Feedback Voltage	V_{FBX} Rising		1.09	1.15	1.20	V
PG Threshold for Negative Feedback Voltage	V_{FBX} Falling		20	65	120	mV
PG Hysteresis for Feedback Voltage				4		mV
PG Output Voltage Low	100µA into PG Pin, V_{FBX} = 1V	●		70	150	mV
PG Leakage Current	V_{PG} = 40V, V_{FBX} = 1.204V			0.01	1	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT8582E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating temperature range are assured by design, characterization and correlation with statistical process controls. The LT8582I is guaranteed over the full –40°C to 125°C operating junction temperature range.

Note 3: Current limit guaranteed by design and/or correlation to static test.

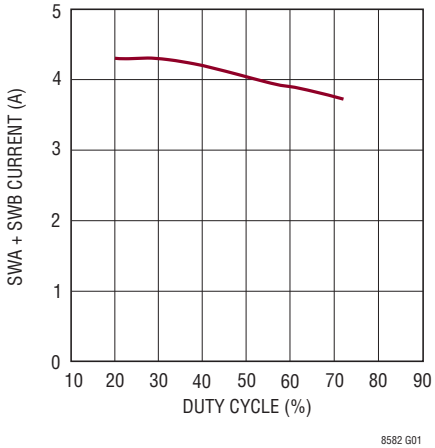
Note 4: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation over the specified maximum operating junction temperature may impair device reliability.

Note 5: Do not apply a positive or negative voltage or current source to CLKOUT, otherwise permanent damage may occur.

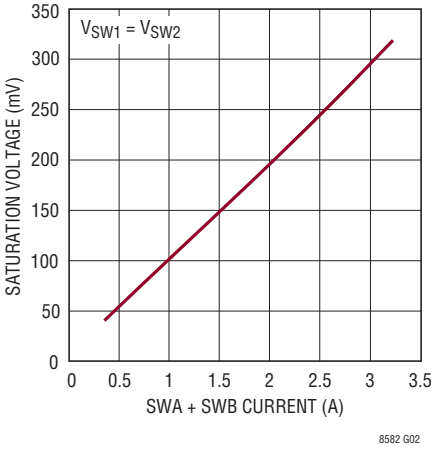
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

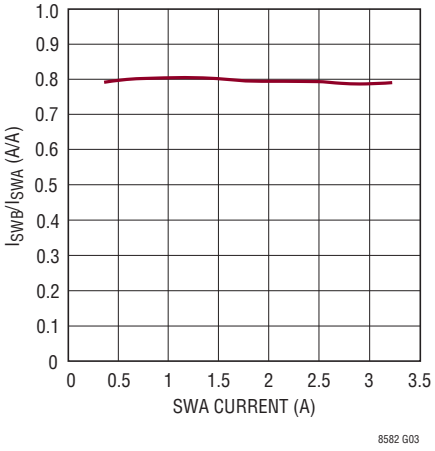
Switch Current Limit vs Duty Cycle



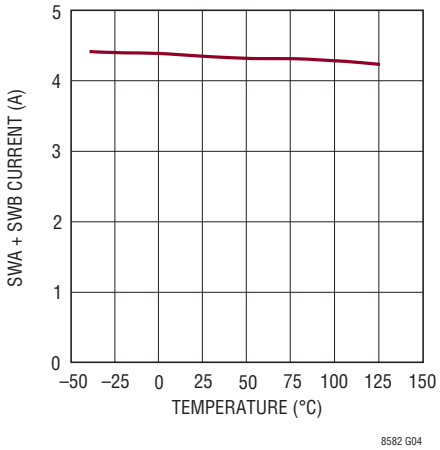
Switch Saturation Voltage



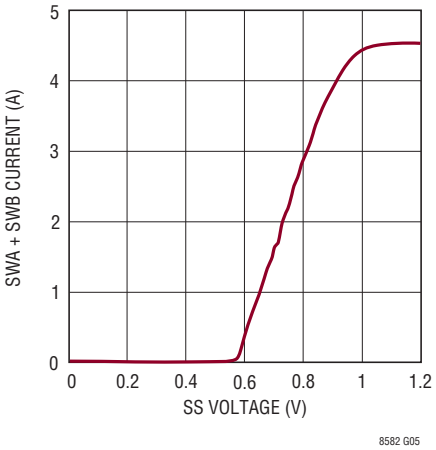
Switch Current Sharing



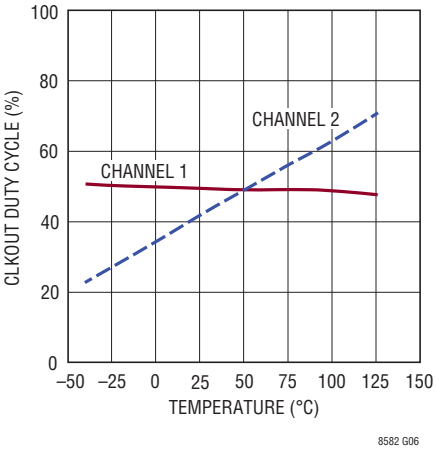
Switch Current Limit at Minimum Duty Cycle



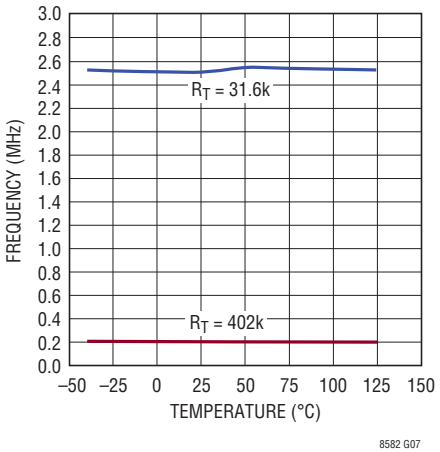
Commanded Current Limit vs SS Voltage



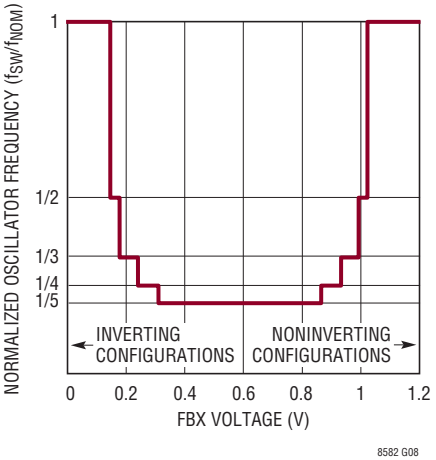
CLKOUT Duty Cycle



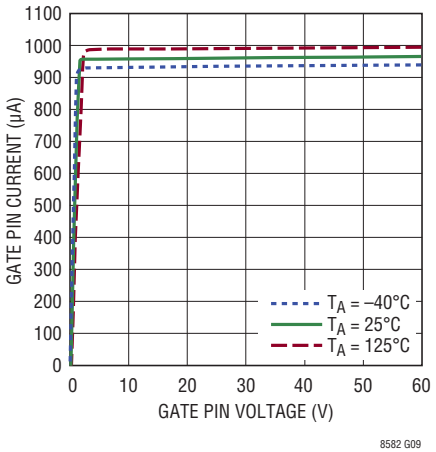
Oscillator Frequency



Switching Frequency During Soft-Start



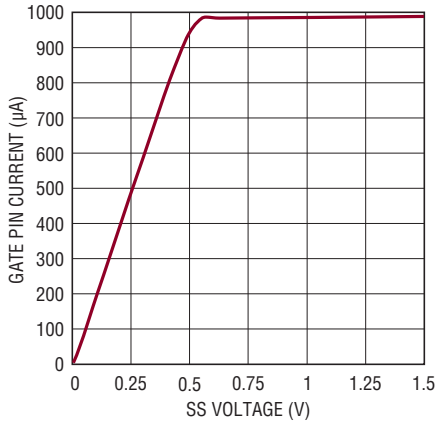
Gate Pin Current (V_{SS} = 2.1V)



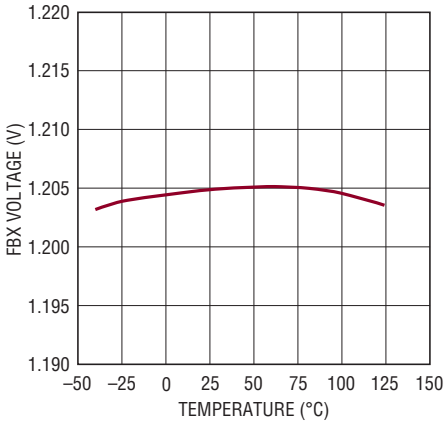
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

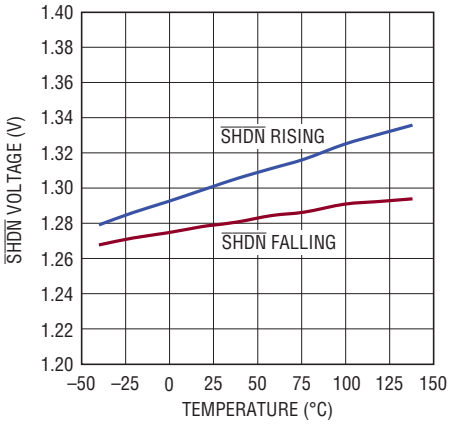
Gate Pin Current (V_{GATE} = 5V)



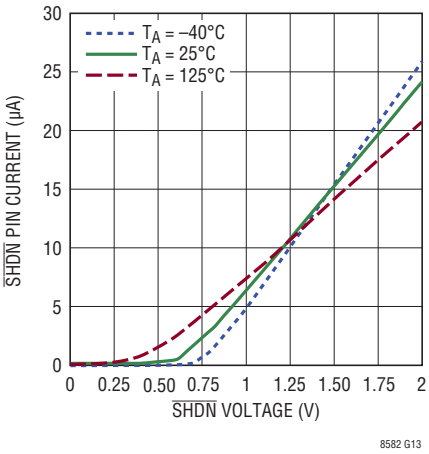
Positive Feedback Voltage



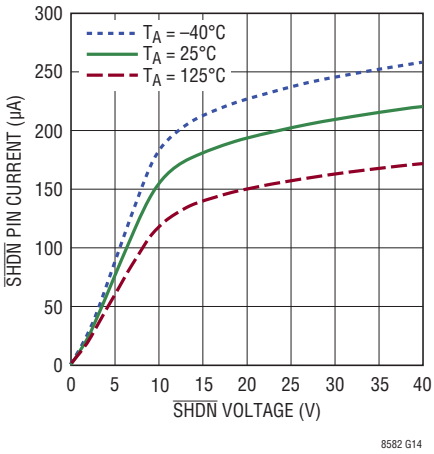
Active/Lockout Threshold



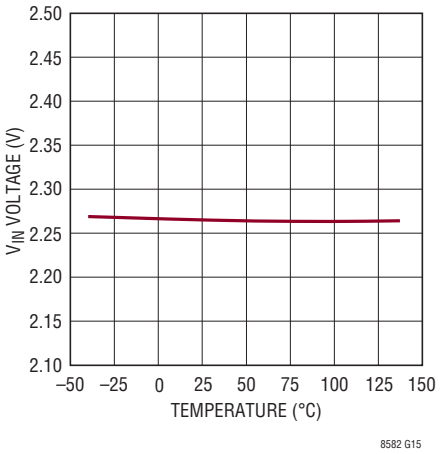
SHDN Pin Current



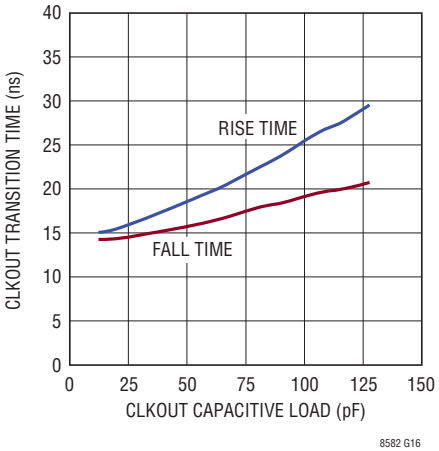
SHDN Pin Current



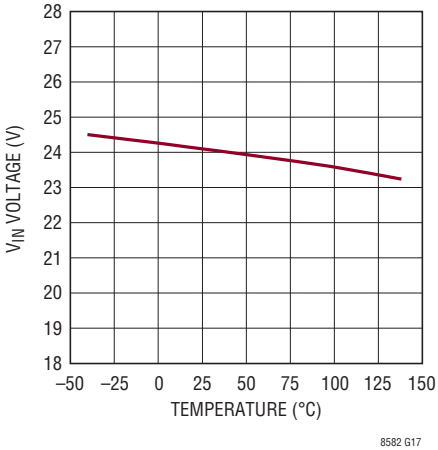
Internal UVLO



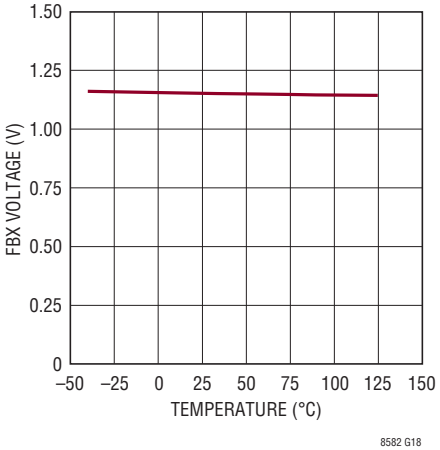
CLKOUT Rise and Fall Times at 1MHz



V_{IN} Overvoltage Lockout



PG Threshold



PIN FUNCTIONS (CH1/CH2)

FBX1, FBX2 (Pin 6/Pin 7): Positive and Negative Feedback Pins. For an inverting or noninverting output converter, tie a resistor from the FBX pin to V_{OUT} according to the following equations:

$$R_{FBX} = \left(\frac{V_{OUT} - 1.204V}{83.3\mu A}\right); \text{ Noninverting Converter}$$

$$R_{FBX} = \left(\frac{|V_{OUT}| + 7mV}{83.3\mu A}\right); \text{ Inverting Converter}$$

VC1, VC2 (Pin 5/Pin 8): Error Amplifier Output Pins. Tie external compensation network to these pins.

GATE1, GATE2 (Pin 4/Pin 9): PMOS Gate Drive Pins. The GATE pin is a pull-down current source and can be used to drive the gate of an external PMOS transistor for output short-circuit protection or output disconnect. The GATE pin current increases linearly with the SS pin voltage, with a maximum pull-down current of 1mA at SS voltages exceeding 550mV. Note that if the SS voltage is greater than 550mV and the GATE pin voltage is less than 2V, the GATE pin looks like a 2kΩ impedance to ground. See the Appendix for more information.

PG1, PG2 (Pin 3/Pin 10): Power Good Indication Pins. This active high pin indicates that the FBX pin voltage for the corresponding channel is within 4% of its regulation voltage (V_{FBX} > 1.15V for noninverting outputs or V_{FBX} < 65mV for inverting outputs). For most applications, a 4% change in V_{FBX} corresponds to an 8% change in V_{OUT}. This open drain output requires a pull-up resistor to indicate power good. Also, the status is valid only when $\overline{SHDN}$ > 1.31V and V_{IN} > 2.3V.

VIN1, VIN2 (Pin 2/Pin 11): Input Supply Pins. Must be locally bypassed.

SWA1, SWA2 (Pin 1/Pin 12): Master Switch Pins. This is the collector of the internal master NPN power switch for each channel. SWA is designed to handle a peak collector current of 1.7A (minimum). Minimize the metal trace area connected to this pin to minimize EMI.

SWB1, SWB2 (Pin 24/Pin 13): Slave Switch Pins. This is the collector of the internal slave NPN power switch for each channel. SWB is designed to handle a peak collector current of 1.3A (minimum). Minimize the metal trace area connected to this pin to minimize EMI.

CLKOUT1, CLKOUT2 (Pin 23/Pin 14): Clock Output Pins. Use these pins to synchronize one or more other ICs to either channel of the LT8582. Can also be used to synchronize channel 1 or channel 2 of the LT8582 with the other channel of the LT8582. This pin oscillates at the same frequency as the internal oscillator of the part or, if active, the SYNC pin. The CLKOUT pin signal on CH1 is 180° out of phase with the internal oscillator or SYNC pin and the duty cycle is fixed at ~50%. The CLKOUT pin signal on CH2 is in phase with the internal oscillator or SYNC pin and the duty cycle varies linearly with the part's junction temperature. Note that CLKOUT of either channel is only meant to drive capacitive loads up to 120pF.

$\overline{SHDN1}$, $\overline{SHDN2}$ (Pin 22/Pin 15): Shutdown Pins. In conjunction with the UVLO (undervoltage lockout) circuit, these pins are used to enable/disable the channel and restart the soft-start sequence. Drive below 0.3V to disable the channel with very low quiescent current. Drive above 1.31V (typical) to activate the channel and restart the soft-start sequence. Do not float these pins.

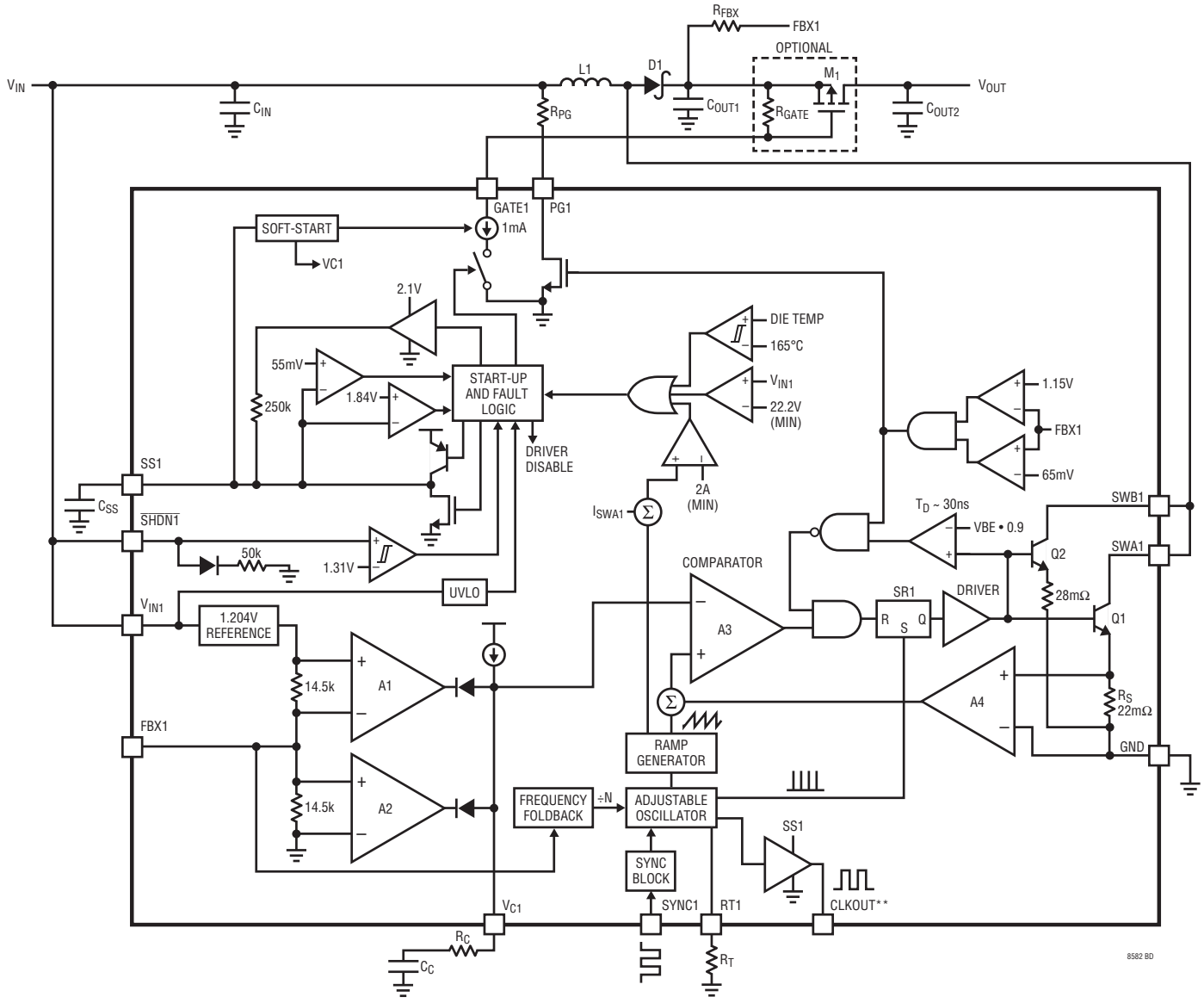
RT1, RT2 (Pin 21/Pin 16): Timing Resistor Pins. Adjusts the switching frequency of the corresponding channel. Place a resistor from these pins to ground to set the frequency to a fixed free running level. Do not float these pins.

SS1, SS2 (Pin 20/Pin 17): Soft-Start Pins. Place a soft-start capacitor here. Upon start-up, the SS pins will be charged by a (nominally) 250k resistor to ~2.1V. During a fault, the SS pin for the corresponding channel will be slowly charged up and discharged as part of a timeout sequence (see the State Diagram for more information).

SYNC1, SYNC2 (Pin 19/Pin 18): Use to synchronize the switching frequency of a channel to an outside clock. The high voltage level of the clock must exceed 1.3V and the low level must be less than 0.4V. Drive these pins to less than 0.4V to revert to the internal free running clock for the corresponding channel. See the Applications Information section for more information.

GND (Exposed Pad Pin 25): Ground. Exposed pad must be soldered directly to local ground plane.

BLOCK DIAGRAM



**BLOCK DIAGRAM FOR CH1 IS SHOWN. BLOCK DIAGRAM FOR CH2 IS IDENTICAL, EXCEPT CLKOUT SIGNAL FOR CH1 IS 180° OUT OF PHASE WITH THE INTERNAL OSCILLATOR AND HAS A FIXED 50% DUTY CYCLE AND CLKOUT SIGNAL FOR CH2 IS IN PHASE WITH THE INTERNAL OSCILLATOR AND ITS DUTY CYCLE VARIES LINEARLY WITH THE PART'S JUNCTION TEMPERATURE.

Figure 1. Block Diagram

STATE DIAGRAM

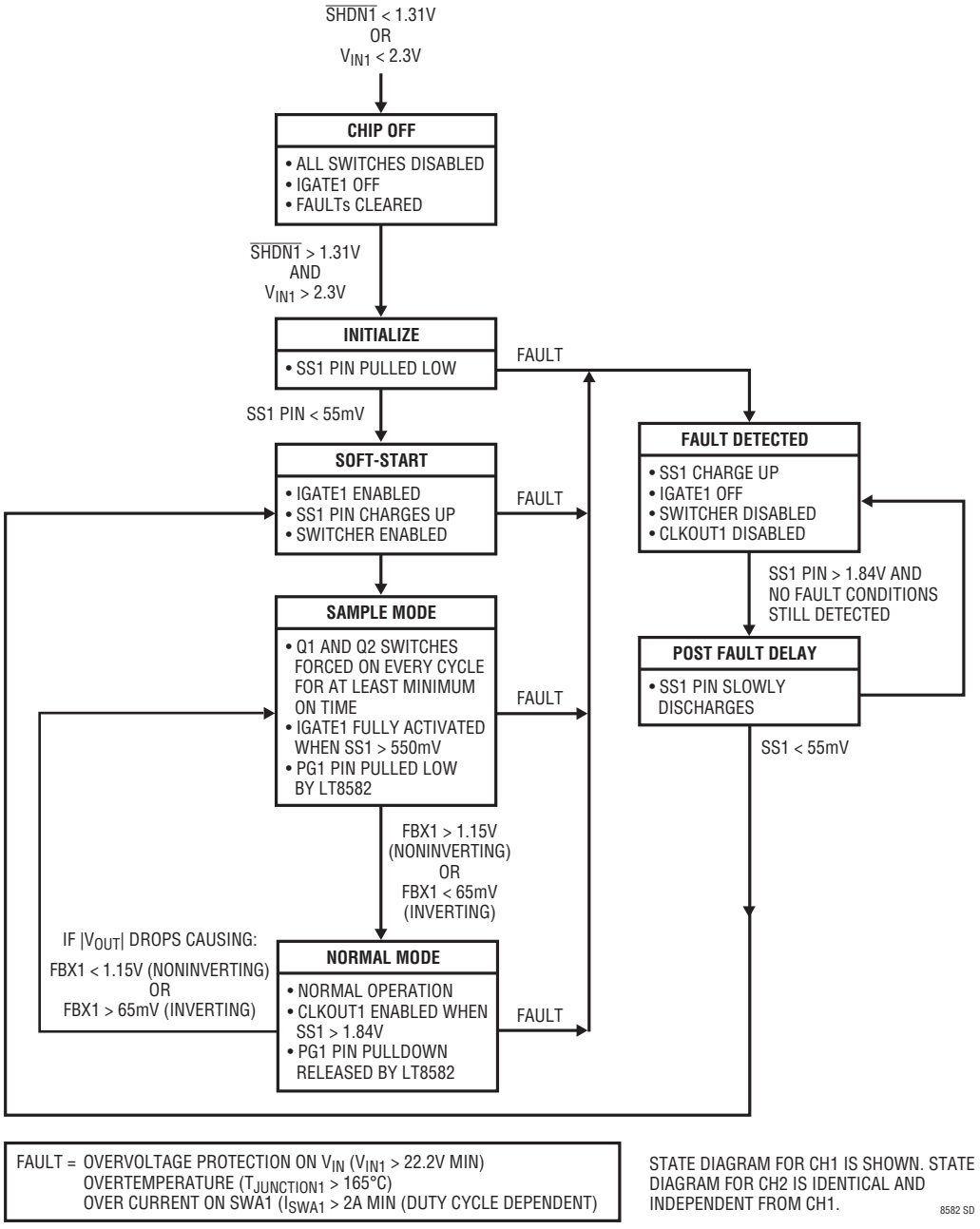


Figure 2. State Diagram

OPERATION

OPERATION – OVERVIEW

The LT8582 uses a constant frequency, current mode control scheme to provide excellent line and load regulation. Each channel's undervoltage lockout (UVLO) function, together with soft-start and frequency foldback, offer a controlled means of starting up. Fault features are incorporated into each channel of the LT8582 to facilitate the detection of output shorts, overvoltage and overtemperature conditions. Please refer to the Block Diagram (Figure 1) and the State Diagram (Figure 2) for the following description of the part's operation.

OPERATION – START-UP

Several functions are provided to enable a very clean start-up of both channels of the LT8582.

Precise Turn-On Voltage

The $\overline{SHDN}$ pin on each channel is compared to an internal voltage reference to give a precise turn on voltage level. Taking each $\overline{SHDN}$ pin above 1.31V enables the corresponding channel. Taking each $\overline{SHDN}$ pin below 300mV shuts down the channel, resulting in extremely low quiescent current for that channel. The $\overline{SHDN}$ pin has 35mV of hysteresis to protect against glitches and slow ramping.

Configurable Undervoltage Lockout (UVLO)

The $\overline{SHDN}$ pin can also be used to create a configurable UVLO for each channel. This function sets the turn on/off of each of LT8582's channels at a desired voltage (VIN_{UVLO}). Figure 3 shows how a resistor divider (or a single resistor) from V_{IN} to the $\overline{SHDN}$ pin can be used to program VIN_{UVLO}. R_{UVLO2} is optional. If left out, set it to infinite in the equation below. For increased accuracy, set $R_{UVLO2} \leq 10k$. Pick R_{UVLO1} as follows:

$$R_{UVLO1} = \frac{VIN_{UVLO} - 1.31V}{\left(\frac{1.31V}{R_{UVLO2}}\right) + 12.3\mu A}$$

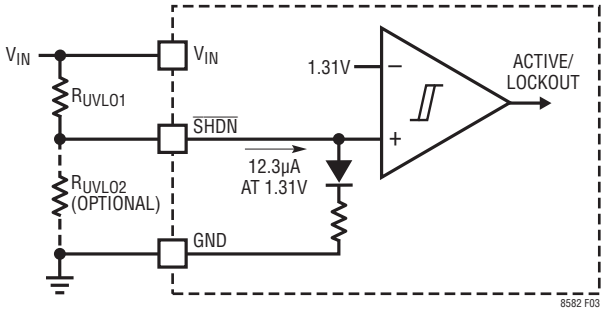


Figure 3. Configurable UVLO

Internal Undervoltage Lockout (UVLO)

Regardless of where external circuitry sets VIN_{UVLO}, the LT8582 also has internal UVLO circuitry that disables the chip when $V_{IN} < 2.3V$ (typical).

Soft-Start of Switch Current

The soft-start circuitry provides for a gradual ramp-up of the switch current in each channel (refer to Commanded Current Limit vs SS Voltage in Typical Performance Characteristics). When the channel is taken out of shutdown, the external SS capacitor is first discharged. This resets the state of the logic circuits in the channel. Then an integrated 250k resistor pulls the channel's SS pin to ~1.84V. The ramp rate of the SS pin voltage is set by this 250k resistor and the external capacitor connected to this pin. Once SS gets to ~1.84V, the CLKOUT pin is enabled and an internal regulator pulls the pin up quickly to ~2.1V. Typical values for the external soft-start capacitor range from 100nF to 1µF.

Soft-Start of External PMOS (if used)

The soft-start circuitry also gradually ramps up the GATE pin pull-down current for the corresponding channel. This allows an external PMOS to slowly turn on (M1 in Block Diagram). The GATE pin current increases linearly with SS voltage, with a maximum current of 1mA when the SS voltage gets above 550mV. Note that if the GATE pin voltage is less than 2V for SS voltages exceeding 550mV, then the GATE pin impedance to ground is 2kΩ. The soft turn on of the external PMOS helps limit inrush current at start up, making hot plugs of LT8582s feasible.

OPERATION

Sample Mode

Sample mode is the mechanism used by the LT8582 to aid in the detection of output shorts. It refers to a state of the LT8582 where the master and slave power switches (Q1 and Q2) are turned on for a minimum period of time every clock cycle (or every few clock cycles in frequency foldback) in order to sample the inductor current. If the sampled current through Q1 exceeds the master switch fault current limit of 2A (minimum), the LT8582 triggers an overcurrent fault internally for that channel (see Operation – Fault section for details). Sample mode exists when FBX for that channel is out of regulation by more than 4% (65mV < FBX < 1.15V). During this mode, PG will be pulled low.

Frequency Foldback

The frequency foldback circuit reduces the switching frequency for that channel when 144mV < FBX < 1.03V (typical). This feature lowers the minimum duty cycle that the channel can achieve, thus allowing better control of the inductor current during start-up. When the FBX voltage is pulled outside of the above mentioned range, the switching frequency for that channel returns to normal.

Note that the peak inductor current at start-up is a function of many variables including load profile, output capacitance, target V_{OUT}, V_{IN}, switching frequency, etc.

OPERATION – REGULATION

The following description of the LT8582's operation assumes that the FBX voltage is close enough to its regulation target so that the part is not in sample mode. Also, this description applies equally to both channels independently of each other. Use the Block Diagram as a reference when stepping through the following description of the LT8582 operating in regulation.

At the start of each oscillator cycle, the SR latch (SR1) is set, which turns on the power switches Q1 and Q2. The collector current through the master switch, Q1, is ~1.3 times the collector current through the slave switch, Q2, when the collectors of the two switches are tied together. Q1's emitter current flows through a current sense resistor (R_S) generating a voltage proportional to the switch current. This voltage (amplified by A4) is added to a stabilizing ramp and the resulting sum is fed into the positive terminal of the PWM comparator A3. When the voltage on the positive input of A3 exceeds the voltage on the negative input, the SR latch is reset, turning off the master and slave power switches. The voltage on the negative input of A3 (V_C pin) is set by A1 (or A2), which is simply an amplified difference between the FBX pin voltage and the reference voltage (1.204V if the LT8582 is configured as a noninverting converter, or 7mV if configured as an inverting converter). In this manner, the error amplifier sets the correct peak current level to maintain output regulation.

As long as the channel is not in fault and the SS pin exceeds 1.84V, the LT8582 drives the CLKOUT pin for that channel at the frequency set by the RT pin or the SYNC pin. The CLKOUT pin can synchronize other ICs, including additional LT8582s or the other channel of an LT8582, up to 120pF load on CLKOUT. For channel 1, CLKOUT1 has a fixed duty cycle and is 180° out of phase with the internal clock. For channel 2, CLKOUT2's duty cycle varies linearly with channel 2's junction temperature and may be used as a temperature monitor.

OPERATION – FAULT

Each of the following events can trigger a fault in the LT8582:

1. SW Overcurrent:
   a. I_{SWA} > 2A (minimum)
   b. (I_{SWA} + I_{SWB}) > 3.5A (minimum)
2. V_{IN} Voltage > 22.2V (minimum)
3. Die Temperature > 165°C

OPERATION

Refer to the State Diagram (Figure 2) for the following description of the LT8582's operation during a fault event. When a fault is detected on a channel, the LT8582 disables the CLKOUT pin for that channel, turns off the power switches for that channel and the GATE pin for that channel becomes high impedance. The external PMOS, M1, is turned off by the external R_{GATE} resistor (see Block Diagram). With the external PMOS turned off, the power path from V_{IN} to V_{OUT} is opened, protecting power path components. Also, as soon as the feedback voltage falls inside the range 65mV < FBX < 1.15V, PG pulls low. Refer to Figure 4 for the case of an output short.

At the beginning of a fault event, a timeout sequence commences where the SS pin for that channel is charged up to 1.84V (the SS pin will continue charging up to ~2.1V and be held there in the case of a FAULT event that still exists) and then discharged to 55mV. This timeout period relieves the chip, the PMOS and other power path components from electrical and thermal stress for a minimum amount of time set by the voltage ramp rate on the SS pin.

OPERATION – CURRENT LIMIT

The current limit operates independently of the FAULT current limit. The current limit sets a maximum switch current. This switch current limit is duty cycle dependent, but for most applications will be around 3A minimum (see the Electrical Characteristics). Once this limit is reached, the switch duty cycle decreases, reducing the magnitude of the output voltage. If, despite the reduced duty cycle the switch current reaches the FAULT current limit, the part will behave as described in the Operation – Fault section.

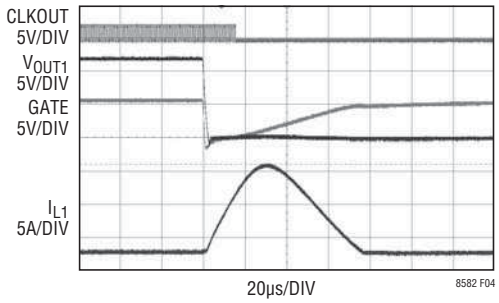


Figure 4. Output Short-Circuit Protection of the LT8582

APPLICATIONS INFORMATION

Boost Converter Component Selection

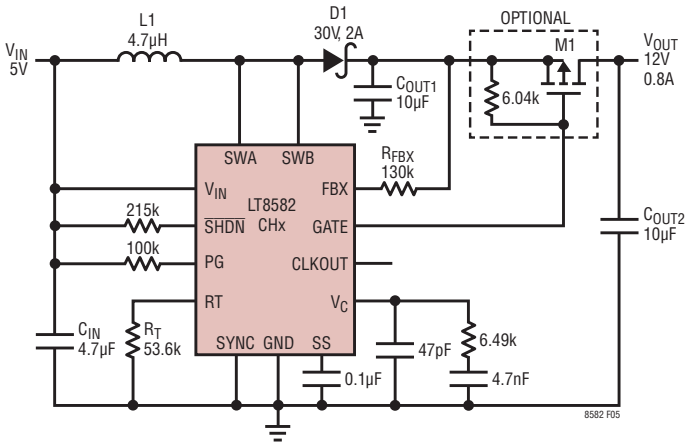


Figure 5. Boost Converter – The Component Values Given Are Typical Values for a 1.5MHz, 5V to 12V Boost

Each channel of the LT8582 can be configured as a boost converter as in Figure 5. This topology allows for positive output voltages that are higher than the input voltage. An external PMOS (optional) driven by the GATE pin of the LT8582 can achieve input or output disconnect during a FAULT event, $\overline{SHDN}$ < 1.31V, or V_{IN} < 2.3V. Figure 5 shows the configuration for output disconnect. A single feedback resistor sets the output voltage. For output voltages higher than 40V, see the Charge Pump Topology in the Charge Pump Aided Regulators section.

Table 1 is a step-by-step set of equations to calculate component values for the LT8582 when operating as a boost converter. Input parameters are input and output voltage and switching frequency (V_{IN}, V_{OUT} and f_{OSC} respectively). Refer to the Appendix for further information on the design equations presented in Table 1.

Variable Definitions:

V_{IN} = Input Voltage
V_{OUT} = Output Voltage
DC = Power Switch Duty Cycle
f_{OSC} = Switching Frequency
I_{OUT} = Maximum Output Current
I_{RIPPLE} = Inductor Ripple Current
R_{DSON_PMOS} = R_{DSON} of External Output PMOS (set to 0 if not using PMOS)

Table 1. Boost Converter Design Equations

	PARAMETERS/EQUATIONS
Step 1: Inputs	Choose V_{IN}, V_{OUT} and f_{OSC} to calculate equations below.
Step 2: DC	$DC \cong \frac{V_{OUT} - V_{IN} + 0.5V}{V_{OUT} + 0.5V - 0.3V}$
Step 3: L1	$L_{TYP} = \frac{(V_{IN} - 0.3) \bullet DC}{f_{OSC} \bullet 1A}$ (1) $L_{MIN} = \frac{(V_{IN} - 0.3V) \bullet (2 \bullet DC - 1)}{1.7A \bullet f_{OSC} \bullet (1 - DC)}$ (2) $L_{MAX} = \frac{(V_{IN} - 0.3V) \bullet DC}{f_{OSC} \bullet 0.18A}$ (3) • Solve equations 1, 2 and 3 for a range of L values • The minimum of the L value range is the higher of L_{TYP} and L_{MIN} • The maximum of the L value range is L_{MAX}
Step 4: I_{RIPPLE}	$I_{RIPPLE} = \frac{(V_{IN} - 0.3V) \bullet DC}{f_{OSC} \bullet L_1}$
Step 5: I_{OUT}	$I_{OUT} = \left(3A - \frac{I_{RIPPLE}}{2}\right) \bullet (1 - DC)$
Step 6: D1	$V_R \geq V_{OUT}$; $I_{AVG} \geq I_{OUT}$
Step 7: C_{OUT}	$C_{OUT1} = C_{OUT2} \geq \frac{I_{OUT} \bullet DC}{f_{OSC}\ (0.01 \bullet V_{OUT} - 0.5 \bullet I_{OUT} \bullet R_{DSON\_PMOS})}$ • If PMOS is not used, then use just one capacitor where $C_{OUT} = C_{OUT1} + C_{OUT2}$
Step 8: C_{IN}	$C_{IN} \geq C_{VIN} + C_{PWR} \geq \frac{3A \bullet DC}{50 \bullet f_{OSC} \bullet 0.005 \bullet V_{IN}} + \frac{I_{RIPPLE}}{8 \bullet f_{OSC} \bullet 0.005 \bullet V_{IN}}$
Step 9: R_{FBX}	$R_{FBX} = \left(\frac{V_{OUT} - 1.204V}{83.3\mu A}\right)$
Step 10: R_T	$R_T = \frac{81.6}{f_{OSC}} - 1$; f_{OSC} in MHz and R_T in kΩ
Step 11: PMOS	Only needed for input or output disconnect. See PMOS Selection in the Appendix for information on sizing the PMOS and the biasing resistor, R_{GATE} and picking appropriate UVLO components.

Note 1: Above equations use numbers good for many applications but for more exact results use the equations from the appendix with numbers from the Electrical Characteristics.

Note 2: The final values for C_{OUT1}, C_{OUT2} and C_{IN} may deviate from the above equations in order to obtain desired load transient performance.

APPLICATIONS INFORMATION

SEPIC Converter Component Selection – Coupled or Uncoupled Inductors

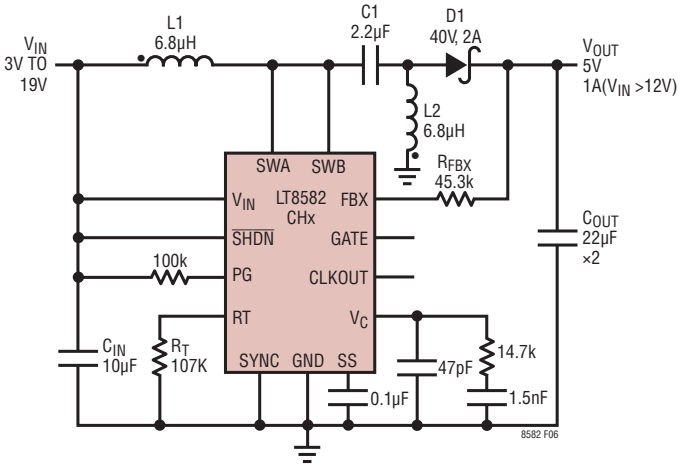


Figure 6. SEPIC Converter – The Component Values Given Are Typical Values for a 700kHz, 3V - 19V to 5V SEPIC Topology Using Coupled Inductors

Each channel of the LT8582 can also be configured as a SEPIC as shown in Figure 6. This topology allows for positive output voltages that are lower, equal, or higher than the input voltage. Output disconnect is inherently built into the SEPIC topology, meaning no DC path exists between the input and output due to capacitor C1. Therefore the external PMOS is not required.

Table 2 is a step-by-step set of equations to calculate component values for the LT8582 when operating as a SEPIC converter. Input parameters are input and output voltage and switching frequency (V_{IN}, V_{OUT} and f_{OSC} respectively). Refer to the Appendix for further information on the design equations presented in Table 2.

Variable Definitions:

V_{IN} = Input Voltage
V_{OUT} = Output Voltage
DC = Power Switch Duty Cycle
f_{OSC} = Switching Frequency
I_{OUT} = Maximum Output Current
I_{RIPPLE} = Inductor Ripple Current

Table 2. SEPIC Design Equations

	PARAMETERS/EQUATIONS
Step 1: Inputs	Choose V_{IN}, V_{OUT} and f_{OSC} to calculate equations below.
Step 2: DC	$DC \cong \frac{V_{OUT}+0.5V}{V_{IN}+V_{OUT}+0.5V-0.3V}$
Step 3: L	$L_{TYP}=\frac{(V_{IN}-0.3V)\bullet DC}{f_{OSC}\bullet 1A}$ (1) $L_{MIN}=\frac{(V_{IN}-0.3V)\bullet(2\bullet DC-1)}{1.7A\bullet f_{OSC}\bullet(1-DC)}$ (2) $L_{MAX}=\frac{(V_{IN}-0.3V)\bullet DC}{f_{OSC}\bullet 0.18A}$ (3) • Solve equations 1, 2 and 3 for a range of L values • The minimum of the L value range is the higher of L_{TYP} and L_{MIN} • The maximum of the L value range is L_{MAX} • L = L1 = L2 for coupled inductors. • L = L1||L2 for uncoupled inductors.
Step 4: I_{RIPPLE}	$I_{RIPPLE}=\frac{(V_{IN}-0.3V)\bullet DC}{f_{OSC}\bullet L}$
Step 5: I_{OUT}	$I_{OUT}=\left(3A-\frac{I_{RIPPLE}}{2}\right)\bullet(1-DC)$
Step 6: D1	$V_R \geq V_{IN}+V_{OUT}$; $I_{AVG} \geq I_{OUT}$
Step 7: C1	C1 ≥ 1µF; $V_{RATING} \geq V_{IN}$
Step 8: C_{OUT}	$C_{OUT} \geq \frac{I_{OUT}\bullet DC}{f_{OSC}\bullet 0.005\bullet V_{OUT}}$
Step 9: C_{IN}	$C_{IN} \geq C_{VIN}+C_{PWR} \geq \frac{3A\bullet DC}{50\bullet f_{OSC}\bullet 0.005\bullet V_{IN}}+\frac{I_{RIPPLE}}{8\bullet f_{OSC}\bullet 0.005\bullet V_{IN}}$
Step 10: R_{FBX}	$R_{FBX}=\left(\frac{V_{OUT}-1.204V}{83.3\mu A}\right)$
Step 11: R_T	$R_T=\frac{81.6}{f_{OSC}}-1$; f_{OSC} in MHz, R_T in kΩ

Note 1: Above equations use numbers good for many applications but for more exact results use the equations from the appendix with numbers from the Electrical Characteristics.

Note 2: The final values for C_{OUT}, and C_{IN} may deviate from the above equations in order to obtain desired load transient performance.

APPLICATIONS INFORMATION

Dual Inductor Inverting Converter Component Selection – Coupled or Uncoupled Inductors

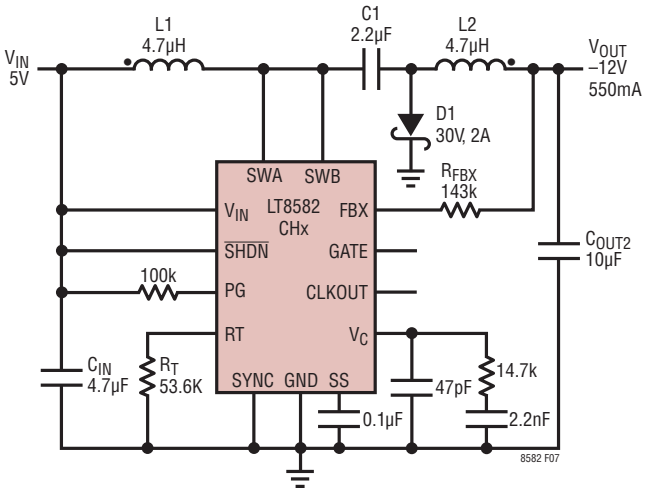


Figure 7. Dual Inductor Inverting Converter – The Component Values Given Are Typical Values for a 1.5MHz, 5V to –12V Inverting Topology Using Coupled Inductors

Due to its unique FBX pin, each channel of the LT8582 can work in a dual inductor inverting configuration as shown in Figure 7. Changing the connections of L2 and the Schottky diode in the SEPIC topology results in generating negative output voltages. This configuration results in very low output voltage ripple due to inductor L2 in series with the output. Output disconnect is inherently built into this topology because of capacitor C1.

Table 3 is a step-by-step set of equations to calculate component values for the LT8582 when operating as a dual inductor inverting converter. Input parameters are input and output voltage and switching frequency (V_{IN}, V_{OUT} and f_{OSC} respectively). Refer to the Appendix for further information on the design equations presented in Table 3.

Variable Definitions:

V_{IN} = Input Voltage
V_{OUT} = Output Voltage
DC = Power Switch Duty Cycle
f_{OSC} = Switching Frequency
I_{OUT} = Maximum Output Current
I_{RIPPLE} = Inductor Ripple Current

Table 3. Dual Inductor Inverting Design Equations

	PARAMETERS/EQUATIONS
Step 1: Inputs	Choose V_{IN}, V_{OUT} and f_{OSC} to calculate equations below.
Step 2: DC	$DC \cong \frac{\lvert V_{OUT}\rvert + 0.5V}{V_{IN} + \lvert V_{OUT}\rvert + 0.5V - 0.3V}$
Step 3: L	$L_{TYP} = \frac{(V_{IN} - 0.3V) \bullet DC}{f_{OSC} \bullet 1A}$ (1) $L_{MIN} = \frac{(V_{IN} - 0.3V) \bullet (2 \bullet DC - 1)}{1.7A \bullet f_{OSC} \bullet (1 - DC)}$ (2) $L_{MAX} = \frac{(V_{IN} - 0.3V) \bullet DC}{f_{OSC} \bullet 0.18A}$ (3) • Solve equations 1, 2 and 3 for a range of L values • The minimum of the L value range is the higher of L_{TYP} and L_{MIN} • The maximum of the L value range is L_{MAX} • L = L1 = L2 for coupled inductors. • L = L1||L2 for uncoupled inductors.
Step 4: I_{RIPPLE}	$I_{RIPPLE} = \frac{(V_{IN} - 0.3V) \bullet DC}{f_{OSC} \bullet L}$
Step 5: I_{OUT}	$I_{OUT} = \left(3A - \frac{I_{RIPPLE}}{2}\right) \bullet (1 - DC)$
Step 6: D1	$V_R > V_{IN} + \lvert V_{OUT}\rvert$; $I_{AVG} > I_{OUT}$
Step 7: C1	C1 ≥ 1µF; $V_{RATING} \geq V_{IN} + \lvert V_{OUT}\rvert$
Step 8: C_{OUT}	$C_{OUT} \geq \frac{I_{RIPPLE}}{8 \bullet f_{OSC} \bullet 0.005 \bullet \lvert V_{OUT}\rvert}$
Step 9: C_{IN}	$C_{IN} \geq C_{VIN} + C_{PWR} \geq \frac{3A \bullet DC}{50 \bullet f_{OSC} \bullet 0.005 \bullet V_{IN}} + \frac{I_{RIPPLE}}{8 \bullet f_{OSC} \bullet 0.005 \bullet V_{IN}}$
Step 10: R_{FBX}	$R_{FBX} = \frac{\lvert V_{OUT}\rvert + 7mV}{83.3\mu A}$
Step 11: R_T	$R_T = \frac{81.6}{f_{OSC}} - 1$; f_{OSC} in MHz, R_T in kΩ

Note 1: Above equations use numbers good for many applications but for more exact results use the equations from the appendix with numbers from the Electrical Characteristics.

Note 2: The final values for C_{OUT}, and C_{IN} may deviate from the above equations in order to obtain desired load transient performance.

APPLICATIONS INFORMATION

LAYOUT GUIDELINES FOR LT8582

General Layout Guidelines

- To improve thermal performance, solder the exposed ground pad of the LT8582 to the ground plane, with multiple vias in and around the pad connecting to additional ground planes.
- A ground plane should be used under the switcher circuitry to prevent interplane coupling and reduce overall noise.
- High speed switching paths (see specific topology below for more information) must be kept as short as possible.
- The V_C, FBX and R_T components should be placed as close to the LT8582 as possible, while being as far away as practically possible from the switch node. The ground for these components should be separated from the switch current path.
- Place the bypass capacitors for the V_{IN} pins (C_{VIN}) as close as possible to the LT8582.
- Place the bypass capacitors for the inductors (C_{PWR}) as close as possible to the inductors.
- Bypass capacitors C_{PWR} and C_{VIN} may be combined into a single bypass capacitor, C_{IN}, if the input side of the inductor can be close to the V_{IN} pin of the LT8582.

Boost Topology Specific Layout Guidelines

- Keep length of loop (high speed switching path) governing switch, diode D1, output capacitor C_{OUT1} and ground return as short as possible to minimize parasitic inductive spikes during switching.

SEPIC Topology Specific Layout Guidelines

- Keep length of loop (high speed switching path) governing switch, flying capacitor C1, diode D1, output capacitor C_{OUT1} and ground return as short as possible to minimize parasitic inductive spikes during switching.

Inverting Topology Specific Layout Guidelines

- Keep ground return path from the cathode of D2 (to chip) separated from output capacitor C_{OUT3}'s ground return path (to chip) in order to minimize switching noise coupling into the output. Notice the separate ground return for D2's cathode in Figure 8.
- Keep length of loop (high speed switching path) governing switch, flying capacitor C1 (in Figure 8), diode D2 and ground return as short as possible to minimize parasitic inductive spikes during switching.

APPLICATIONS INFORMATION

THERMAL CONSIDERATIONS

Overview

For the LT8582 to deliver its full output power, it is imperative that a good thermal path be provided to dissipate the heat generated within the package. This can be accomplished by taking advantage of the thermal pad on the underside of the chip. It is recommended that multiple vias in the printed circuit board be used to conduct heat away from the chip and into copper planes with as much area as possible.

Power and Thermal Calculations

Power dissipation in the LT8582 chip comes from four primary sources: switch I^2R loss, NPN base drive loss (AC + DC) and chip bias current. The following formulas assume continuous mode operation, so they should not be used for calculating thermal losses or efficiency in discontinuous mode or at light load currents.

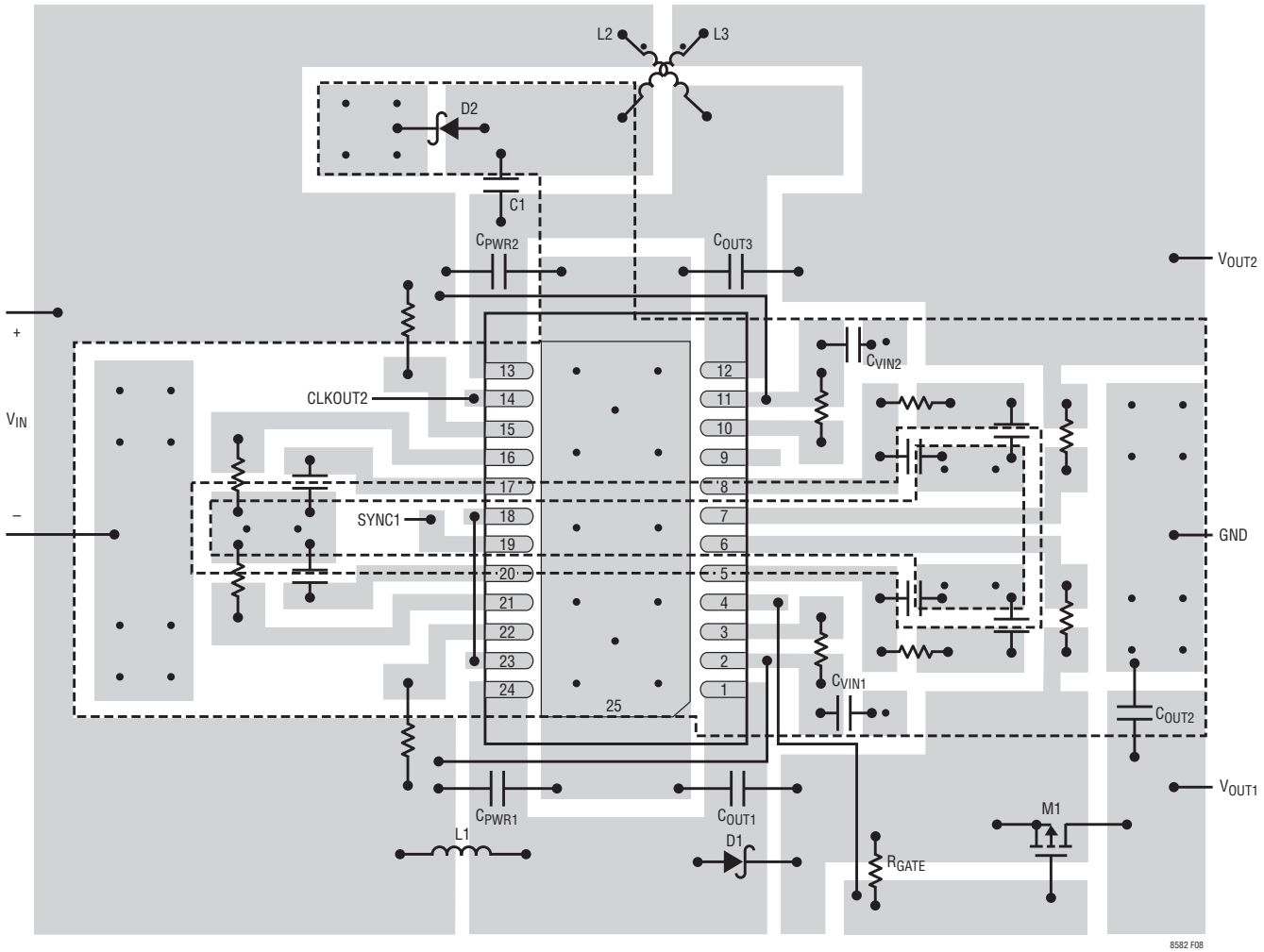


Figure 8. Suggested Component Placement for Boost and Dual Inductor Inverting Topologies. Note the Separate Ground Return for the R_T, SS, and V_C Components as Well as D2's Cathode

APPLICATIONS INFORMATION

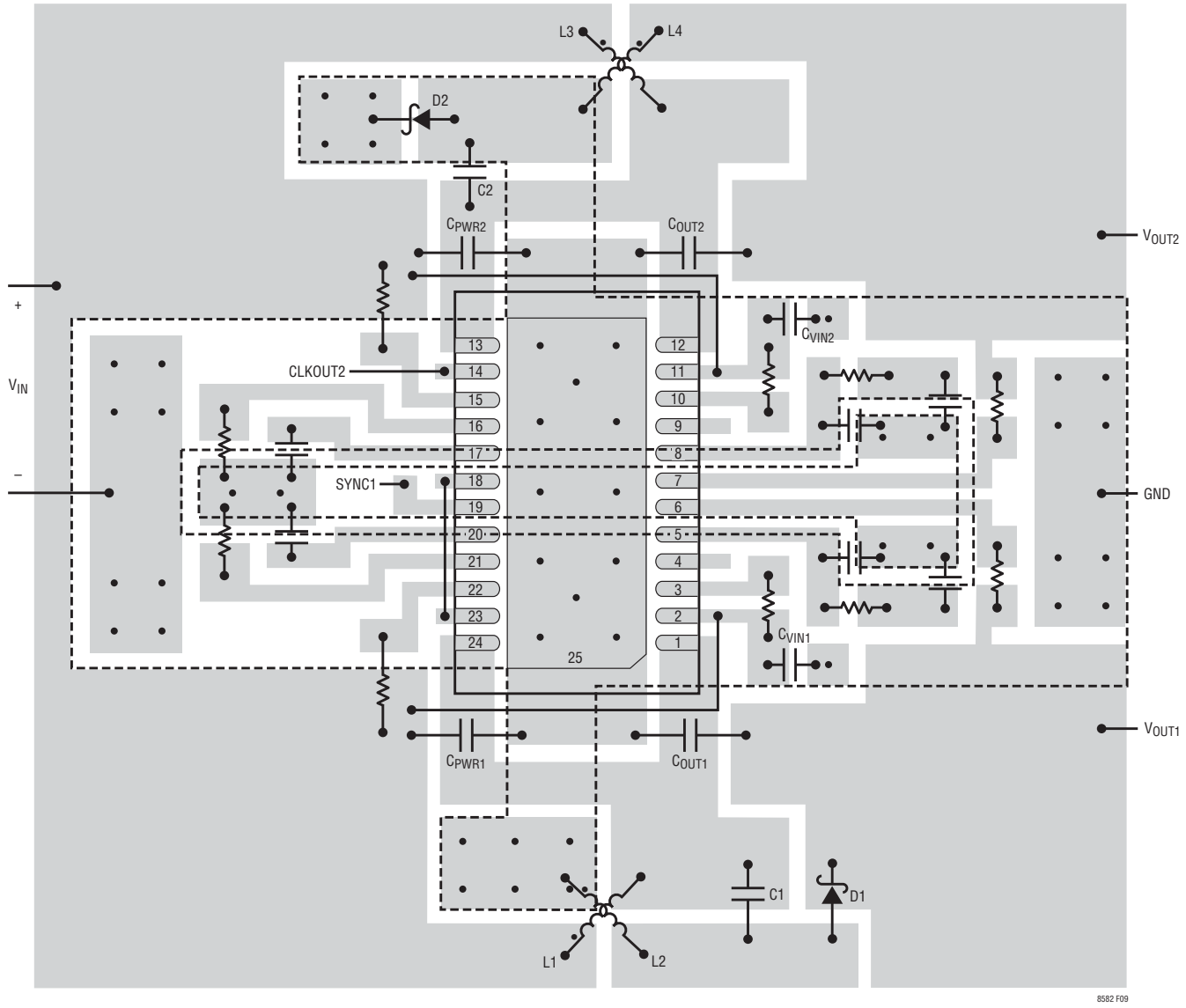


Figure 9. Suggested Component Placement for SEPIC and Dual Inductor Inverting Topologies. Note the Separate Ground Return for the R_T, SS, and V_C Components as Well as D2's Cathode

APPLICATIONS INFORMATION

Table 4 calculates the power dissipation of one channel of the LT8582 for a particular boost application (V_{IN} = 5V, V_{OUT} = 12V, I_{OUT} = 0.8A, f_{OSC} = 1.5MHz, V_D = 0.5V, V_{CESAT} = 0.270V).

From P_{TOTAL} in Table 4, die junction temperature can be calculated using the appropriate thermal resistance number and worst-case ambient temperature:

$$T_J = T_A + \theta_{JA} \bullet P_{TOTAL}$$

where T_J = die junction temperature, T_A = ambient temperature and θ_{JA} is the thermal resistance from the silicon junction to the ambient air.

The published θ_{JA} value is 34°C/W for the 7mm × 4mm 24-pin DFN package package. In practice, lower θ_{JA} values are realizable if board layout is performed with appropriate grounding (accounting for heat sinking properties of the board) and other considerations listed in the Board Layout Guidelines section. For instance, a θ_{JA} value of ~16°C/W was consistently achieved for DFN packages of the LT8582 (at V_{IN} = 5V, V_{OUT} = 12V, I_{OUT} = 0.8A, f_{OSC} = 1.5MHz) when board layout was optimized as per the suggestions in the Board Layout Guidelines section.

Junction Temperature Measurement

The duty cycle of CLKOUT2 is linearly proportional to die junction temperature (T_J) near the CLKOUT2 pin. To get an accurate reading, measure the duty cycle of the CLKOUT signal and use the following equation to approximate the junction temperature:

$$T_J = \frac{DC_{CLKOUT} - 34.5\%}{0.3\%}$$

where DC_{CLKOUT} is the CLKOUT duty cycle in % and T_J is the die junction temperature in °C. Although the absolute die temperature can deviate from the above equation by ±10°C, the relationship between the CLKOUT duty cycle and change in die temperature is well defined. A 3% increase in CLKOUT duty cycle corresponds to ~10°C increase in die temperature.

Note that the CLKOUT pin is only meant to drive capacitive loads up to 120pF.

Thermal Lockout

When the die temperature exceeds 165°C (see Operation Section), a fault condition occurs and the part goes into thermal lockout. The fault condition ceases when the die temperature drops to ~160°C (nominal).

Table 4. Calculations Example with V_{IN} = 5V, V_{OUT} = 12V, I_{OUT} = 0.8A, f_{OSC} = 1.5MHz, V_D = 0.5V, V_{CESAT} = 0.27V

DEFINITION OF VARIABLES	EQUATION	DESIGN EXAMPLE	VALUE
DC = Switch Duty Cycle	$DC = \frac{V_{OUT} - V_{IN} + V_D}{V_{OUT} + V_D - V_{CESAT}}$	$DC = \frac{12V - 5V + 0.5V}{12V + 0.5V - 0.270V}$	DC = 61.3%
I_{IN} = Average Input Current η = Power Conversion Efficiency (typically 88% at high currents)	$I_{IN} = \frac{V_{OUT} \bullet I_{OUT}}{V_{IN} \bullet \eta}$	$I_{IN} = \frac{12V \bullet 0.8A}{5V \bullet 0.88}$	I_{IN} = 2.18A
P_{SW} = Switch I^2R Loss R_{SW} = Switch Resistance (typically 95mΩ combined SWA and SWB)	$P_{SW} = DC \bullet I_{IN}^2 \bullet R_{SW}$	$P_{SW} = 0.613 \bullet (2.18A)^2 \bullet 95m\Omega$	P_{SW} = 277mW
P_{BAC} = Base Drive Loss (AC)	$P_{BAC} = 13ns \bullet I_{IN} \bullet V_{OUT} \bullet f_{OSC}$	$P_{BAC} = 13ns \bullet 2.18A \bullet 12V \bullet 1.5MHz$	P_{BAC} = 511mW
P_{BDC} = Base Drive Loss (DC)	$P_{BDC} = \frac{V_{IN} \bullet I_{IN} \bullet DC}{\beta_{SW\_at\_I_{IN}}}$	$P_{BDC} = \frac{5V \bullet 2.18A \bullet 0.613}{50}$	P_{BDC} = 134mW
P_{INP} = Chip Bias Loss	$P_{INP} = 11mA \bullet V_{IN}$	$P_{INP} = 11mA \bullet 5V$	P_{INP} = 55mW
			P_{TOTAL} = 977mW

Note: These power calculations are for one channel of the LT8582. The power consumption of both channels should be taken into account when calculating die temperature.

APPLICATIONS INFORMATION

SWITCHING FREQUENCY

There are several considerations in selecting the operating frequency of the converter. The first is staying clear of sensitive frequency bands, which cannot tolerate any spectral noise. For example, in RF communication products with a 455kHz IF, switching above 600kHz is desired. Communication products with sensitivity to 1.1MHz would require to set the switching frequency to 1.5MHz or higher. Also, like any other switching regulator, harmonics of much higher frequency than the switching frequency are also produced. The second consideration is the physical size of the converter. As the operating frequency goes up, the inductor and filter capacitors go down in value and size. The trade-off is efficiency, since the switching losses due to inductor AC loss, NPN base drive (see Thermal Calculations), Schottky diode charge and other capacitive loss terms increase proportionally with frequency.

Oscillator Timing Resistor (R_T)

The operating frequency of the LT8582 can be set by the internal free running oscillator. When the SYNC pin for a channel is driven low (< 0.4V), the oscillator frequency for that channel is set by a resistor from the RT pin to ground. The oscillator frequency is calculated using the following formula:

$$f_{OSC} = \frac{81.6}{R_T + 1}$$

where f_{OSC} is in MHz and R_T is in kΩ. Conversely, R_T (in kΩ) can be calculated from the desired frequency (in MHz) using:

$$R_T = \frac{81.6}{f_{OSC}} - 1$$

Clock Synchronization

The operating frequency of each channel of the LT8582 can be set by an external source by simply providing a clock into the SYNC pin for that channel (R_T resistor still required). The LT8582 will revert to its internal free running oscillator clock (set by the R_T resistor) when the SYNC pin is driven below 400mV for several free running clock periods.

Driving the SYNC pin of a channel high for an extended period of time effectively stops the oscillator for that channel. As a result, the switching operation for that channel of the LT8582 will stop and the CLKOUT pin of that channel will be pulled low.

The duty cycle of the SYNC signal must be between 20% and 80% for proper operation. Also, the frequency of the SYNC signal must meet the following two criteria:

(1) SYNC may not toggle outside the frequency range of 200kHz to 2.5MHz.

(2) The SYNC frequency can be higher than the free running oscillator frequency (as set by the R_T resistor), f_{OSC}, but should not be less than 25% below f_{OSC}.

Clock Synchronization of Additional Regulators

The CLKOUT pins of the LT8582 can be used to synchronize additional switching regulators or other channels of LT8582s, as shown in the Typical Application figure on the front page.

The frequency of channel 1 of the LT8582 is set by the external R_T resistor. The SYNC pin of channel 2 of the LT8582 is driven by the CLKOUT pin of channel 1 of the LT8582. Channel 1's CLKOUT pin has a 50% duty cycle intended for driving SYNC2 and is 180° out of phase for reduced input ripple or multiphase topologies.

Note that the RT pin of channel 2 of the LT8582 must have a resistor tied to ground. It takes a few clock cycles for the CLKOUT signal to begin oscillating and it is preferable for all LT8582 channels to have the same internal free running frequency. Therefore, in general, use the same value R_T resistor for all of the synchronized LT8582s.

EVENT BASED SEQUENCING

The PG pin may be used to sequence other ICs since it is pulled low as long as the LT8582 is enabled and the magnitude of the output voltage is below regulation (refer to the Block Diagram). Since the PG pin is an open drain output, it can be used to pull the $\overline{SHDN}$ pin of another IC low until the output of one of the channels of the LT8582

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is close to its regulation voltage. This method allows the PG pin to disable multiple ICs. Refer to Figure 10 for the necessary connections. Alternatively, the PG pin may be used to pull the SS pin of another switching regulator low, preventing the other regulator from switching.

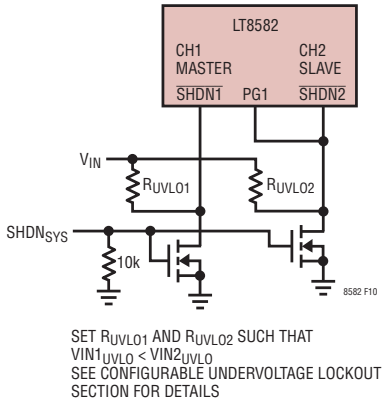

Figure 10. Using the Two LT8582 Channels, with Power Supply Sequencing

CHARGE PUMP AIDED REGULATORS

Designing charge pumps with the LT8582 can offer efficient solutions with fewer components than traditional circuits because of the master/slave switch configuration on the IC. Although the slave switch, SWB, operates in phase with the master switch, SWA, only the current through the master switch (SWA) is sensed by the current comparator (A4 in the Block Diagram). This method of operation by the master/slave switches can offer the following benefits to charge pump designs:

- The slave switch, by not performing a current sense operation like the master switch, can sustain fairly large current spikes without falsely tripping the current comparator. In a charge pump, these spikes occur when the flying capacitors charge up. Since this current spike flows through SWB, it does not affect the operation of the current comparator (A4 in the Block Diagram).
- The master switch, immune from the flying capacitor current spike (seen only by the slave switch), can therefore sense the inductor current more accurately.
- Since the slave switch can sustain large current spikes, the diodes that feed current into the flying capacitors do not need current limiting resistors, leading to efficiency and thermal improvements, as well as a smaller solution size.

High V_{OUT} Charge Pump Topology

The LT8582 can be used in a charge pump topology as shown in Figure 11, multiplying the output of a boost converter. The master switch (SWA) can be used to drive the boost converter, while the slave switch (SWB) can be used to drive one or more charge pump stages. This topology is useful for high voltage applications including VFD bias supplies.

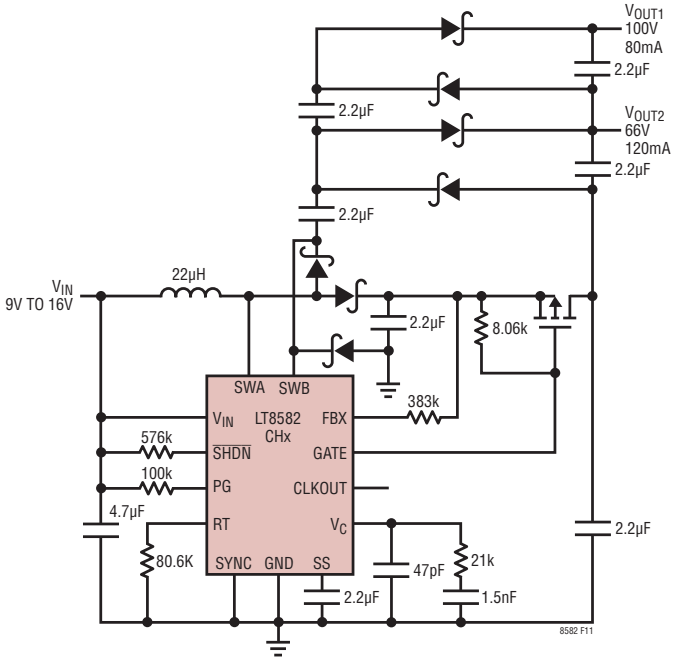

Figure 11. High V_{OUT} Charge Pump Topology

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Single Inductor Inverting Topology

If there is a need to use just one inductor to generate a negative output voltage whose magnitude is greater than V_{IN}, the single inductor inverting topology (shown in Figure 12) can be used. Since the master and slave switches are isolated by a Schottky diode, the current spike through C1 will flow only through the slave switch, preventing the current comparator, (A4 in the Block Diagram) from false tripping. Output disconnect is inherently built into the single inductor topology.

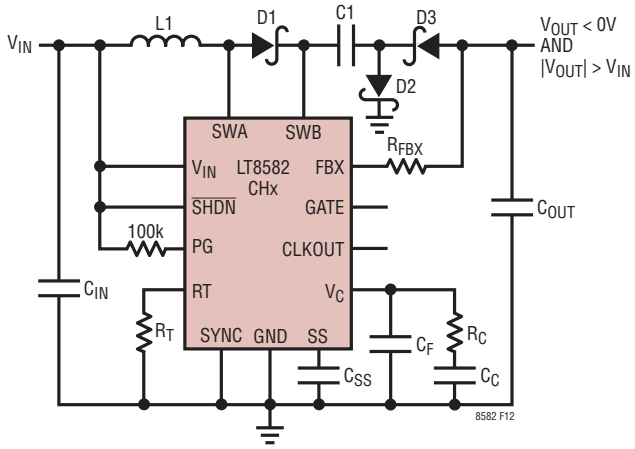

Figure 12. Single Inductor Inverting Topology

HOT-PLUG

High inrush currents associated with hot-plugging V_{IN} can largely be rejected with the use of an external PMOS. A simple hot-plug controller can be designed by connecting an external PMOS in series with V_{IN}, with the gate of the PMOS being driven by the GATE pin of the LT8582. The GATE pin pull-down current is linearly proportional to the SS voltage. Since the SS charge up time is relatively slow, the GATE pin pull-down current will increase gradually, thereby turning on the external PMOS slowly. Controlled in this manner, the PMOS acts as an input current limiter when V_{IN} hot-plugs or ramps up sharply.

Likewise, when the PMOS is connected in series with the output, inrush current into the output capacitor can be limited during a hot-plug event. To illustrate this, the circuit in Figure 5 was reconfigured by adding a large 1500µF capacitor to the output. An 18Ω resistive load was used and C_{SS} was increased to 10µF. Figure 13 shows the results of hot-plugging this reconfigured circuit. Notice how the inductor current is well behaved.

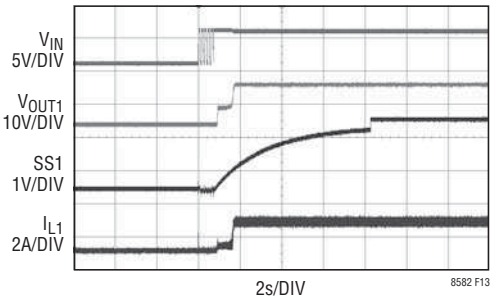

Figure 13. V_{IN} Hot-Plug Control. Inrush Current Is Well Controlled

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INDEPENDENT CHANNELS

Either channel may be used independently of the other channel. To disable one channel, drive $\overline{SHDN}$ of that channel low. Activating or deactivating one channel will not alter the functionality of the other channel.

SETTING THE OUTPUT VOLTAGE

The output voltage is set by connecting a resistor (R_{FBX}) from V_{OUT} to the FBX pin. R_{FBX} is determined by using the following equation:

$$R_{FBX} = \frac{|V_{OUT} - V_{FBX}|}{83.3\mu A}$$

where V_{FBX} is 1.204V (typical) for noninverting topologies (i.e. boost and SEPIC regulators) and 7mV (typical) for inverting topologies (see the Electrical Characteristics).

POWER SWITCH DUTY CYCLE

In order to maintain loop stability and deliver adequate current to the load, the power NPNs (Q1 and Q2 in the Block Diagram) cannot remain on for 100% of each clock cycle. The maximum allowable duty cycle is given by:

$$DC_{MAX} = \frac{(T_P - MinOffTime)}{T_P} \bullet 100\%$$

where T_P is the clock period and MinOffTime (found in the Electrical Characteristics) is typically 45ns.

Conversely, the power NPNs (Q1 and Q2 in the Block Diagram) cannot remain off for 100% of each clock cycle and will turn on for a minimum on time (MinOnTime) when in regulation. This MinOnTime governs the minimum allowable duty cycle given by:

$$DC_{MIN} = \frac{MinOnTime}{T_P} \bullet 100\%$$

Where T_P is the clock period and MinOnTime (found in the Electrical Characteristics) is typically 55ns.

The application should be designed such that the operating duty cycle is between DC_{MIN} and DC_{MAX}.

Duty cycle equations for several common topologies are given below where V_D is the diode forward voltage drop and V_{CESAT} is the collector to emitter saturation voltage of the switch. V_{CESAT}, with SWA and SWB tied together, is typically 270mV when the combined switch current (I_{SWA} + I_{SWB}) is 2.75A.

For the boost topology (see Figure 5):

$$DC_{BOOST} \cong \frac{V_{OUT} - V_{IN} + V_D}{V_{OUT} + V_D - V_{CESAT}}$$

For the SEPIC or dual inductor inverting topology (see Figure 6 and Figure 7):

$$DC_{SEPIC\_\&\_INVERT} \cong \frac{|V_{OUT}| + V_D}{V_{IN} + |V_{OUT}| + V_D - V_{CESAT}}$$

For the single inductor inverting topology (see Figure 12):

$$DC_{SI\_INVERT} \cong \frac{|V_{OUT}| - V_{IN} + V_{CESAT} + 3 \bullet V_D}{|V_{OUT}| + 3 \bullet V_D}$$

The LT8582 can be used in configurations where the duty cycle is higher than DC_{MAX}, but it must be operated in the discontinuous conduction mode so that the effective duty cycle is reduced.

INDUCTOR SELECTION

General Guidelines

The high frequency operation of the LT8582 allows for the use of small surface mount inductors. For high efficiency, choose inductors with high frequency core material, such as ferrite, to reduce core losses. Also to improve efficiency, choose inductors with more volume for a given inductance. The inductor should have low DCR (copper-wire resistance) to reduce I^2R losses and must be able to handle the peak inductor current without saturating. Note that in some applications, the current handling requirements of the inductor can be lower, such as in the SEPIC topology where each inductor only carries one half of the total switch current. Multilayer chip inductors usually do not have enough core volume to support peak inductor currents in the 2A to 6A range. To minimize radiated noise,

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use a toroidal or shielded inductor. See Table 5 for a list of inductor manufacturers.

Table 5. Inductor Manufacturers

Coilcraft	MSD7342 XAL6060 Series	www.coilcraft.com
Vishay	IHLP-2020BZ-01 IHLP-2525CZ-01 Series	www.vishay.com
WÜRTH	WE-PD WE-DD WE-TDC Series	www.we-online.com
Cooper Bussman	Octa-Pac Plus DRQ-125 DRQ-74 Series	www.cooperbussmann.com
Sumida	CDR6D28MN CDR7D28MN Series	www.sumida.com
Taiyo Yuden	NR Series	www.t-yuden.com
TDK	VLF, SLF, RLF Series	www.tdk.com

Minimum Inductance

Although there can be a trade-off with efficiency, it is often desirable to minimize board space by choosing smaller inductors. When choosing an inductor, there are three conditions that limit the minimum inductance: (1) providing adequate load current, (2) avoiding subharmonic oscillation and (3) supplying a minimum ripple current to avoid false tripping of the current comparator.

Adequate Load Current

Small value inductors result in increased ripple currents and thus, due to the limited peak switch current, decrease the average current that can be provided to the load. In order to provide adequate load current, L should be at least:

$$L_{BOOST} > \frac{DC \bullet (V_{IN} - V_{CESAT})}{2 \bullet f_{OSC} \bullet \left(I_{PK} - \frac{V_{OUT} \bullet I_{OUT}}{V_{IN} \bullet \eta} \right)} \quad \text{Boost Topology}$$

or

$$L_{DUAL} > \frac{DC \bullet (V_{IN} - V_{CESAT})}{2 \bullet f_{OSC} \bullet \left(I_{PK} - \frac{|V_{OUT}| \bullet I_{OUT}}{V_{IN} \bullet \eta} - I_{OUT} \right)} \quad \text{SEPIC or Inverting Topologies}$$

where

L_{BOOST} = L1 for boost topologies (see Figure 5)

L_{DUAL} = L1 = L2 for coupled dual inductor topologies (see Figures 6 and 7)

L_{DUAL} = L1 || L2 for uncoupled dual inductor topologies (see Figures 6 and 7)

DC = Switch duty cycle (see Power Switch Duty Cycle section in Appendix)

I_{PK} = Maximum Peak Switch Current; should not exceed 3A for a combined SWA + SWB current, or 1.7A if only SWA is being used.

η = Power conversion efficiency (typically 88% for boost and 82% for dual inductor topologies at high currents)

f_{OSC} = Switching frequency

I_{OUT} = Maximum load current

Negative values of L_{BOOST} or L_{DUAL} indicate that the output load current I_{OUT} exceeds the switch current limit capability of the LT8582.

Avoiding Subharmonic Oscillations

Subharmonic oscillations can occur when the duty cycle is greater than 50%. The LT8582's internal slope compensation circuit will avoid this, provided that the inductance exceeds a certain minimum value. In applications that operate with duty cycles greater than 50%, the inductance must be at least:

$$L_{MIN} > \frac{(V_{IN} - V_{CESAT}) \bullet (2 \bullet DC - 1)}{1.7A \bullet f_{OSC} \bullet (1 - DC)}$$

where

L_{MIN} = L1 for boost topologies (see Figure 5)

L_{MIN} = L1 = L2 for coupled dual inductor topologies (see Figures 6 and 7)

L_{MIN} = L1 || L2 for uncoupled dual inductor topologies (see Figures 6 and 7)

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Maximum Inductance

Excessive inductance can reduce current ripple to levels that are difficult for the current comparator (A4 in the Block Diagram) to easily distinguish the peak current. This causes duty cycle jitter and/or poor regulation. The maximum inductance can be calculated by:

$$L_{MAX} = \frac{V_{IN} - V_{CESAT}}{180mA} \bullet \frac{DC}{f_{OSC}}$$

where

L_{MAX} = L1 for boost topologies (see Figure 5)

L_{MAX} = L1 = L2 for coupled dual inductor topologies (see Figures 6 and 7)

L_{MAX} = L1 || L2 for uncoupled dual inductor topologies (see Figures 6 and 7)

Inductor Current Rating

Inductors must have a rating greater than their peak operating current to prevent saturation, which results in efficiency losses. The maximum inductor current (considering start-up, transient, and steady-state conditions) is given by:

$$I_{L\_PEAK} = I_{LIM} + \frac{V_{IN} \bullet T_{MIN\_PROP}}{L}$$

where

I_{L_PEAK} = Peak of Inductor Current in L1 for boost topology, or peak of the sum of inductor currents in L1 and L2 for dual inductor topologies.

I_{LIM} = For hard saturation inductors, 5.4A when SWA and SWB are tied together, or 3A when only SWA is being used. For soft saturation inductors, 3.3A when SWA and SWB are tied together, or 1.8A when only SWA is being used.

T_{MIN_PROP} = 55ns (propagation delay through the current feedback loop)

Note that these equations offer conservative results for the required inductor current ratings. The current ratings could be lower for applications with light loads and small transients if the SS capacitor is sized appropriately to limit inductor currents at start-up.

DIODE SELECTION

Schottky diodes, with their low forward voltage drops and fast switching speeds, are recommended for use with the LT8582. Choose a Schottky diode with low parasitic capacitance to reduce reverse current spikes through the power switch of the LT8582. The Diodes Inc. PD3S230H diode is a very good choice with a 30V reverse voltage rating and an average forward current of 2A.

OUTPUT CAPACITOR SELECTION

Low ESR (equivalent series resistance) capacitors should be used at the output to minimize the output ripple voltage. Multilayer ceramic capacitors are an excellent choice, as they have an extremely low ESR and are available in very small packages. X5R or X7R types are preferred, as these retain their capacitance over wide voltage and temperature ranges. A 10µF to 22µF output capacitor is sufficient for most applications, but systems with very low output currents may need only 2.2µF to 10µF. Always use a capacitor with a sufficient voltage rating. Many ceramic capacitors, particularly 0805 or 0603 case sizes, have greatly reduced capacitance at the desired output voltage. Tantalum polymer or OS-CON capacitors can be used, but it is likely that these capacitors will occupy more board area than ceramics and will have a higher ESR with greater output ripple.

INPUT CAPACITOR SELECTION

Ceramic capacitors make a good choice for the input bypass capacitor and should be placed as close as possible to the V_{IN} pin of the chip as well as to the inductor connected to the input of the power path. If it is not possible to optimally place a single input capacitor, then use two separate capacitors—use one at the V_{IN} pin of the chip (see the equation for C_{VIN} in Table 1, Table 2 and Table 3)

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and one at the input to the power path (see the equation for C_{PWR} in Table 1, Table 2 and Table 3). A 4.7µF to 20µF input capacitor is sufficient for most applications.

Table 6 shows a list of several ceramic capacitor manufacturers. Consult the manufacturers for detailed information on their entire selection of ceramic parts.

Table 6. Ceramic Capacitor Manufacturers

TDK	www.tdk.com
Murata	www.murata.com
Taiyo Yuden	www.t-yuden.com
Kemet	www.kemet.com

PMOS SELECTION

An external PMOS, controlled by the LT8582's GATE pin, can be used to facilitate input or output disconnect. The GATE pin turns on the PMOS gradually during start-up (see soft-start of external PMOS in the Operation section) and turns the PMOS off when the LT8582 is in shutdown or in fault.

The use of the external PMOS, controlled by the GATE pin, is particularly beneficial when dealing with unintended output shorts in a boost regulator. In a conventional boost regulator, the inductor, Schottky diode and power switches are susceptible to damage in the event of an output short. Using an external PMOS in the boost regulator's power path (path from V_{IN} to V_{OUT}) controlled by the GATE pin, will serve to disconnect the input from the output when the output has a short. This helps to save the chip and the other components in the power path from damage. Ensure that both the diode and the inductor can survive low duty cycle current pulses of 5 to 6 times their steady state levels.

The PMOS chosen must be capable of handling the maximum input or output current depending on whether it is used at the input or the output (see Figure 5).

Ensure that the PMOS is biased with enough source to gate voltage (V_{SG}) to enhance the device into the triode mode of operation. The higher the V_{SG} voltage that biases the PMOS into triode, the lower the R_{DSON} of the PMOS, thereby lowering power dissipation in the device during normal operation, as well as improving the efficiency of the application. The following equations show the relationship between R_{GATE} (see Block Diagram) and the desired V_{SG} that the PMOS is biased with, where V_S is the PMOS source voltage:

$$V_{SG} = \begin{cases} V_S \dfrac{R_{GATE}}{R_{GATE} + 2k\Omega} \text{ if } V_{GATE} < 2V \\ 1mA \bullet R_{GATE} \text{ if } V_{GATE} \geq 2V \end{cases}$$

When using a PMOS, it is advisable to configure the specific application for undervoltage lockout (see the Operations section). The goal is to have V_{IN} get to a certain minimum voltage where the PMOS has sufficient V_{SG}.

Figure 5 shows the PMOS connected in series with the output to act as an output disconnect during a fault condition. Using a PMOS with a high V_T (~2V) can help to reduce extraneous current spikes during hot-plug. The resistor divider from V_{IN} to the $\overline{SHDN}$ pin sets UVLO at 4V for this application.

Connecting the PMOS in series with the output offers certain advantages over connecting it in series with the input:

- Since the load current is always less than the input current for a boost converter, the current rating of the PMOS will be reduced.
- A PMOS in series with the output can be biased with a higher overdrive voltage than a PMOS used in series with the input, since $V_{OUT} > V_{IN}$. This higher overdrive results in a lower R_{DSON} rating for the PMOS, thereby improving the efficiency of the regulator.

In contrast, an input connected PMOS works as a simple hot-plug controller (covered in more detail in the Hot-Plug section). The input connected PMOS also functions as an inexpensive means of protecting against multiple output shorts in boost applications that synchronize the LT8582 with other compatible chips.

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Table 7 shows a list of several discrete PMOS manufacturers. Consult the manufacturers for detailed information on their entire selection of PMOSs.

Table 7. Discrete PMOS Manufacturers

Vishay	www.vishay.com
ON Semiconductor	www.onsemi.com
Fairchild Semiconductor	www.fairchildsemi.com
Diodes Incorporated	www.diodes.com

COMPENSATION – ADJUSTMENT

To compensate the feedback loop of the LT8582, a series resistor capacitor network in parallel with an optional single capacitor should be connected from the V_C pin to GND. For most applications, choose a series capacitor in the range of 1nF to 10nF with 2.2nF being a good starting value. The optional parallel capacitor should range in value from 22pF to 220pF with 47pF being a good starting value. The compensation resistor, R_C, is usually in the range of 5k to 50k with 10k being a good starting value. A good technique to compensate a new application is to use a 100k potentiometer in place of the series resistor R_C. With the series and parallel capacitors at 4.7nF and 47pF respectively, adjust the potentiometer while observing the transient response and the optimum value for R_C can be found. Figures 14a to Figure 14c illustrate this process for the circuit of Figure 17 with a load current stepped between 300mA and 800mA. Figure 14a shows the transient response with R_C equal to 1k. The phase margin is poor as evidenced by the excessive ringing in the output voltage and inductor current. In Figure 14b, the value of R_C is increased to 3.15k, which results in a more damped response. Figure 14c shows the results when R_C is increased further to 6.49k. The transient response is nicely damped and the compensation procedure is complete.

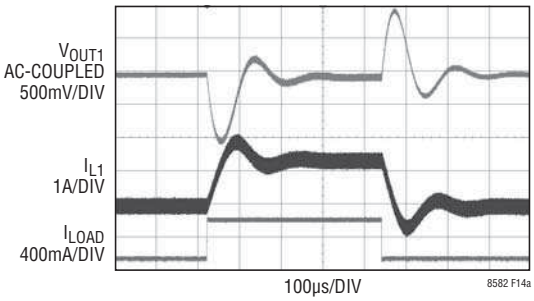

Figure 14a. Transient Response Shows Excessive Ringing

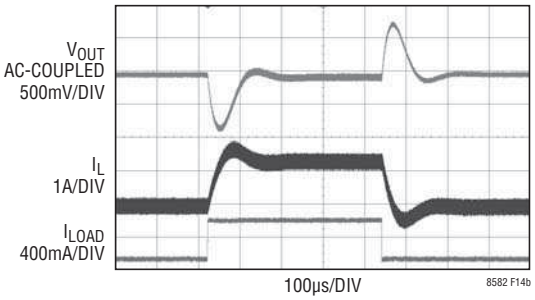

Figure 14b. Transient Response Is Better

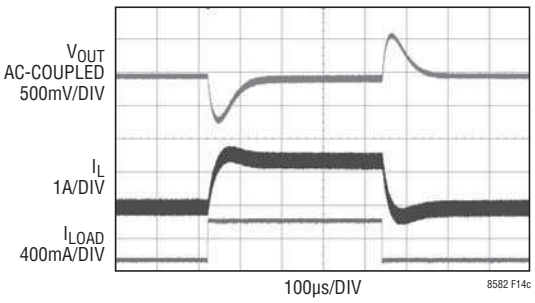

Figure 14c. Transient Response Is Well Damped

Compensation – Theory

Like all other current mode switching regulators, the LT8582 needs to be compensated for stable and efficient operation. Two feedback loops are used in the LT8582: a fast current loop which does not require compensation and a slower voltage loop which does. Standard bode plot analysis can be used to understand and adjust the voltage feedback loop.

As with any feedback loop, identifying the gain and phase contribution of the various elements in the loop is critical. Figure 15 shows the key equivalent elements of a boost converter. Because of the fast current control loop, the power stage of the chip, inductor and diode have been replaced by a combination of the equivalent transconductance amplifier g_{mp} and the current controlled current source (which converts I_{VIN} to $(\eta V_{IN}/V_{OUT}) \bullet I_{VIN}$). g_{mp} acts as a current source where the peak input current, I_{VIN}, is proportional to the V_C voltage. η is the efficiency of the switching regulator and is typically about 88% at higher currents.

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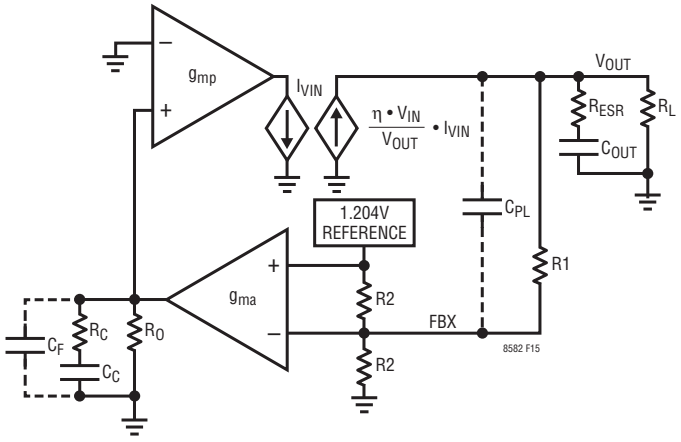

C_C: COMPENSATION CAPACITOR
C_{OUT}: OUTPUT CAPACITOR
C_{PL}: PHASE LEAD CAPACITOR
C_F: HIGH FREQUENCY FILTER CAPACITOR
g_{ma}: TRANSCONDUCTOR ERROR AMPLIFIER INSIDE THE CHIP
g_{mp}: POWER STAGE TRANSCONDUCTANCE AMPLIFIER
R_C: COMPENSATION RESISTOR
R_L: OUTPUT RESISTANCE DEFINED AS $V_{OUT}/I_{LOADMAX}$
R_O: OUTPUT RESISTANCE OF gma
R1, R2: OUTPUT VOLTAGE FEEDBACK RESISTOR DIVIDER
R_{ESR}: OUTPUT CAPACITOR ESR
η: CONVERTER EFFICIENCY (~88% AT HIGHER CURRRENTS)

Figure 15. Boost Converter Equivalent Model

Note that the maximum output currents of g_{mp} and g_{ma} are finite. The output current of the g_{mp} stage is limited by the minimum switch current limit (see the Electrical Specifications) and the output of the g_{ma} stage is nominally limited to about ±12µA.

From Figure 15, the DC gain, poles and zeros can be calculated as follows:

DC GAIN:

$$A_{DC} = (g_{ma} \bullet R_O) \bullet g_{mp} \bullet \left(\eta \bullet \frac{V_{IN}}{V_{OUT}} \bullet \frac{R_L}{2}\right) \bullet \frac{0.5R_2}{R_1 + 0.5R_2}$$

Output Pole:

$$P_1 = \frac{2}{2 \bullet \pi \bullet R_L + C_{OUT}}$$

Error Amp Pole:

$$P2 = \frac{1}{2 \bullet \pi \bullet (R_O + R_C) C_C}$$

Error Amp Zero:

$$Z1 = \frac{1}{2 \bullet \pi \bullet R_C \bullet C_C}$$

ESR Zero:

$$Z2 = \frac{1}{2 \bullet \pi \bullet R_{ESR} \bullet C_{OUT}}$$

RHP Zero:

$$Z3 = \frac{V_{IN}^2 \bullet R_L}{2 \bullet \pi \bullet V_{OUT}^2 \bullet L}$$

High Frequency Pole:

$$P3 > \frac{f_s}{3}$$

Phase Lead Zero:

$$Z4 = \frac{1}{2 \bullet \pi \bullet R1 \bullet C_{PL}}$$

Phase Lead Pole:

$$P4 = \frac{1}{2 \bullet \pi \frac{0.5 \bullet R_1 \bullet R_2}{R_1 + 0.5R_2} \bullet C_{PL}}$$

Error Amp Filter Pole:

$$P5 = \frac{1}{2 \bullet \pi \bullet \frac{R_C \bullet R_O}{R_C + R_O} \bullet C_F}, C_F < \frac{C_C}{10}$$

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The current mode zero (Z3) is a right half plane zero which can be an issue in feedback control design, but is manageable with proper external component selection.

Using the circuit in Figure 17 as an example, Table 8 shows the parameters used to generate the bode plot shown in Figure 16.

Table 8. Bode Plot Parameters

PARAMETER	VALUE	UNITS	COMMENT
R_L	20	Ω	Application Specific
C_{OUT}	22	µF	Application Specific
R_{ESR}	1	mΩ	Application Specific
R_O	305	kΩ	Not Adjustable
C_C	4700	pF	Adjustable
C_F	47	pF	Optional/Adjustable
C_{PL}	0	pF	Optional/Adjustable
R_C	6.49	kΩ	Adjustable
R1	130	kΩ	Adjustable
R2	14.5	kΩ	Not Adjustable
V_{REF}	1.204	V	Not Adjustable
V_{OUT}	12	V	Application Specific
V_{IN}	5	V	Application Specific
g_{ma}	270	µmho	Not Adjustable
g_{mp}	15.1	mho	Not Adjustable
L	4.7	µH	Application Specific
f_{OSC}	1.5	MHz	Adjustable

From Figure 16, the phase is –130° when the gain reaches 0dB, giving a phase margin of 50°. The crossover frequency is 5kHz, which is many times lower than the frequency of the RHP zero Z3, thus providing for adequate phase margin.

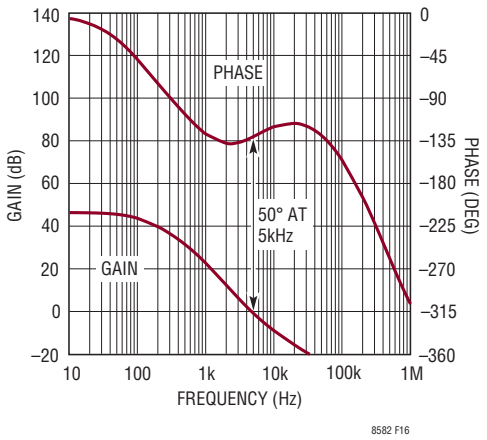


Figure 16. Bode Plot for Example Boost Converter

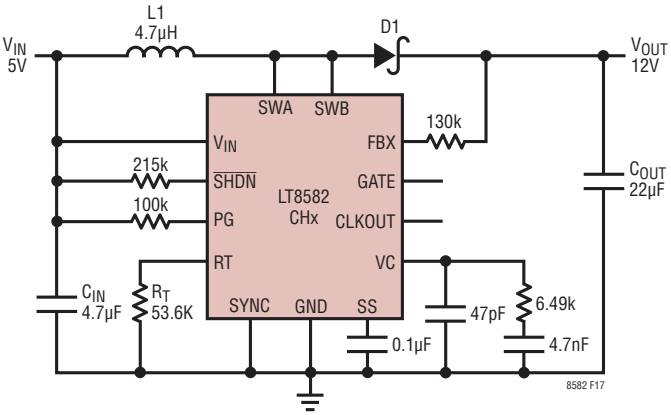
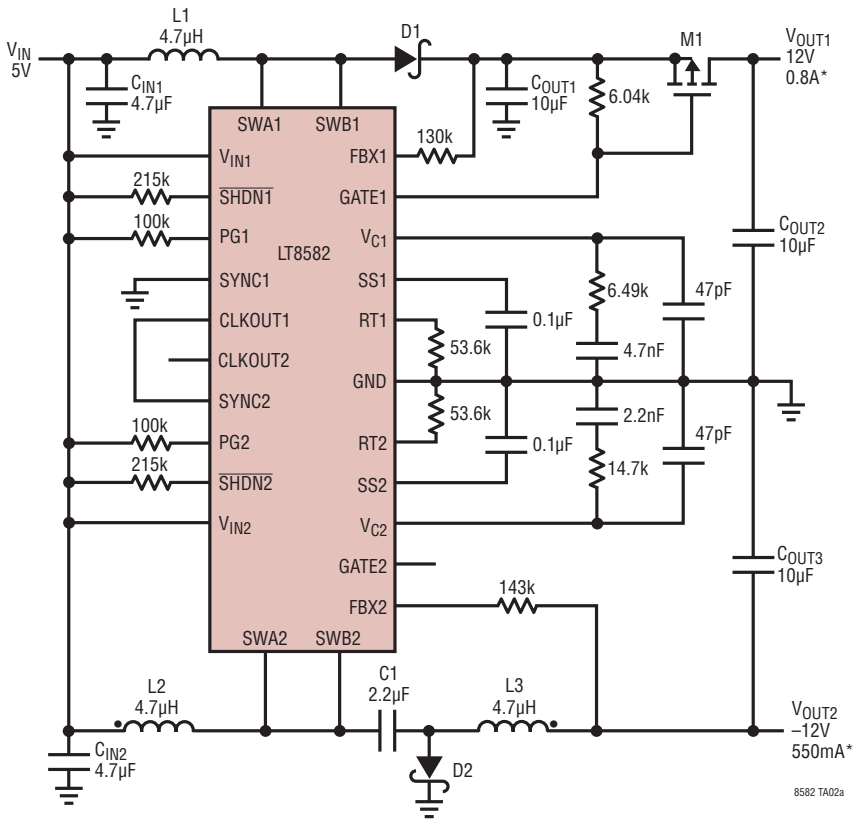


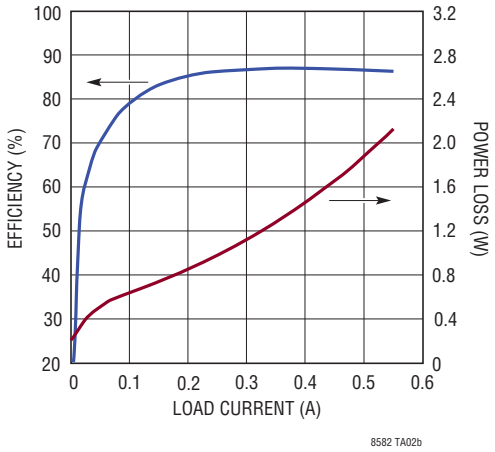
Figure 17. 5V to 12V Boost Converter

TYPICAL APPLICATIONS

1.5MHz, 5V to ±12V Boost and Inverting Converter Can Survive Output Shorts



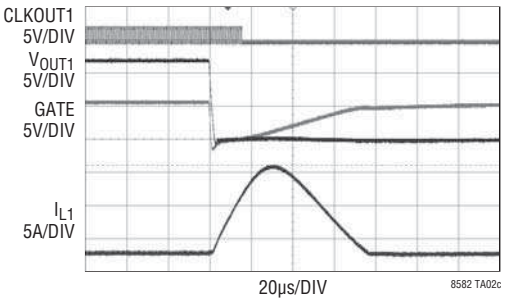
Efficiency and Power Loss (Load Between 12V and –12V Outputs)



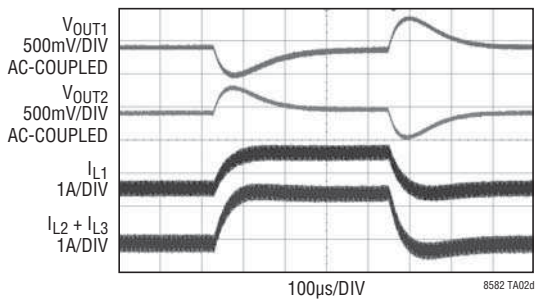
C_{IN1}, C_{IN2}: 4.7µF, 16V, X7R, 1206
C_{OUT1}, C_{OUT2}, C_{OUT3}: 10µF, 25V, X7R, 1206
C1: 2.2µF, 25V, X7R, 1206
D1, D2: DIODES INC. PD3S230H
L1: COILCRAFT XAL6060-472ML
L2, L3: COILCRAFT MSD7342-472
M1: FAIRCHILD FDMC510P

*MAX TOTAL OUTPUT POWER: 14.4W

Output Short from 12V Output to Ground

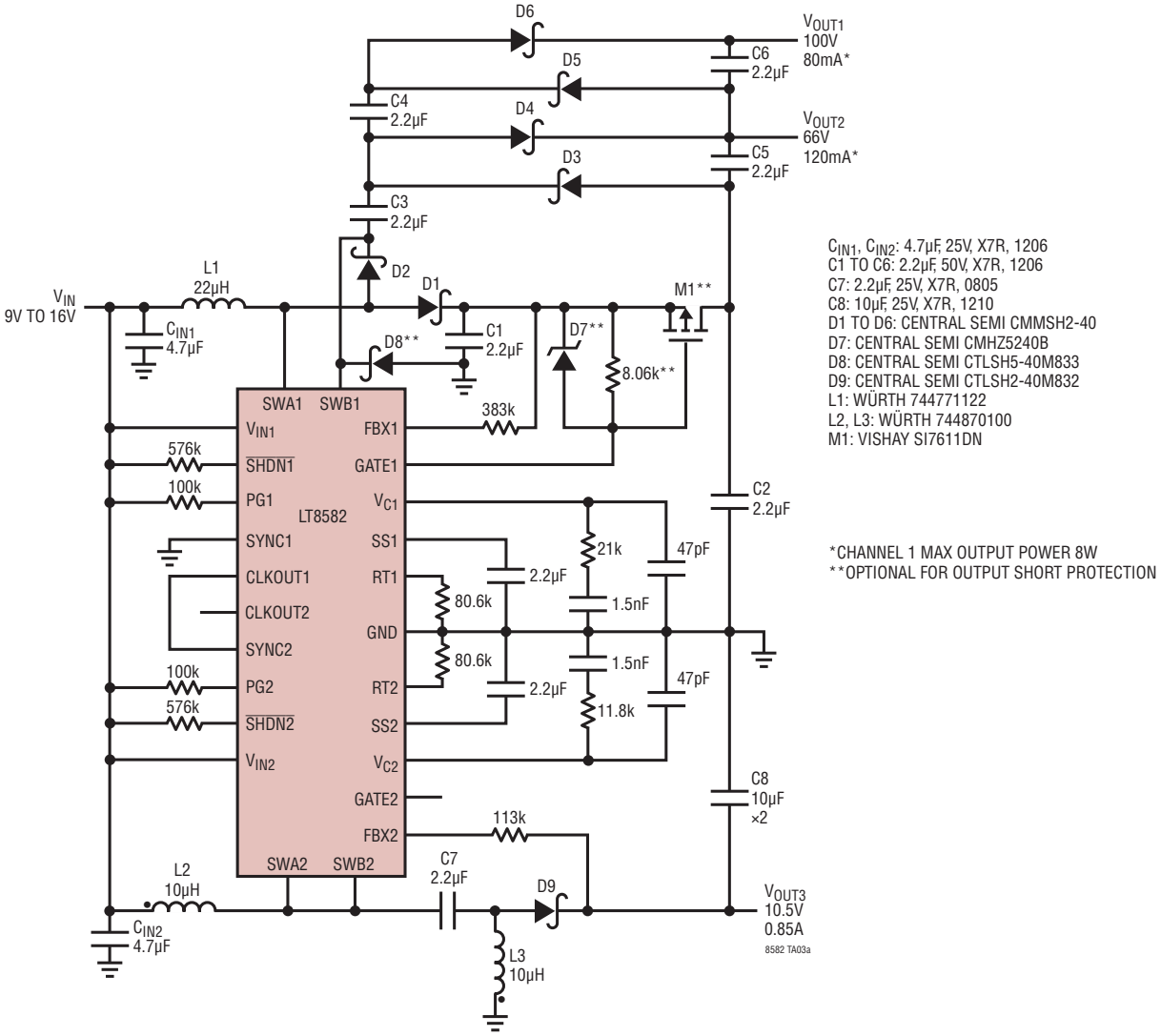


Transient Response with 0.15A to 0.45A to 0.15A Output Load Step Between Rails



TYPICAL APPLICATIONS

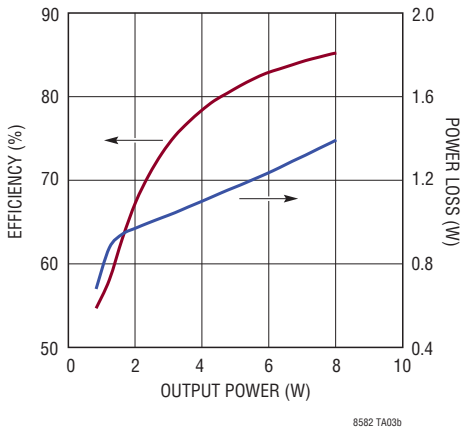
VFD (Vacuum Fluorescent Display) and Filament Power Supply Switches at 1MHz



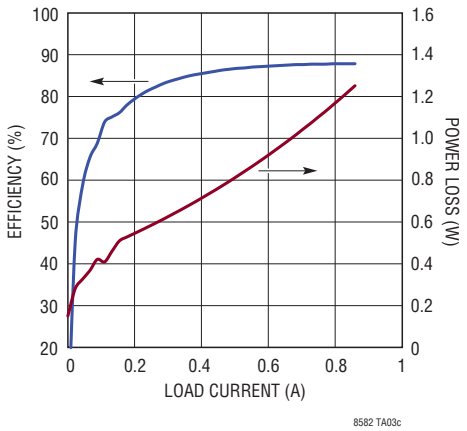
C_{IN1}, C_{IN2}: 4.7µF, 25V, X7R, 1206
C1 TO C6: 2.2µF, 50V, X7R, 1206
C7: 2.2µF, 25V, X7R, 0805
C8: 10µF, 25V, X7R, 1210
D1 TO D6: CENTRAL SEMI CMMSH2-40
D7: CENTRAL SEMI CMHZ5240B
D8: CENTRAL SEMI CTLSH5-40M833
D9: CENTRAL SEMI CTLSH2-40M832
L1: WÜRTH 744771122
L2, L3: WÜRTH 744870100
M1: VISHAY SI7611DN

*CHANNEL 1 MAX OUTPUT POWER 8W
**OPTIONAL FOR OUTPUT SHORT PROTECTION

Efficiency and Power Loss (V_{IN} = 12V with Load on 100V Output)

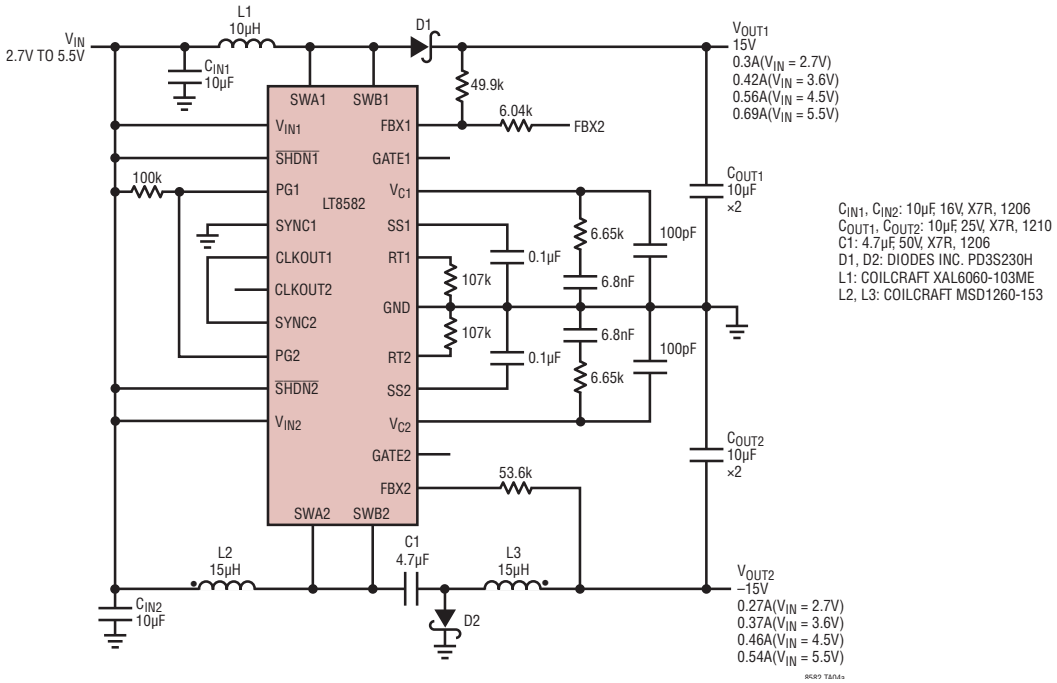


Efficiency and Power Loss (V_{IN} = 12V with Load on 10.5V Output)

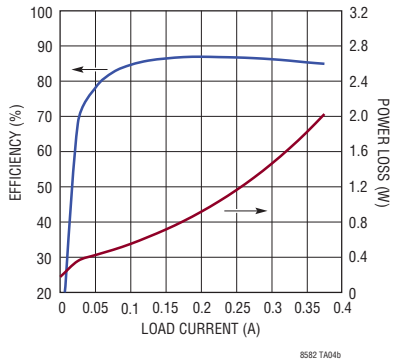


TYPICAL APPLICATIONS

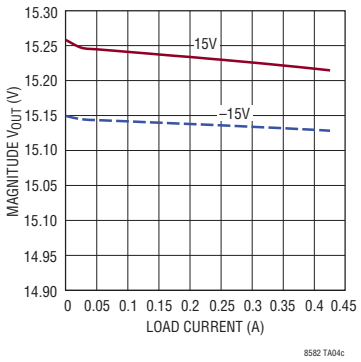
Tracking ±15V Supplies from a 2.7V to 5.5V Input



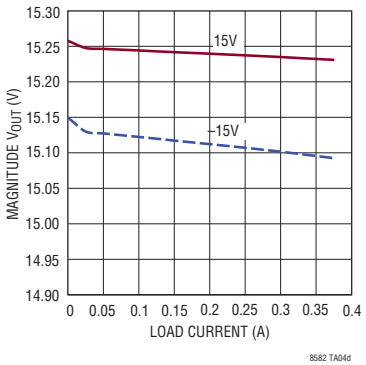
Efficiency and Power Loss (V_{IN} = 3.6V with Load Between 15V and –15V Outputs)



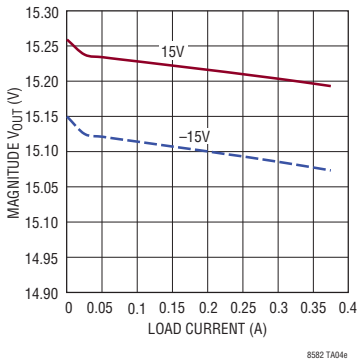
15V and –15V Outputs vs Load Current (V_{IN} = 3.6V, Load on 15V Output)



15V and –15V Outputs vs Load Current (V_{IN} = 3.6V, Load on –15V Output)

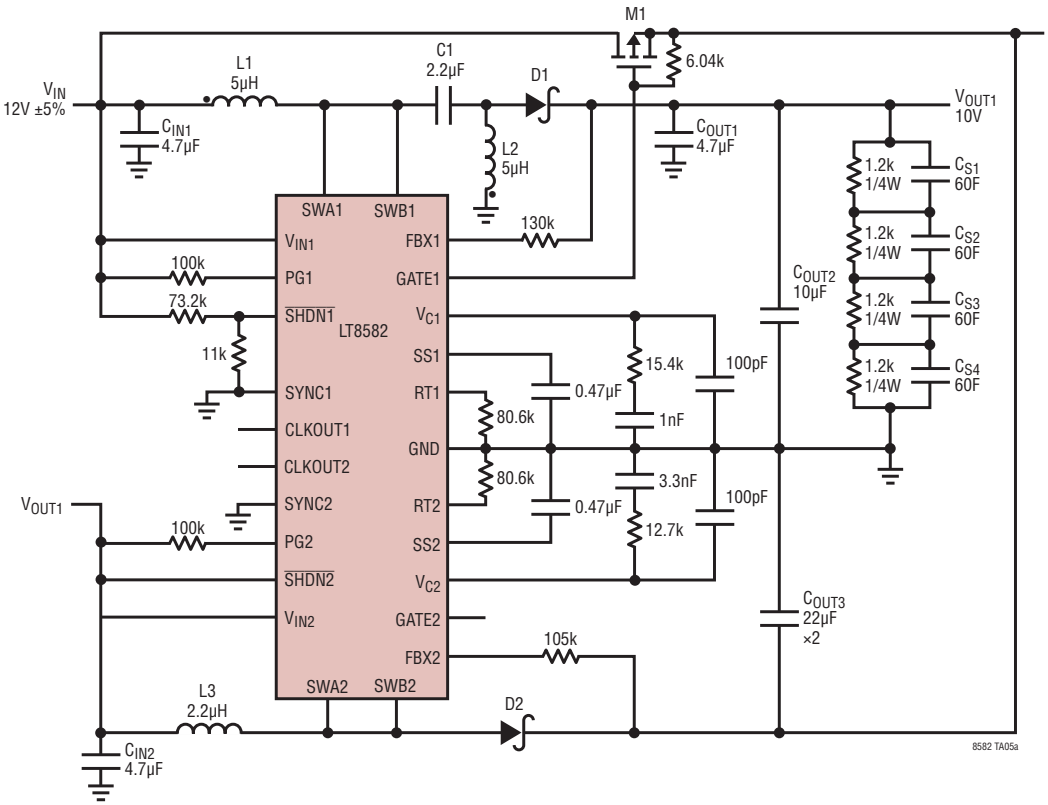


15V and –15V Outputs vs Load Current (V_{IN} = 3.6V, Load Between 15V and –15V Outputs)



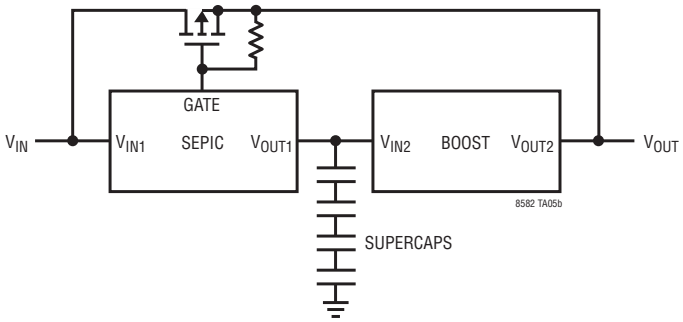
TYPICAL APPLICATIONS

SuperCap Backup Power

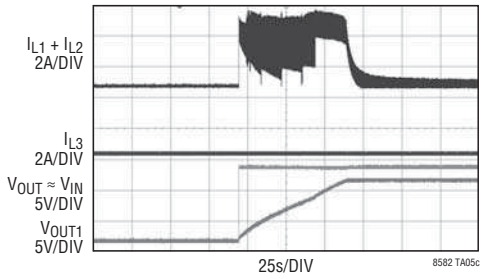


CIN1, CIN2: 4.7µF, 16V, X7R, 1206
COUT1: 4.7µF, 25V, X7R, 1206
COUT2: 10µF, 25V, X7R, 1210
COUT3: 22µF, 16V, X7R, 1210
C1: 2.2µF, 25V, X7R, 0805
CS1 TO CS4: 60F, 2.5V, COOPER HB1840-2R5606-R
D1, D2: CENTRAL SEMI CTLSH5-40M833
L1, L2: COOPER CTX5-1A
L3: COOPER HCM0703-2R2
M1: VISHAY SI7123DN

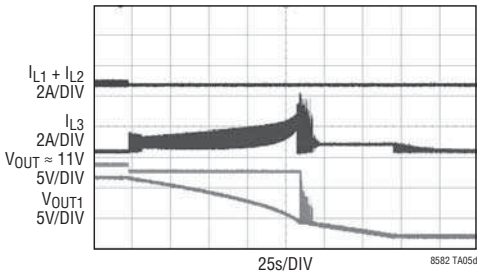
System Level Diagram



Charging SuperCaps

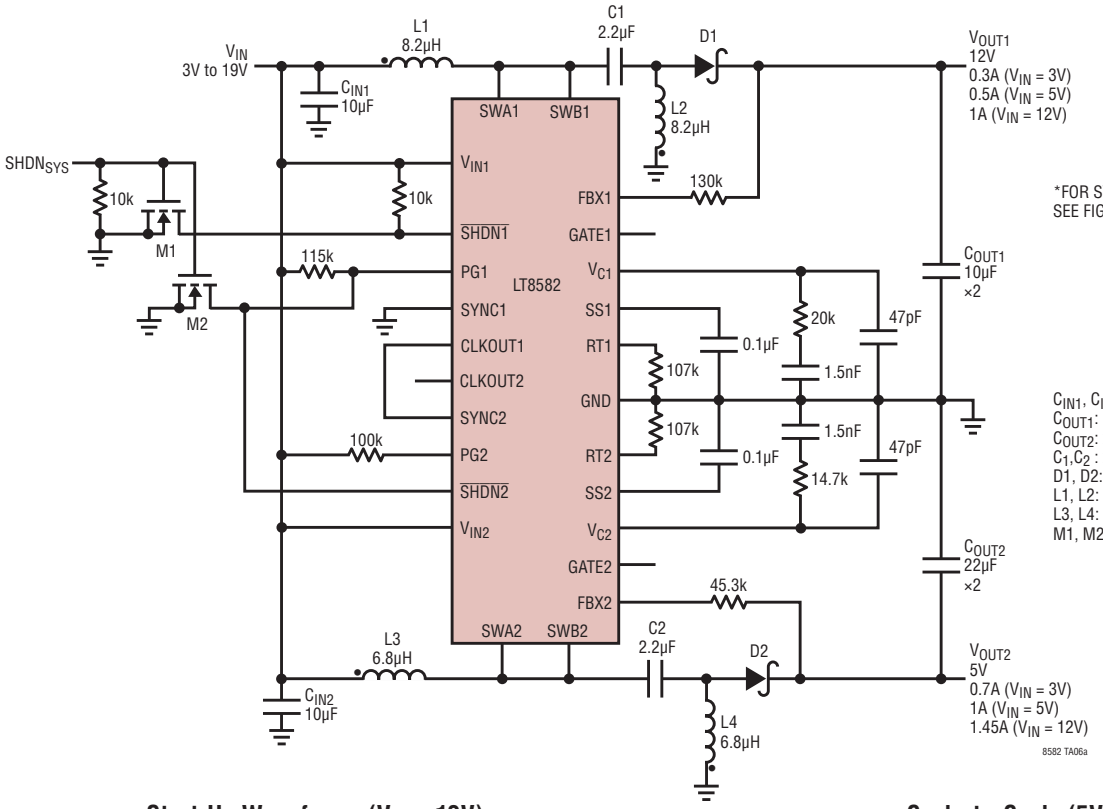


Input Removed, Holdup for ~110s with 500mA Load



TYPICAL APPLICATIONS

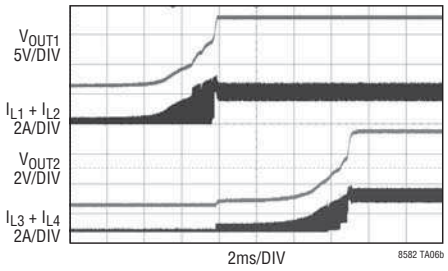
12V and 5V Sequenced Outputs from a 3V to 19V Input*



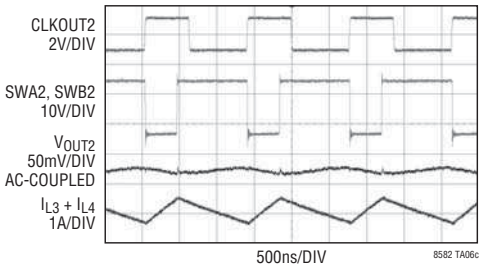
*FOR SYSTEM LEVEL DIAGRAM, SEE FIGURE 10

C_{IN1}, C_{IN2}: 10µF, 25V, X7R, 1210
C_{OUT1}: 10µF, 25V, X7R, 1210
C_{OUT2}: 22µF, 16V, X7R, 1210
C_1,C_2 : 2.2µF, 25V, X7R, 0805
D1, D2: CENTRAL SEMI CTLSH2-40M832
L1, L2: COOPER DRQ125-8R2
L3, L4: COOPER DRQ125-6R8
M1, M2: 2N7002

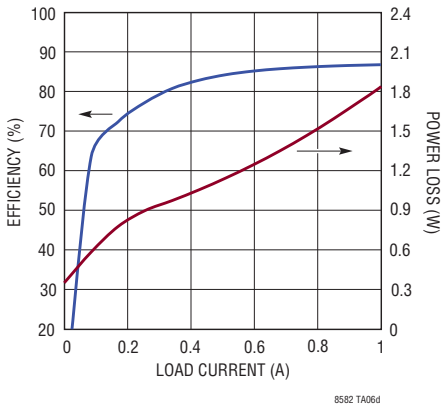
Start-Up Waveforms (V_{IN} = 12V)



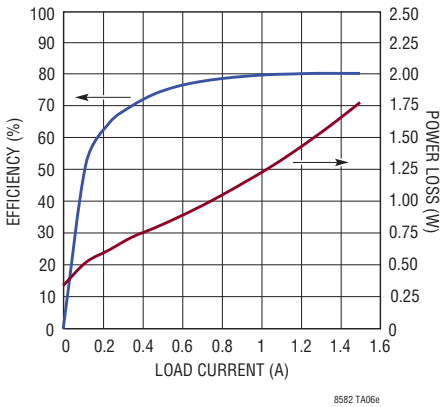
Cycle-to-Cycle (5V Output)



Efficiency and Power Loss (V_{IN} = 12V with Load on 12V Output)



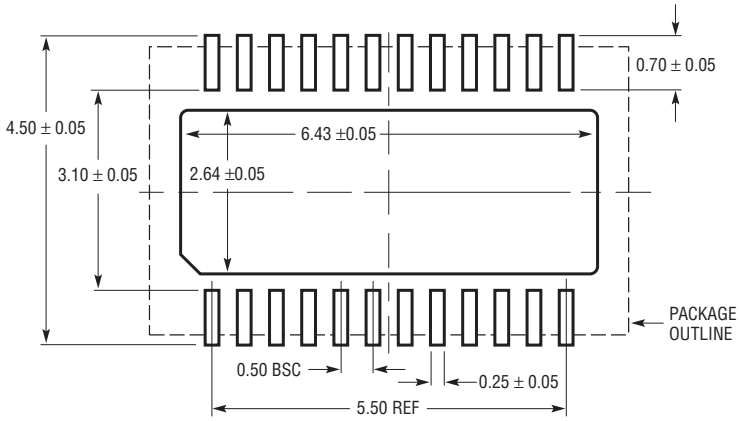
Efficiency and Power Loss (V_{IN} = 12V with Load on 5V Output)



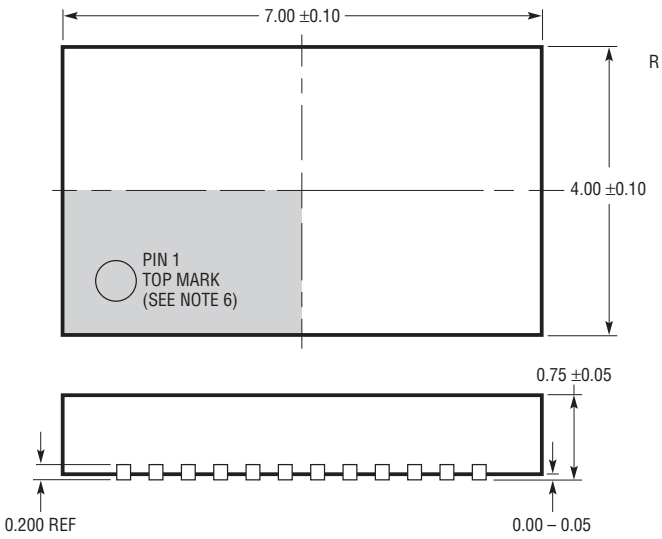
PACKAGE DESCRIPTION

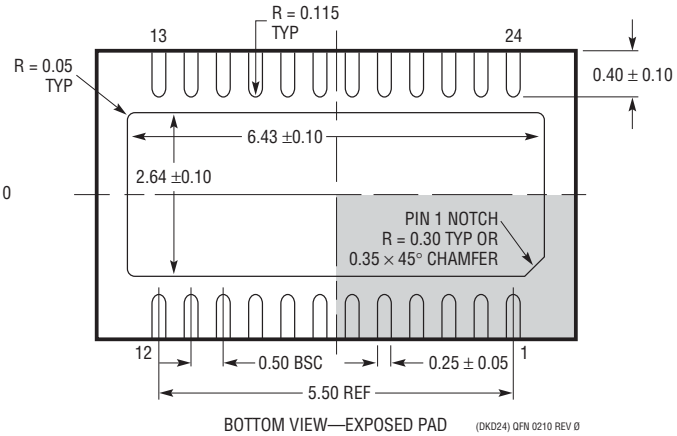
Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DKD Package
24-Lead Plastic DFN (7mm × 4mm)
(Reference LTC DWG # 05-08-1864 Rev Ø)



RECOMMENDED SOLDER PAD LAYOUT
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



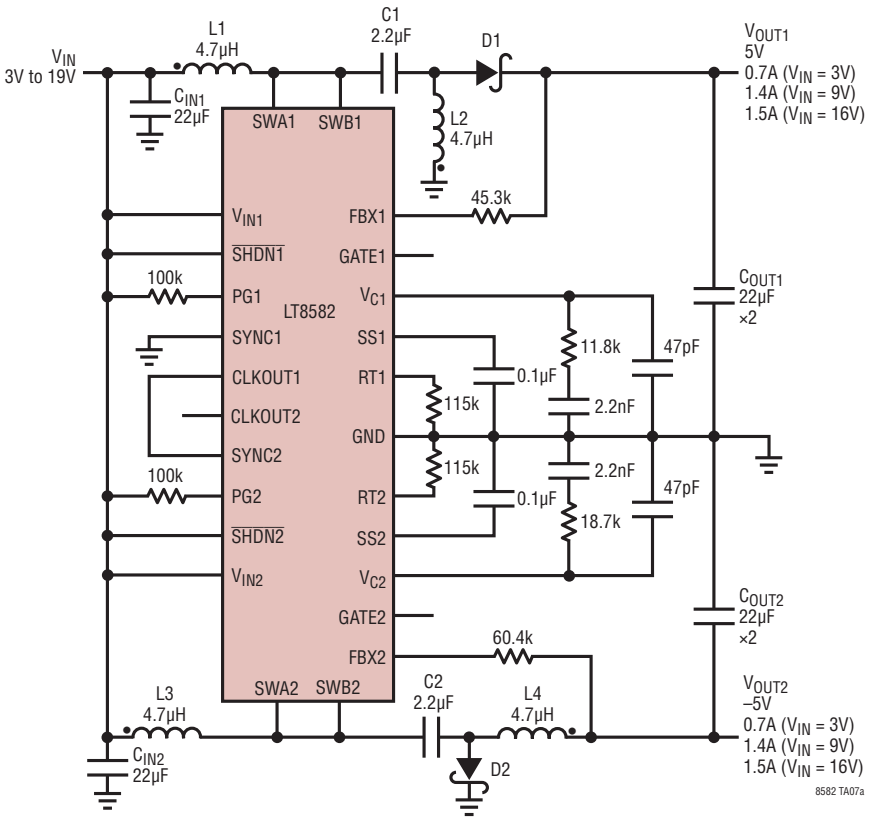


BOTTOM VIEW—EXPOSED PAD (DKD24) QFN 0210 REV Ø

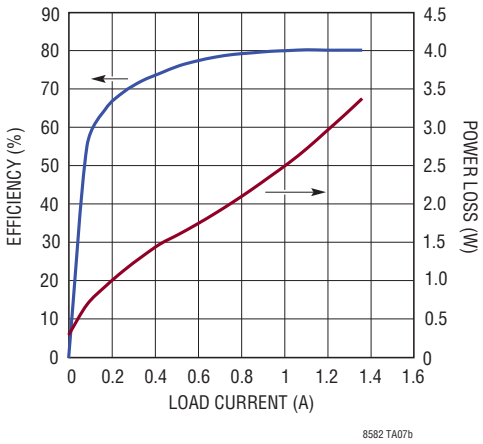
NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WXXX) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

700kHz SEPIC and Inverting Converter Generates ±5V Outputs from a 3V to 19V Input



Efficiency and Power Loss (V_{IN} = 12V with Load Between 5V and –5V Outputs)



C_{IN1}, C_{IN2}: 22µF, 25V, X7R, 1210
C_{OUT1}, C_{OUT2}: 22µF, 16V, X7R, 1210
C_1, C_2: 2.2µF, 50V, X7R, 1206
D1, D2: VISHAY MSS2P3
L1, L2: WÜRTH WE TDC 74489440047
L3, L4: WÜRTH WE TDC 74489440047

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT3581	3.3A (I_{SW}), 42V, 2.5MHz, High Efficiency Step-Up DC/DC Converter	V_{IN}: 2.5V to 22V, $V_{OUT(MAX)}$ = 42V, I_Q = 1.9mA, I_{SD} = < 1µA, 4mm × 3mm DFN-14, MSOP-16E
LT3579	6A (I_{SW}), 42V, 2.5MHz, High Efficiency Step-Up DC/DC Converter	V_{IN}: 2.5V to 16V, $V_{OUT(MAX)}$ = 42V, I_Q = 1.9mA, I_{SD} = < 1µA, 4mm × 5mm QFN-20, TSSOP-20
LT3580	2A (I_{SW}), 42V, 2.5MHz, High Efficiency Step-Up DC/DC Converter	V_{IN}: 2.5V to 32V, $V_{OUT(MAX)}$ = 42V, I_Q = 1mA, I_{SD} = < 1µA, 3mm × 3mm DFN-8, MSOP-8E
LT3471	Dual Output 1.3A (I_{SW}), 1.2MHz, High Efficiency Step-Up DC/DC Converter	V_{IN} = 2.4V to 16V, $V_{OUT(MAX)}$ = ±40V, I_Q = 2.5mA, I_{SD} < 1µA, 3mm × 3mm DFN-10 Package
LT3479	3A (I_{SW}), 40V, 3.5MHz, High Efficiency Step-Up DC/DC Converter	V_{IN}: 2.5V to 24V, $V_{OUT(MAX)}$ = 40V, I_Q = 5mA, I_{SD} = < 1µA, 4mm × 3mm DFN-14, TSSOP-16E
LT3477	40V, 3A, Full Featured DC/DC Converter	V_{IN} = 2.5V to 25V, $V_{OUT(MAX)}$ = 40V, I_Q = 5mA, I_{SD} < 1µA, QFN, TSSOP-20E Packages
LT1946/LT1946A	1.5A (I_{SW}), 1.2MHz/2.7MHz, High Efficiency Step-Up DC/DC Converter	V_{IN} = 2.6V to 16V, $V_{OUT(MAX)}$ = 34V, I_Q = 3.2mA, I_{SD} < 1µA, MS8E Package
LT1935	2A (I_{SW}), 40V, 1.2MHz, High Efficiency Step-Up DC/DC Converter	V_{IN} = 2.3V to 16V, $V_{OUT(MAX)}$ = 40V, I_Q = 3mA, I_{SD} < 1µA, ThinSOT™ Package
LT1310	2A (I_{SW}), 40V, 1.2MHz, High Efficiency Step-Up DC/DC Converter	V_{IN} = 2.3V to 16V, $V_{OUT(MAX)}$ = 40V, I_Q = 3mA, I_{SD} < 1µA, ThinSOT Package
LT3436	3A (I_{SW}), 800kHz, 34V Step-Up DC/DC Converter	V_{IN} = 3V to 25V, $V_{OUT(MAX)}$ = 34V, I_Q = 0.9mA, I_{SD} < 6µA, TSSOP-16E Package

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