R-IN32M3 Series

LSI for Industrial Ethernet

R18DS0008EJ0204

Dec 25, 2014

1. Overview

1.1 Introduction

Ethernet communication continues to spread rapidly in the field of industrial automation as manufacturers seek to improve the capability, efficiency, and flexibility of their organizations. Modern Industrial Ethernet applications require high-speed real-time response, low power consumption, and high performance. These requirements are not necessarily met by traditional methods such as hard-wired Ethernet processors or dedicated high-speed CPUs.

Renesas' R-IN32M3 series of large-scale integrated circuits (LSI) are specifically tailored to meet the demands of Industrial Ethernet applications. Key features include:

- High-speed, real-time, deterministic, low-latency, low-jitter response for real-time applications
- Low power consumption
- Integrated ARM Cortex-M3 core for flexibility
- Integrated Real-Time OS Accelerator with support for µITRON version 4.0
- Integrated Gigabit Ethernet MAC (R-IN32M3-CL only)
- Integrated 10/100Mbps EtherPHY (R-IN32M3-EC only)
- Dedicated, DMA controller and buffer for the network processor
- High performance with low CPU usage by offloading functions to Real-Time OS Accelerator
- Multiple timers, serial interfaces, general purpose I/O (GPIO), external memory interfaces

1.2 Product Lineup

Renesas’s R-IN32M3 series includes the following two devices:

Table1.1 R-IN32M3 Product Lineup

Product name	Feature
R-IN32M3-EC	R-IN32M3 with built-in EtherCAT™ Slave Controller
R-IN32M3-CL	R-IN32M3 with built-in CC-Link IE Field™ (Intelligent device station)

1.3 Overview

Table1.2 Overview of R-IN32M3 (1/2)

Item \ Product	R-IN32M3
CPU cores	ARM Cortex-M3 32-bit RISC CPU + Real-Time OS Accelerator (Hardware Real-Time OS, HW-RTOS)
Operating frequency	100MHz
Instruction set	Thumb®-2 instruction ARMv7-M architecture
Instruction RAM	768KByte (RAM w/ECC)
Data RAM	512KByte (RAM w/ECC)
Buffer RAM	64KByte (RAM w/ECC)
Internal System Bus	- 32-bit system bus at 100MHz - 128-bit communication bus at 100MHz
DMA	- 4 channels + 1 channel (for Real-time port) - Supports software and/or various interrupt-triggered DMA
Boot options	- Serial Flash ROM Boot - External Memory Boot - External MPU Boot
External Memory Support	- 16-bit or 32-bit bus interface - Page ROM / ROM / SRAM interface - Synchronous burst memory interface - Four chip selects for external SRAM - 256MByte (max) external memory space - Programmable wait function
External MPU interface	- 16-bit or 32-bit bus interface - General-purpose interface for static memory - Address space:2MByte (Instruction RAM, Data RAM, Register area)
Serial Flash ROM Memory Controller	- Support serial interface compatible with SPI of the companies - Support direct boot from serial memory device - Support Fast Read, Fast Read Dual Output, Fast Read Dual I/O mode - Direct layout in memory space
Interrupt Support	- 29 external interrupt ports
Internal Peripherals	
I/O Ports	- 96 CMOS I/O ports (max)
System Timers	- Hardware RTOS interal timer
	- CPU internal timer
	- 4 channels timer array - 32-bit counter & 32-bit data register - counter by external signal
Watchdog Timer	- 1 channel - Software-triggered start mode - Watchdog error response options: - Generate Non-Maskable Interrupt (NMI) - Generate Reset

Table1.2 Overview of R-IN32M3 (2/2)

Item \ Product	R-IN32M3
Internal Peripherals (cont.)	
Asynchronous serial interface	- 2 channels - Full duplex - FIFOs: 10-bit x 16 receive and 8-bit x 16 transmit - Support output of receive errors and status - Character length: 7 or 8-bit - Parity bit options: odd, even, 0- , none - Transmit stop bits: 1 or 2-bit
I2C Serial interface	- 2 channels - Operation modes: normal or high-speed - Transfer modes: single-transfer mode, or continuous-transfer mode - Transmission data length: 8-bit
CAN controller	- 2 channels - Conforming to ISO11898 - Support to transfer and receive normal frame and expand frame - Transmission speed: 1Mbps (max)
Clock Synchronized Serial Interface	- 2 channels - Synchronized Serial data transmission by three-wire system - Selectable Master mode or Slave mode - Built-in Baud-rate generator - Transmission data length: 7bit - 16bit
CC-Link	- Intelligent device station Note3 <R> - Remote device station
10/100/1000Mbps Ether MAC Note1	- 1 channel - Built-in 2-port switch - GMII / MII interface
10/100Mbps EtherPHY Note2	- 2ports - Support for 10BaseT and 100BaseTX/FX
CC-Link IE Note1	CC-Link IE Field (Intelligent device station)
EtherCAT Note2	EtherCAT Slave controller
On-chip debug function	- Select serial wire or JTAG - Support Full Trace (Built-in ETM)
Internal PLL	Generates various clocks from 25MHz input clock
Power supply voltage	I/O:VDD33 = 3.3±0.3V Internal circuit :VDD10 = 1.0±0.1V

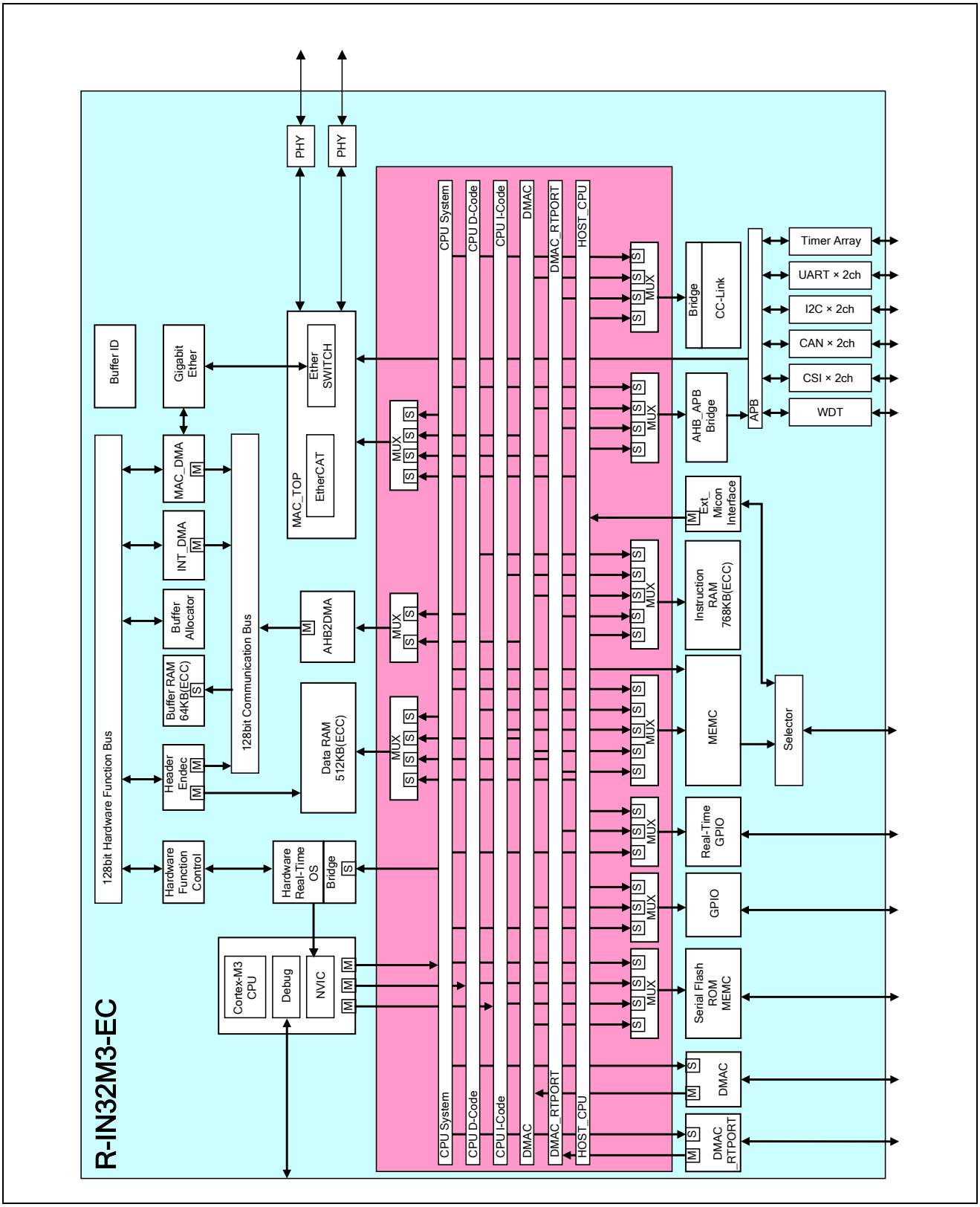
Note1. Supported by R-IN32M3-CL

Note2. Supported by R-IN32M3-EC

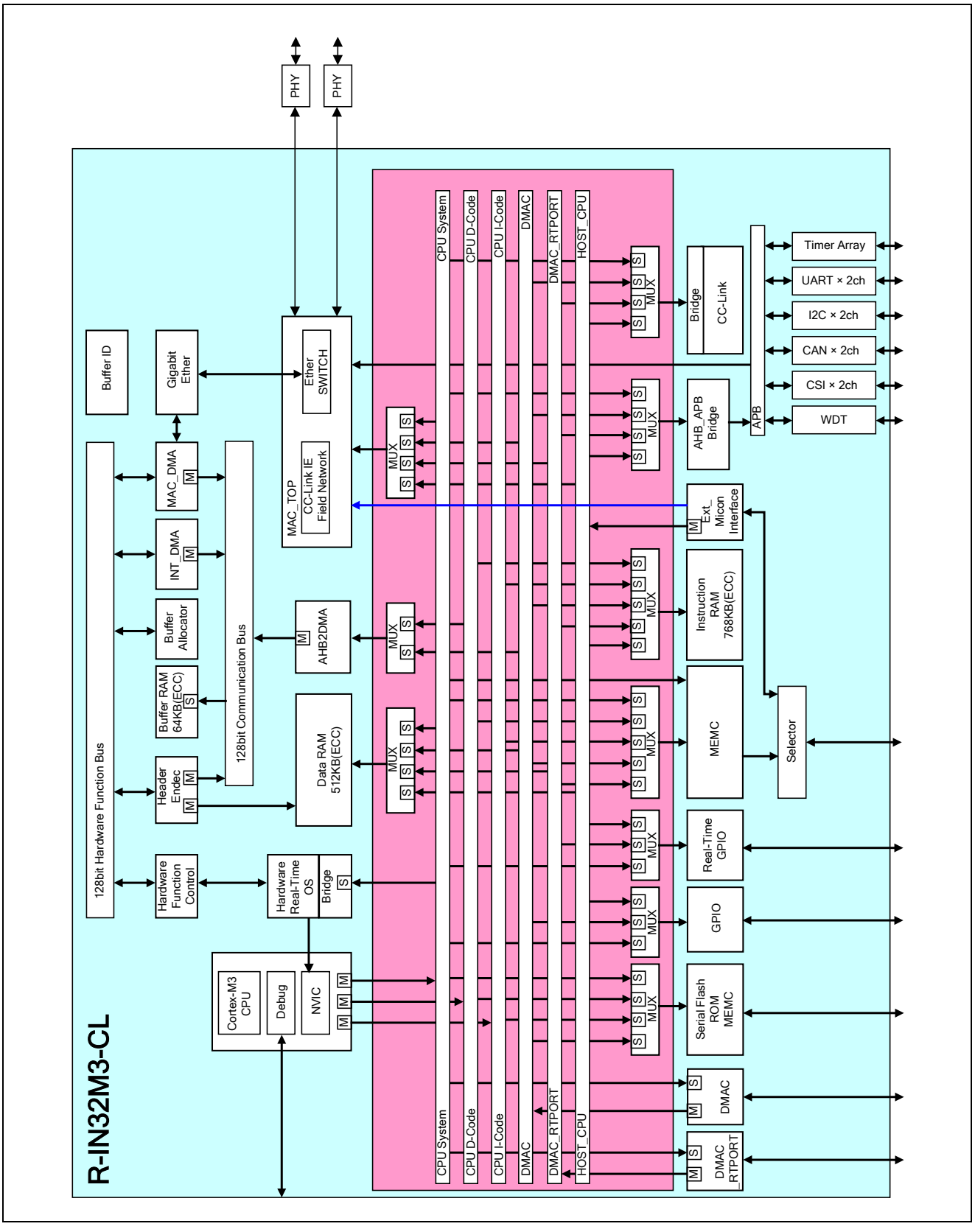
Note3. Please ask us about a detail for support.

1.4 Internal Block Diagram

1.4.1 R-IN32M3-EC Block Diagram



1.4.2 R-IN32M3-CL Block Diagram



1.5 Memory Maps

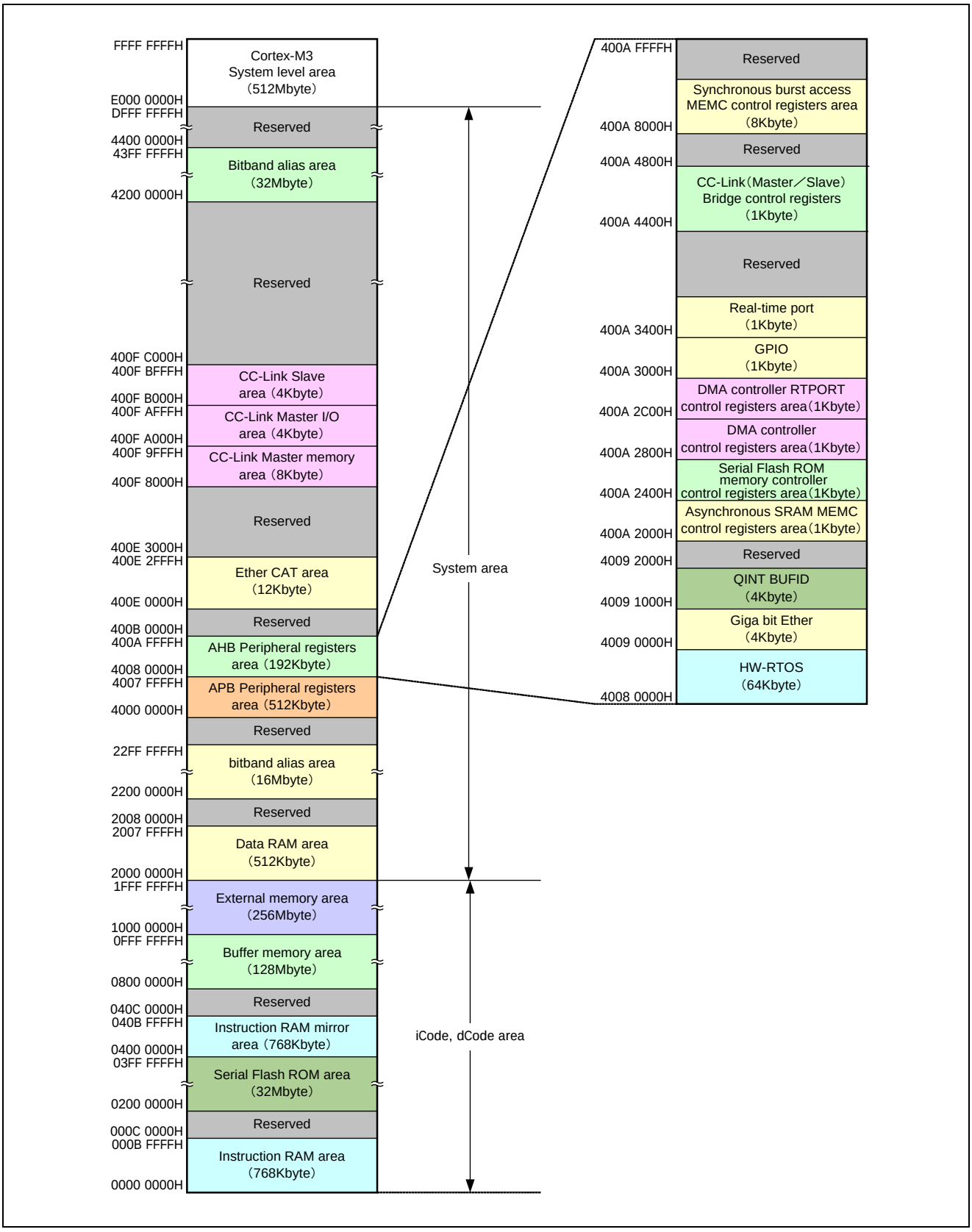


Figure 1.1 Memory map (ALL) (R-IN32M3-EC) <R>

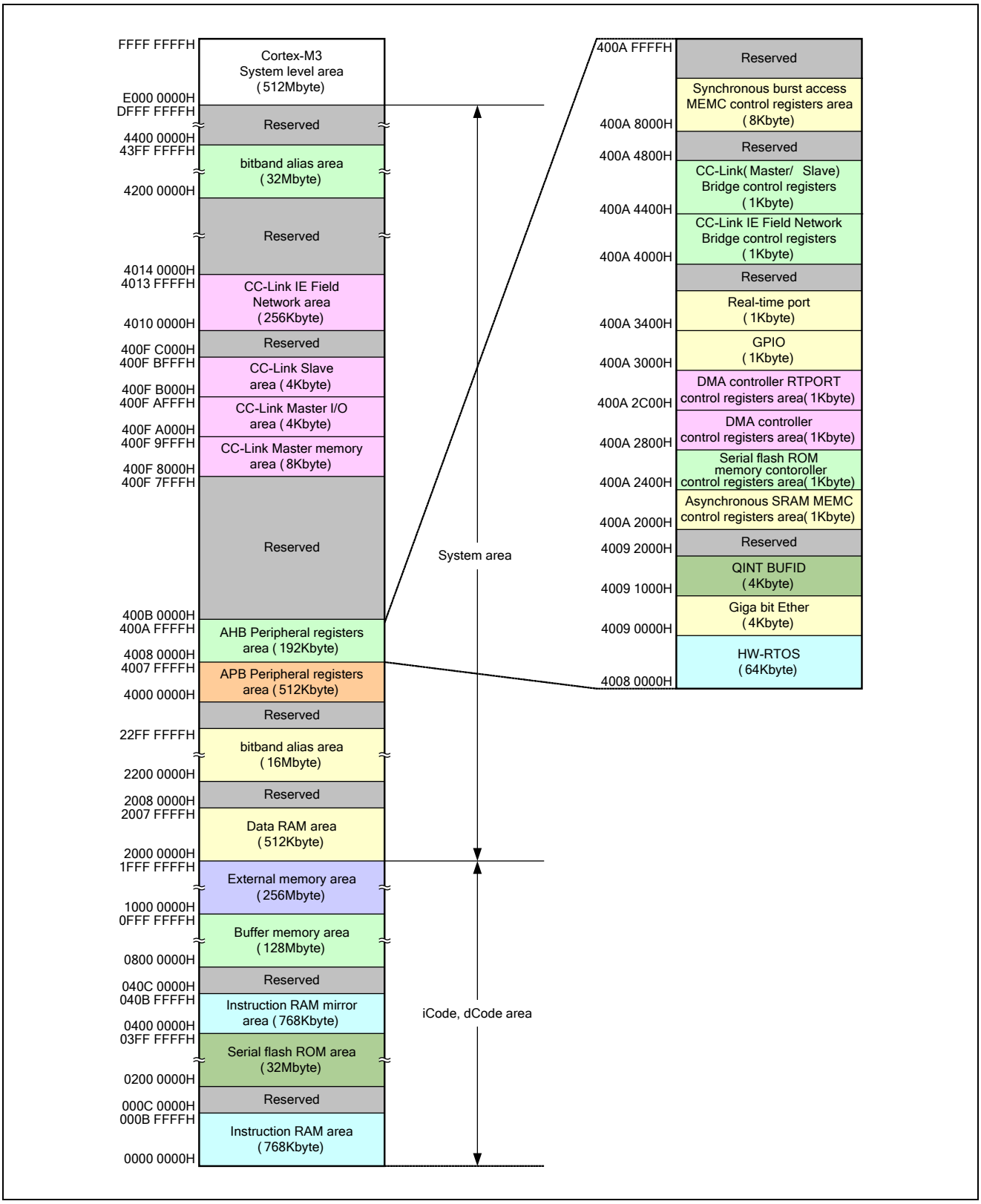


Figure 1.2 Memory map (ALL) (R-IN32M3-CL)

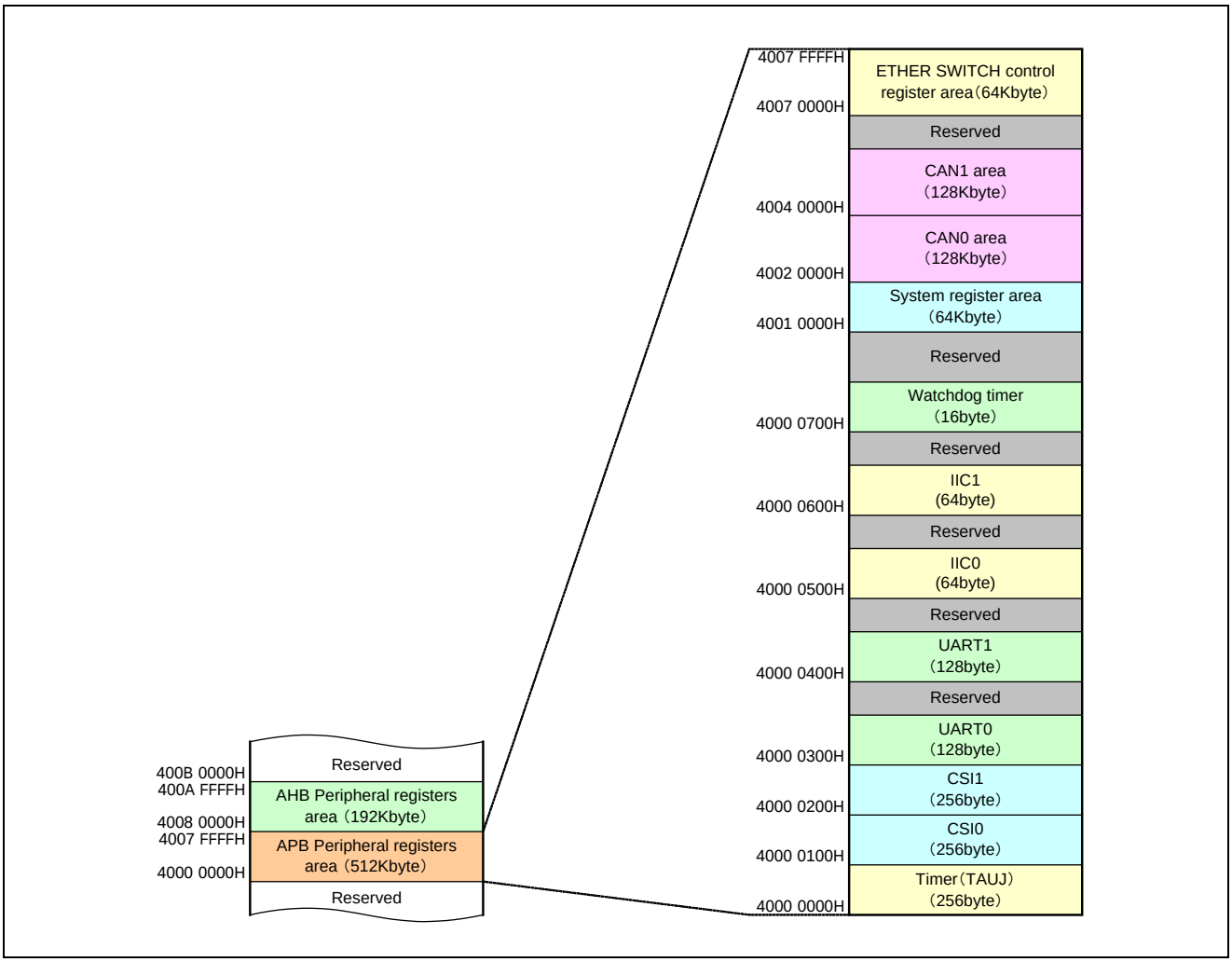


Figure 1.3 Memory map (APB Peripheral registers area; common to R-IN32M3-EC/CL)

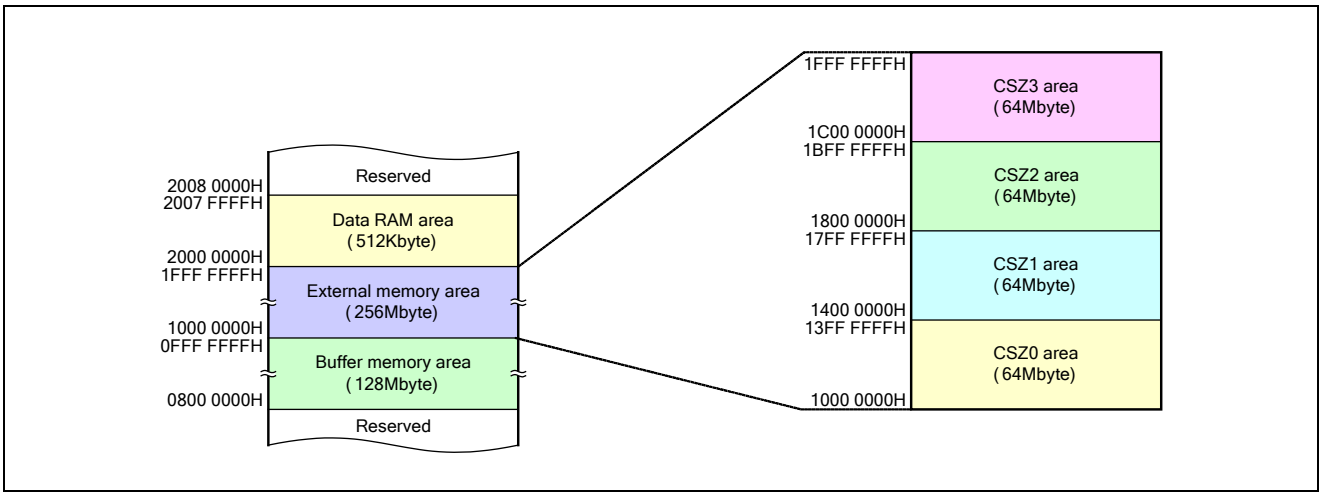


Figure 1.4 Memory map (External memory area; common to R-IN32M3-EC/CL)

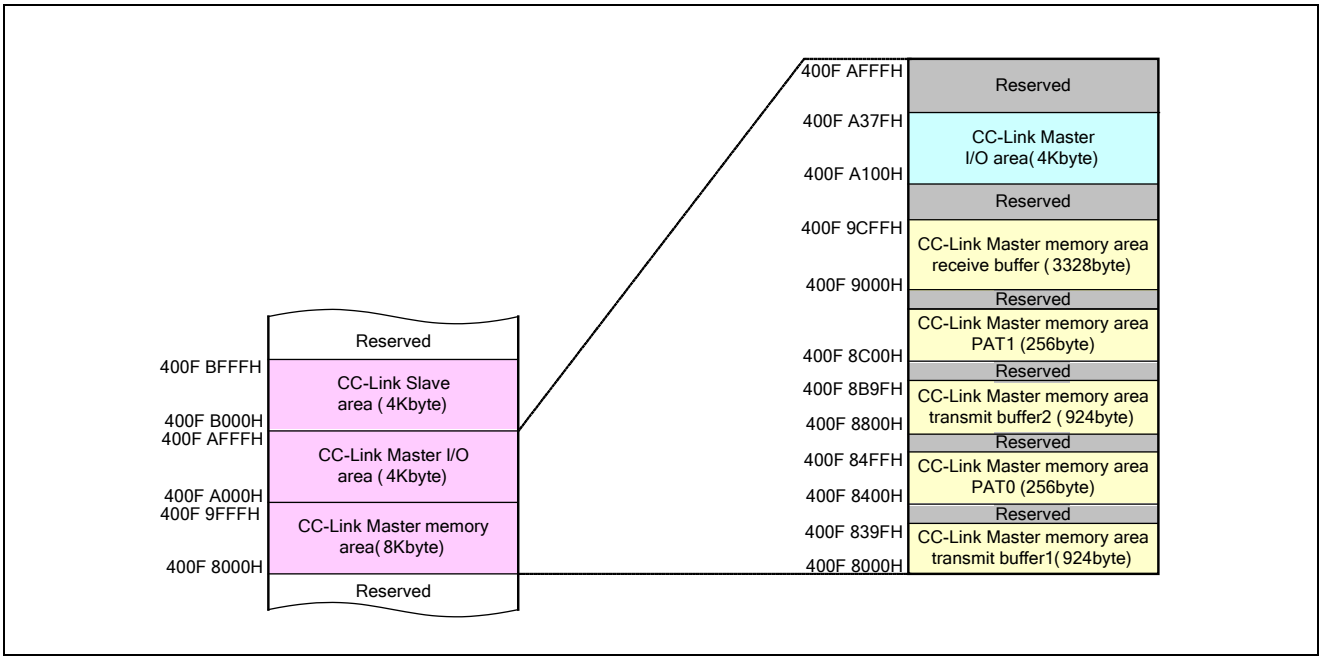


Figure 1.5 Memory map (CC-Link Master area; common to R-IN32M3-EC/CL)

Caution 1. CC-Link Master shows the function block of Intelligent Device station.

2. CC-Link Slave shows the function block of the Remote Device station.

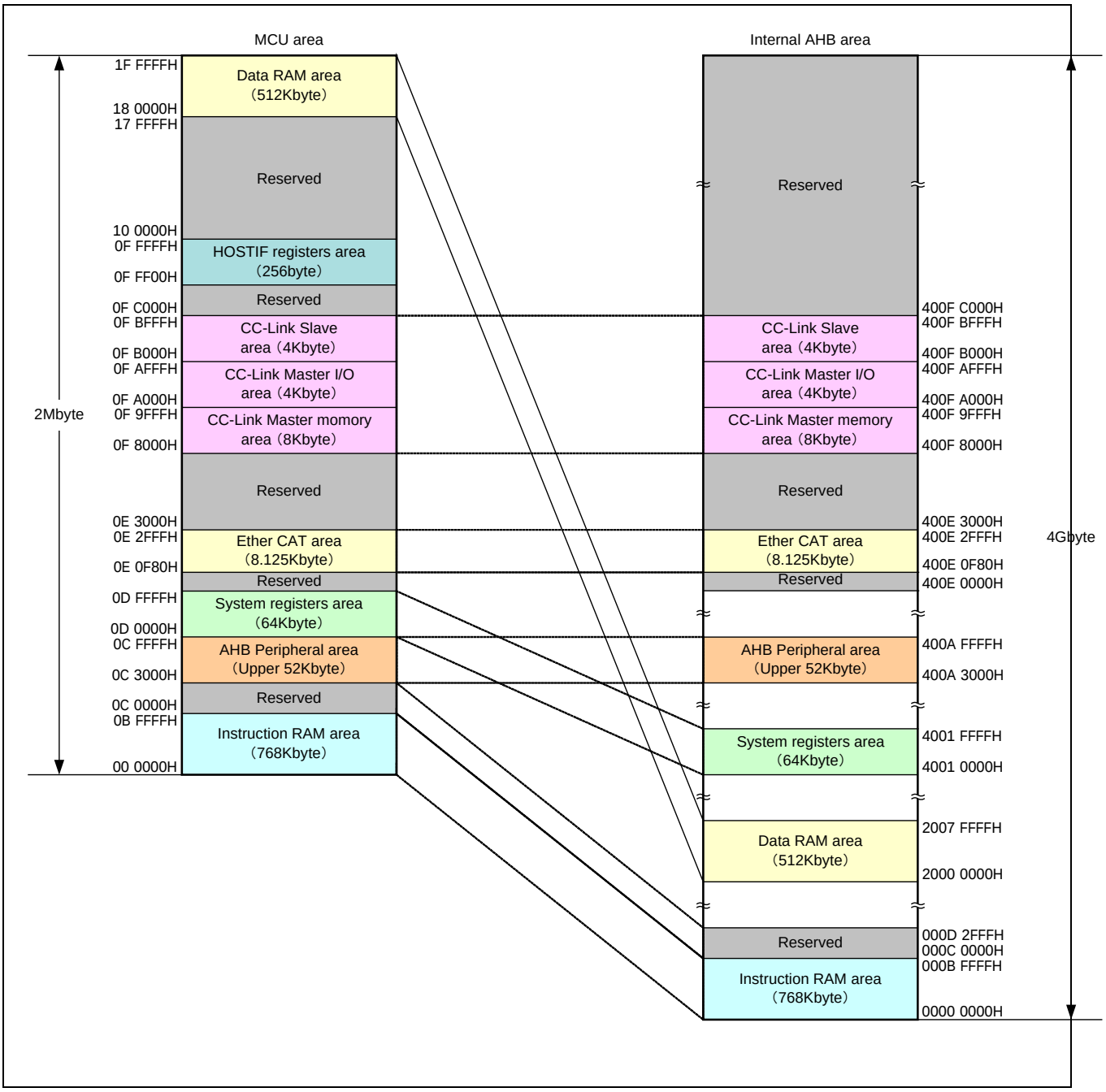


Figure 1.6 External MPU interface area (R-IN32M3-EC) <R>

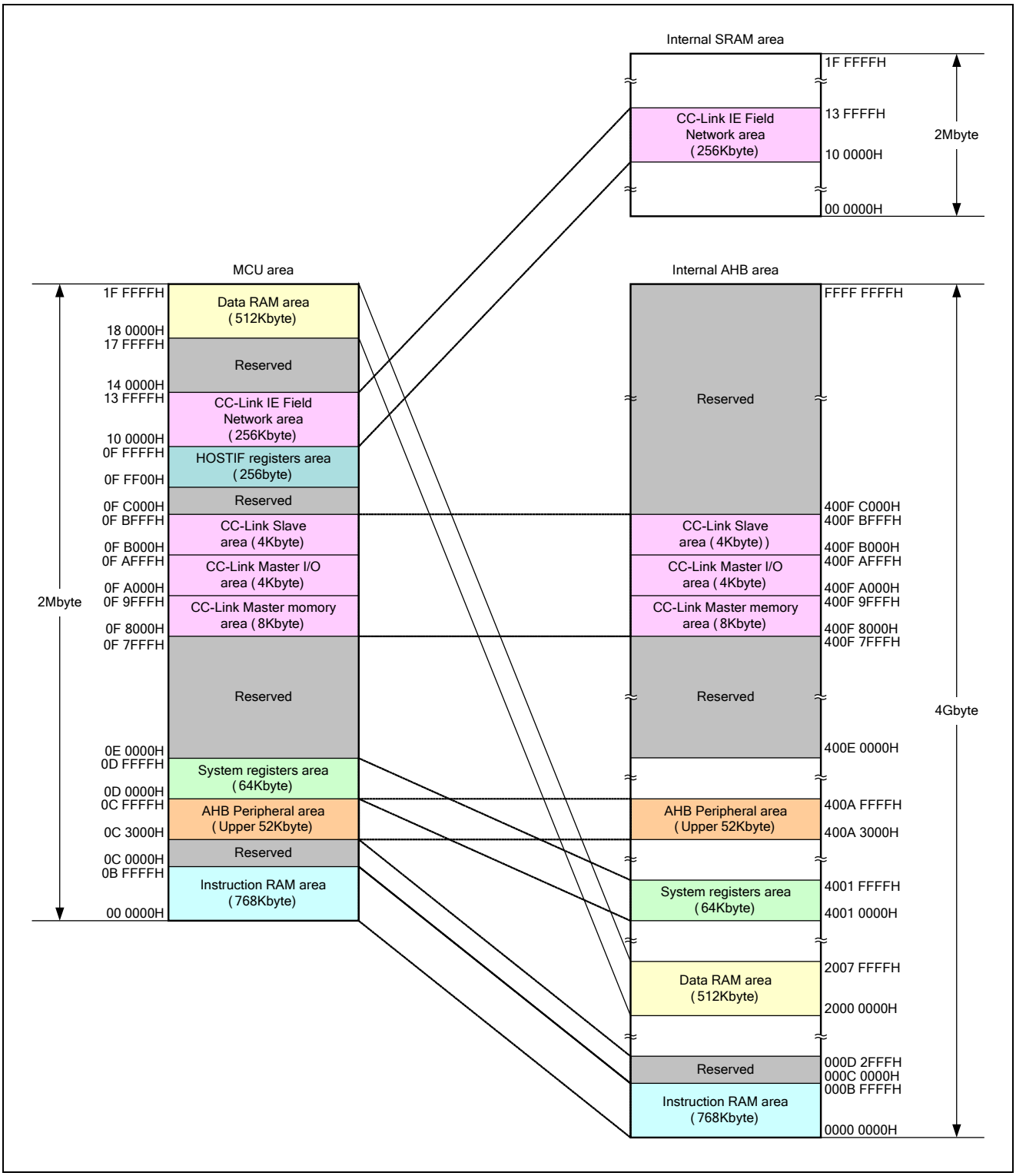
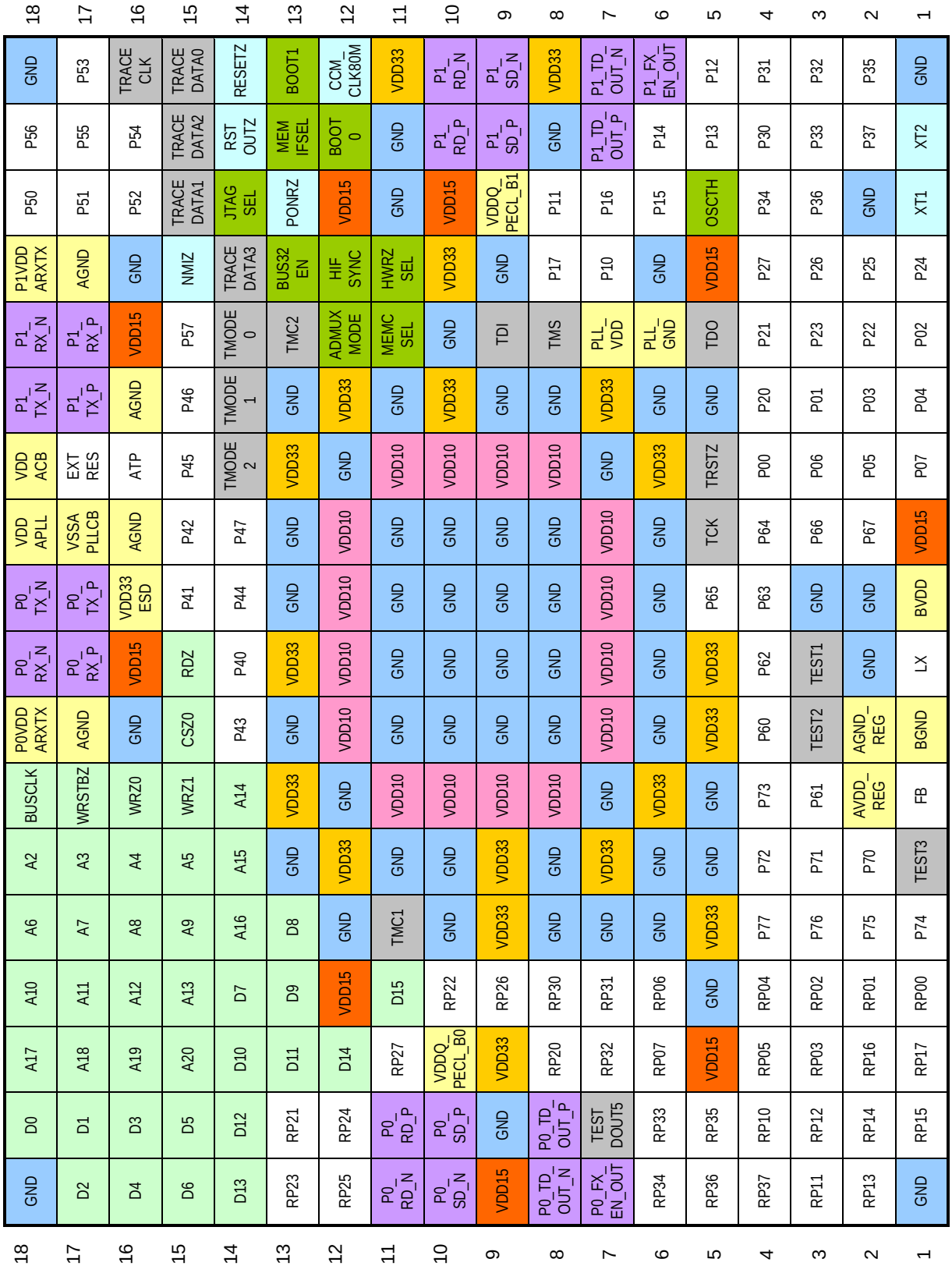


Figure 1.7 External MPU interface area (R-IN32M3-CL)

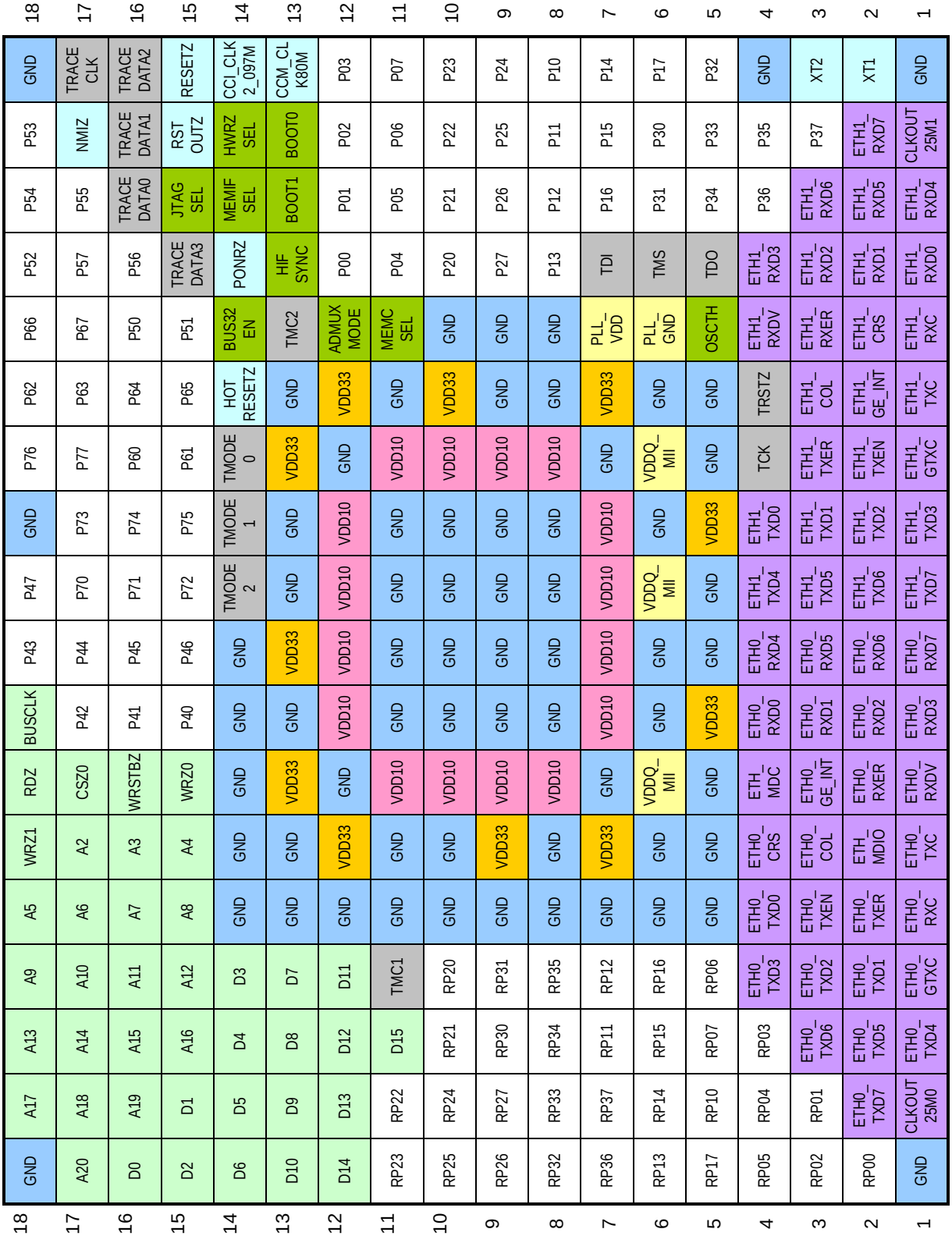
2. Pin Information

2.1 Pin Placement (R-IN32M3-EC Top View)



	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
A	GND	D2	D4	D6	D13	RP23	RP25	P0_RD_N	P0_SD_N	VDD15	P0_TD_OUT_N	P0_FX_EN_OUT	RP34	RP36	RP37	RP11	RP13	GND
B	D0	D1	D3	D5	D12	RP21	RP24	P0_RD_P	P0_SD_P	GND	P0_TD_OUT_P	TEST DOUT5	RP33	RP35	RP10	RP12	RP14	RP15
C	A17	A18	A19	A20	D10	D11	D14	RP27	VDDQ_PECL_B0	VDD33	RP20	RP32	RP07	VDD15	RP05	RP03	RP16	RP17
D	A10	A11	A12	A13	D7	D9	VDD15	D15	RP22	RP26	RP30	RP31	RP06	GND	RP04	RP02	RP01	RP00
E	A6	A7	A8	A9	A16	D8	GND	TMC1	GND	VDD33	GND	GND	GND	VDD33	P77	P76	P75	P74
F	A2	A3	A4	A5	A15	GND	VDD33	GND	GND	VDD33	GND	VDD33	GND	GND	P72	P71	P70	TEST3
G	BUSCLK	WRSTBZ	WRZ0	WRZ1	A14	VDD33	GND	VDD10	VDD10	VDD10	VDD10	GND	VDD33	GND	P73	P61	AVDD_REG	FB
H	P0VDD ARXTX	AGND	GND	CSZ0	P43	GND	VDD10	GND	GND	GND	GND	VDD10	GND	VDD33	P60	TEST2	AGND_REG	BGND
J	P0_RX_N	P0_RX_P	VDD15	RDZ	P40	VDD33	VDD10	GND	GND	GND	GND	VDD10	GND	VDD33	P62	TEST1	GND	LX
K	P0_TX_N	P0_TX_P	VDD33 ESD	P41	P44	GND	VDD10	GND	GND	GND	GND	VDD10	GND	P65	P63	GND	GND	BVDD
L	VDD APLL	VSSA PLLCB	AGND	P42	P47	GND	VDD10	GND	GND	GND	GND	VDD10	GND	TCK	P64	P66	P67	VDD15
M	VDD ACB	EXT RES	ATP	P45	TMODE 2	VDD33	GND	VDD10	VDD10	VDD10	VDD10	GND	VDD33	TRSTZ	P00	P06	P05	P07
N	P1_TX_N	P1_TX_P	AGND	P46	TMODE 1	GND	VDD33	GND	VDD33	GND	GND	VDD33	GND	GND	P20	P01	P03	P04
P	P1_RX_N	P1_RX_P	VDD15	P57	TMODE 0	TMC2	ADMUX MODE	MEMC SEL	GND	TDI	TMS	PLL_VDD	PLL_GND	TDO	P21	P23	P22	P02
R	P1VDD ARXTX	AGND	GND	NMIZ	TRACE DATA3	BUS32 EN	HIF SYNC	HWRZ SEL	VDD33	GND	P17	P10	GND	VDD15	P27	P26	P25	P24
T	P50	P51	P52	TRACE DATA1	JTAG SEL	PONRZ	VDD15	GND	VDD15	VDDQ_PECL_B1	P11	P16	P15	OSCTH	P34	P36	GND	XT1
U	P56	P55	P54	TRACE DATA2	RST OUTZ	MEM IFSEL	BOOT 0	GND	P1_RD_P	P1_SD_P	GND	P1_TD_OUT_P	P14	P13	P30	P33	P37	XT2
V	GND	P53	TRACE CLK	TRACE DATA0	RESETZ	BOOT1	CCM_CLK80M	VDD33	P1_RD_N	P1_SD_N	VDD33	P1_TD_OUT_N	P1_FX_EN_OUT	P12	P31	P32	P35	GND
	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1

2.2 Pin Placement (R-IN32M3-CL Top View)



	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
V	GND	TRACE CLK	TRACE DATA2	RESETZ	CCI_CLK 2_097M	CCM_CL K80M	P03	P07	P23	P24	P10	P14	P17	P32	GND	XT2	XT1	GND
U	P53	NMIZ	TRACE DATA1	RST OUTZ	HWRZ SEL	BOOT0	P02	P06	P22	P25	P11	P15	P30	P33	P35	P37	ETH1_ RXD7	CLKOUT 25M1
T	P54	P55	TRACE DATA0	JTAG SEL	MEMIF SEL	BOOT1	P01	P05	P21	P26	P12	P16	P31	P34	P36	ETH1_ RXD6	ETH1_ RXD5	ETH1_ RXD4
R	P52	P57	P56	TRACE DATA3	PONRZ	HIF SYNC	P00	P04	P20	P27	P13	TDI	TMS	TDO	ETH1_ RXD3	ETH1_ RXD2	ETH1_ RXD1	ETH1_ RXD0
P	P66	P67	P50	P51	BUS32 EN	TMC2	ADMUX MODE	MEMC SEL	GND	GND	GND	PLL_ VDD	PLL_ GND	OSCTH	ETH1_ RXDV	ETH1_ RXER	ETH1_ CRS	ETH1_ RXC
N	P62	P63	P64	P65	HOT RESETZ	GND	VDD33	GND	VDD33	GND	GND	VDD33	GND	GND	TRSTZ	ETH1_ COL	ETH1_ GE_INT	ETH1_ TXC
M	P76	P77	P60	P61	TMODE 0	VDD33	GND	VDD10	VDD10	VDD10	VDD10	GND	VDDQ_ MII	GND	TCK	ETH1_ TXER	ETH1_ TXEN	ETH1_ GTXC
L	GND	P73	P74	P75	TMODE 1	GND	VDD10	GND	GND	GND	GND	VDD10	GND	VDD33	ETH1_ TXD0	ETH1_ TXD1	ETH1_ TXD2	ETH1_ TXD3
K	P47	P70	P71	P72	TMODE 2	GND	VDD10	GND	GND	GND	GND	VDD10	VDDQ_ MII	GND	ETH1_ TXD4	ETH1_ TXD5	ETH1_ TXD6	ETH1_ TXD7
J	P43	P44	P45	P46	GND	VDD33	VDD10	GND	GND	GND	GND	VDD10	GND	GND	ETH0_ RXD4	ETH0_ RXD5	ETH0_ RXD6	ETH0_ RXD7
H	BUSCLK	P42	P41	P40	GND	GND	VDD10	GND	GND	GND	GND	VDD10	GND	VDD33	ETH0_ RXD0	ETH0_ RXD1	ETH0_ RXD2	ETH0_ RXD3
G	RDZ	CSZ0	WRSTBZ	WRZ0	GND	VDD33	GND	VDD10	VDD10	VDD10	VDD10	GND	VDDQ_ MII	GND	ETH_ MDC	ETH0_ GE_INT	ETH0_ RXER	ETH0_ RXDV
F	WRZ1	A2	A3	A4	GND	GND	VDD33	GND	GND	VDD33	GND	VDD33	GND	GND	ETH0_ CRS	ETH0_ COL	ETH_ MDIO	ETH0_ TXC
E	A5	A6	A7	A8	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	ETH0_ TXD0	ETH0_ TXEN	ETH0_ TXER	ETH0_ RXC
D	A9	A10	A11	A12	D3	D7	D11	TMC1	RP20	RP31	RP35	RP12	RP16	RP06	ETH0_ TXD3	ETH0_ TXD2	ETH0_ TXD1	ETH0_ GTXC
C	A13	A14	A15	A16	D4	D8	D12	D15	RP21	RP30	RP34	RP11	RP15	RP07	RP03	ETH0_ TXD6	ETH0_ TXD5	ETH0_ TXD4
B	A17	A18	A19	D1	D5	D9	D13	RP22	RP24	RP27	RP33	RP37	RP14	RP10	RP04	RP01	ETH0_ TXD7	CLKOUT 25M0
A	GND	A20	D0	D2	D6	D10	D14	RP23	RP25	RP26	RP32	RP36	RP13	RP17	RP05	RP02	RP00	GND

2.3 Signals by Function

2.3.1 Ethernet Signals

(1) PHY Interface (R-IN32M3-CL only)

Caution These signals apply to R-IN32M3-CL only.

Pin Name	I/O	Function	Active	Level during reset
ETH0_TXC	I	Ethernet 0 10M/100M Transmit clock port (2.5MHz/25MHz)	↑	-
ETH0_GTXC	O	Ethernet 0 1G Transmit clock port (125MHz)	↑	- Note
ETH0_TXEN	O	Ethernet 0 Transmit enable port	High	Low
ETH0_TXER	O	Ethernet 0 Transmit error port	High	Low
ETH0_TXD0-ETH0_TXD7	O	Ethernet 0 Transmit data port	-	Low
ETH0_GE_INT	I	Ethernet 0 PHY interrupt port	High/Low	-
ETH0_RXC	I	Ethernet 0 Receive clock port	↑	-
ETH0_RXDV	I	Ethernet 0 Receive enable port	High	-
ETH0_RXER	I	Ethernet 0 Receive error port	High	-
ETH0_RXD0-ETH0_RXD7	I	Ethernet 0 Receive data port	-	-
ETH0_CRS	I	Ethernet 0 Carrier sense port	High	-
ETH0_COL	I	Ethernet 0 Collision port	High	-
ETH1_TXC	I	Ethernet 1 10M/100M Transmit clock port (2.5MHz/25MHz)	↑	-
ETH1_GTXC	O	Ethernet 1 1G Transmit clock port (125MHz)	↑	- Note
ETH1_TXEN	O	Ethernet 1 Transmit enable port	High	Low
ETH1_TXER	O	Ethernet 1 Transmit error port	High	Low
ETH1_TXD0-ETH1_TXD7	O	Ethernet 1 Transmit data port	-	Low
ETH1_GE_INT	I	Ethernet 1 PHY interrupt port	High/Low	-
ETH1_RXC	I	Ethernet 1 Receive clock port	↑	-
ETH1_RXDV	I	Ethernet 1 Receive enable port	High	-
ETH1_RXER	I	Ethernet 1 Receive error port	High	-
ETH1_RXD0-ETH1_RXD7	I	Ethernet 1 Receive data port	-	-
ETH1_CRS	I	Ethernet 1 Carrier sense port	High	-
ETH1_COL	I	Ethernet 1 Collision port	High	-
ETH_MDC	O	Ethernet Serial management interface clock	↑	Low
ETH_MDIO	I/O	Ethernet Serial management interface data input/output	-	Hi-Z

Note Out put the 125MHz clock.

(2) Media Interface (R-IN32M3-EC only)

Caution These signals apply to R-IN32M3-EC only.

Pin Name	I/O	Function	Active	Level during reset
P0_RX_P	I	PHY0 Receive data (+)	-	-
P0_RX_N	I	PHY0 Receive data (-)	-	-
P1_RX_P	I	PHY1 Receive data (+)	-	-
P1_RX_N	I	PHY1 Receive data (-)	-	-
P0_TX_P	O	PHY0 Transmit data (+)	-	-
P0_TX_N	O	PHY0 Transmit data (-)	-	-
P1_TX_P	O	PHY1 Transmit data (+)	-	-
P1_TX_N	O	PHY1 Transmit data (-)	-	-
P0_SD_P	I	PHY0 100BASE-FX Signal Detect (+)	High	-
P0_SD_N	I	PHY0 100BASE-FX Signal Detect (-)	Low	-
P1_SD_P	I	PHY1 100BASE-FX Signal Detect (+)	High	-
P1_SD_N	I	PHY1 100BASE-FX Signal Detect (-)	Low	-
P0_RD_P	I	PHY0 100BASE-FX Receive data (+)	-	-
P0_RD_N	I	PHY0 100BASE-FX Receive data (-)	-	-
P1_RD_P	I	PHY1 100BASE-FX Receive data (+)	-	-
P1_RD_N	I	PHY1 100BASE-FX Receive data (-)	-	-
P0_TD_OUT_P	O	PHY0 100BASE-FX Transmit data (+)	-	-
P0_TD_OUT_N	O	PHY0 100BASE-FX Transmit data (-)	-	-
P1_TD_OUT_P	O	PHY1 100BASE-FX Transmit data (+)	-	-
P1_TD_OUT_N	O	PHY1 100BASE-FX Transmit data (-)	-	-
P0_FX_EN_OUT	O	PHY0 100BASE-FX FX Enable Indication 1：100BASE-FX mode	High	-
P1_FX_EN_OUT	O	PHY1 100BASE-FX FX Enable Indication 1：100BASE-FX mode	High	-

Remark In MDI-X mode, the input and output attributes of TXP/TXN and RXP/RXN are reversed.

(3) Other Signals

Pin Name	I/O	Function	Shared Port	Active	Level during reset
PHYLINK0, PHYLINK1	I	PHY Link port Note1 (for EtherSwitch)	P06-P07	High	Hi-Z With internal pull-up resistor
P0LINKLEDZ	O	SIP_PHY0 Link status LED port Note 2	P06	Low	Hi-Z
P1LINKLEDZ	O	SIP_PHY1 Link status LED port Note 2	P07	Low	
ETHSWSECOUT	O	EtherSwitch Ivent par 1sec output port	P24	High	Hi-Z With internal pull-up resistor
P0DUPLEXLEDZ	O	SIP_PHY0 half-duplex status LED port Note2	P70	-	
P0SPEED100LEDZ	O	SIP_PHY0 100-BASE status LED port Note2	P72	Low	
P0SPEED10LEDZ	O	SIP_PHY0 10-BASE status LED port Note2	P73	Low	
P1DUPLEXLEDZ	O	SIP_PHY1 half-duplex status LED port Note2	P74	-	
P1SPEED100LEDZ	O	SIP_PHY1 100-BASE status LED port Note2	P76	Low	
P1SPEED10LEDZ	O	SIP_PHY1 10-BASE status LED port Note2	P77	Low	
P0ACTLEDZ	O	SIP_PHY0 RX status LED port Note2	RP02	Low	
P1ACTLEDZ	O	SIP_PHY1 TX status LED port Note2	RP04	Low	

Note1. Supported only by R-IN32M3-CL

Note2. Supported only by R-IN32M3-EC

2.3.2 EtherCAT Slave Controller Signals (R-IN32M3-EC only)

Caution These signals apply to R-IN32M3-EC only.

Pin Name	I/O	Function	Shared Port	Active	Level during reset
CATLEDRUN	O	Ether CAT RUN LED port	P00	High	Hi-Z
CATIRQ	O	Ether CAT IRQ port	P01	High	
CATLEDSTER	O	Ether CAT Dual-color State LED port	P02	High	
CATLEDERR	O	Ether CAT Error LED port	P03	High	
CATLINKACT0, CATLINKACT1	O	Ether CAT Link / Activity LED port	P04-P05	High	
CATSYNC1	O	Ether CAT SYNC1 port	P10	High	Hi-Z With internal pull-up resistor
CATSYNC0	O	Ether CAT SYNC0 port	P11	High	Hi-Z With internal pull-down resistor
CATLATCH1	I	Ether CAT LATCH1 port	P10	High	Hi-Z With internal pull-up resistor
CATLATCH0	I	Ether CAT LATCH0 port	P11	High	Hi-Z With internal pull-down resistor
CATI2CCLK	O	Ether CAT EEPROM I2C clock port	P22	-	Hi-Z
CATI2CDATA	I/O	Ether CAT EEPROM I2C data port	P23	-	
CATRESTOUT	O	Ether CAT PHY RESETOUT port	P56	-	Hi-Z With internal pull-up resistor

2.3.3 External Memory Interface Signals

Pin Name	I/O	Function	Shared Signal	Shared port	Active	Level during reset
BUSCLK	O	Bus clock output port	-	-	-	-
CSZ0	O	Chip select signal output port	HCSZ	-	Low	Hi-Z With internal pull-up resistor
CSZ1	O		HPGCSZ	P44		
CSZ2	O		-	P51		
CSZ3	O		-	P50		
A1	O	Address output port	HA1	P40	-	Hi-Z With internal pull-up resistor
A2-A20	O		HA2-HA20	-		Hi-Z With internal pull-down resistor
A21-A27	O		-	RP21-RP27		
D0-D15 Note1	I/O	Data bus port	HD0-HD15	-		
D16-D31 Note1	I/O		HD16-HD31	RP30-RP37 RP10-RP17	-	Hi-Z With internal pull-up resistor
RDZ	O	Read strobe output port	HRDZ	-	Low	Hi-Z With internal pull-up resistor
WRSTBZ	O	Write strobe output port	HWRSTBZ	-	Low	
WRZ0, WRZ1/ BENZ0, BENZ1	O	Effectively Byte lane strobe output port	HWRZ0, HWRZ1/ HBENZ0, HBENZ1	-	Low	
WRZ2, WRZ3/ BENZ2, BENZ3	O		HWRZ2, HWRZ3/ HBENZ2, HBENZ3	RP06, RP07		
WAITZ	I	Wait signal input port	HWAITZ	P41	Low	Hi-Z With internal pull-up resistor
WAITZ1-WAITZ3 Note2			-	P45-P47		
BCYSTZ / ADVZ Note3	O	Address valid output port	HBCYSTZ	RP20	Low	Hi-Z With internal pull-up resistor

Remark External Memory Interface Signal expects BUSCLK is an input signal while the internal reset signal (HRESETZ) is active.

Note1. When using synchronous burst access MEMC this port is shared with Address port when ADMUXMODE is high.

Note2. This port is available only when using synchronous burst access MEMC.

Note3. This port functions as BCYSTZ when using asynchronous SRAM MEMC, it functions as ADVZ when using synchronous burst access MEMC

2.3.4 External MPU Interface Signals

Pin Name	I/O	Function	Shared Signal	Shared port	Active	Level during reset
HBUSCLK	I	Bus clock for Host MPU output port	INTPZ11	P43	-	Hi-Z With internal pull-up resistor
HCSZ	I	Chip select signal input port	CSZ0	-	Low	
HPGCSZ	I	Pogrom mode Chip select signal input port	CSZ1	P44	Low	
HWAITZ	O	Wait signal output port	WAITZ	P41	Low	
HA1	I	Address input port	A1	P40	-	Hi-Z With internal pull-up resistor
HA2-HA20	I		A2-A20	-		Hi-Z With internal pull-down resistor
HD0-HD15	I/O	Data bus port	D0-D15	-	-	
HD16-HD31	I/O		D16-D31	RP30-RP37 RP10-RP17		Hi-Z With internal pull-up resistor
HRDZ	I	Read strobe input port	RDZ	-	Low	Hi-Z With internal pull-up resistor
HWRSTBZ	I	Write strobe output port	WRSTBZ	-	Low	
HWRZ0, HWRZ1/ HBENZ0,HBENZ1	I	Effectively Byte lane strobe input port	WRZ0, WRZ1/ BENZ0, BENZ1	-	Low	
HWRZ2, HWRZ3/ HBENZ2,HBENZ3	I		WRZ2, WRZ3/ BENZ2, BENZ3	RP06, RP07		
HERROUTZ	O	Error interrupt output port	SLEEPING	P42	Low	High
HBCYSTZ	I	Bus cycle input port	BCYSTZ / ADVZ	RP20	Low	Hi-Z With internal pull-up resistor

Caution When you use asynchronous mode, please input Low into a HBUSCLK pin..

Remark External MPU interface signals operate as an External MPU interface durinug reset.

2.3.5 Port Signals and Real-time Port Signals

Port Signals and Real-time port Signals are configured as 12 sets of 8-bit ports.
They are able to realize 32-bit access by grouping 4 ports; i.e. Ports 0-3, Ports 4-7 or Real-time ports 0-3.

(1/4)

	Port Name	Mode 1	Mode 2	Mode 3	Mode 4	Level during reset
P0	P00	INTPZ0	CATLEDRUN Note1	CCI_RUNLEDZ Note2	-	Hi-Z R-IN32M3-EC: Hi-Z (without internal resistor) R-IN32M3-CL: With internal pull-up resistor
	P01	INTPZ1	CATIRQ Note1	-	-	
	P02	INTPZ2	CATLEDSTER Note1	CCI_DLINKLEDZ Note2	-	
	P03	INTPZ3	CATLEDERR Note1	CCI_ERRLEDZ Note2	CCS_MON5	
	P04	INTPZ4	CATLINKACT0 Note1	CCI_LERR1LEDZ Note2	CCS_MON6	
	P05	INTPZ5	CATLINKACT1 Note1	CCI_LERR2LEDZ Note2	CCS_MON7	
	P06	PHYLINK0 Note2	P0LINKLEDZ Note1	CCI_SDLEDZ Note2	CCS_MON0	
	P07	PHYLINK1 Note2	P1LINKLEDZ Note1	CCI_RDLEDZ Note2	CCS_RESOUT	
P1	P10	CATLATCH1 Note1	CATSYNC1 Note1	-	CCS_REFSTB	Hi-Z With internal pull-up resistor
	P11	CATLATCH0 Note1	CATSYNC0 Note1	-	CCS_MON4	Hi-Z With internal pull-down resistor
	P12	INTPZ6	-	CCI_NMIZ Note2	-	Hi-Z With internal pull-up resistor
	P13	INTPZ7	-	CCI_WDTIZ Note2 / CCS_WDTZ / CCM_WDTENZ	-	
	P14	SMSCK	-	-	-	
	P15	SMSI	-	-	-	
	P16	SMSO	-	-	-	
	P17	SMCSZ	-	-	-	
P2	P20	RXD0	-	CCM_LINKERRZ	-	Hi-Z R-IN32M3-EC: Hi-Z (without internal resistor) R-IN32M3-CL: With internal pull-up resistor
	P21	TXD0	-	CCM_ERRZ	-	
	P22	INTPZ8	CATI2CCLK Note1	CCS_IOTENSU	-	
	P23	INTPZ9	CATI2CDATA Note1	CCS_SENYU0	-	
	P24	INTPZ10	ETHSWSECOUT	CCS_SENYU1	-	
	P25	WDTOUTZ	−	CCS_ERRZ	-	
	P26	TIN1	TOUT1	CCM_RUNZ / CCS_RUNZ	-	
	P27	TIN0	TOUT0	-	-	

Note1. Only used by R-IN32M3-EC.

Note2. Only used by R-IN32M3-CL.

(2/4)

	Port Name	Mode 1	Mode 2	Mode 3	Mode 4	Level during reset
P3	P30	RXD1	-	-	-	Hi-Z With internal pull-up resistor
	P31	TXD1	-	-	-	
	P32	DMAREQZ1	-	-	CCS_MON1	
	P33	DMAACKZ1	CCI_ WAITEDGEH Note2	-	CCS_MON2	
	P34	DMATCZ1	CCI_WRLENH Note2	-	CCS_MON3	
	P35	CSISCK1	INTPZ22	CCM_IRZ	-	
	P36	CSISI1	INTPZ23	CCS_FUSEZ	-	
	P37	CSISO1	INTPZ24	CCM_MSTZ	-	
P4	P40	A1	HA1	-	-	Hi-Z 内蔵 Pull-up 抵抗により ハイ・レベル
	P41	WAITZ	HWAITZ	-	-	
	P42	SLEEPING	HERROUTZ	CCM_SDGCZ	-	
	P43	INTPZ11	HBUSCLK	-	-	
	P44	CSZ1	HPGCSZ	-	-	
	P45	CSISCK0	WAITZ1	-	-	
	P46	CSISI0	WAITZ2	-	-	
	P47	CSISO0	WAITZ3	-	-	
P5	P50	CSZ3	-	CCM_LNKRUNZ / CCS_LNKRUNZ	-	
	P51	CSZ2	-	CCM_RDLEDZ / CCS_RDLEDZ	-	
	P52	TIN3	TOUT3	CCS_SDGATEON	-	Hi-Z With internal pull-down resistor
	P53	CRXD0	CCS_RD	CCM_RD	-	Hi-Z With internal pull-up resistor
	P54	CTXD0	CCS_SD	CCM_SD	-	
	P55	CRXD1	-	-	-	
	P56	CTXD1	CATRESTOUT Note1	CCI_PHYREZ1 Note2	-	
	P57	TIN2	TOUT2	CCI_PHYREZ0 Note2	-	

Note1. Only used by R-IN32M3-EC.

Note2. Only used by R-IN32M3-CL.

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	Port Name	Mode 1	Mode 2	Mode 3	Mode 4	Level during reset
P6	P60	SCL0	–	–	–	Hi-Z R-IN32M3-EC: Hi-Z (without internal resistor) R-IN32M3-CL: With internal pull-up resistor
	P61	SDA0	–	–	–	
	P62	RTDMAREQZ	–	CCM_MDIN0	–	
	P63	RTDMAACKZ	–	CCM_MDIN1	–	
	P64	RTDMATCZ	–	CCM_MDIN2	–	
	P65	DMAREQZ0	–	CCM_MDIN3	–	
	P66	DMAACKZ0	–	CCI_INTZ Note2	–	
	P67	DMATCZ0	–	–	–	
P7	P70	CSICS00	P0DUPLEXLEDZ Note1	CCS_STATION_NO_0 / CCM_SNIN0	–	
	P71	CSICS01	–	CCS_STATION_NO_1 / CCM_SNIN1	–	
	P72	CSICS10	P0SPEED100LEDZ Note1	CCS_STATION_NO_2 / CCM_SNIN2	–	
	P73	CSICS11	P0SPEED10LEDZ Note1	CCS_STATION_NO_3 / CCM_SNIN3	–	
	P74	INTPZ12	P1DUPLEXLEDZ Note1	CCS_STATION_NO_4 / CCM_SNIN4	–	
	P75	INTPZ13	–	CCS_STATION_NO_5 / CCM_SNIN5	–	
	P76	INTPZ14	P1SPEED100LEDZ Note1	CCS_STATION_NO_6 / CCM_SNIN6	–	
	P77	INTPZ15	P1SPEED10LEDZ Note1	CCS_STATION_NO_7 / CCM_SNIN7	–	

Note1. Only used by R-IN32M3-EC.

Note2. Only used by R-IN32M3-CL.

RP0x-RP3x are Real-time ports which can transfer data via a dedicated DMA comtroller, and are unaffected by bus congestion. They are able to perform input and output of the port by 32 bit unit in sync with DMA transfer trigger by DMA Controller for exclusive use of the Real-time port.

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	Port Name	Mode 1	Mode 2	Mode 3	Mode 4	Level during reset
RP0	RP00	INTPZ16	SCL1	CCM_SDLEDZ / CCS_SDLEDZ	–	Hi-Z With internal pull-up resistor
	RP01	INTPZ17	SDA1	CCM_SMSTZ	–	
	RP02	INTPZ18	P0ACTLEDZ Note	CCS_BS1	–	
	RP03	INTPZ19	–	CCS_BS2	–	
	RP04	INTPZ20	P1ACTLEDZ Note	CCS_BS4	–	
	RP05	INTPZ21	–	CCS_BS8	–	
	RP06	WRZ2/BENZ2	HWRZ2/HBENZ2	-	–	
	RP07	WRZ3/BENZ3	HWRZ3/HBENZ3	–	–	
RP1	RP10	D24/HD24	–	–	–	Hi-Z With internal pull-up resistor
	RP11	D25/HD25	–	–	–	
	RP12	D26/HD26	–	–	–	
	RP13	D27/HD27	–	–	–	
	RP14	D28/HD28	–	–	–	
	RP15	D29/HD29	–	–	–	
	RP16	D30/HD30	–	–	–	
	RP17	D31/HD31	–	–	–	
RP2	RP20	BCYSTZ / ADVZ	HBCYSTZ	–	–	Hi-Z With internal pull-up resistor
	RP21	A21	–	–	–	Hi-Z With internal pull-down resistor
	RP22	A22	–	–	–	
	RP23	A23	–	–	–	
	RP24	A24	INTPZ25	–	–	
	RP25	A25	INTPZ26	–	–	
	RP26	A26	INTPZ27	–	–	
	RP27	A27	INTPZ28	–	–	
RP3	RP30	D16/HD16	–	–	–	Hi-Z With internal pull-up resistor
	RP31	D17/HD17	–	–	–	
	RP32	D18/HD18	–	–	–	
	RP33	D19/HD19	–	–	–	
	RP34	D20/HD20	–	–	–	
	RP35	D21/HD21	–	–	–	
	RP36	D22/HD22	–	–	–	
	RP37	D23/HD23	–	–	–	

Note Only used by R-IN32M3-EC.

2.3.6 Serial Flash ROM Interface Signals

The Serial Flash ROM Interface supports Fast Read, Fast Read Dual Output and Fast Read Dual I/O mode.

Pin Name	I/O	Function	Shared Port	Active	Level during reset
SMSCK	O	Serial clock output port for serial flash ROM	P14	↑ / ↓	Hi-Z With internal pull-up resistor
SMSI	I/O	Serial data port for serial flash ROM (Connect to SO of serial flash ROM)	P15	High	
SMSO	I/O	Serial data port for serial flash ROM (Connect to SI of serial flash ROM)	P16	High	
SMCSZ	O	Chip select output port for serial flash ROM	P17	Low	

2.3.7 DMA Interface Signals

There are two DMA Controllers: one with four internal channels but only two external interfaces, and one with one internal channel and one external interce as real-time DMA controller.

Pin Name	I/O	Function	Shared Port	Active	Level during reset
RTDMAREQZ	I	RTDMAC DMA transfer request port	P62	Low	Hi-Z R-IN32M3-EC: Hi-Z (without internal resistor) R-IN32M3-CL: With internal pull-up resistor
RTDMAACKZ	O	RTDMAC DMA acknowledge output port	P63	Low	
RTDMATCZ	O	RTDMAC Terminal count output port	P64	Low	
DMAREQZ0	I	DMA transfer request port 0	P65	Low	
DMAACKZ0	O	DMA acknowledge output port 0	P66	Low	
DMATCZ0	O	DMA Terminal count output port 0	P67	Low	
DMAREQZ1	I	DMA transfer request port 1	P32	Low	Hi-Z With internal pull-up resistor
DMAACKZ1	O	DMA acknowledge output port 1	P33	Low	
DMATCZ1	O	DMA Terminal count output port 1	P34	Low	

Caution Each DMA interface is assigned to a specific DMA channel.
DMA channel 0 = interface 0 (DMAREQZ0, DMAACKZ0, DMATCZ0)
DMA channel 1 = interface 1 (DMAREQZ1, DMAACKZ1, DMATCZ1)
DMA channels 2, 3 = no external interface

2.3.8 External Interrupt Input Signals

Pin Name	I/O	Function	Shared Port	Active	Level during reset
NMIZ	I	Non-maskable external interrupt input port	-	Low	Hi-Z High level by internal Pull-up register
INTPZ0-INTPZ5	I	External interrupt input port	P00-P05	Low	Hi-Z R-IN32M3-EC: Hi-Z (without internal resistor) R-IN32M3-CL: With internal pull-up resistor
INTPZ6, INTPZ7			P12,P13	Low	Hi-Z With internal pull-up resistor
INTPZ8-INTPZ10			P22-P24	Low	Hi-Z R-IN32M3-EC: Hi-Z (without internal resistor) R-IN32M3-CL: With internal pull-up resistor
INTPZ11			P43	Low	Hi-Z With internal pull-up resistor
INTPZ12-INTPZ15			P74-P77	Low	Hi-Z R-IN32M3-EC: Hi-Z (without internal resistor) R-IN32M3-CL: With internal pull-up resistor
INTPZ16-INTPZ21			RP00-RP05	Low	Hi-Z With internal pull-up resistor
INTPZ22-INTPZ24			P35-P37		
INTPZ25-INTPZ28			RP24-RP27		Hi-Z With internal pull-down resistor

2.3.9 Timer I/O Signals

Pin Name	I/O	Function	Shared Port	Active	Level during reset
TIN0 / TOUT0	I/O	Timer TAUJ0 port	P27	-	Hi-Z R-IN32M3-EC: Hi-Z (without internal resistor) R-IN32M3-CL: With internal pull-up resistor
TIN1 / TOUT1	I/O	Timer TAUJ1 port	P26	-	
TIN2 / TOUT2	I/O	Timer TAUJ2 port	P57	-	Hi-Z With internal pull-up resistor
TIN3 / TOUT3	I/O	Timer TAUJ3 port	P52	-	Hi-Z With internal pull-down resistor

2.3.10 Watchdog Timer Output Signal

Pin Name	I/O	Function	Shared Port	Active	Level during reset
WDTOUTZ	O	Watchdog Timer output port	P25	Low	Hi-Z R-IN32M3-EC: Hi-Z (without internal resistor) R-IN32M3-CL: With internal pull-up resistor

2.3.11 Trace Signals

Pin Name	I/O	Function	Active	Level during reset
TRACECLK	O	Trace port clock output port	-	-
TRACEDATA3- TRACEDATA0	O	Trace port data output port	-	Low

2.3.12 CPU Power Control Signal

Pin Name	I/O	Function	Shared Port	Active	Level during reset
SLEEPING	O	CPU SLEEP mode output port	P42	High	Hi-Z With internal pull-up resistor

2.3.13 Serial Interface Signals

Pin Name	I/O	Function	Shared Port	Active	Level during reset
TXD0	O	UART0 serial data output port	P21	-	Hi-Z R-IN32M3-EC: Hi-Z (without internal resistor) R-IN32M3-CL: With internal pull-up resistor
RXD0	I	UART0 serial data input port	P20	-	
TXD1	O	UART1 serial data output port	P31	-	Hi-Z With internal pull-up resistor
RXD1	I	UART1 serial data input port	P30	-	
CSISCK0	I/O	CSI0 serial clock port	P45	-	
CSISI0	I	CSI0 serial data input port	P46	-	
CSISO0	O	CSI0 serial data output port	P47	-	
CSICS00,CSICS01	O	CSI0 chip select 0,1 port	P70, P71	Low	Hi-Z R-IN32M3-EC: Hi-Z (without internal resistor) R-IN32M3-CL: With internal pull-up resistor
CSISCK1	I/O	CSI1 serial clock port	P35	-	Hi-Z With internal pull-up resistor
CSISI1	I	CSI1 serial data input port	P36	-	
CSISO1	O	CSI1 serial data output port	P37	-	
CSICS10,CSICS11	O	CSI1 chip select 0,1 port	P72, P73	Low	Hi-Z R-IN32M3-EC: Hi-Z (without internal resistor) R-IN32M3-CL: With internal pull-up resistor
SCL0	I/O	I2C0 serial clock port	P60	-	
SDA0	I/O	I2C0 serial data port	P61	-	
SCL1	I/O	I2C1 serial clock port	RP00	-	Hi-Z With internal pull-up resistor
SDA1	I/O	I2C1 serial data port	RP01	-	
CRXD0	I	CAN0 receive data port (5V-Tolerant buffer)	P53	-	
CTXD0	O	CAN0 transfer data port	P54	-	
CRXD1	I	CAN1 receive data port (5V-Tolerant buffer)	P55	-	
CTXD1	O	CAN1 transfer data port	P56	-	

2.3.14 CC-Link IE Field (Intelligent device station) Signals (R-IN32M3-CL only)

Pin Name	I/O	Function	Shared Port	Active	Level during reset
CCI_RUNLEDZ	O	RUN LED control port	P00	Low	Hi-Z With internal pull-up resistor
CCI_DLINKLEDZ	O	Cyclic communication status check LED control port	P02	Low	
CCI_ERRLEDZ	O	Field Network Error LED control port	P03	Low	
CCI_LERR1LEDZ	O	Link error LED control port 1	P04	Low	
CCI_LERR2LEDZ	O	Link error LED control port 2	P05	Low	
CCI_SDLEDZ	O	Transfer data LED control port	P06	Low	
CCI_RDLEDZ	O	Receive data LED control port	P07	Low	
CCI_NMIZ	O	Output NMI interrupt to MPU	P12	Low	Hi-Z With internal pull-up resistor
CCI_WDTIZ	I	Input from Watchdog Timer	P13	Low	
CCI_WAITEDGEH	I/O	Wait Synchronized edge setting 0：rise edge mode 1：low edge mode	P33	-	
CCI_WRLENH	I/O	WRL enable setting 0：byte write enable mode 1：byte enable mode	P34	-	
CCI_PHYREZ1	O	PHY reset output 1 port	P56	Low	
CCI_PHYREZ0	O	PHY reset output 0 port	P57	Low	
CCI_INTZ	O	Output Interrupt signal to MPU	P66	Low	
CCI_CLK2_097M	I	2.097152MHz clock	-	-	-

2.3.15 CC-Link Signals (Intelligent device station)

Pin Name	I/O	Function	Shared Port	Active	Level during reset
CCM_LINKERRZ	O	Link error LED control port	P20	Low	Hi-Z R-IN32M3-EC: Hi-Z (without internal resistor) R-IN32M3-CL: With internal pull-up resistor
CCM_ERRZ	O	Error LED control port	P21	Low	
CCM_RUNZ	O	RUN LED control port	P26	Low	
CCM_MDIN0- CCM_MDIN3	I	Mode setting switch input port	P62-P65	-	
CCM_SNIN0- CCM_SNIN7	I	Station No. setting switch port	P70-P77	-	
CCM_LNKRUNZ	O	Link RUN LED control port	P50	Low	Hi-Z With internal pull-up resistor
CCM_RDLEDZ	O	Receive data LED control port	P51	Low	
CCM_SDLEDZ	O	Transfer data LED control port	RP00	Low	
CCM_IRZ	O	Interrupt output port	P35	Low	
CCM_WDTENZ	I	Watchdog Timer error input port	P13	Low	
CCM_MSTZ	O	Operation check LED port	P37	Low	
CCM_SMSTZ	O	Stand-by master LED control port	RP01	Low	
CCM_RD	I	Data receive port	P53	-	
CCM_SD	O	Data transfer port	P54	-	
CCM_SDGCZ	O	Transfer data & gate control port	P42	Low	
CCM_CLK80M	I	CC-Link Clock	-	-	-

2.3.16 CC-Link Signals (Remote device station)

Caution To use a remote device station, it is necessary to connect a CCS_REFSTB pin to an external interrupt pin (INTPZ).

Pin Name	I/O	Function	Shared Port	Active	Level during reset
CCS_MON1-CCS_MON3	O	Monitor port	P32-P34	-	Hi-Z With internal pull-up resistor
CCS_MON4	O	Monitor port	P11	-	Hi-Z With internal pull-down resistor
CCS_MON0	O	Monitor port	P06	-	Hi-Z R-IN32M3-EC: Hi-Z (without internal resistor) R-IN32M3-CL: With internal pull-up resistor
CCS_MON5-CCS_MON7	O	Monitor port	P03-P05	-	
CCS_RESOUT	O	reset port	P07	High	
CCS_IOTENSU	I	Initial setting port	P22	-	
CCS_SENYU0	I	Initial setting port	P23	-	
CCS_SENYU1	I	Initial setting port	P24	-	
CCS_ERRZ	O	Operation check LED port	P25	Low	
CCS_RUNZ	O	Operation check LED port	P26	Low	
CCS_STATION_NO_0-CCS_STATION_NO_7	I	Station No. setting switch port	P70-P77	-	
CCS_LNKRUNZ	O	Link RUN LED control port	P50	Low	Hi-Z With internal pull-up resistor
CCS_REFSTB	O	Interrupt port	P10	High	
CCS_WDTZ	I	Watchdog Timer port	P13	Low	
CCS_RDLEDZ	O	Receive data LED control port	P51	Low	
CCS_RD	I	Data receive port	P53	-	
CCS_SD	O	Data transfer port	P54	-	
CCS_SDLEDZ	O	Operation check LED port	RP00	Low	
CCS_SDGATEON	O	Transfer data & gate control port	P52	High	Hi-Z With internal pull-down resistor
CCS_BS1	I	Baud rate setting switch port	RP02	-	Hi-Z With internal pull-up resistor
CCS_BS2	I	Baud rate setting switch port	RP03	-	
CCS_BS4	I	Baud rate setting switch port	RP04	-	
CCS_BS8	I	Baud rate setting switch port	RP05	-	
CCS_FUSEZ	I	Fuse cutting signal port	P36	Low	
CCM_CLK80M	I	CC-Link operation lock	-	-	-

2.3.17 System Signals

Pin Name	I/O	Function	Active	Level during reset
XT1	I	Crystal Oscillator ports for system clock *Oscillator output connects to X2 for direct connection.	-	-
XT2	I/O		-	-
RESETZ	I	Reset input port	Low	-
HOTRESETZ Note1	I	Hot reset Input port	Low	—
PONRZ	I	Internal RAM Power on reset input port	Low	-
OSCTH	I	Input High level when external clock input mode	-	-
JTAGSEL	I	JTAG Operation mode setting port	-	-
RSTOUTZ	O	Reset to external circuit output port	Low	-
CLKOUT25M0	O	PHY clock output port	—	—
CLKOUT25M1	O	PHY clock output port	—	—
PLL_VDD	-	PLL power supply (1.0V)	-	-
PLL_GND	-	PLL power Ground supply (GND)	-	-
VDD33	-	I/O power supply (3.3V)	-	-
VDD10	-	Internal power supply (1.0V)	-	-
GND	-	Ground supply (GND)	-	-
VDDQ_MII Note1	-	Ethernet I/O power supply (3.3V)	-	-
LX Note2	O	Regulator 1.5V power Output	—	—
EXTRES Note2	-	Reference resistor for EtherPHY connect port	—	—
P0VDDARXTX Note2	-	Analog Port Rx/Tx power supply (1.5V) - Port 0	-	-
P1VDDARXTX Note2	-	Analog Port Rx/Tx power supply (1.5V) - Port 0	-	-
VDDACB Note2	-	EtherPHY Analog Central power supply (3.3V)	-	-
AGND Note2	-	EtherPHY Analog Ground supply (GND)	-	-
VDD15 Note2	-	EtherPHY power supply (1.5V)	-	-
VDDAPLL Note2	-	EtherPHY Analog Central power supply (1.5V)	-	-
VSSAPLLCB Note2	-	EtherPHY Analog Central Ground supply (GND)	-	-
VDD33ESD Note2	-	EtherPHY Analog Test power supply (3.3V)	-	-
AVDD_REG Note2	-	Regulator Analog power supply (3.3V)	-	-
AGND_REG Note2	-	Regulator Analog Ground supply (GND)	-	-
BVDD Note2	-	Regulator power supply (3.3V)	-	-
BGND Note2	-	Regulator Ground supply (GND)	-	-
FB Note2	I <R>	Regulator Feedback port	-	-
VDDQ_PECL_B0 Note2	-	PECL Buffer supply (3.3V)	-	-
VDDQ_PECL_B1 Note2	-	PECL Buffer supply (3.3V)	-	-

Note1. Only applies to R-IN32M3-CL.

Note2. Only applies to R-IN32M3-EC.

2.3.18 Test Signals

Pin Name	I/O	Function	Active	Level during reset
TMODE0-TMODE2	I	Test mode select port	-	-
TMS	I/O	JTAG mode select port	-	-
TDI	I	JTAG serial data input port	-	-
TDO	O	JTAG serial data output port	-	-
TRSTZ	I	JTAG reset port	Low	-
TCK	I	JTAG clock input port	-	-
ATP Note	I	Renesas test ports		
TMC1	I		-	-
TMC2	I		-	-
TEST1 Note	I		-	-
TEST2 Note	I		-	-
TEST3 Note	I		-	-
TESTOUT5 Note	O		-	-

Note Only applies to R-IN32M3-EC.

2.3.19 Operation Mode Setting Signal

Pin Name	I/O	Function	Active	Level during reset
BOOT1-BOOT0	I	Boot mode select port 00 : External memory boot 01 : External serial flash ROM boot 10 : External MPU boot 11 : Instruction RAM boot(debugger used ONLY)	-	-
MEMIFSEL	I	External Memory Interface select port 0 : Slave memory Interface 1 : External MPU Interface	-	-
BUS32EN	I	External Memory Interface Bus width select port 0 : 16bit bus 1 : 32bit bus	-	-
HIFSYNC	I	External MPU I/F Operation mode select port 0 : asynchronous SRAM Interface 1 : synchronous SRAM Interface	-	-
HWRZSEL	I	External MPU Interface HWRZ/HBENZ select port 0 : HBENZ use 1 : HWRZ use	-	-
MEMCSEL	I	Internal Memory Controller select port 0 : asynchronous SRAM MEMC 1 : synchronous burst access MEMC	-	-
ADMUXMODE Note	I	Multiplex of Address / Data port Note 0 : Separate 1 : Multiplex of Address / Data	-	-

Note ADMUXMODE port is only available when MEMCSEL port is High (which selects synchronous burst access MEMC). The asynchronous SRAM MEMC does not support address/data multiplexing.

2.4 Buffer Types and Recommended Connections for Unused Pins

2.4.1 Ethernet Signals

(1) PHY Interface Signals

Caution These signals apply to R-IN32M3-CL only.

Pin Name	I/O	Interface	Recommended connection when not in use
ETH0_TXC	I	Input Buffer (3.3V)	Connect to GND
ETH0_GTXC	O	BID_BUF(3.3V_GMII_MII)_with_IOLH_Control	Open
ETH0_TXEN			
ETH0_TXER			
ETH0_TXD0- ETH0_TXD7			
ETH0_GE_INT	I	Input Buffer (3.3V)	Connect to GND
ETH0_RXC	I	BID_BUF (3.3V_GMII_MII)_with_IOLH_Control	Connect to GND
ETH0_RXDV			
ETH0_RXER			
ETH0_RXD0- ETH0_RXD7			
ETH0_CRS	I	Input Buffer (3.3V)	Connect to GND
ETH0_COL			
ETH1_TXC			
ETH1_GTXC	O	BID_BUF (3.3V_GMII_MII)_with_IOLH_Control	Open
ETH1_TXEN			
ETH1_TXER			
ETH1_TXD0- ETH1_TXD7			
ETH1_GE_INT	I	Input Buffer (3.3V)	Connect to GND
ETH1_RXC	I	BID_BUF (3.3V_GMII_MII)_with_IOLH_Control	Connect to GND
ETH1_RXDV			
ETH1_RXER			
ETH1_RXD0- ETH1_RXD7			
ETH1_CRS	I	Input Buffer (3.3V)	Connect to GND
ETH1_COL			
ETH_MDC	O	Output Buffer (3.3V) 6mA	Open
ETH_MDIO	I/O	I/O Buffer (3.3V) 6mA	Connect to GND

(2) Media Interface Signals

Caution These signals apply to R-IN32M3-EC only.

Pin Name	I/O	Interface	Recommended connection when not in use
P0_RX_P	I	3.3V Analog Input Buffer	Open
P0_RX_N	I		
P1_RX_P	I		
P1_RX_N	I		
P0_TX_P	O	3.3V Analog Input Buffer	Open
P0_TX_N	O		
P1_TX_P	O		
P1_TX_N	O		
P0_SD_P	I	3.3V PECL Input Buffer	Connect to GND
P0_SD_N	I		
P1_SD_P	I		
P1_SD_N	I		
P0_RD_P	I		
P0_RD_N	I		
P1_RD_P	I		
P1_RD_N	I		
P0_TD_OUT_P	O	3.3V PECL Output Buffer	Open
P0_TD_OUT_N	O		
P1_TD_OUT_P	O		
P1_TD_OUT_N	O		
P0_FX_EN_OUT	O	Output Buffer (3.3V) 12mA	Open
P1_FX_EN_OUT	O		

2.4.2 External Memory/ MPU Interface Signals

Pin Name	I/O	Interface	Recommended connection when not in use
BUSCLK	O	Output Buffer (3.3V) 9mA	Open
CSZ0 / HCSZ	I/O	I/O Buffer (3.3V) 6mA 50kΩ Pull-up	Open
A2-A20 / HA2-HA20	I/O	I/O Buffer (3.3V) 6mA 50kΩ Pull-down	Open
D0-D15 / HD0-HD15			
RDZ / HRDZ	I/O	I/O Buffer (3.3V) 6mA 50kΩ Pull-up	Open
WRSTBZ / HWRSTBZ			
WRZ0, WRZ1 / BENZ0, BENZ1 / HWRZ0, HWRZ1			

2.4.3 System Signals

Pin Name	I/O	Interface	Recommended connection when not in use
NMIZ	I	Input Buffer (3.3V) Schmitt in 50kΩ Pull-up	Connect to VDD33 (3.3V)
XT1	I	Oscillator with EN	Connect to GND
XT2	-		-
RSTOUTZ	O	Output Buffer (3.3V) 6mA	Open
RESETZ	I	Input Buffer (3.3V) Schmitt in	-
PONRZ			
HOTRESETZ			Connect to VDD33 (3.3V)
OSCTH	I	Input Buffer (3.3V) Schmitt in, 50kΩ Pull-down	-
JTAGSEL			

2.4.4 Test Signals

Pin Name	I/O	Interface	Required Connection when not in use
TMODE0-TMODE2	I	Input Buffer (3.3V) Schmitt in, 50kΩ Pull-down	Connect to GND
TMS	I/O	I/O Buffer (3.3V) 6mA 50kΩ Pull-up	Open
TDI	I	Input Buffer (3.3V) , 50kΩ Pull-up	Open
TDO	O	3-state Output Buffer (3.3V) 6mA	Open
TRSTZ	I	Input Buffer (3.3V) Schmitt in 50kΩ Pull-up	Open
TCK	I	Input Buffer (3.3V) , 50kΩ Pull-down	Open
TMC1	I	(TMC1) Input Buffer (3.3V) for TMC Terminal	Connect to GND
TMC2	I	(TMC2) Input Buffer (3.3V) for TMC Terminal	Connect to GND
ATP Note	I	Input Buffer (3.3V)	Open
TEST1 Note	I	Input Buffer (3.3V)	Connect to GND
TEST2 Note	I	Input Buffer (3.3V)	
TEST3 Note	I	Input Buffer (3.3V)	
TESTDOUT5 Note	O	Output Buffer (3.3V)	Open

Note These signals apply to R-IN32M3-EC only.

2.4.5 Port Signals

(1/2)

Pin Name	I/O	Interface	Recommended connection when not in use
P00-P07	I/O	[R-IN32M3-EC] I/O Buffer (3.3V) (6mA) [R-IN32M3-CL] Programmable I/O Buffer (3.3V) Load Drive select function (6mA, 12mA) Resistor select function (50kΩ Pull-up or 50kΩ Pull-down or neither)	R-IN32M3-EC : Connect to GND R-IN32M3-CL : Open
P10	I/O	Programmable I/O Buffer (3.3V) Load Drive select function (6mA, 12mA) Resistor select function (50kΩ Pull-up or 50kΩ Pull-down or neither)	Open
P11-P17	I/O	Programmable I/O Buffer (3.3V)(6mA) Resistor select function (50kΩ Pull-up or 50kΩ Pull-down or neither)	Open
P20-21, P25-26	I/O	[R-IN32M3-EC] I/O Buffer (3.3V) (6mA) [R-IN32M3-CL] Programmable I/O Buffer (3.3V) Load Drive select function (6mA, 12mA) Resistor select function (50kΩ Pull-up or 50kΩ Pull-down or neither)	R-IN32M3-EC : Connect to GND R-IN32M3-CL : Open
P22-24, 27	I/O	[R-IN32M3-EC] I/O Buffer (3.3V) (6mA) [R-IN32M3-CL] Programmable I/O Buffer (3.3V) (6mA) Resistor select function (50kΩ Pull-up or 50kΩ Pull-down or neither)	
P30, P31	I/O	Programmable I/O Buffer (3.3V) Load Drive select function (6mA, 12mA) Resistor select function (50kΩ Pull-up or 50kΩ Pull-down or neither)	Open
P32-P36	I/O	Programmable I/O Buffer (3.3V)(6mA) Resistor select function (50kΩ Pull-up or 50kΩ Pull-down or neither)	
P37	I/O	Programmable I/O Buffer (3.3V) Load Drive select function (6mA, 12mA) Resistor select function (50kΩ Pull-up or 50kΩ Pull-down or neither)	

(2/2)

Pin Name	I/O	Interface	Recommended connection when not in use
P40-P47	I/O	Programmable I/O Buffer (3.3V)(6mA) Resistor select function (50kΩ Pull-up or 50kΩ Pull-down or neither)	Open
P50-P52	I/O	Programmable I/O Buffer (3.3V) Load Drive select function (6mA, 12mA) Resistor select function (50kΩ Pull-up or 50kΩ Pull-down or neither)	
P53-P56	I/O	5V-tolerant I/O Buffer 4mA 50kΩ Pull-up	
P57	I/O	Programmable I/O Buffer (3.3V)(6mA) Resistor select function (50kΩ Pull-up or 50kΩ Pull-down or neither)	
P60, P65-P67	I/O	[R-IN32M3-EC] I/O Buffer (3.3V) (6mA) [R-IN32M3-CL] Programmable I/O Buffer (3.3V) (6mA) Resistor select function (50kΩ Pull-up or 50kΩ Pull-down or neither)	R-IN32M3-EC : Connect to GND R-IN32M3-CL : Open
P61-P64	I/O	[R-IN32M3-EC] I/O Buffer (3.3V) (6mA) [R-IN32M3-CL] Programmable I/O Buffer (3.3V) Load Drive select function (6mA, 12mA) Resistor select function (50kΩ Pull-up or 50kΩ Pull-down or neither)	
P70-P77	I/O	[R-IN32M3-EC] I/O Buffer (3.3V) (6mA) [R-IN32M3-CL] Programmable I/O Buffer (3.3V) (6mA) Resistor select function (50kΩ Pull-up or 50kΩ Pull-down or neither)	R-IN32M3-EC : Connect to GND R-IN32M3-CL : Open
RP00-RP07 RP10-RP17 RP20-RP27 RP30-RP37	I/O	Programmable I/O Buffer (3.3V) Load Drive select function (6mA, 12mA) Resistor select function (50kΩ Pull-up or 50kΩ Pull-down or neither)	Open

2.4.6 Operation Mode Setting Signals

Pin Name	I/O	Interface	Recommended connection when not in use
BOOT0, BOOT1	I	Input Buffer (3.3V) Schmitt in	-
MEMIFSEL			
BUS32EN			
HIFSYNC			
HWRZSEL			
MEMCSEL			
ADMUXMODE			

2.4.7 CC-Link IE Field (Intelligent device station) Signal (R-IN32M3-CL Only)

Pin Name	I/O	Interface	Recommended connection when not in use
CCI_CLK2_097M	I	Input Buffer (3.3V)	2.097152MHz clock input

Caution This pin is needed clock input even if user does not use CC-Link IE Field function.

2.4.8 CC-Link Signal (Intelligent device station, Remote device station)

Pin Name	I/O	Interface	Recommended connection when not in use
CCM_CLK80M	I	Input Buffer (3.3V)	Connect to GND

2.4.9 Trace Signals

Pin Name	I/O	Interface	Recommended connection when not in use
TRACECLK	O	Output Buffer (3.3V) 6mA	Open
TRACEDATA[3:0]			

3. Specifications

This chapter includes information specific to the R-IN32M3 series.

3.1 CPU (Cortex-M3)

The R-IN32M3 includes high-efficiency 32-bit (ARM Cortex-M3 core) processor.

3.1.1 CPU Core Information

The version of the Cortex-M3 core included in R-IN32M3 is shown below..
More information about the architecture of the CPU can be obtained from:.
http://infocenter.arm.com/help/topic/com.arm.doc.set.cortexm/index.html

Product Name	Core revision
R-IN32M3 Series (R-IN32M3-EC/CL)	Cortex-M3 r2p1

3.1.2 CPU Core Configuration

The Cortex-M3 included in R-IN32M3 has the following configuration.

Category	Configuration Item	Setting	Remark
Process	Process	CB90-MR	Arbitrary value
Interrupts	NUM_IRQ	128	Non-maskable Interrupt (NMI) + 1 to 240 physical interrupts
Interrupt Priority Levels	LVL_WIDTH	4	Priority Bit Number 3 to 8 (8 to 256 priority levels)
MPU	MPU_PRESENT	Yes	Memory Protection is present
Debug Level	DEBUG_LVL	3	Debug Level 1 to 3
Trace Level	TRACE_LVL	2	Trace Level 0 to 2
SW/SWJ-DP Select	JTAG_PRESENT	SWJ-DP	SWJ-DP selected in case of JTAG Access circuit built-in.
Bit Band Area	BB_PRESENT	Yes	Bit band function is present

Debug Level	1	2	3 (R-IN32M3's setting)
Function outline	Minimum Debug configuration	Full Debug configuration (Data Matching function: unavailable)	Full Debug configuration (Data Matching function: available)
Debug Halt	Yes	Yes	Yes
Breakpoints	2 (Instruction)	6 (Instruction) 2 (Literal)	6 (Instruction) 2 (Literal)
DWT comparator number	1 (Data Matching function: unavailable)	4 (Data Matching function: unavailable)	4
Flash patch function	No	Yes	Yes

Trace Level	0	1	2 (R-IN32M3's setting)
Function outline	Non-Trace	Standard Trace	Full Trace
ITM, TPIU Function	No	Yes	Yes
DWT Trigger and Counter	No	Yes	Yes
ETM Function	No	No	Yes

Caution R-IN32M3 does not support SLEEPDEEP mode;
please do not set the SLEEPDEEP bit of the SCR register to "1".

3.2 Giga bit Ethernet MAC

3.2.1 Features

- Port Number : 1Port (2port switch built-in)
- 10BASE, 100BASE, 1000BASE MAC Function
- 1000BASE-X PCS support
- Full-duplex and Half-duplex Communication support
- Automatic pause packet transmission function
- Automatic suspend function when receiving pause packet
- MII/GMII Interface

3.2.2 Switch functions

R-IN32M3 includes the following switch features:

- Integrated Ethernet Switch engine
- Two port interfaces with integrated 10/100 or 10/100/1000 MAC modules
- Implements hardware switching, look-up and filtering
- QoS Support with frame priority classification for flexible output queue management
- Priority Classification based on VLAN Priority (IEEE802.1q) with priority remapping
- Optional Classification and Priority assignment based on Ipv4 DiffServ Code Point Field, Ipv6 Class of Service
- Implements 4 priority queues with strict priority on the line interfaces
- Supports Ethernet Multicast, Broadcast with flooding control to avoid unnecessary duplication of frames
- Supports VLAN frames reception and transmission (TBD)
- Cut-Through/Hub Extension Module
- Device Level Ring (DLR) Extension Module (TBD)

3.3 EtherCAT Slave Controller Function (R-IN32M3-EC only)

The EtherCAT Slave Controller (ESC) core is made by Beckhoff Automation GmbH, Germany.

The ESC processes EtherCAT communications and acts as interface between EtherCAT Field bus and Slave applications.

Table 3.1 Features of the EtherCAT Slave Controller

Feature	R-IN32M3-EC	ET1100	Remark
Ports	2	2-4	-
FMMUs	8	8	-
SyncManagers	8	8	-
RAM [KByte]	8	8	-
Distributed Clocks	64bit	64bit	-
EBus	No	Yes (0-4)	-
Process Data Interfaces			
Digital I/O	No	Yes	-
SPI Slave	No	Yes	-
External MPU Interface	Cortex-M3 and 16bit/32bit, async./sync. SRAM Host Interface	8bit/16bit, async./sync.	R-IN32M3 does not support direct access to the ESC from an external CPU.

3.4 CC-Link IE Field (Intelligent device station) Function (R-IN32M3-CL only)

The outline specifications of CC-Link IE Field network are as follows.

Please refer to the following URL of CC-Link Partner Association (CLPA) for additional details and specifications for the CC-Link IE Field core.

http://www.cc-link.org/jp/cclink/cclinkie/index.html

Table 3.2 CC-Link IE Field Outline Specifications

Item	Specification
Ethernet Standards	IEEE802.3ab (1000BASE-T) compliant
Communication speed	1Gbps
Topology	Line, star, ring
Maximum number of connected units	254 modules (total of master and slave stations)
Maximum station-to-station distance	100m

3.5 General DMA Controller

3.5.1 Features

- Instances : 4 channels (each channel is independent)
- Transfer data size
  - Independently selectable source and destination size
  - Size range: 8- bit to 512-bit
- Maximum number of transfer bytes : 2^{32}-1
- Channel priority control
  - Fixed priority mode
  - Round robin mode
- DMA Transfer methods
  - Register mode :
    DMA transfer is performed using the values set in the control registers of the DMA controller written by the CPU. This mode supports conventional general DMA transfer.
  - Link mode :
    DMA transfer is performed according to a descriptor located in Data RAM and external memory. The responsiveness of this mode is inferior to register mode because access of the descriptor occurs at every DMA transfer.
- Skip function
  Continuous access size and discrete access size can each be set for the areas that are accessed with DMA transfer. Following access of the set size, it is possible to skip to the next address to be accessed.
- Intra-buffer data sweep function
  The data in the buffer can be output when the DMAC is forcibly stopped. After sweeping, DMA transfers continue sequentially.
- Suspend function
  Execution of a DMA transaction can be paused (suspended).
- DMA transfers interval setting function
  The interval between DMA transfers can be set in order to adjust the bus usage rate.
- Transfer mode
  - Single transfer mode
    When a DMA transfer request is acknowledged, the DMAC controls and then releases the bus once for each transfer. Additional DMA requests are required for each subsequent transfer.
  - Block transfer mode
    When DMA transfer request is acknowledged, the DMAC takes control of the bus and repeats data transmission until completion of the number of transfers indicated bhy the control register.. But this mode does not occupy the bus.

Caution Please align data at 512-bit boundaries for 512-bit transfers.

3.6 DMA Controller for Real-time Port

3.6.1 Features

- Instances : 1 channel
- Transfer data size
  - Independently selectable source and destination size
  - Size range : 8-bit to 128-bit
- Maximum number of transfer bytes : 2^{32}-1
- DMA Transfer methods
  - Register mode :
    DMA transfer is performed using the values set in the control registers of the DMA controller written by the CPU. This mode supports the conventional general DMA transfer.
  - Link mode :
    DMA transfer is performed according to a descriptor located in Data RAM and external memory. The responsiveness of this mode is inferior to register mode because the access of the descriptor occurs at every DMA transfer.
- SKIP function
  Continuous access size and discrete access size can each be set for the areas that are accessed with DMA transfer. Following access of the set size, it is possible to skip to the next address to be accessed.
- Intra-buffer data sweep function
  The data in the buffer can be output when the DMAC is forcibly stopped. After sweeping, DMA transfers continue sequentially.
- Suspend function
  Execution of a DMA transaction can be paused (suspended).
- DMA transfers interval setting function
  The interval between DMA transfers can be set in order to adjust the bus usage rate.
- Transfer mode
  - Single transfer mode
    When a DMA transfer request is acknowledged, the DMAC controls and then releases the bus once for each transfer. Additional DMA requests are required for each subsequent transfer.
  - Block transfer mode
    When DMA transfer request is acknowledged, the DMAC takes control of the bus and and repeats data transmission until completion of the number of transfers indicated by the control register. But this mode does not occupy the bus.

Caution Please align data at 128-bit boundaries for 128-bit transfer.

3.7 Watchdog Timer

3.7.1 Features

- Configuration after reset is based on option settings
- Software triggered start mode
- Error mode options
  - Generates NMI on error detection
  - Generates Reset on error detection
- Window watchdog function
- Overflow interval time
  - 25MHz operation : 163µs to 5.36s

3.8 Timer Array Unit

3.8.1 Features

- 1 Unit (4 channels)
- 32-bit counter and 32-bit data registers per channel
- Independent channel operation
- Synchronous channel operation (master and slave operation)
- Generation of different types of output signals
- Counter can be triggered by an external signal
- Interrupt generation

Independent channel operation	Synchronous channel operation
Independent channel operation functions	Synchronous channel operation function
Interval timer function	PWM output function
External input interval timer function	
Independent channel signal measurement functions	
Overflow interrupt output function (during External width measurement)	
External input period count detection function	
External input pulse interval judgment function	
External input signal width judgment function	
Other independent channel function	
External input position detection function	

- Supplement

Timers support prescaler options: selectable count clock from among four types of internal clocks as well as from an external clock. Each timer may be configured to PCLK frequency divided by 2^0 to 2^{15} , and one clock may be configured to be divided by 1 to 256.

3.9 Asynchronous Serial Interface

3.9.1 Features

- Full-duplex communication via built-in receive and transmit FIFOs
  - Internal 10-bit x 16 receive data FIFO
  - Internal 8-bit x 16 transmit data FIFO
- 2-pin configuration
  - Transmit data output pin
  - Receive data input pin
- Error detection functions
  - Rx parity error
  - Rx framing error
  - Tx data consistency error
- Tx FIFO overflow error
  - Rx FIFO overrun error
  - Rx timeout error
  - Rx BF receive error
- FIFO status information
  - Rx FIFO full/empty status
  - Tx FIFO empty/empty status
  - Rx FIFO fill level
  - Tx FIFO fill level
- Interrupt requests: 3
  - Transmission interrupt
  - Reception interrupt
  - Status interrupt
- Character length: 7 or 8-bits
- Parity options: odd, even, 0, none
- Transmission stop bits: 1 or 2-bits
- MSB-/LSB-first transfer selectable
- Transmit/receive data inverted input/output option
- 13 to 20 bits selectable for the BF (Break Field) in the LIN (Local Interconnect Network) communication format
  - Recognition of 11 bits or more possible for BF reception in LIN communication format
  - BF reception flag provided
- BF reception can be detected during data communication
- Bus monitor function to keep data consistency of the transmit data
- Supported Baud rate: 300 to 12,500,000bps (TBD)

Table 3.3 Baud rate generator clocks output (PCLK：100MHz)

Baud rate (bps)	Prescaler Clock (PRSCLK) Divisor “URTJnPRS”	Baud Rate Clock (BRCLK) Divisor “URTJnBRS”	ERR (%)
300	6	2604	0.01
600	5	2604	0.01
1200	4	2604	0.01
2400	3	2604	0.01
4800	2	2604	0.01
9600	1	2604	0.01
19200	0	2604	0.01
31250	0	1600	0.01
38400	0	1302	0.01
76800	0	651	0.01
115200	0	434	0.01
153600	0	326	-0.15
312500	0	160	0.00
1000000	0	50	0.00
2000000	0	25	0.00
2500000	0	20	0.00
5000000	0	10	0.00
6250000	0	8	0.00
1000000	0	5	0.00
1250000	0	4	0.00

3.10 Clocked Serial Interface

3.10.1 Features

- Three-wire serial synchronous data transfer
- Selectable master mode or slave mode
- Multiple slave configuration plus RCB (Recessive Configuration for Broadcasting) thanks to two configurable chip select output signals (selectable chip selec priority)
- Built-in baud rate generator
- Adjustable baud rate; in slave mode it is determined by the input clock
- Maximum transmission speed: (at 100MHz PCLK operation)
  - in master mode: PCLK/4
  - in slave mode: PCLK/6
- Phase of clock and data selectable
- Data transfer with MSB or LSB first selectable
- Transfer data length selectable from 7 to 16 bits in 1-bit increments
- Extended data length (EDL) function for transferring more than 16 bits of data
- Three selectable transfer modes:
  - Transmission mode
  - Reception mode
  - Transmission/reception mode
- Error detection (data consistency check, parity, timeout, overflow, overrun)
- Full support of job concept
- 128 words I/O buffer memory
- Memory mode selectable (FIFO, dual buffer, Tx-only buffer, direct access)
- Four different interrupt request signals
  - communication interrupt
  - reception interrupt
  - error interrupt
  - job completion interrupt
- Loop back mode (LBM) function for self-test

3.11 I2C BUS

3.11.1 Features

- Operating mode
  - Standard mode (SCL clock frequency: 100 kHz max.)
  - Fast mode (SCL clock frequency: 400 kHz max.)
- Transfer mode
  - Single transfer mode
  - Continuous transfer mode
- Pin configuration
  - Serial clock pin
  - Serial transmit/receive data pin
- Interrupt request signal
  - Data transmit/receive interrupt request signal
  - Status interrupt request signal
- Communication data length
  - 8 bits
- Multi master support
  - Multiple masters can control the bus simultaneously.
- Serial clock signal level width
  - Serial clock signal (SCLn) high- and low-level pulse width can be changed.
- Automatic detection
  - Start and stop conditions can be detected automatically

3.12 CC-Link Function

The outline specifications of CC-Link are as follows.
Please refer to the following URL for the additional details of CC-Link.

http://www.cc-link.org/jp/cclink/index.html

Table 3.4 CC-Link outline specifications

Item	Specification
Version	Ver1.10 and Ver.2.00
Kind of supported station	Intelligent device station (TBD), Remote device station
Max. number of link points	Remote I/O : 8192 points each, Remote register : 2048 words
Max. number of units connect	64 units
Communication speed and max. overall cable extension length	10Mbps : 100m 5Mbps : 160m 2.5Mbps : 400m 625kbps : 900m 156kbps : 1200m
Communication system	Broadcast polling system

Caution To use a remote device station, it is necessary to connect a CCS_REFSTB pin to an external interrupt pin (INTPZ).

3.13 CAN Controller

3.13.1 Features

- Compliant with ISO-11898
- Standard frame and extended frame transmission/reception enabled
- Transfer rate: 1 Mbps max.
- 64 message buffers per channel
- Receive/transmit history list function (can be set individually for each message buffer)
- Automatic block transmission function
- Multi-buffer receive block function
- Mask setting of 8 patterns is possible for each channel, applicable for data and remote frames
- Data bit time, communication baud rate and sample point can be controlled
  - For example : 66.7%, 70.0%, 75.0%, 80.0%, 81.3%, 85.0%, 87.5%
  - Baud rates in the range of 10 kbps up to 1 Mbps can be configured
- Enhanced features :
  - Each message buffer can be configured to operate as a transmit or a receive message buffer
  - A transmission request can be aborted by clearing the Transmit-Request flag of the relevant message buffer. Supported by Transmission Abort Interrupt, on successful abortion.
  - Automatic block transmission operation mode (ABT)
  - Time stamp function in collaboration with timers capture channels
  - A centralized global data update bit monitor register makes it possible to check all data update bits from one location

3.14 External MPU Interface

The external MPU interface supports connection of an external MPU. Note that the External MPU interface signals are shared with the Asynchronous SRAM MEMC and synchronous burst access MEMC ports. Set MEMIFSEL to high to use these signals for an external MPU rather than for an external memory interface. When BOOT[0-1] is set to 1'b01, the device will boot from memory connected to CSZ0. Please set MEMIFSEL pin level and hold it until after reset release ; dynamic switching of MEMIFSEL is not supported.

3.14.1 Features

(1) External MPU Interface

- Interface direction
  - SRAM (Read, Write) with WAIT output
  - page ROM (Read) with WAIT output
- Synchronization-related
  - HBUSCLK sync, async (set by HIFSYNC pin)

Caution When you use asynchronous mode, please input Low into a HBUSCLK pin..

- Bus width
  - 32-bit, 16-bit (set by BUS32EN pin)

Remark 8 bit bus width is not supported.

- Transfer data size
  - 32-bit, 16-bit, 8-bit
- Buffer function
  - Write buffer : 1 step
  - Read buffer : Max. 32-Byte prefetch supported
- Transfer type
  - Single transfer
  - Page read transfer
- Timing control function

(2) AHB Master port function

- AMBA Ver2.0 following
  - 32-bit AHB-Lite
  - Little endian fixed
- Address conversion
  - Accusable to 2MByte area in AHB memory area (4GByte) from external MPU
- Bus sizing function
  - External 16-bit => 32-bit
- Error response function
  - Output interrupt request (HERROUTZ) in case of receiving error response
  - Stored the access information of the cause of error in the register

(3) Status check function

- Check status of:
  - Internal reset
  - HIFSYNC pin and BUS32EN pin states

3.15 Asynchronous SRAM MEMC

Asynchronous SRAM MEMC can be connected to page ROM, ROM, SRAM or other peripheral device thar provides a 16- or 32-bit SRAM interface.

Asynchronous SRAM MEMC's signals are shared with the same ports used for synchronous burst access MEMC and the External MPU interface; please set MEMCSEL and MEMIFSEL low to enable Asynchronous SRAM MEMC mode..

When BOOT0 is low and BOOT1 is high, the device will boot from memory connected to CSZ0.

3.15.1 Features

- Memory controller supporting page ROM, ROM, SRAM
- 32- or 16-bit data Bus
- Static memory control function
  - Supports SRAM and peripheral devices with SRAM interface
  - Page ROM support (supported STCSZ0 only)
  - Four chip select signals are available (STCSZ0-STCSZ3)

    STCSZ0 : page ROM / SRAM : 1000 0000H-13FF_FFFFH (64MByte)

    STCSZ1 : SRAM only：1400 0000H-17FF_FFFFH (64MByte)

    STCSZ2 : SRAM only：1800 0000H-1BFF_FFFFH (64MByte)

    STCSZ3 : SRAM only：1C00 0000H-1FFF_FFFFH (64MByte)
- Programmable wait function
  - Address setting wait
  - Data wait
  - Write recovery wait
  - Idle state

3.16 Synchronous burst access MEMC

The Synchronous burst access MEMC can be connected to page ROM, ROM, SRAM, PSRAM, NOR-Flash and other peripheral devices which provide a 16- or 32-bit SRAM interface.

It can also support multiplexed address/data signals when ADMUXMODE pin is set high.

Synchronous burst access MEMC's signals are shared with the same ports used for asynchronous SRAM MEMC and External MPU interface; please set MEMCSEL high and MEMIFSEL low to enable synchronous burst access MEMC mode.

When BOOT0 is low and BOOT1 is high, the device will boot from memory connected to CSZ0.

3.16.1 Features

- Memory controller supports page ROM, ROM, SRAM (sync or async), PSRAM and NOR-Flash
- 32- or 16-bit data Bus
- Address / data multiplex option

Remark Page access is supported in async access mode only.

- Static memory control function
  - SRAM (sync or async) and other peripheral devices which provide a 16- or 32-bit SRAM interface
  - Four chip select signals is available (CSZ0-CSZ3)

    CSZ0 : 1000 0000H-13FF_FFFFH (64MByte)

    CSZ1 : 1400 0000H-17FF_FFFFH (64MByte)

    CSZ2 : 1800 0000H-1BFF_FFFFH (64MByte)

    CSZ3 : 1C00 0000H-1FFF_FFFFH (64MByte)

Remark Each CS can be set between 1000_0000H - 1FFF_FFFFH by the programmable SMADSEL register .

- Programmable wait setting functions
  - Data wait
  - Write recovery wait
  - Idle state
- Memory access frequency option (by dividing 100MHz signal by 2 to 6)
- Up to four wait state signals available (WAITZ0 - WAITZ3)

3.17 Instruction RAM

Instruction RAM is 768Kbytes of memory that can be accessed from I-code AHB, D-code AHB, DMAC or an external MPU.

3.17.1 Features

- 128-bit (32-bit x 4) read buffer
- Low latency :
  - Read latency: 2 (1 for accessing read buffer)
  - Write latency: 1
- 32-bit AHB Bus
- 128-bit RAM data bus width (without ECC circuit)
- Selectable 16- or 32-bit transfer size
- Burst transmission: single, imprecise burst, precise burst (INCR4/8/16, WRAP4/8/16)
- Little endian fixed

3.17.2 Read buffer features

- 128-bit (32bit x 4) read buffer
- Reply to AHB with 0 wait in cases of accessing read buffer
- Clear the data in the read buffer in case of 2-bit ECC error
- A 2-bit ECC error at the time of the read response generates an ECC error interrupt and treats it as an error response of the AHB bus.

3.17.3 Write interface features

- 16-bit write access is supported; when two 16-bit words are written to IRAM, they are automatically merged into a 32-bit word in the RAM.
- Error is generated on 8-bit write attempts

Caution Always ensure external host MPU writed 32-bits at a time.

3.18 Data RAM

Data RAM is 512Kbytes of memory that can be accessed from AHB and the Ethernet Accelerator (Header Endec (encoder/decoder)).

3.18.1 Features

- AHB latency:
  - Read / write latency 1 (latency 2 for read access after write access)
- Communication bus latency : 1 for read /write access
- Round-robin bus arbitration
- 32-bit AHB bus width
- 128-bit Communication bus width
- 128-bit RAM Bus width (without ECC)
- AHB transfer size : 8/16/ 32-bit selectable
- Communication bus transfer size : 8/16/32/128-bit selectable
- Burst transmission : single, imprecise burst, precise burst (INCR4/8/16, WRAP4/8/16)
- Little endian fixed

3.19 Buffer RAM

Buffer RAM is 64KByte of memory that can be accessed by the AHB and Communication busses.

3.19.1 Features

- Communication bus latency: 1 for read / write access
- Fixed-priority communication bus arbitration
- 128-bit communication bus width
- 128-bit RAM bus width (without ECC)
- Communication bus transfer size: 8/16/32/128-bit selectable

3.20 Hardware Real-time OS

The Hardware Real-time OS supports 30 types of system-calls including event, semaphore and mailbox.

3.20.1 Features

- Task Scheduler
  - Hardware ISR : Maximum 32 selectable from 128 QINTs
  - Contexts : 64
  - Semaphores : 128
  - Events : 64
  - Mailboxes : 64
  - Mailbox elements : 92
  - Context priorities: 16
- Hardware Function Manager

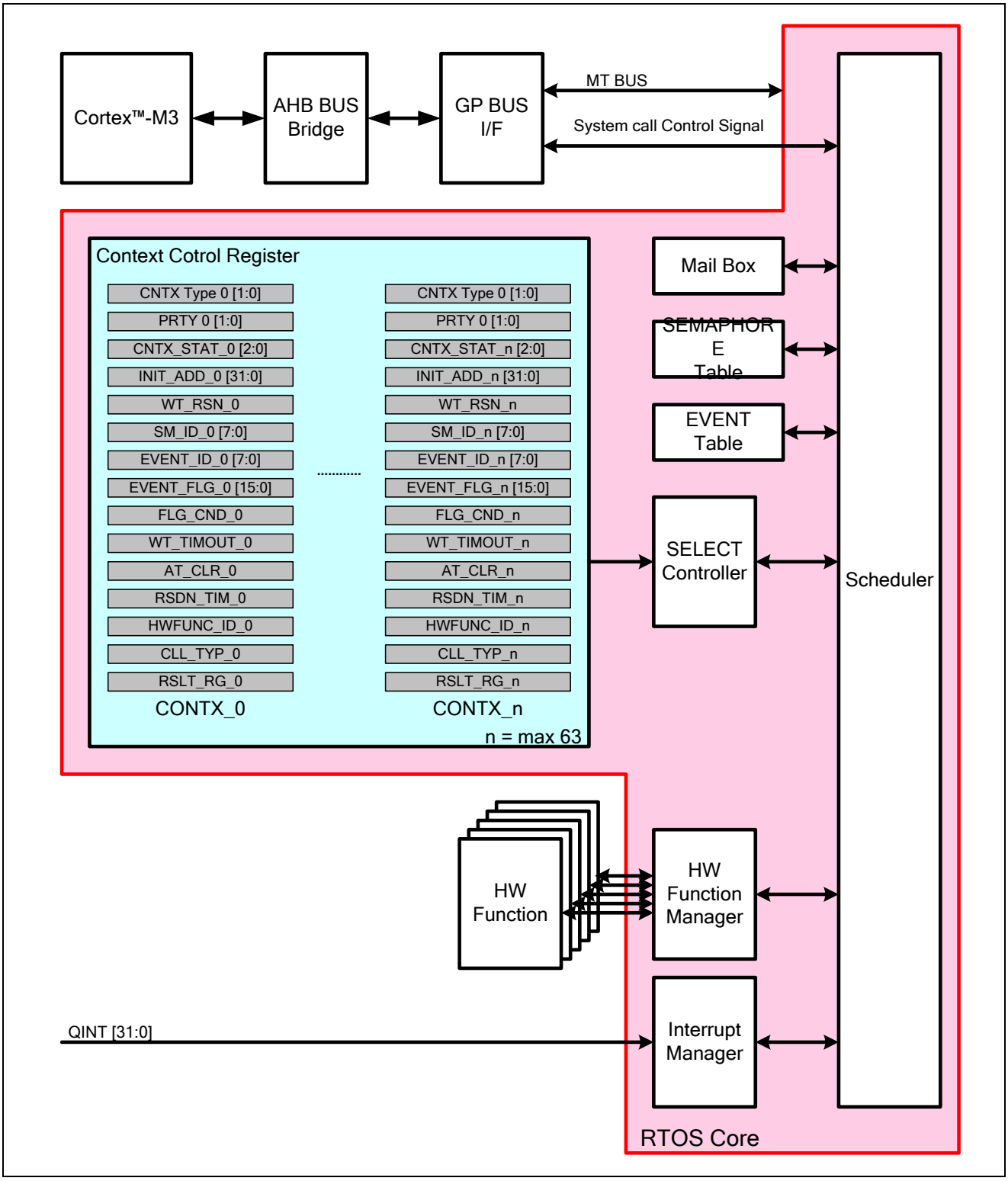


Figure 3.1 Structure of Hardware Real-time OS

3.20.2 Service Calls

(1/3)

Item		Name	Function	HW-RTOS Driver	µITRON Ver. 4.0 Standard Profile
Task management functions		act_tsk	Active task	-	√
		iact_tsk	Active task	-	√
		can_act	Cancel task activation request	-	√
		sta_tsk	Active task (with a start code)	√	-
		ext_tsk	Terminate and delete invoking task	√	√
		ter_tsk	Terminate task	√	√
		chg_pri	Change task priority	√	√
		get_pri	Reference task priority	√	√
Task dependent synchronization functions		slp_tsk	Put task to sleep	√	√
		tslp_tsk	Put task to sleep (with timeout)	√	√
		wup_tsk	Wakeup task	√	√
		iwup_tsk	Wakeup task	√	√
		can_wup	Cancel task wakeup request	√	√
		rel_wai	Release task from waiting	√	√
		irel_wai	Release task from waiting	√	√
		sus_tsk	Suspend task	-	√
		frsm_tsk	Forcibly resume suspended task	-	√
		dly_tsk	Delay task	-	√
Task exception handling functions		ras_tex	Raise task exception handling	-	√
		iras_tex	Raise task exception handling	-	√
		dis_tex	Disable task exception	-	√
		ena_tex	Enable task exception	-	√
		sns_tex	Reference task exception handling state	-	√
Synchronization and communication functions	Semaphore	cre_sem	Create semaphore	√	-
		del_sem	Delete semaphore	√	-
		wai_sem	Acquire semaphore resource	√	√
		pol_sem	Acquire semaphore resource (polling)	√	√
		twai_sem	Acquire semaphore resource (with timeout)	√	√
		sig_sem	Release semaphore resource	√	√
		isig_sem	Release semaphore resource	√	√

(2/3)

Item		Name	Function	HW-RTOS Driver	µITRON Ver. 4.0 Standard Profile
Synchronization and communication functions	Eventflag	cre_flg	Create eventflag	√	-
		del_flg	Delete eventflag	√	-
		set_flg	Set eventflag	√	√
		iset_flg	Set eventflag	√	√
		clr_flg	Clear eventflag	√	-
		wai_flg	Wait for eventflag	√	√
		pol_flg	Wait for eventflag (polling)	√	√
		twai_flg	Wait for eventflag (with timeout)	√	√
	Data queue	snd_dtq	Send to data queue	-	√
		psnd_dtq	Send to data queue (polling)	-	√
		ipsnd_dtq	Send to data queue (polling)	-	√
		tsnd_dtq	Send to data queue (with timeout)	-	√
		fsnd_dtq	Forced send to data queue	-	√
		ifsnd_dtq	Forced send to data queue	-	√
		rcv_dtq	Receive from data queue	-	√
		prcv_dtq	Receive from data queue (polling)	-	√
	Mailbox	cre_mbx	Create mailbox	√	-
		del_mbx	Delete mailbox	√	-
		snd_mbx	Send to mailbox	√	√
		rcv_mbx	Receive from mailbox	√	√
		prcv_mbx	Receive from mailbox (polling)	√	√
		trcv_mbx	Receive from mailbox (with timeout)	√	√
Extended synchronization and communication functions	Mutex	cre_mtx	Create Mutex	√	-
		del_mtx	Delete Mutex	√	-
		loc_mtx	Lock Mutex	√	-
		ploc_mtx	Lock Mutex (polling)	√	-
		tloc_mtx	Lock Mutex (with timeout)	√	-
		unl_mtx	Unlock Mutex	√	-
Memory pool management functions (fixed-sized)		get_mpf	Acquire fixed-sized memory block	-	√
		pget_mpf	Acquire fixed-sized memory block (polling)	-	√
		tget_mpf	Acquire fixed-sized memory block (with timeout)	-	√
		rel_mpf	Release Variable-sized memory block	-	√

(3/3)

Item	Name	Function	HW-RTOS Driver	µITRON Ver. 4.0 Standard Profile
Time management functions	set_tim	Set system time	√	√
	get_tim	Acquire system time	√	√
	isig_tim	Supply time tick	-	√
System state management functions	rot_rdq	Rotate task precedence	√	√
	irot_rdq	Rotate task precedence	√	√
	get_tid	Acquire task ID in the running state	√	√
	iget_tid	Reference task ID in the running state	√	√
	loc_cpu	Lock the CPU	√	√
	iloc_cpu	Lock the CPU	-	√
	unl_cpu	Unlock the CPU	√	√
	iunl_cpu	Unlock the CPU	-	√
	sns_loc	Reference CPU state	√	√
	dis_dsp	Disable dispatching	√	√
	ena_dsp	Enable dispatching	√	√
	sns_dsp	Reference dispatching state	-	√
	sns_dpn	Reference dispatching pending state	-	√

3.21 Port Functions

The ports RP0 - RP3 provide dedicated interfaces to the AHB bus separate from other ports and enables, allowing for real-time 32-bit data transmission.

For each register, grouping into 8, 16, or 32 bit-access is supported.

3.21.1 Features

- 96 I/O ports
- Shared with I/O ports of other peripheral circuits
- Ports can be designated as input or output on a1-bit basis

Caution1. When changing the Port Mode Control (PMCTn) registers, shared signals may generate spike noise.
Therefore, please take the following general spike noise countermeasures via software:
- **Change signals only after stopping operation of the related internal peripheral circuits**
- **Release the mask after clearing the interrupt request flag in ports shared with interrupt signals**
- **Change mode after setting the output value.**

Caution2. Please do not supply intermediate voltage from external sources because input buffers are not protected against input through current. Make sure inputs are “full-rail” 0 or 1.

3.21.2 Configuration

There are 8 ports of 3 state I/O port and 4 ports controlling in real time built-in. Input and output configuration is possible to 1 bit unit. The port is a basic 8 bits unit, but can read / write by the 32bit unit that aligned P0x - P3x, P4x - P7x, RP0x - RP3x. (x = 0 to 7) In addition, real-time port (RP0x - RP3x) can input and output in sync with interrupt.

For each register, grouping into 8, 16, or 32 bit-access is supported.

4. Electrical Specifications

4.1 Terminology

Table4.1 Terms Used in Absolute Maximum Ratings

Parameter	Symbol	Meaning
Power supply voltage	V_{DD}	Indicates the voltage range within which damage or reduced reliability will not result when power is applied to a VDD pin.
Input voltage	V_I	Indicates the voltage range within which damage or reduced reliability will not result when power is applied to an input pin.
Output voltage	V_O	Indicates the voltage range within which damage or reduced reliability will not result when power is applied to an output pin.
Output current	I_O	Indicates the absolute tolerance value for DC current to prevent damage or reduced reliability when a current flows out of or into an output pin.
Operating ambient temperature	T_A	Indicates the ambient temperature range for normal logic operations.
Storage temperature	T_{stg}	Indicates the element temperature range within which damage or reduced reliability will not result while no voltage or current is being applied to the device.

Table4.2 Terms Used in Recommended Operating Range Ratings

Parameter	Symbol	Meaning
Power supply voltage	V_{DD}	Indicates the voltage range for normal logic operations that occur when VSS = 0 V.
Input voltage, high	V_{IH}	Indicates the voltage, which is applied to the input pins of R-IN32M3, is the voltage indicates that the high level state for normal operation of the input buffer. -If a voltage that is equal to or greater than the “Min.” value is applied, the input voltage is guaranteed as a high level voltage.
Input voltage, low	V_{IL}	Indicates the voltage, which is applied to the input pins of R-IN32M3, is the voltage indicates that the low level state for normal operation of the input buffer. -If a voltage that is equal to or less than the “Max.” value is applied, the input voltage is guaranteed as a low level voltage.
Positive trigger voltage	V_P	Indicates the input level at which the output level is inverted when the input to R-IN32M3 is changed from the low-level side to the high-level side.
Negative trigger voltage	V_N	Indicates the input level at which the output level is inverted when the input to R-IN32M3 is changed from the high-level side to the low-level side.
Hysteresis Voltage	V_H	Indicates the differential between the positive trigger voltage and the negative trigger voltage.
Input rise time	t_{rid}, t_{ric}, t_{ris}	Indicates the limit value for the time period when an input voltage applied to R-IN32M3 rises from 10% to 90%. trid, tric, and tris each indicate the input rise time for the data clock and Schmitt buffer.
Input fall time	t_{fid}, t_{fic}, t_{fis}	Indicates the limit value for the time period when an input voltage applied to R-IN32M3 falls from 90% to 10%. trid, tric, and tris each indicate the input fall time for the data clock and Schmitt buffer.

Table4.3 Terms Used for DC Characteristics

Parameter	Symbol	Meaning
Static current consumption	I_{DDS}	Indicates the current that flows from the power supply pins when the rated power supply voltage is being applied without any changes in the input or output pin voltage.
Off-state output current	I_{OZ}	Indicates the current that flows from the power supply pins when the rated power supply voltage is applied when a 3-state output has high impedance.
Output short circuit current	I_{OS}	Indicates the current that flows when the output pins are shorted (to GND pins) when output is at high level.
Input leakage current	I_{LI}	Indicates the current that flows via an input pin when a voltage is applied to that pin.
Output current, low	I_{OL}	Indicates the current that flows to the output pins when the rated low-level output voltage is being applied.
Output current, high	I_{OH}	Indicates the current that flows from the output pins when the rated high-level output voltage is being applied.
Output voltage, low	V_{OL}	Indicates the output voltage at low level and when the output pin is open.
Output voltage, high	V_{OH}	Indicates the output voltage at high level and when the output pin is open.

4.2 solute Maximum Ratings

Table4.4 Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	V_{DD}	1.0V type	-0.5 to +1.4	V
		3.3V type	-0.5 to +4.6	V
I/O voltage	V_I/V_O	3.3V buffer $V_I/V_O < V_{DD} + 0.5V$	-0.5 to +4.6	V
		5V-Tolerant buffer $V_I/V_O < V_{DD} + 3.0V$	-0.5 to +6.6	V
Output current (3.3V buffer)	I_O	6mA type	15	mA
		12mA type	25	mA
Output current (5V-Tolerant buffer)	I_O	4mA type	10.35	mA
Operating ambient temperature	T_A	-	-40 to +85	°C
Storage temperature	T_{stg}	-	-65 to +125	°C

Caution **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

Remark **3.3 V must be applied to the I/O pins only after applying the power supply voltage.**

4.3 Recommended Operating Conditions

Table4.5 Recommended Operating Conditions

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage	V_{DD}	1.0V power supply	0.9	1.0	1.1	V
		3.3V power supply	3.0	3.3	3.6	V
Negative trigger voltage	V_N	3.3V buffer	0.6	-	1.8	V
		5V-Tolerant buffer	0.8	-	1.1	V
Positive trigger voltage	V_P	3.3V buffer	1.2	-	2.4	V
		5V-Tolerant buffer	1.7	-	2.2	V
Hysteresis voltage	V_H	3.3V buffer	0.3	-	1.5	V
		5V-Tolerant buffer	0.9	-	1.1	V
Input voltage, low	V_{IL}	3.3V buffer	-0.3	-	0.8	V
		5V-Tolerant buffer	0	-	0.8	V
Input voltage, high	V_{IH}	3.3V buffer	2.0	-	V_{DD} + 0.3	V
		5V-Tolerant buffer	2.0	-	5.5	V
Input rise/fall time	t_{rid}	-	0	-	200	ns
	t_{fid}	-	0	-	200	ns
Input rise/fall time (Clock)	t_{ric}	-	0	-	4	ns
	t_{fic}	-	0	-	4	ns
Input rise/fall time (Schmitt input)	t_{ris}	-	0	-	1	ms
	t_{fis}	-	0	-	1	ms
Operating ambient temperature	T_A	-	-40	-	85	°C

4.4 DC Characteristics

Table4.6 DC Characteristics (VDD = 3.3 ± 0.3 V, TA = –40 to +85°C) (1/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Supply current (R-IN32M3-EC)	I_{DD}	$V_I = V_{DD}$ or GND	Internal regulator using	-	-	-	
			1.0V	-	270	880	mA
			3.3V	-	210	220	mA
			Internal regulator not using			-	
			1.0V		270	880	mA
			3.3V		120	130	mA
			1.5V	-	150	170	mA
Supply current (R-IN32M3-CL)	I_{DD}	$V_I = V_{DD}$ or GND	1.0V	-	280	890	mA
			3.3V	-	45	50	mA
Off-state current	I_{OZ}	$V_I = V_{DD}$ or GND	3.3V output	-	-	±10	μA
			5V-Tolerant buffer	-	-	±10	μA
Output short circuit current Note	I_{OS}	V_O = GND	-	-	-	-250	mA
Input leakage current (3.3V buffer)	I_I	$V_I = V_{DD}$ or GND	Normal input	-	-	±10	μA
		V_I = GND	With Pull-up resistor (5kΩ)	-293.8	-645.7	-1181.3	μA
			With Pull-up resistor (50kΩ)	-28.9	-65.7	-129.8	μA
		$V_I = V_{DD}$	With Pull-down resistor (50kΩ)	10.2	43.4	83.9	μA
Input leakage current (5V-Tolerant buffer)	I_I	V_I = GND	With Pull-down resistor (50kΩ)	39.0	-	100.9	μA

Note The output short circuit time is no more than one second and is only for one pin on the LSI.

Remark In the notes for the table, the (+) and (–) signs indicate the current direction. Current flowing to the device is indicated by (+) and current flowing out is indicated by (–).

Table4.7 DC Characteristics (VDD = 3.3 ± 0.3 V, TA = –40 to +85°C) (2/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low (3.3V buffer)	I_{OL}	V_{OL} = 0.4V	6 mA type	6.0	-	-	mA
			12 mA type	12.0	-	-	mA
Output current, low (5V-Tolerant buffer)	I_{OL}	V_{OL} = 0.4V	4mA type	4.0	-	-	mA
Output current, high (3.3V buffer)	I_{OH}	V_{OH} = 2.4V	6 mA type	-6.0	-	-	mA
			12 mA type	-12.0	-	-	mA
Output current, high (5V-Tolerant buffer)	I_{OH}	V_{OH} = 2.4V	4mA type	-4.0	-	-	mA
Output voltage, low	V_{OL}	I_{OL} = 0mA	3.3V buffer	-	-	0.1	V
			5V-Tolerant buffer	-	-	0.1	V
Output voltage, high	V_{OH}	I_{OL} = 0mA	3.3V buffer	VDD - 0.1	-	-	V
			5V-Tolerant buffer	VDD - 0.1	-	-	V

4.5 Pull-up/Pull-down Resistor Values

Table4.8 Pull-up/Pull-down Resistor Values (VDD = 3.3 ± 0.3 V, TA = –40 to +85°C)

Parameter	Library specification	MIN.	TYP.	MAX.	Unit
Pull-up resistor (3.3V buffer)	50kΩ	27.7	50.2	103.9	kΩ
Pull-up resistor (5V-Tolerant buffer)	50kΩ	35.7	51.2	77.0	kΩ
Pull-down resistor (3.3V buffer)	50kΩ	42.9	76.1	295.5	kΩ

4.6 Power-on/off sequence

Power structure of the R-IN32M3 series is internal power (VDD10 : 1.0V) and I/O power (VDD33 : 3.3V) and PHY power supply (VDD15 : 1.5V) . (PHY power is subject only R-IN32M3-EC.)

Power is recommended to put the I/O power (VDD33 : 3.3V) after switching on the internal power supply (VDD10 : 1.0V). In addition, power-off is recommend internal power-off(VDD1 : 1.0V) after cut-off of I/O power(VDD33 : 3.3V).

In the case of supplying internal power after I/O power,

Please note that I/O value becomes an indefinite due to uncertain mode while I/O is powered on but internal power isn't , regardless of an input(output)mode. Also, 3.3 V must be applied to the I/O pins only after applying the power supply voltages.

Power on/off time difference, that regardless of the power-on sequence, it does not matter which power supply is applied to (or removed from) the device first (VDD1/IVDD or VDD3/EVDD), but it is recommended to ensure 100ms or less time difference between the application or removal of each power supply. The 100ms or less time measurement is based on the period from 10% to 90% of each voltage range.

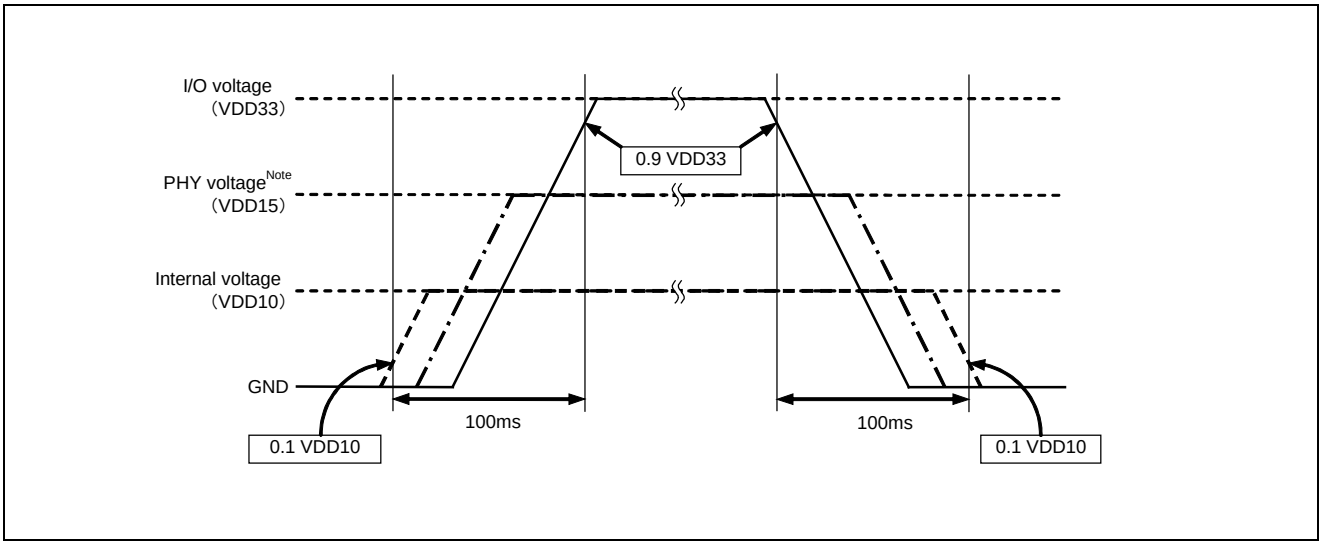


Figure 4.1 Recommended sequence of Power-on/off

Note The timing for PHY power supply voltage VDD15 only needs to be observed, when the internal regulator in the R-IN32M3-EC device is not used.

4.7 AC characteristics

4.7.1 Clock signals

(1) Input clock characteristics

Parameter	Symbol	Conditions	MIN	MAX	Unit
XT1, XT2	t_{SYSCLK}	-	25 ± 50ppm		MHz
ETH0_TXC, ETH1_TXC	t_{TXC}	-	-	25	MHz
ETH0_RXC, ETH1_RXC	t_{RXC}	-	-	125	MHz
CCM_CLK80M	t_{CCLCLK}	-	80 ± 50ppm		MHz
CLK2_097M	$t_{CCLIECLK}$	-	2.097 ± 100ppm		MHz
HBUSCLK	$t_{HBUSCLK}$	-	-	50	MHz
CSISCK0, CSISCK1	$t_{CSISSCK}$	Slave mode	-	16.6	MHz
TCK	t_{TCK}	-	-	50.	MHz

(2) Output clock characteristics

Parameter	Symbol	Conditions	MIN	MAX	Unit
BUSCLK output cycle	t_{BUSCLK}	C_L = 15pF	10	-	ns
BUSCLK high level width	t_{BCKH}		0.5 × t_{BUSCLK} - 2.0	0.5 × t_{BUSCLK} + 2.0	ns
BUSCLK low level width	t_{BCKL}		0.5 × t_{BUSCLK} - 2.0	0.5 × t_{BUSCLK} + 2.0	ns
BUSCLK rise time	t_{BCKR}		-	1.2	ns
BUSCLK fall time	t_{BCKF}		-	1.2	ns
CLKOUT25M output cycle	t_{CO25M}	C_L = 15pF	40	-	ns
CLKOUT25M high level width	t_{CO25MH}		0.5 × t_{BUSCLK} - 5.3	0.5 × t_{BUSCLK} + 5.3	ns
CLKOUT25M low level width	t_{CO25ML}		0.5 × t_{BUSCLK} - 5.3	0.5 × t_{BUSCLK} + 5.3	ns
CLKOUT25M rise time	t_{CO25MR}		-	3.4	ns
CLKOUT25M fall time	t_{CO25MF}		-	3.4	ns
ETC_GTXC output frequency	t_{GTXC}	C_L = 13pF	-	125	MHz
CSISCK output frequency	$t_{CSIMSCK}$	Master mode C_L = 15pF	-	25	MHz
SCL output frequency	t_{SCL}	High speed mode C_L = 30pF	-	400	KHz
SMSCK output frequency	t_{SMSCK}	C_L = 15pF	-	50	MHz
CATI2CCLK output frequency	$t_{ECIICCLK}$	C_L = 30pF	-	148.8	kHz
TRACECLK output frequency	$t_{TRACECLK}$	C_L = 15pF	-	50	MHz

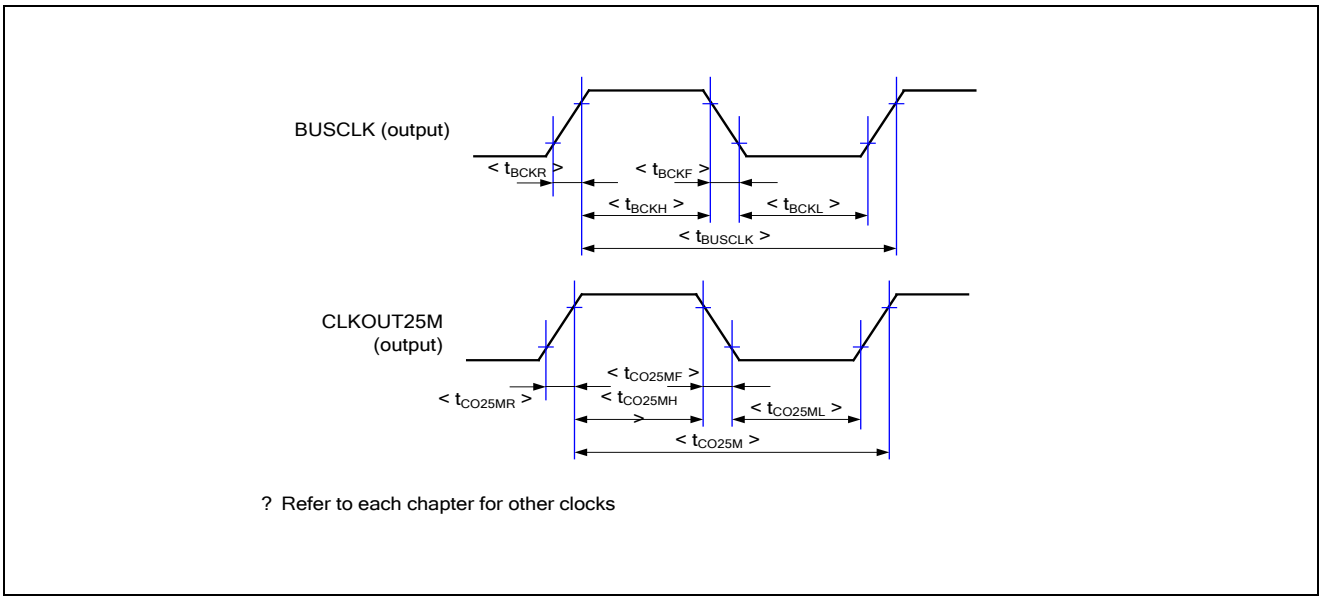


Figure 4.2 Output clock timing diagram

4.7.2 Reset signals

Parameter	Symbol	Conditions	MIN	MAX	Unit
RESETZ low level width	t_{WRSL}	-	The time required for the time (until the external oscillator be stable + 1usec) <R>	-	ns
HOTRESETZ low level width	t_{WHRSL}	-		-	ns
PONRZ low level width	t_{WPRSL}	-		-	ns
PONRZ input timing	t_{SKPR}	-	0	-	ns

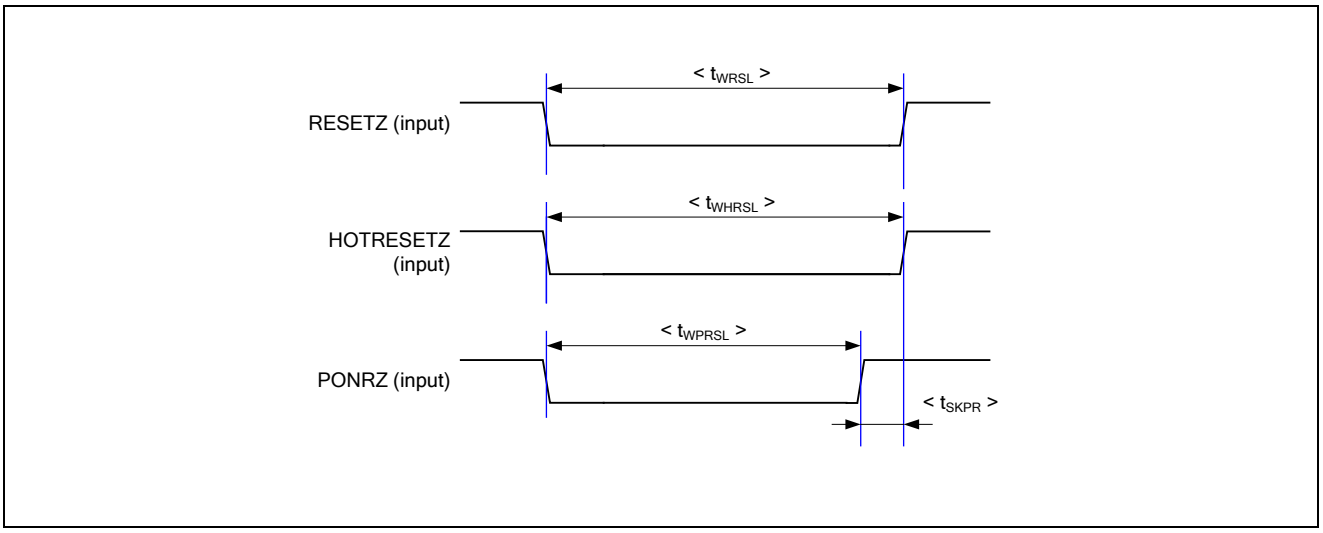


Figure 4.3 Reset timing diagram

4.7.3 External memory interface signals

(1) Delay value calculation method

The transition delay of the external memory interface pins depend on the capacirtive load driven, including both load input pins and substrate / PCB capacitance. The table below shows how to calculate the delay based on capacitive load.

Drive capability	Delay value per pF (ns)	
	MIN.	MAX.
6mA	0.026	0.067
12mA	0.012	0.034

example）

When an address pin (6-mA output buffer) has 30-pF load, the actual delay is as follows.

MIN. 1.0ns(The MIN delay value at the time of 0 pF) + (0.026×30) ns = 1.78ns
MAX. 7.0ns(The MAX delay value at the time of 0 pF) + (0.067×30) ns = 9.01ns

(2) Asynchronous SRAM MEMC access timing

Parameter	Symbol	MIN	MAX	Unit
Address, CSZ0-CSZ3 output delay time	t_{DKA}	1.0 (1.78) Note	7.0 (9.01) Note	ns
RDZ output delay time	t_{DKRD}	1.0 (1.78) Note	7.0 (9.01) Note	ns
WRZ0 - WRZ3 (BENZ0-BENZ3), WRSTBZ output delay time	t_{DKWR}	1.0 (1.78) Note	7.0 (9.01) Note	ns
BCYSTZ output delay time	t_{DKBSL}	1.0 (1.78) Note	7.0 (9.01) Note	ns
WAITZ input setup time	t_{SKW}	4.0	-	ns
WAITZ input hold time	t_{HKW}	0	-	ns
Date input setup time	t_{SKID}	4.0	-	ns
Data input hold time	t_{HKID}	0	-	ns
Date output delay time	t_{DKOD}	1.0 (1.78) Note	7.0 (9.01) Note	ns
Data float delay time	t_{HKOD}	1.0 (1.78) Note	7.0 (9.01) Note	ns

Note. Values in parenthesis are based on a 30pF capacitive load.

(a) Read timing

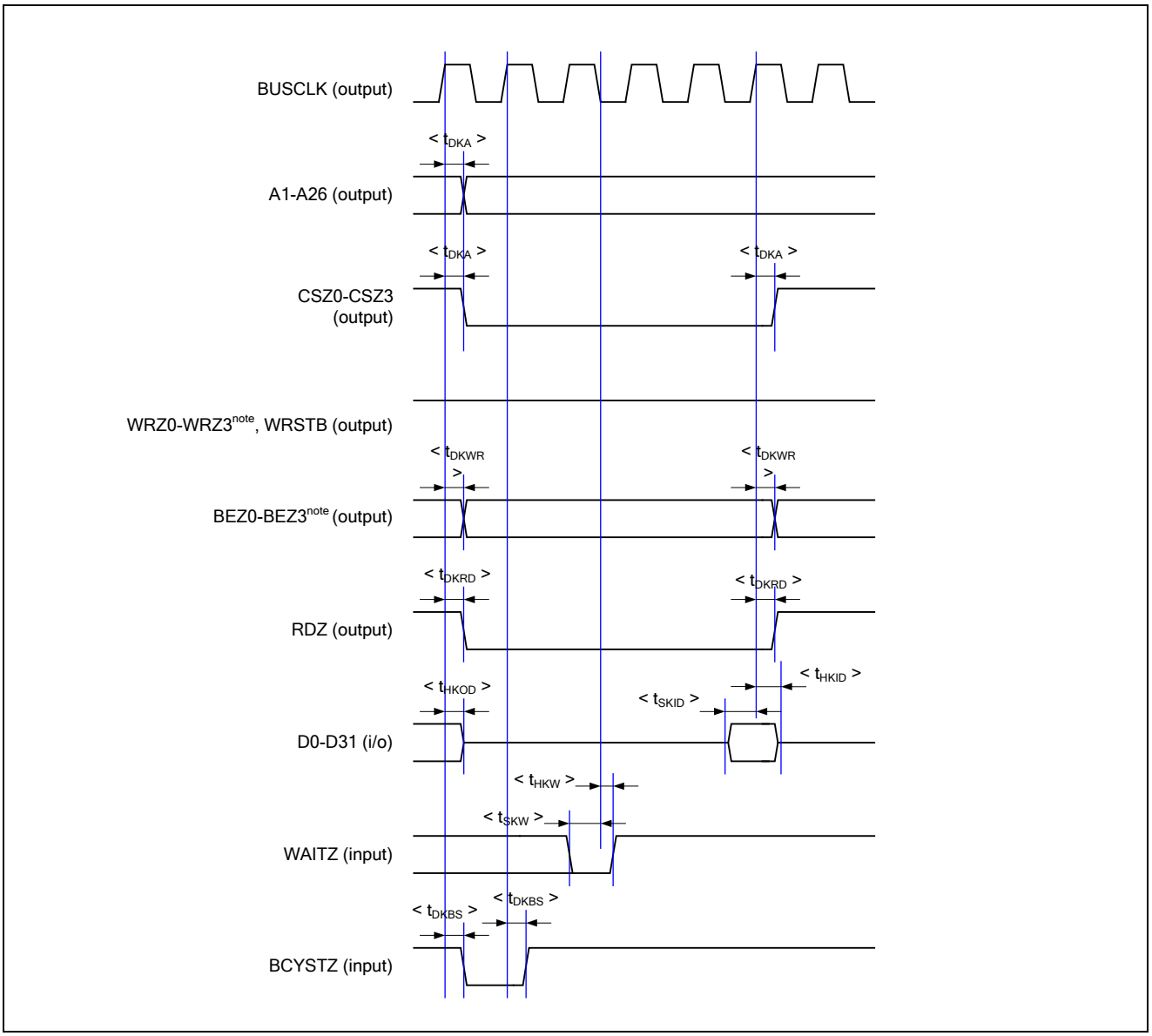


Figure 4.4 Memory controller read timing diagram (asynchronous memory)

Note. WRZ0-WRZ3 and BENZ0-BENZ3 serve a dual purposes; the function is selected by the WREN registers.

Remark. The timing diagram in Figure 4.4 shows the case for when “Idle Wait”, “Write Recovery Wait”,, and “Address Wait” are set to 0, and “Data Wait” is set to 3.

(b) Write timing

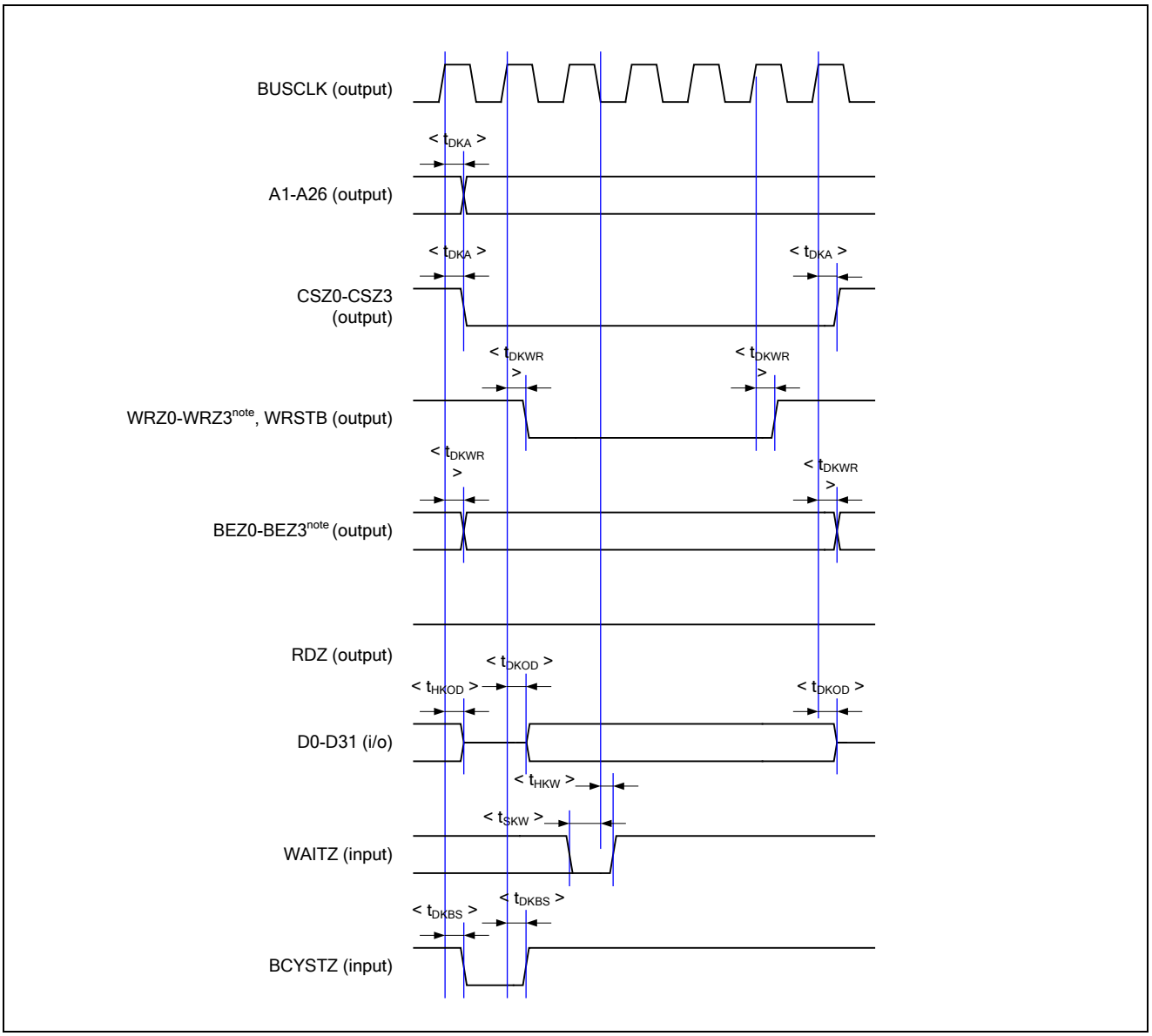


Figure 4.5 Memory controller read timing diagram (asynchronous memory)

Note. WRZ0-WRZ3 and BENZ0-BENZ3 serve dual purposes; The function is selected by the WREN registers.

Remark. The timing diagram in Figure 4.4 shows the case for when “Idle Wait”, “Write Recovery Wait”,, and “Address Wait” are set to 0, and “Data Wait” is set to 3.

(3) Synchronous burst access MEMC access timing

Parameter	Symbol	MIN	MAX	Unit
BUSCLK output Frequency	t_{BUSCLK}	-	50	MHz
Address、CSZ0-CSZ3 output delay time	t_{DKA}	1.0 (1.78) Note	7.8 (9.81) Note	ns
RDZ output delay time	t_{DKRD}	1.0 (1.78) Note	7.8 (9.81) Note	ns
WRZ0 - WRZ3 (BENZ0-BENZ3), WRSTBZ output delay time	t_{DKWR}	1.0 (1.78) Note	7.8 (9.81) Note	ns
ADVZ output delay time	t_{DKBSL}	1.0 (1.78) Note	7.8 (9.81) Note	ns
WAITZ input setup time	t_{SKW}	5.3	-	ns
WAITZ input hold time	t_{HKW}	0	-	ns
Data input setup time	t_{SKID}	5.3	-	ns
Data input hold time	t_{HKID}	0	-	ns
Data output delay time	t_{DKOD}	1.0 (1.78) Note	7.8 (9.81) Note	ns
Data float delay time	t_{HKOD}	1.0 (1.78) Note	7.8 (9.81) Note	ns

Note. Values in parenthesis are based on a 30pF capacitive load.

(a) Read timing

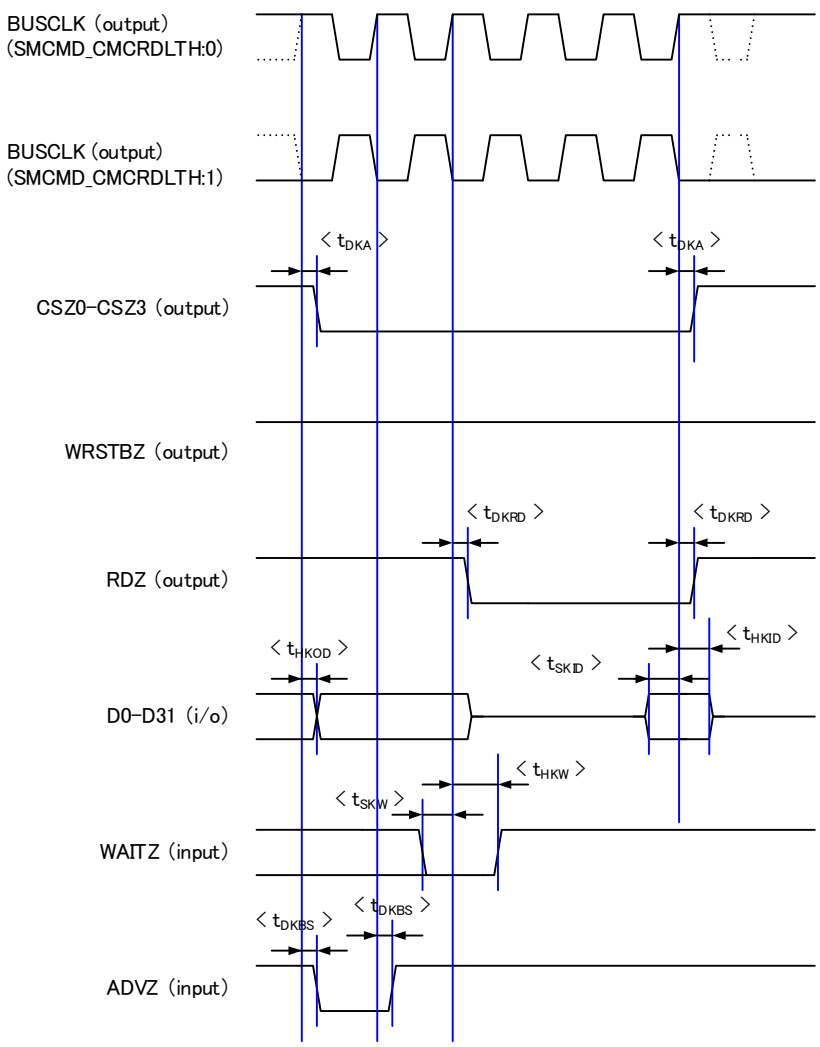


Figure 4.6 Memory controller read timing diagram (synchronous memory)

Remark. Above timing is for the case where “t_ceoe” is 2 and “t_rc” is 4.

(b) Write timing

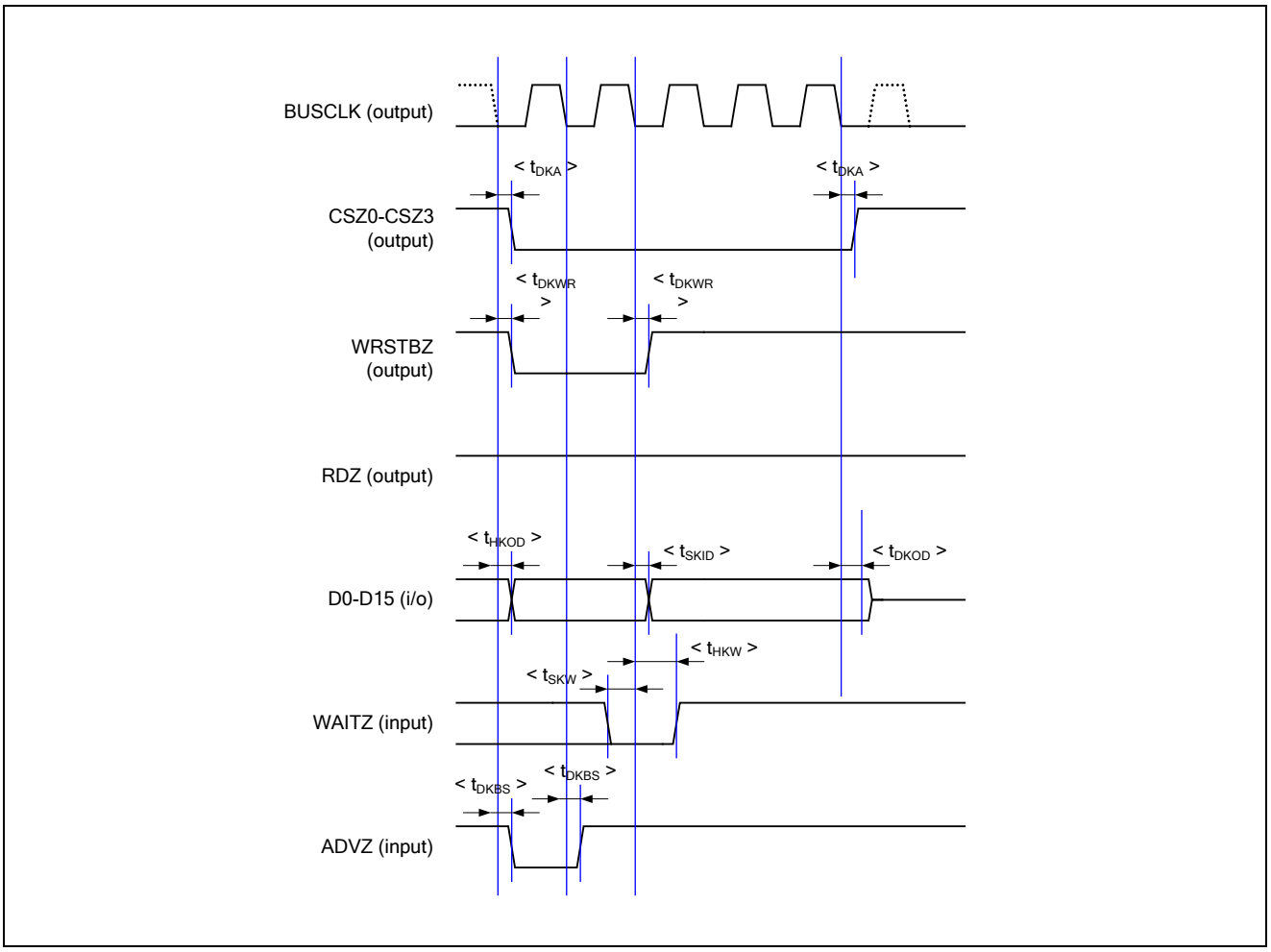


Figure 4.7 Memory controller write timing diagram (synchronous memory)

Remark. Above timing is for the case where “t_ceoe” is 2 and “t_rc” is 4.

4.7.4 External microcomputer interface signal

(1) Synchronous mode

Parameter	Symbol	MIN	MAX	Unit
Address, HCSZ/HPGCSZ input setup time	t_{SKHA}	4.0	–	ns
Address, HCSZ/HPGCSZ input hold time	t_{HKHA}	1.0	–	ns
HRDZ input setup time	t_{SHRD}	4.0	–	ns
HRDZ input hold time	t_{HHRD}	1.0	–	ns
HBENZ0-HBENZ3 (HWRZ0-HWRZ3), HWRSTBZ input setup time	t_{SKHWR}	4.0	–	ns
HBENZ0-HBENZ3 (HWRZ0-HWRZ3), HWRSTBZ input hold time	t_{HKHWR}	1.0	–	ns
HBCYSTZ input setup time	t_{SKHBS}	4.0	–	ns
HBCYSTZ input hold time	t_{HKHBS}	1.0	–	ns
WAITZ output delay time	t_{DKHW}	2.0	10.0	ns
Data input setup time	t_{SKIHD}	4.0	–	ns
Data input hold time	t_{HKIHD}	1.0	–	ns
Data output delay time	t_{DKOHD}	2.0	10.0	ns
Data float delay time	t_{HKOHD}	2.0	10.0	ns
HBUSCLK input cycle	$t_{HBUSCLK}$	20	–	ns
HBUSCLK high level width	t_{HBHIGH}	$0.5t_{HBCYC}$ - 2.1	$0.5t_{HBCYC}$ + 2.1	ns
HBUSCLK low level width	t_{HBLOW}	$0.5t_{HBCYC}$ - 2.1	$0.5t_{HBCYC}$ + 2.1	ns

(a) Read timing

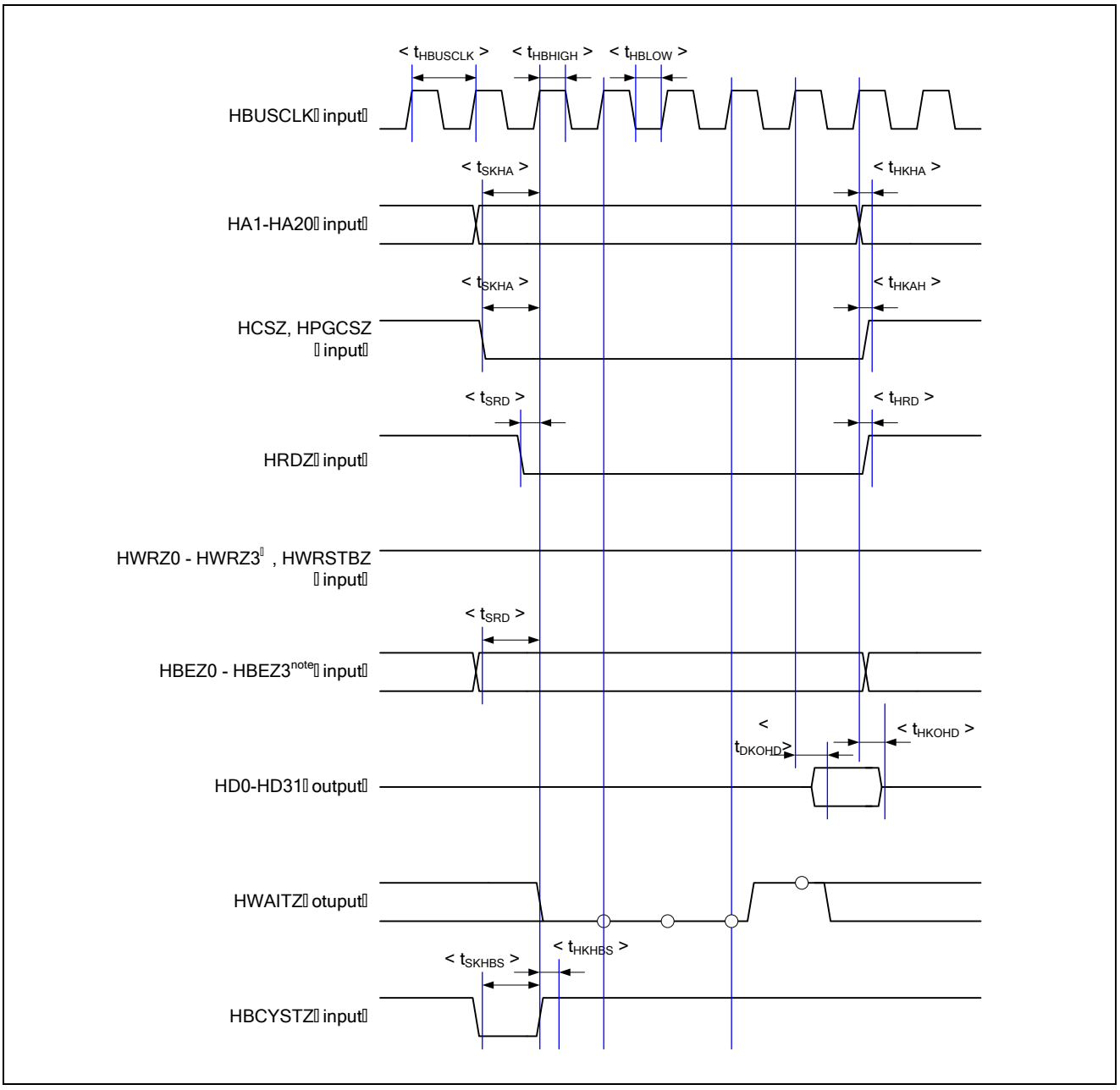


Figure4.8 External microcomputer interface read timing (synchronous mode)

Note HWRZ0-HWRZ3 and HBENZ0-HBENZ3 are made to serve a double purpose. It is decided which function will be used by the level which a HWRZSEL pin inputs.

(b) Write timing

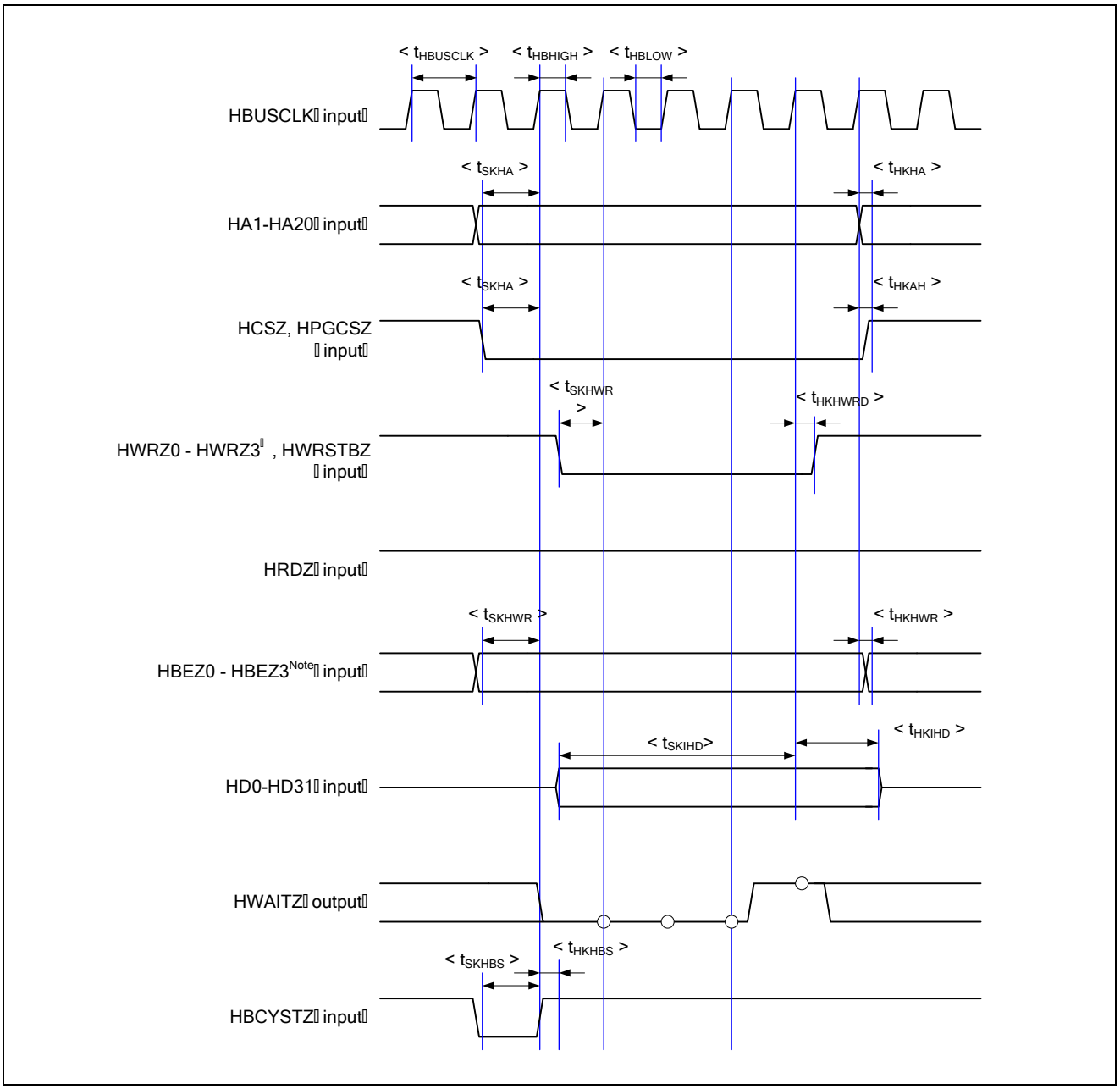


Figure4.9 External microcomputer interface write timing (synchronous mode)

Note HWRZ0-HWRZ3 and HBENZ0-HBENZ3 are made to serve a double purpose. It is decided which function will be used by the level which a HWRZSEL pin inputs.

(2) Asynchronous mode <R>

Parameter	Symbol	MIN	MAX	Unit
HCSZ, HPGCSZ to output in low-Z	t_{CLZ}	–	10	ns
HRDZ to output in low-Z	t_{RDLZ}	–	10	ns
HRDZ to wait active	$t_{RDWAITF}$	–	10	ns
Data valid to wait inactive	t_{WAITR}	10 Note1	–	ns
HRDZ to output in high-Z	t_{RDHZ}	3	–	ns
HWRZ0-3, HWRSTBZ to wait active	$t_{WRWAITF}$	–	10	ns
HWRZ0-3, HWRSTBZ to Data Setup	t_{WRS}	1 Note2	–	ns
HCSZ, HPGCSZ to output in high-Z	t_{CHZ}	3	–	ns

Note 1 At the case RDDTS1-0 bit on HIFBTC register is set to 01B.
This value can be changed from 10nsec to 30nsec by resister setting.

Note 2 At the case WRSTD1-0 bit on HIFBTC register is set to 00B.
This value can be changed from -70nsec to +1nsec by resister setting.

(a) Read timing

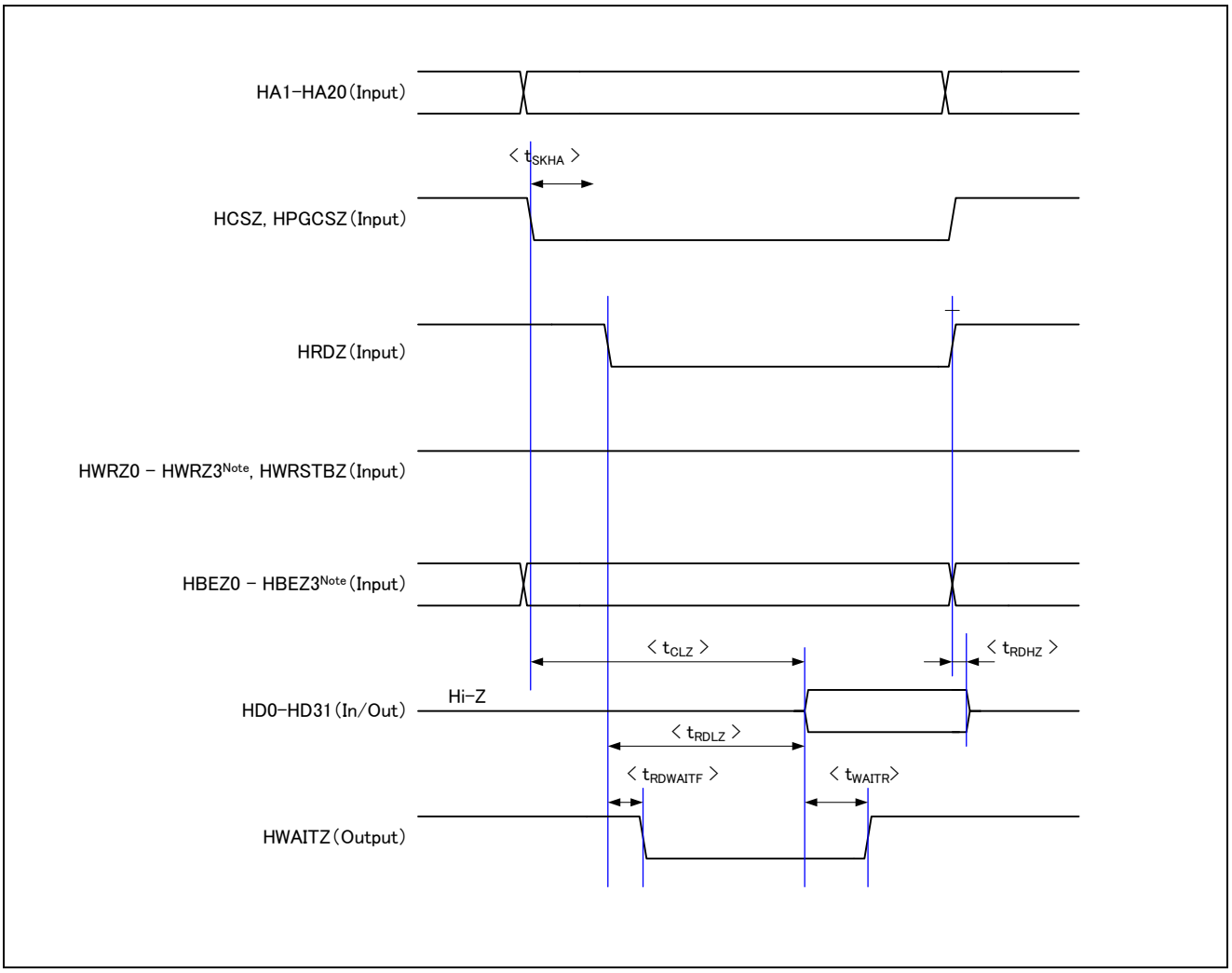


Figure4.10 External microcomputer interface read timing (Asynchronous mode)

Note HWRZ0-HWRZ3 and HBENZ0-HBENZ3 are made to serve a double purpose. It is decided which function will be used by the level which a HWRZSEL pin inputs.

(b) Write timing

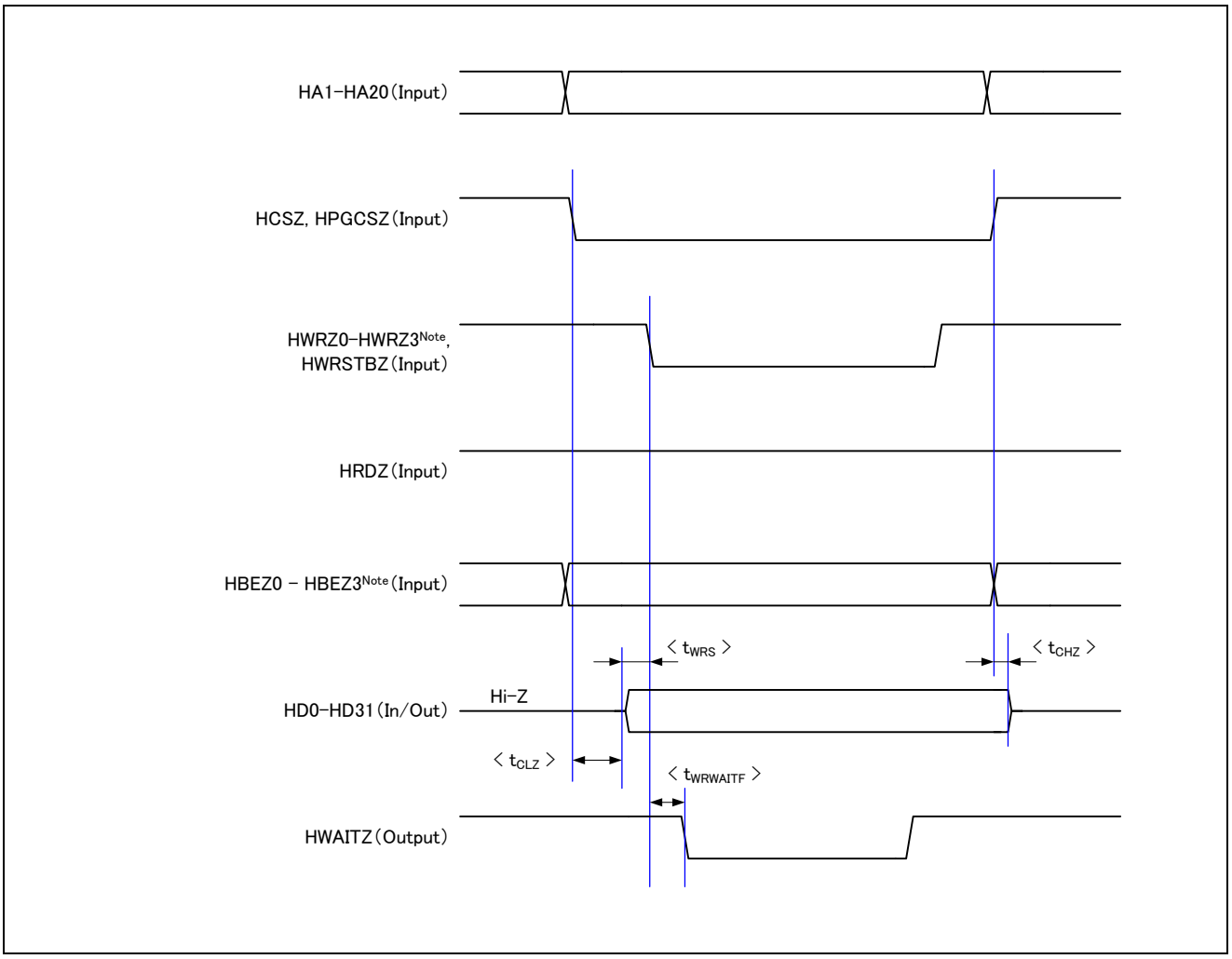


Figure4.11 External microcomputer interface write timing (Asynchronous mode)

Note HWRZ0-HWRZ3 and HBENZ0-HBENZ3 are made to serve a double purpose. It is decided which function will be used by the level which a HWRZSEL pin inputs.

4.7.5 Serial flash ROM interface

Parameter	Symbol	Conditions	MIN	MAX	Unit
SMSCK output cycle	t_{SFRCYC}	C_L = 15pF	20	-	ns
SMSCK high level width	t_{SMCKH}		0.5 t_{SFRCYC} - 2.0	0.5 t_{SFRCYC} + 2.0	ns
SMSCK low level width	t_{SMCKL}		0.5 t_{SFRCYC} - 2.0	0.5 t_{SFRCYC} + 2.0	ns
SMSCK rise time	t_{SMCKR}		–	1.9	ns
SMSCK fall time	t_{SFRCYC}		–	1.9	ns
SMSCK output delay time	$t_{DSMCSCK}$	C_L = 15pF Freq = 50Mhz	7.5 Note	–	ns
SMCSZ output delay time	$t_{DSMCKCS}$	C_L = 15pF Freq = 50MHz	11.5 Note	–	ns
SMCSZ high level width	t_{SMCSH}	C_L = 15pF	14 Note	–	ns
SMSI input setup time	t_{SSMI}	-	6.0	-	Ns
SMSI input hold time	t_{HSMI}	-	0	-	ns
SMSI output delay time	t_{DSMI}	C_L = 15pF	-1.0	5.0	ns
SMSO input setup time	t_{SSMO}	-	6.0	-	ns
SMSO input hold time	t_{HSMO}	-	0	-	ns
SMSO output delay time	t_{DSMO}	C_L = 15pF	-1.0	5.0	ns

Note Timing can be extended by setting of SFMSSC registor.
Please refer to 12.2.2 Chip Selection Control Register (SFMSSC)
of User's Manual (Peripherals Function)

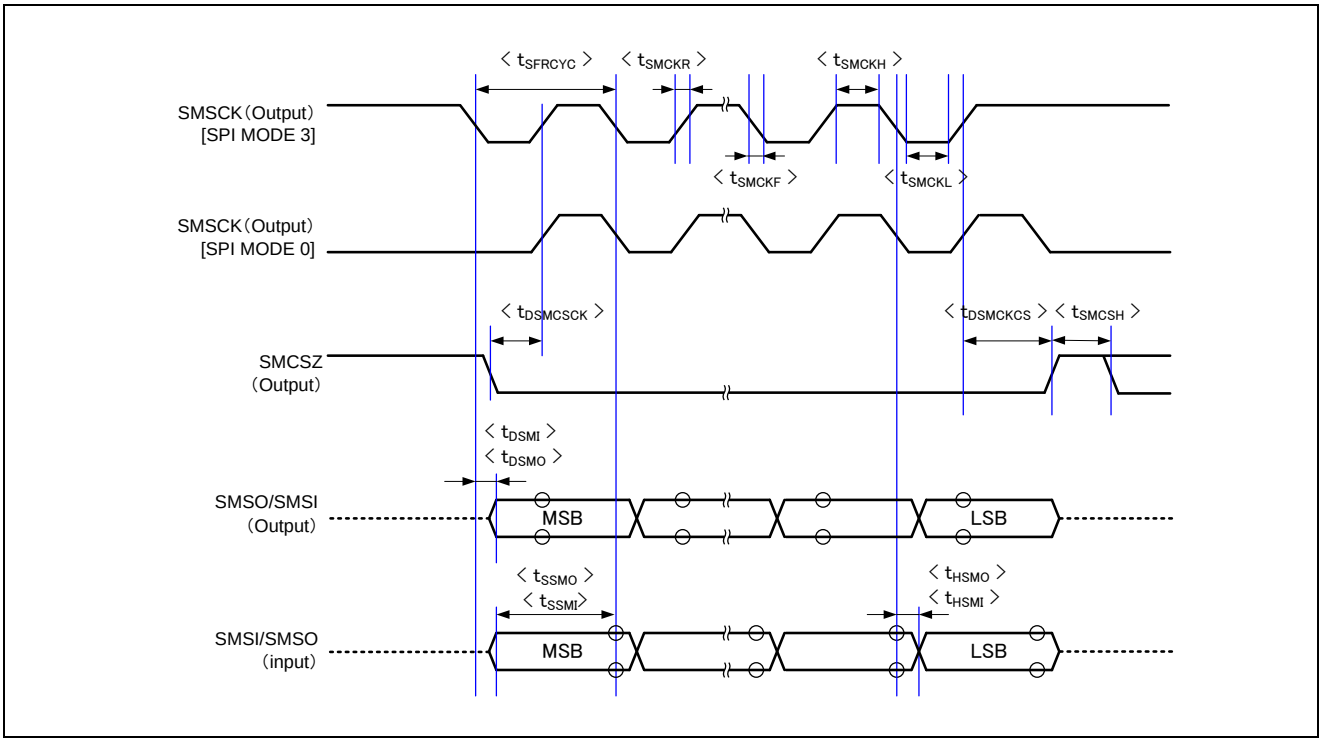


Figure 4.12Serial flash ROM access timing diagram

4.7.6 External DMA interface

Parameter	Symbol	Conditions	MIN	MAX	Unit
DMAREQZ [1:0], RTDMAREQZ input setup time	t_{SKDR}	-	7.0	-	ns
DMAREQZ [1:0], RTDMAREQZ input hold time 1	t_{HKDR1}	-	Until DMAACKZ↓ RTDMAACKZ↓	-	ns
DMAREQZ [1:0], REDMAREQZ input hold time 2	t_{HKDR2}	-	-	t_{BUSCLK} Note1 × m Note2 - 7.0	ns
DMAACKZ [1:0], RTDMACKZ output delay time	t_{DKDA}	C_L = 30pF	2.0	10.0	ns
DMAACKZ [1:0], RTDMAACKZ output high level width	t_{WDAH}	-	t_{BUSCLK} Note1 × m Note2 - 8	t_{BUSCLK} Note1 × m Note2 + 8	ns
DMATCZ [1:0], RTDMATCZ output delay time	t_{DKTC}	C_L = 30pF	2.0	10.0	ns

Note1. t_{BUSCLK} is one cycle (10 ns) of BUSCLK.
Note2. m = 1-31 (DMAIFC0, DMAIFC1, RTMDAIFC registers).

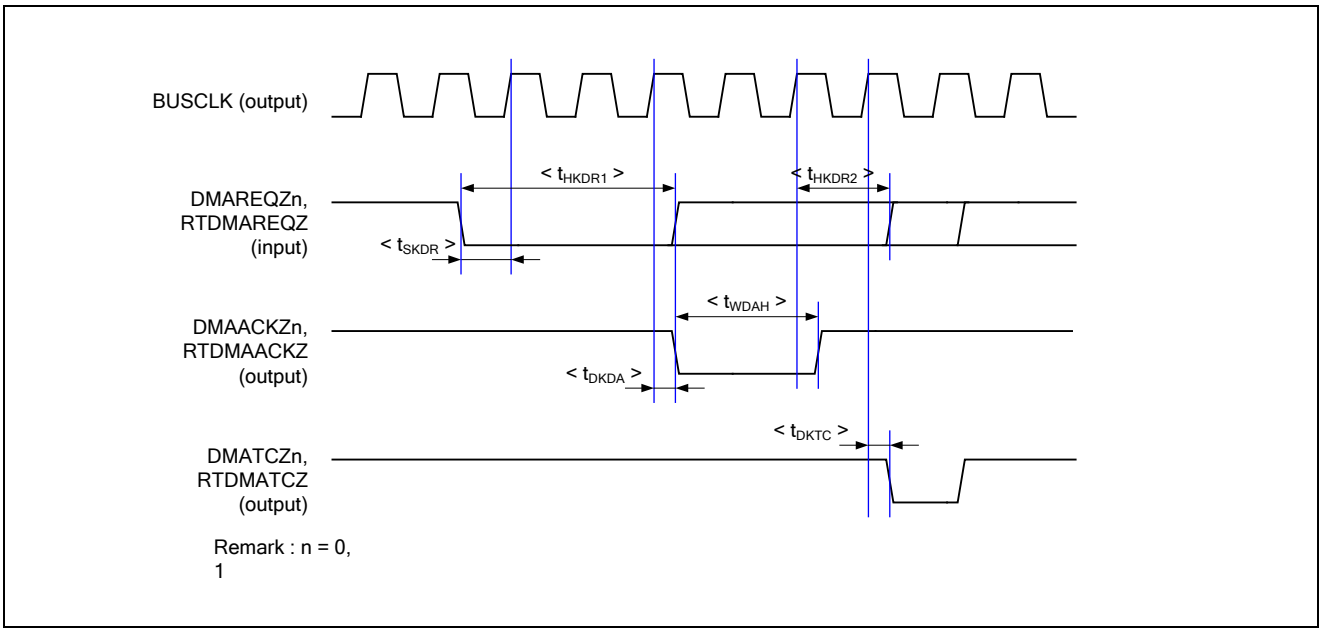


Figure 4.13External DMA access timing diagram

4.7.7 CSI interface

The Clocked serial interface (CSI) supports both master and slave mode.

(1) Master mode

Parameter	Symbol	Conditions	MIN	MAX	Unit
CSISCKn output cycle	$t_{CSIMSCK}$	C_L = 15pF	40	-	ns
CSISIn input setup time (CSISCKn posedge)	t_{SMSI}	-	8.5	-	ns
CSISIn input setup time (CSISCKn negedge)	t_{SMSI}	-	8.5	-	ns
CSISIn input hold time (CSISCKn posedge)	t_{HMSI}	-	7.0	-	ns
CSISIn input hold time (CSISCKn negedge)	t_{HMSI}	-	7.0	-	ns
CSISOn output delay time (CSISCKn posedge)	t_{DMSO}	C_L = 15pF	-	7.0	ns
CSISOn output delay time (CSISCKn negedge)	t_{DMSO}		-	7.0	ns
CSISOn output hold time (CSISCKn posedge)	t_{HMSO}		$t_{CSIMSCK}$ × 0.5 - 5.0	-	ns
CSISOn output hold time (CSISCKn negedge)	t_{HMSO}		$t_{CSIMSCK}$ × 0.5 - 5.0	-	ns

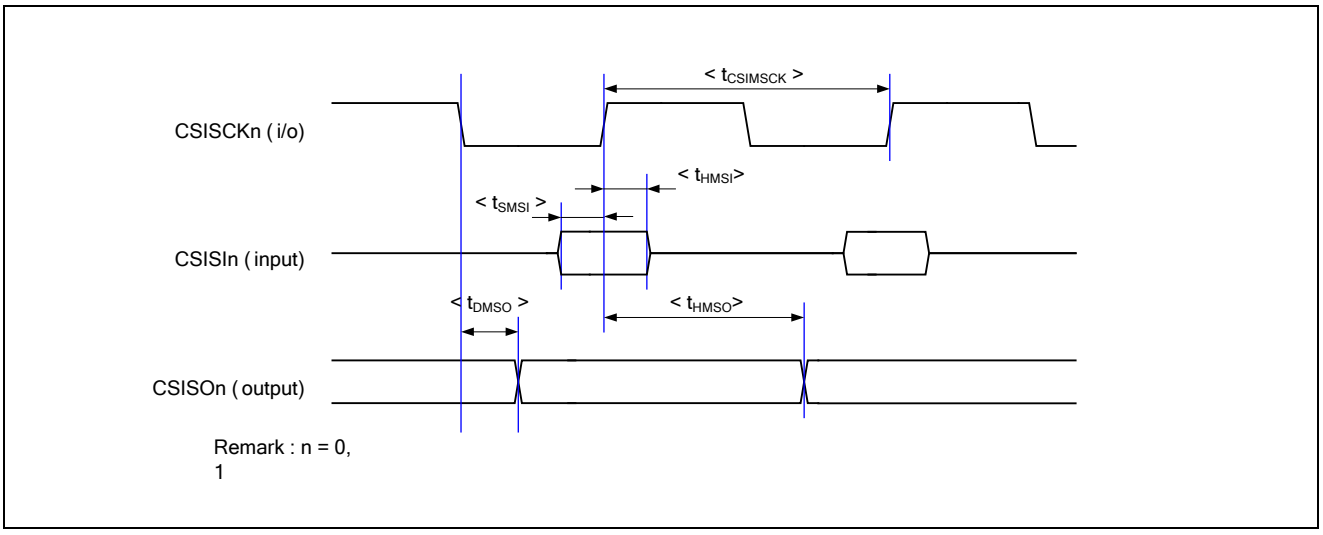


Figure 4.14 CSI access timing diagram (master mode)

(2) Slave mode

Parameter	Symbol	Conditions	MIN	MAX	Unit
CSISCKn input cycle	$t_{CSISSCK}$	-	60	-	ns
CSISIn input setup time (CSISCKn posedge)	t_{SSSI}	-	10.0	-	ns
CSISIn input setup time (CSISCKn negedge)	t_{SSSI}	-	10.0	-	ns
CSISIn input hold time (CSISCKn posedge)	t_{HSSI}	-	15	-	ns
CSISIn input hold time (CSISCKn negedge)	t_{HSSI}	-	15	-	ns
CSISOn output delay time (CSISCKn posedge)	t_{DSSO}	C_L = 15pF	-	10.0	ns
CSISOn output delay time (CSISCKn negedge)	t_{DSSO}		-	10.0	ns
CSISOn output hold time (CSISCKn posedge)	t_{HSSO}		$t_{CSISSCK}$ × 0.5 - 5.0	-	ns
CSISOn output hold time (CSISCKn negedge)	t_{HSSO}		$t_{CSISSCK}$ × 0.5 - 5.0	-	ns

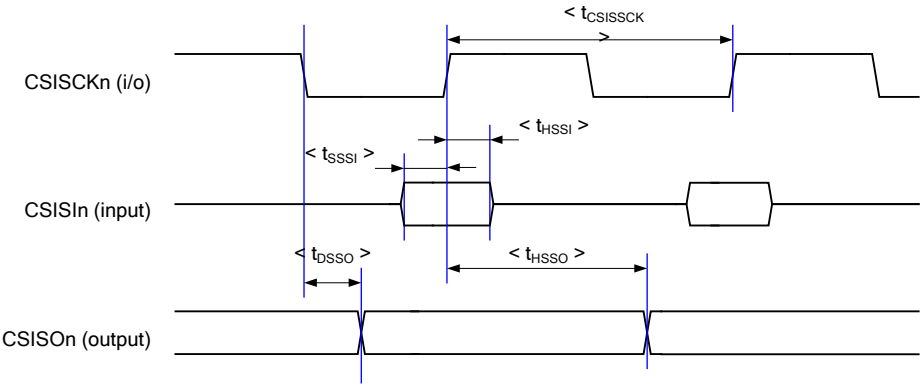
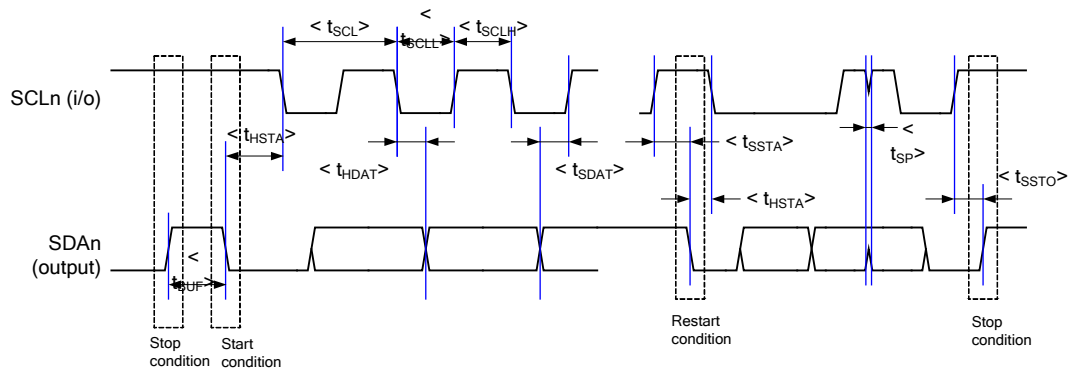


Figure 4.15 CSI access timing diagram (slave mode)

4.7.8 I2C interface

Parameter		Symbol	Conditions	Normal mode		High speed mode		Unit
				MIN	MAX	MIN	MAX	
SCL clock frequency		t_{SCL}	C_L = 30pF	0	100	0	400	kHz
Bus-free time between the stop condition and start condition		t_{BUF}		4.7	-	1.3	-	µs
Hold time		t_{HSTA}		4.0	-	0.6	-	µs
SCL clock low-level width		t_{SCLL}		4.7	-	1.3	-	µs
SCL clock high-level width		t_{SCLH}		4.0	-	0.6	-	µs
Setup time for the start and restart conditions		t_{SSTA}		4.7	-	0.6	-	µs
Data hold time	For a CBUS compatible master	t_{HDAT}		5.0	-	-	-	µs
	For an IIC bus			0	-	0	0.9	µs
Data setup time		t_{SDAT}		250	-	100	-	ns
SDA and SCL signal rise time		t_{SCLR}		-	1000	20 + 0.1C_b	300	ns
SDA and SCL signal fall time		t_{SCLF}		-	300	20 + 0.1C_b	300	ns
Stop condition setup time		t_{SSTO}		4.0	-	0.6	-	µs
Pules width of spike suppressed by input filter		t_{SP}		-	-	0	50	ns
Capacitance load of each bus line		C_b	-	-	400	-	400	pF



Remark : n = 0, 1.
The statement of t_{SCLR}, and t_{SCLF} is omitted.

Figure 4.16 I2C access timing diagram

4.7.9 CAN interface

Parameter	Symbol	Conditions	MIN	MAX	Unit
Internal delay time	t_{NODE}	C_L = 30pF	-	75	ns

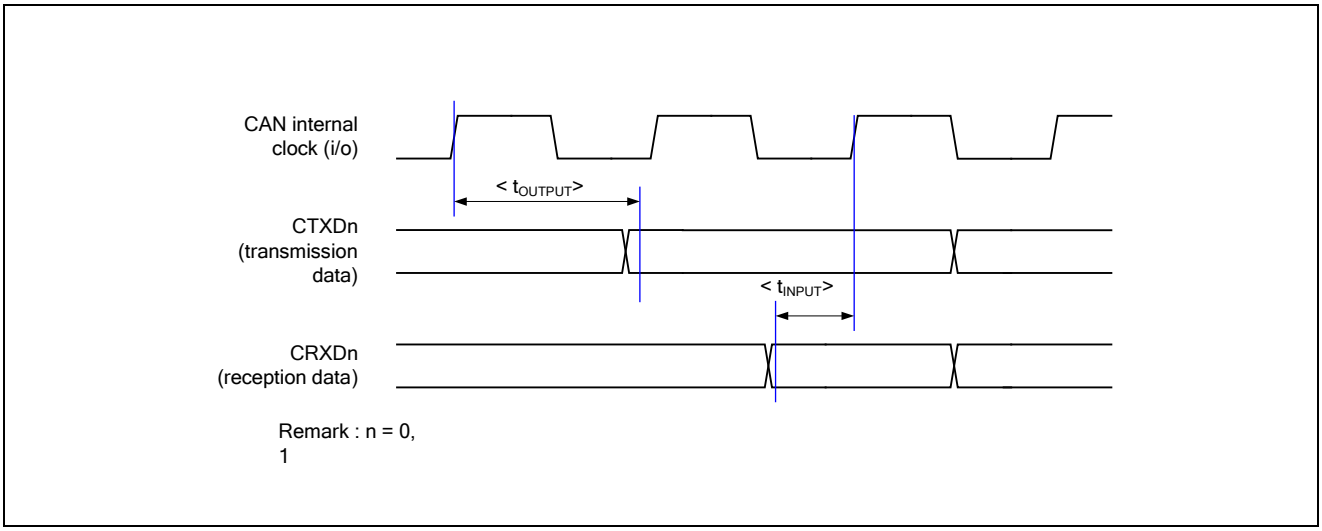


Figure 4.17 CAN access timing diagram

Remark. CAN internal clock (f_{CAN}) : CAN baud late clock

Internal delay time (t_{NODE}) = Internal transmission delay time (t_{OUTPUT}) + Internal reception delay time (t_{INPUT})

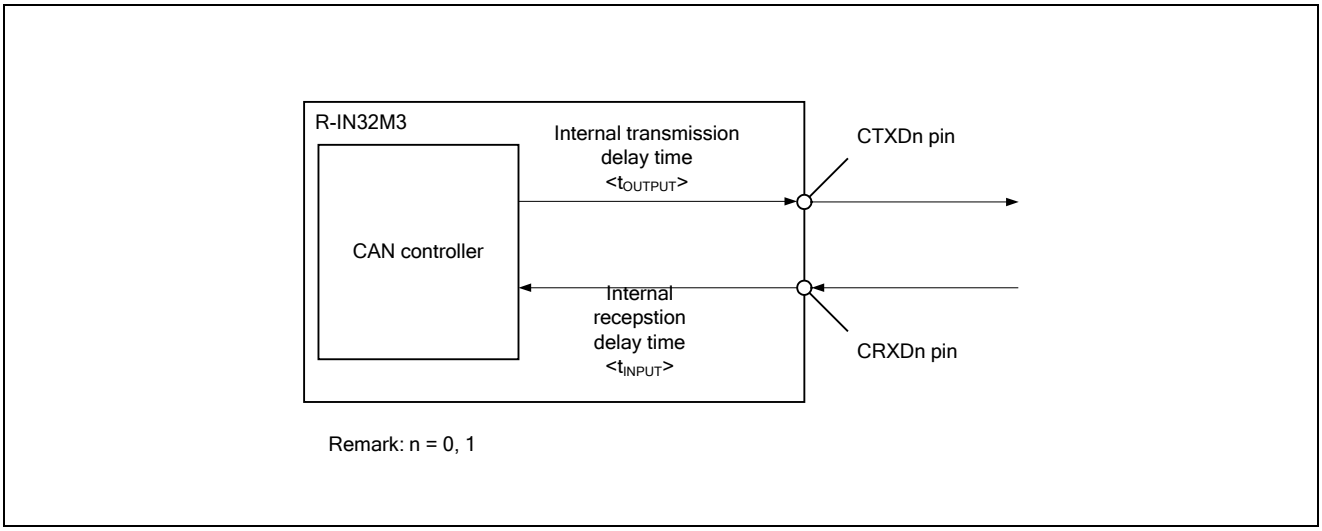


Figure 4.18 CAN access timing (supplement)

4.7.10 Ethernet interface

(1) GMII interface

Parameter	Symbol	Conditions	MIN	MAX	Unit
ETHn_GTXC output cycle	t_{GTXC}	C_L = 13pF	8	-	ns
ETHn_RXC input cycle	t_{GRXC}	-	8	-	ns
ETHn_TXDm output delay time	t_{DGTKTD}	C_L = 13pF	0.5	5.5	ns
ETHn_TXEN, ETHn_TXER output delay time	t_{DGTKTE}	C_L = 13pF	0.5	5.5	ns
ETHn_RXD input setup time	t_{SGRDRK}	-	2.0	-	ns
ETHn_RXD input hold time	t_{HGRDRK}	-	0	-	ns
ETHn_RXDV, ETHn_RXER input setup time	t_{SGRVRK}	-	2.0	-	ns
ETHn_RXDV, ETHn_RXER input hold time	t_{HGRVRK}	-	0	-	ns

Remark. n = 0, 1, m = 0-7.

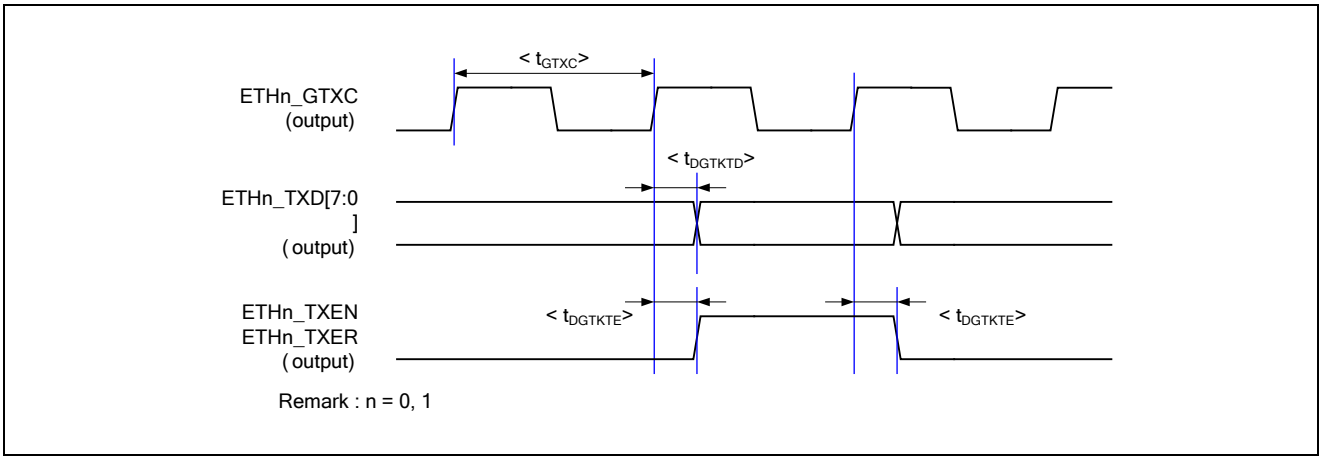


Figure 4.19 Ethernet access timing diagram (GMII transmission)

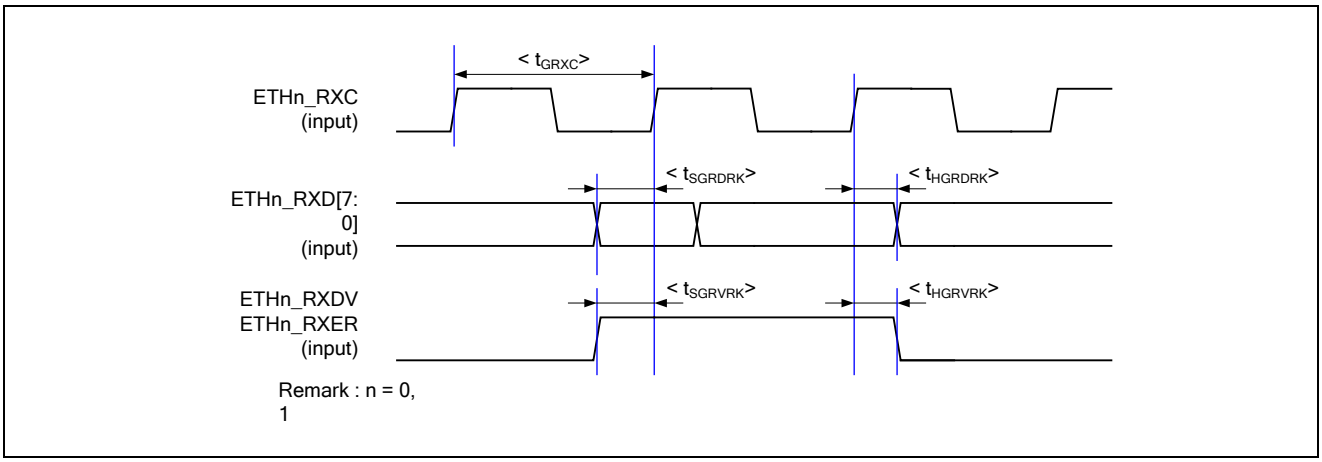


Figure 4.20 Ethernet access timing diagram (GMII reception)

(2) MII interface

Parameter	Symbol	Conditions	MIN	MAX	Unit
ETHn_TXC input cycle	t_{TXC}	-	40	-	ns
ETHn_RXC input cycle	t_{RXC}	-	40	-	ns
ETHn_TXDm output delay time	t_{DTKTD}	C_L = 30pF	0	25	ns
ETHn_TXEN, ETHn_TXER output delay time	t_{DTKTE}	C_L = 30pF	0	25	ns
ETHn_RXD input setup time	t_{SRDRK}	-	10	-	ns
ETHn_RXD input hold time	t_{HRDRK}	-	10	-	ns
ETHn_RXDV, ETHn_RXER input setup time	t_{SRVRK}	-	10	-	ns
ETHn_RXDV, ETHn_RXER input hold time	t_{HRVRK}	-	10	-	ns

Remark. n = 0, 1, m = 0-7.

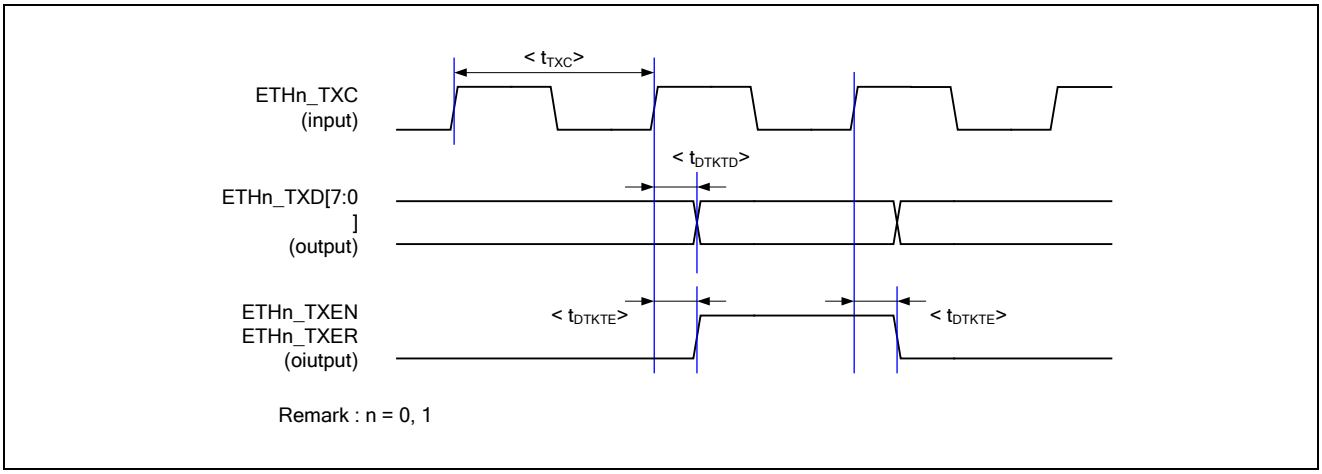


Figure 4.21 Ethernet access timing diagram (MII transmission)

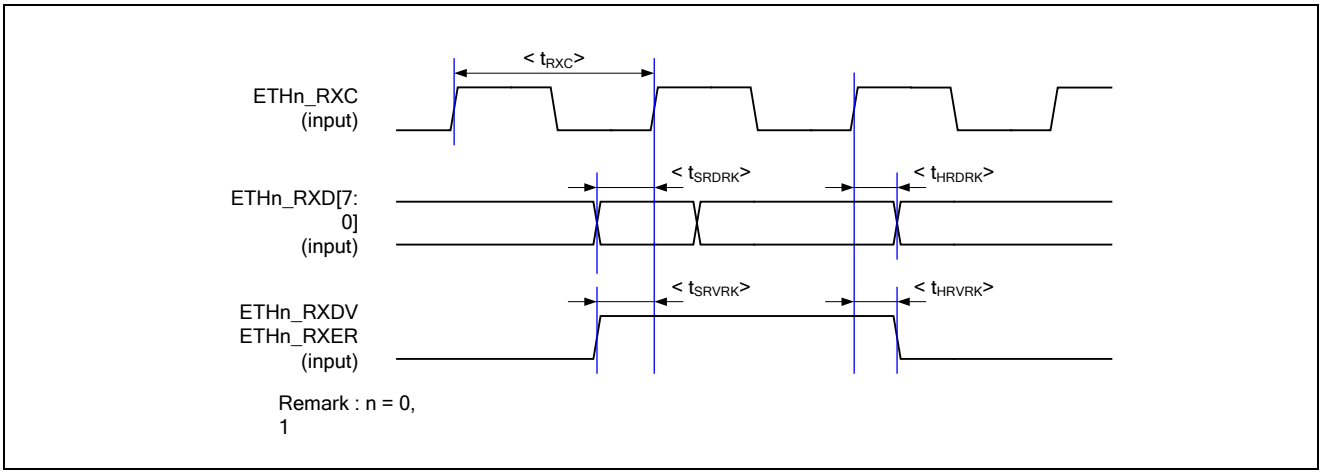


Figure 4.22 Ethernet access timing (MII reception)

(3) Serial management interface

Parameter	Symbol	Conditions	MIN	MAX	Unit
ETH_MDC output cycle	t_{MDC}	C_L = 30pF	80	-	ns
ETH_MDIO input setup time	t_{SMDIO}		10	-	ns
ETH_MDIO input hold time	t_{HMDIO}		0	-	ns
ETH_MDIO output delay time	t_{DMDIO}		20	-	ns

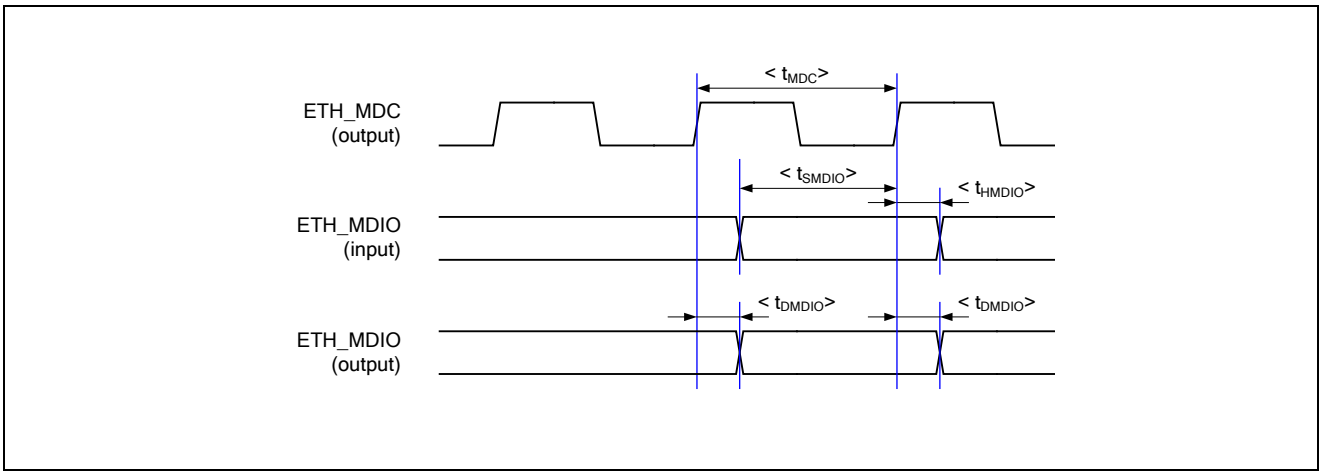


Figure 4.23 Ethernet access timing diagram (serial management)

4.7.11 Debug interface

(1) Debug serial interface

Parameter	Symbol	Conditions	MIN	MAX	Unit
TCK input cycle	t_{TCK}	-	20	-	ns
TMS input setup time	t_{STMS}	-	6.5	-	ns
TMS input hold time	t_{HTMS}	-	0	-	ns
TDI input setup time	t_{STDI}	-	6.5	-	ns
TDI input hold time	t_{HTDI}	-	0	-	ns
TDO output delay time	t_{DTDO}	C_L = 30pF	3.0	13.0	ns

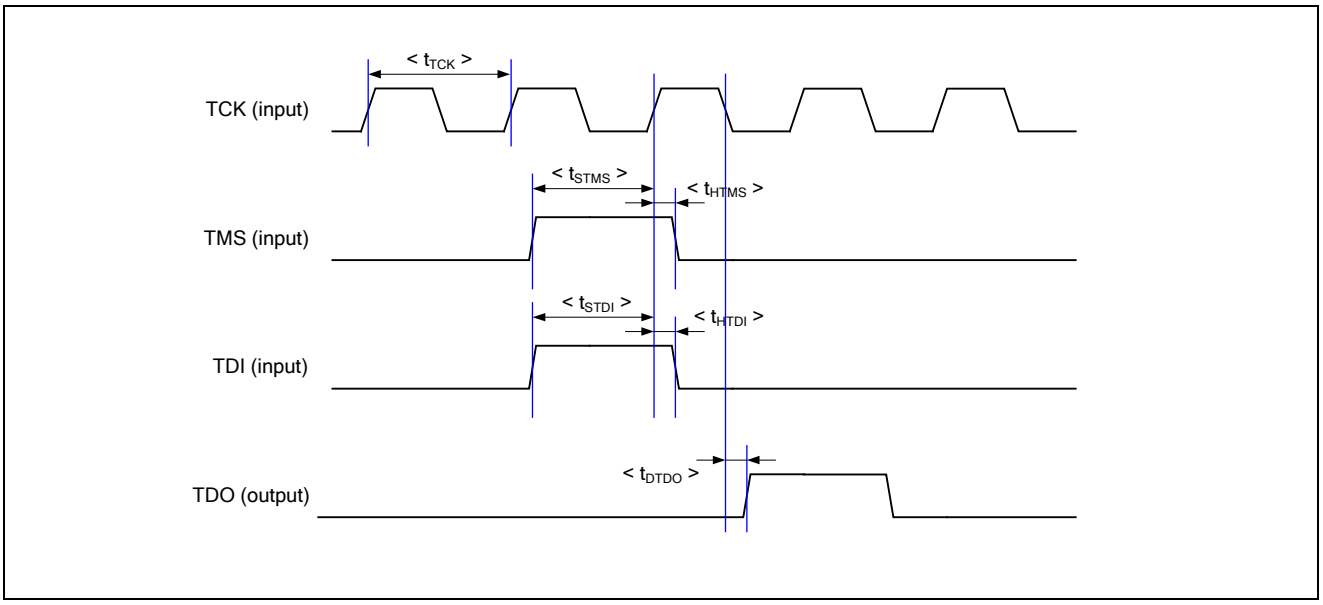


Figure 4.24 Debug serial interface

(2) Trace interface

Parameter	Symbol	Conditions	MIN	MAX	Unit
TRACECLK output frequency	t_{TRCCLK}	C_L = 15pF	20	-	ns
TRACEDATA output delay time	$t_{DTRCDAT}$	C_L = 15pF	0.26	3.43	ns

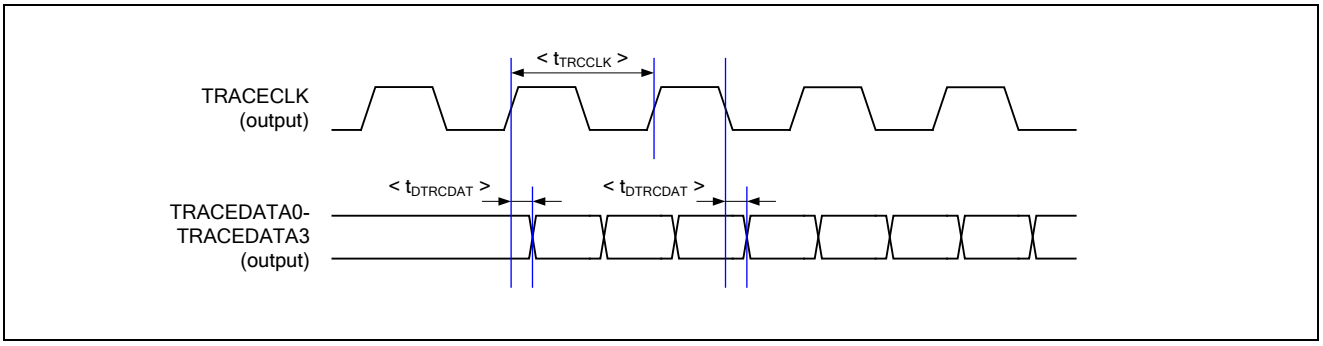
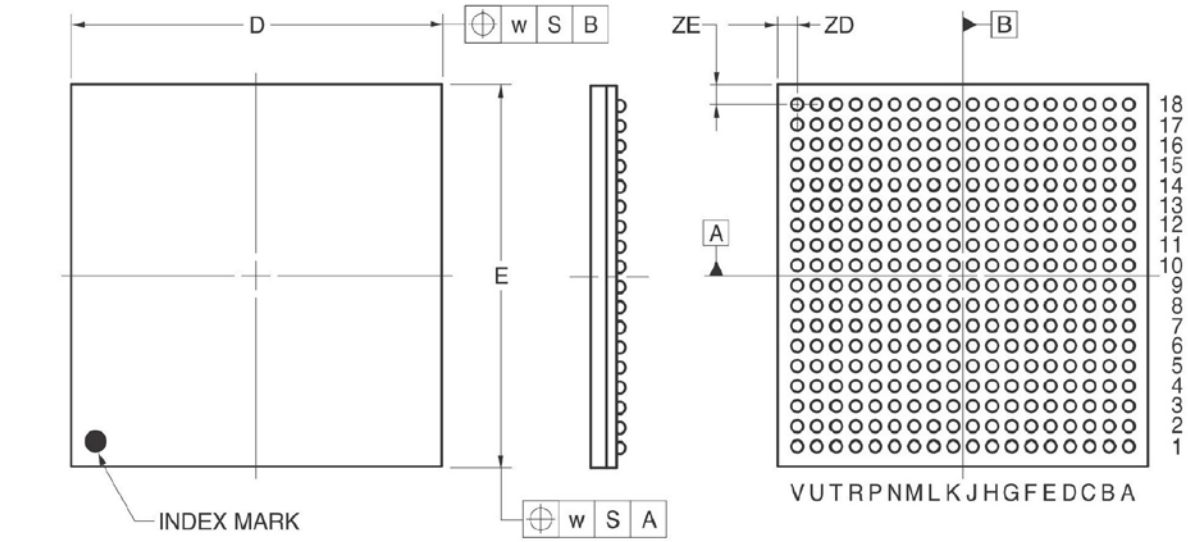
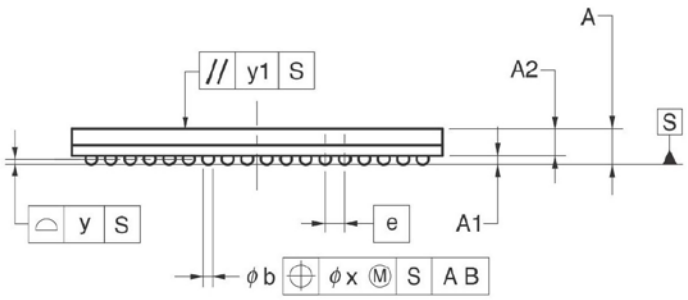


Figure 4.25 Trace interface

5. Package Drawing

324-PIN PLASTIC BGA (19x19)





(UNIT:mm)

ITEM	DIMENSIONS
D	19.00±0.10
E	19.00±0.10
w	0.30
e	1.00
A	1.83±0.12
A1	0.50±0.10
A2	1.33
b	0.60±0.10
x	0.10
y	0.15
y1	0.35
ZD	1.00
ZE	1.00

P324F1-100-HN4-1

REVISION HISTORY	R-IN32M3 Series Data Sheet

Rev.	Date	Description	
		Page	Summary
Preliminary 1.00	2011.06.14	-	First edition issued
Preliminary 2.00	2012.12.03	overall	Change the description of “CC-Link IE Field” “CC-Link IE Field network” → “CC-Link IE Field”
		12-13	Addition of ***2.1 Pin Placement***
		14-16	Modification of ***2.3.1 Ethernet Signal***
		20	Modification of pin name of ***2.3.5 Port Signal, Real-time port Signal***
		26	Modification of level during reset of ***2.3.9 Timer I/O Signal***
		28	Addition of new pin information of ***2.3.14 System Signal***
		29	Addition of new pin information of ***2.3.15 Test Signal***
		30	Addition of new pin information of ***2.3.16 Operation mode Setting Signal***
		36	Addition of new pin information of ***2.4.4Test Signal***
		39-62	Addition of ***3 Specification***
		65-68	Modification of the description of output buffer of ***4 Electrical Specifications***
		69	Addition of ***4.6 Power-on/off sequence***
		70-89	Addition of ***4.7 AC characteristics***
Preliminary 3.00	2013.1.17	2	Modification of Access to External Memory of ***1.3 Overview***
		3	Modification of status of CC-Link of ***1.3 Overview*** Addition EtherPHY Information of ***1.3 Overview***
		4	Modification of block diagram of R-IN32M3-EC of ***1.4 INTERNAL BLOCK DIAGRAM***
		5	Modification of block diagram of R-IN32M3-CL of ***1.4 INTERNAL BLOCK DIAGRAM***
		14	Modification of list of PHY Interface of ***2.3.1 Ethernet Signal***
		16	Modification of level during reset of PHYLINK0/1 of ***2.3.1 Ethernet Signal***
		17	Modification of level during reset of CATSYNC1 of ***2.3.2 EtherCAT Slave Controller Signal***
		18	Addition of WAITZ1-3 port and list of note of ***2.3.3 External Memory Interface Signal***
		25	Modification of level during reset of ***2.3.8 External Interrupt Input Signal***
		26	Modification of level during reset of TIN2/TOUT2 of ***2.3.8 External Interrupt Input Signal*** and level during reset of ***2.3.10 Watchdog Timer Output Signal***
		30	Modification of level during reset of ***2.3.16 CC-Link (Remote device station)***
		31	Addition the signal of VDDQ_PECL_B0/ VDDQ_PECL_B1 of ***2.3.17 System signal***
		34	Modification of Required Connection when not in use of ETH0_TXC of ***2.4.1 Ethernet Signal***

Rev.	Date	Description	
		Page	Summary
Preliminary 3.00	2013.1.17	36	Modification of Required Connection when not in use of TRSTZ of ***2.4.4 Test Signal***
		64	Addition the figure of HW-RTOS structure of ***3.20 Hardware Real-time OS***
		65	Addition the list of service call of ***3.20 Hardware Real-time OS***
1.00	Mar 29,2013	overall	Modification of English expressions
		overall	Change the description of “CC-Link IE Field” “CC-Link IE Field Slave” → “CC-Link IE Field (Intelligent device station)”
		overall	Change the description of “CC-Link” “CC-Link (Slave)” → “CC-Link (Remote device station)”
		1	Modification of the contents of ***1.1 Introduction***
		14	Modification of the status of ETH_MDC during the reset of ***2.3.1 Ethernet Signals*** Modification of the contents of Note of ***2.3.1 Ethernet Signals***
		18	Modification of the status of BUSCLK during the reset of ***2.3.3 External Memory Interface Signals***
		19	Modification of the status of HD0-HD15 during the reset of ***2.3.4 External MPU Interface Signals***
		31	Addition the signals of HOTRESETZ, VDDQ_MII, CLKOUT25M0, CLKOUT25M1 of ***2.3.17 System Signals*** Modification of the function of PONRZ of ***2.3.17 System Signals***
		53	Modification of the status of the kind of supported station of ***3.12 CC-Link Function***
		78	Modification of the example calculation of ***4.7.3 External memory interface signals (1)***
		78	Modification of the MIN calculation result at the time of 30pF of ***4.7.3 External memory interface signals (2)***
		81	Modification of the MIN calculation result at the time of 30pF of ***4.7.3 External memory interface signals (3)***
		84	Addition the ***4.7.4 External microcomputer interface signal***
2.00	Dec 9 ,2013	overall	Change the kind of CC-Link station to support
		3	Standby mode deletion of Table1.1 Overview of R-IN32M3
		6 to 10	Modification of the accessable area of EtherCAT of ***1.5 Memory Map***
		28	Addition explanation of Function of ***2.1.14 CC-Link IE Field Signals***
		31	Modification of the function of VDD15 of ***2.3.17 System Signals*** Addition the note to VDDQ_MII of ***2.3.17 System Signals***
		47	Modification of WDT overflow time of ***3.7 Watchdog Timer***
		71	Addition of the value of Supply current of ***4.4 DC Characteristics***
		73	Modification of the contents of ***4.6 Power-on/off sequence***
		80	Modification of the contents of ***4.7.3 External memory interface signals (3)***
		81	Modification of the contents of ***Figure 4.6 Memory controller read timing diagram (synchronous memory)***
		92	Modification of thevalue of output delay time of ETHn_TXDm/ETHn_TXEN, ETHn_TXER of ***4.7.10 Ethernet interface (1)***

Rev.	Date	Description	
		Page	Summary
2.01	Feb 07 ,2014	6, 10	Modification of the accessable area of EtherCAT of ***1.5 Memory Map***
		30	Add ***CCM_CLK80M*** pins to list of ***2.3.16 CC-Link Signals (Remote device station)***
		33	Modification of Boot mode select of ***2.3.19 Operation mode Setting Signals***
		37	Addition the resister value for Pull-up/down
		39	Modification of title name of ***2.4.8 CC-Link Signal (Intelligent device station, Remote device station)***
		72	Delete the description of 5kΩ row of ***4.5 Pull-up/down Resister Values***
		71	Addition Table4.6 DC Characteristics TYP value
		86	Addition the description at 4.7.5 Serial flash ROM interface
2.02	Apr 18 ,2014	overall	Modification of ***CC-Link Signals (Remote device station)***
		39	Modification of the description about 'recommended connection' and addition a caution description at ***2.4.7 CC-Link IE Field Signal***
2.03	May 30 ,2014	73	Add a notes of "4.6 Power-on-off sequence"
2.04	Dec 25 ,2014	3	Change status for Intelligent device station for CC-Link in ***1.3 Overview***
		6 to 10	Modification of the accessible area of EtherCAT of ***1.5 Memory Map***
		31	Modify the property for FB pin from "-" to "Input"
		76	Modify the description of MIN value for low level width in ***4.7.2 Reset signals***
		86	Add description for "Asynchronous mode" in ***4.7.4 External microcomputer interface signal***.

Instructions for the use of product

In this section, the precautions are described for over whole of CMOS device.
Please refer to this manual about individual precaution.
When there is a mention unlike the text of this manual, a mention of the text takes first priority

1.Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

-The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2.Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

-The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3.Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

-The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4.Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

-When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

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