Datasheet

Isolation voltage 2500Vrms
1ch Gate Driver Providing Galvanic Isolation

BM6105FW-LBZ

General Description

This is the product guarantees long time support in Industrial market.

The BM6105 is a gate driver with isolation voltage 2500Vrms, I/O delay time of 120ns, and minimum input pulse width of 60ns, and incorporates the fault signal output functions, undervoltage lockout (UVLO) function, and desaturation protection (DESAT) function.

Key Specifications

■Isolation voltage:	2500Vrms
■Maximum gate drive voltage:	20V
■I/O delay time:	95ns (Max.)
■Minimum input pulse width:	60ns (Max.)

Package

Package	W(Typ) x D(Typ) x H(Max)
SOP16WM	10.34mm x 10.31mm x 2.64mm

Features

- Long Time Support Product for Industrial Applications.
- Providing Galvanic Isolation
- Miller Clamp Function
- Fault signal output function
- Ready signal output function
- Undervoltage lockout function
- Desaturation protection function
- Supporting Negative VEE2

Applications

- Driving IGBT Gate for Industrial Equipment
- Driving MOSFET Gate for Industrial Equipment

Typical Application Circuit

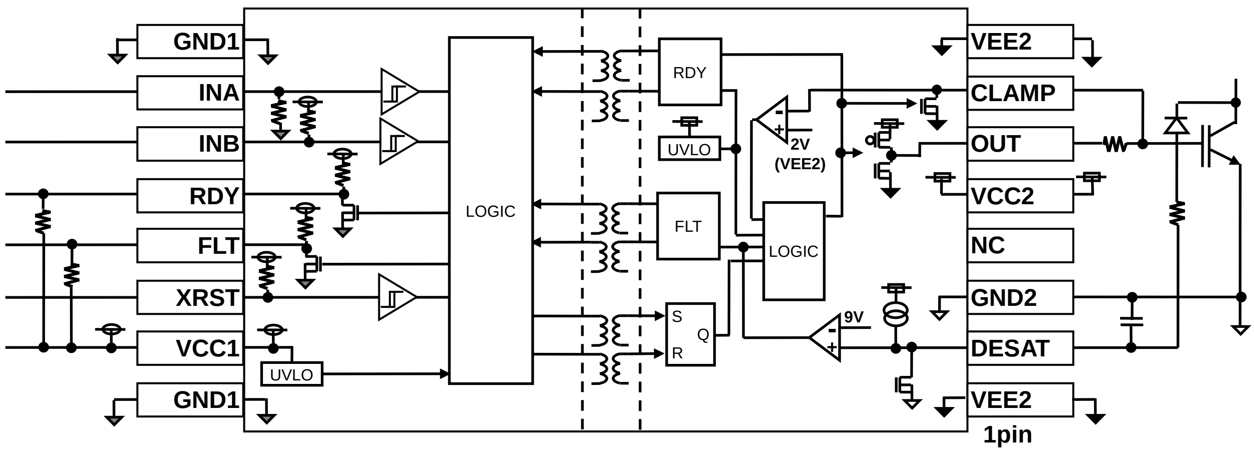


Figure 1. Typical application circuit

○Product structure：Silicon integrated circuit ○This product is not designed protection against radioactive rays

Recommended range of external constants

Pin Name	Symbol	Recommended Value			Unit
		Min	Typ	Max	
VCC1	C_{VCC1}	0.1	1.0	-	μF
VCC2	C_{VCC2}	0.33	-	-	μF

Pin Configurations

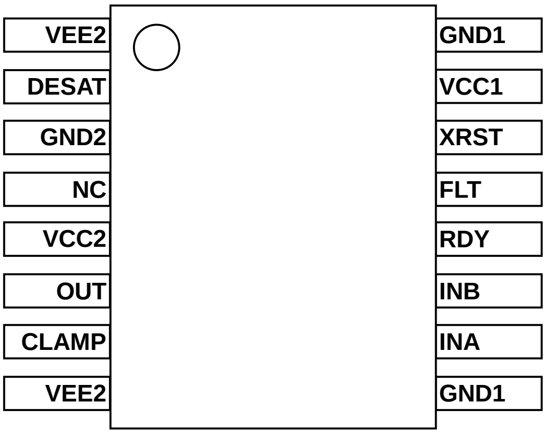


Figure 2. Pin configuration

Pin Descriptions

Pin No.	Pin Name	Function
1	VEE2	Output-side negative power supply pin
2	DESAT	Desaturation protection pin
3	GND2	Output-side ground pin
4	NC	No connect
5	VCC2	Output-side positive power supply pin
6	OUT	Output pin
7	CLAMP	Miller clamp pin
8	VEE2	Output-side negative power supply pin
9	GND1	Input-side ground pin
10	INA	Control input pin A
11	INB	Control input pin B
12	RDY	Ready output pin
13	FLT	Fault output pin
14	XRST	Reset input pin
15	VCC1	Input-side power supply pin
16	GND1	Input-side ground pin

Absolute Maximum Ratings

Parameter	Symbol	Limits	Unit
Input-side supply voltage	V_{CC1}	-0.3 to +7.0(Note1)	V
Output-side positive supply voltage	V_{CC2}	-0.3 to +24.0(Note2)	V
Output-side negative supply voltage	V_{EE2}	-15.0 to +0.3(Note3)	V
Maximum difference between output-side positive and negative voltages	V_{MAX2}	30.0	V
INA, INB, XRST pin input voltage	V_{IN}	-0.3 to +VCC1+0.3 or 7.0(Note1)	V
RDY, FLT pin input voltage	V_{FLT}	-0.3 to +VCC1+0.3 or 7.0(Note1)	V
DESAT pin input voltage	$V_{DESATIN}$	-0.3 to VCC2+0.3(Note2)	V
OUT pin output current (10μs)	$I_{OUTPEAK}$	5.0	A
OUT, CLAMP pin voltage	V_{OUT}	VEE2-0.3V to VCC2+0.3V	V
RDY, FLT output current	I_{FLT}	10	mA
Power dissipation	P_d	1.20(Note4)	W
Operating temperature range	T_{opr}	-40 to +105	°C
Storage temperature range	T_{stg}	-55 to +150	°C
Junction temperature	T_{jmax}	+150	°C

(Note1) Relative to GND1.
(Note2) Relative to GND2.
(Note3) Should not exceed Pd and Tj=150°C.
(Note4) Derate above Ta=25°C at a rate of 9.6mW/°C. Mounted on a glass epoxy of 114.3 mm × 76.2 mm × 1.6 mm.
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Units
Input-side supply voltage	V_{CC1}(Note5)	4.5	5.5	V
Output-side positive supply voltage	V_{CC2}(Note6)	13.3	20.0	V
Output-side negative supply voltage	V_{EE2}(Note6)	-12	0	V
Maximum difference between output-side positive and negative voltages	V_{MAX2}	-	28.0	V

(Note5) Relative to GND1.
(Note6) Relative to GND2.

Insulation Related Characteristics

Parameter	Symbol	Characteristic	Units
Insulation Resistance (V_{IO}=500V)	R_S	$>10^9$	Ω
Insulation Withstand Voltage / 1min	V_{ISO}	2500	Vrms
Insulation Test Voltage / 1sec	V_{ISO}	3000	Vrms

Electrical Characteristics

(Unless otherwise specified Ta=-40°C to 105°C, V_{CC1}=4.5V to 5.5V, V_{CC2}=13.3V to 20V, V_{EE2}=-12V to 0V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
General						
Input side circuit current 1	I_{CC11}	0.16	0.32	0.48	mA	
Input side circuit current 2	I_{CC12}	0.21	0.42	0.63	mA	INA=10kHz, Duty=50%
Input side circuit current 3	I_{CC13}	0.26	0.52	0.78	mA	INA=20kHz, Duty=50%
Output side circuit current 1	I_{CC21}	0.9	1.8	2.7	mA	OUT=L
Output side circuit current 2	I_{CC22}	0.8	1.7	2.5	mA	OUT=H
Logic block						
Logic high level input voltage	V_{INH}	2.0	-	V_{CC1}	V	INA, INB, XRST
Logic low level input voltage	V_{INL}	0	-	0.8	V	INA, INB, XRST
Logic pull-down resistance	R_{IND}	25	50	100	kΩ	INA
Logic pull-up resistance	R_{INU}	25	50	100	kΩ	INB, XRST, RDY, FLT
Logic input mask time	t_{INMSK}	-	-	60	ns	INA, INB
Minimum XRST pulse width	$t_{XRSTMIN}$	800	-	-	ns	
Output						
OUT ON resistance (Source)	R_{ONH}	0.3	0.8	1.5	Ω	I_{OUT}=40mA
OUT ON resistance (Sink)	R_{ONL}	0.2	0.5	0.9	Ω	I_{OUT}=40mA
OUT maximum current	I_{OUTMAX}	3.0	4.5	-	A	Guaranteed by design
CLAMP ON resistance	R_{ONCLP}	0.2	0.5	0.9	Ω	I_{CLAMP}=40mA
Low level CLAMP current	I_{CLAMPL}	3.0	4.5	-	A	Guaranteed by design
Turn ON time	t_{PON}	45	70	95	ns	
Turn OFF time	t_{POFF}	45	70	95	ns	
Propagation distortion	t_{PDIST}	-20	0	20	ns	t_{POFF} - t_{PON}
Rise time	t_{RISE}	-	50	100	ns	10Ω, 10nF between OUT-VEE2 Guaranteed by design
Fall time	t_{FALL}	-	50	100	ns	
CLAMP ON threshold voltage	V_{CLPON}	1.8	2	2.2	V	Relative to VEE2
Common Mode Transient Immunity	CM	100	-	-	kV/μs	Guaranteed by design

Electrical Characteristics - continued

(Unless otherwise specified Ta=-40°C to 105°C, V_{CC1}=4.5V to 5.5V, V_{CC2}=13.3V to 20V, V_{EE2}=-12V to 0V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Protection functions						
VCC1 UVLO OFF voltage	V_{UVLO1H}	3.35	3.50	3.65	V	
VCC1 UVLO ON voltage	V_{UVLO1L}	3.25	3.40	3.55	V	
VCC1 UVLO mask time	$t_{UVLO1MSK}$	1.0	2.5	5.0	μs	
VCC2 UVLO OFF voltage	V_{UVLO2H}	11.3	12.3	13.3	V	
VCC2 UVLO ON voltage	V_{UVLO2L}	10.3	11.3	12.3	V	
VCC2 UVLO mask time	$t_{UVLO2MSK}$	1.0	2.0	3.0	μs	
DESAT source current	I_{DESAT}	450	500	550	μA	
DESAT threshold voltage	V_{DESAT}	8.5	9.0	9.5	V	
DESAT filter time	$t_{DESATFIL}$	0.16	0.25	0.34	μs	
DESAT delay time (OUT)	$t_{DESATOUT}$	0.31	0.38	0.45	μs	
DESAT delay time (FLT)	$t_{DESATFLT}$	0.34	0.42	0.50	μs	
DESAT low voltage	V_{DESATL}	-	0.1	0.22	V	I_{DESAT}=1mA
Leading edge blanking	$t_{DESATLEB}$	0.28	0.4	0.52	μs	Guaranteed by design
RDY output low voltage	V_{RDYL}	-	0.08	0.15	V	I_{RDY}=5mA
FLT output low voltage	V_{FLTL}	-	0.08	0.15	V	I_{FLT}=5mA

Typical Performance Curves

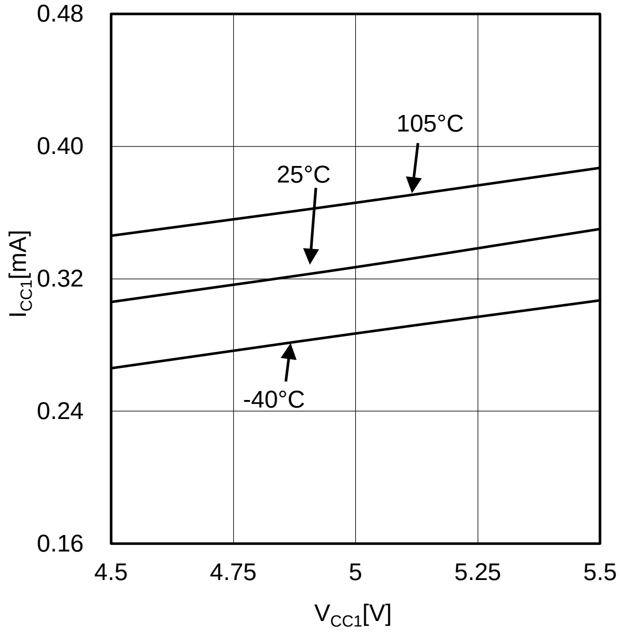


Figure 3. Input side circuit current 1

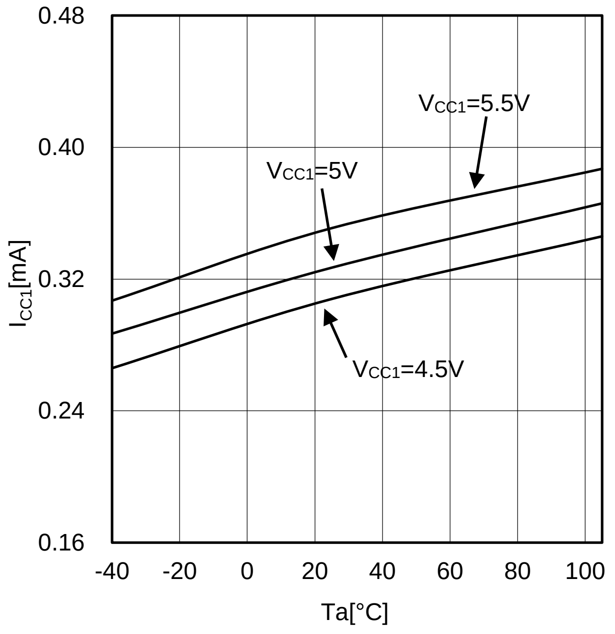


Figure 4. Input side circuit current 1

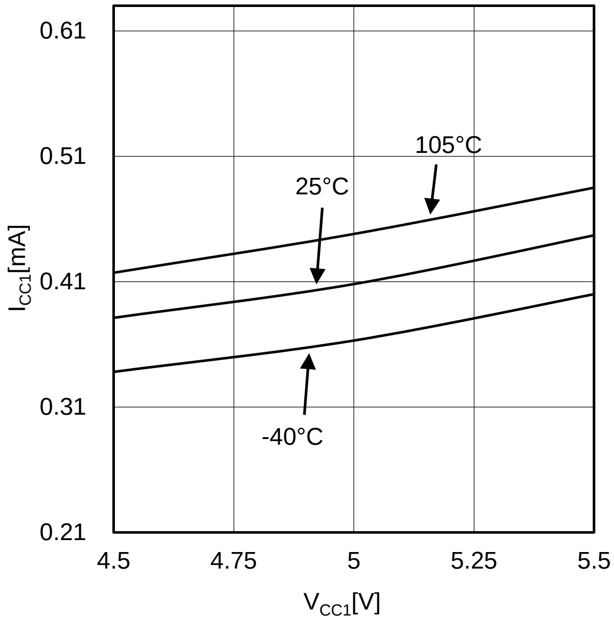


Figure 5. Input side circuit current 2
(INA=10kHz, Duty=50%)

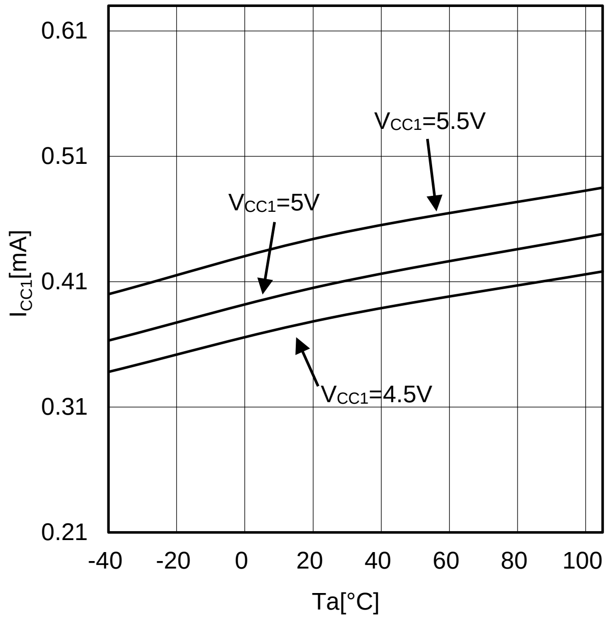


Figure 6. Input side circuit current 2
(INA=10kHz, Duty=50%)

Typical Performance Curves - continued

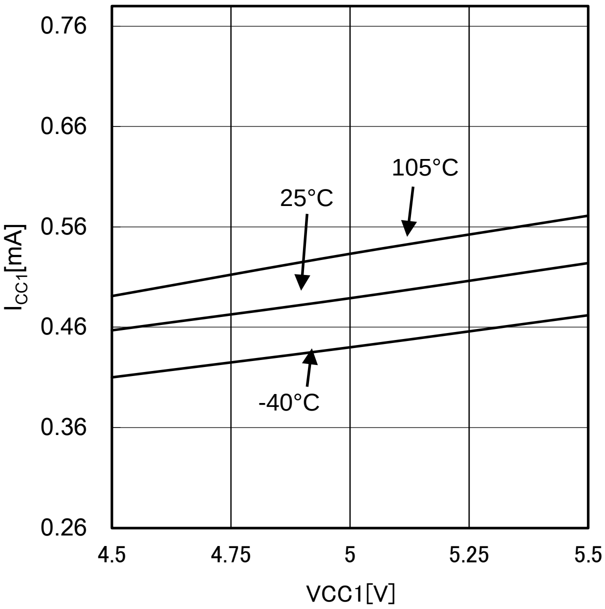


Figure 7. Input side circuit current 3
(INA=20kHz, Duty=50%)

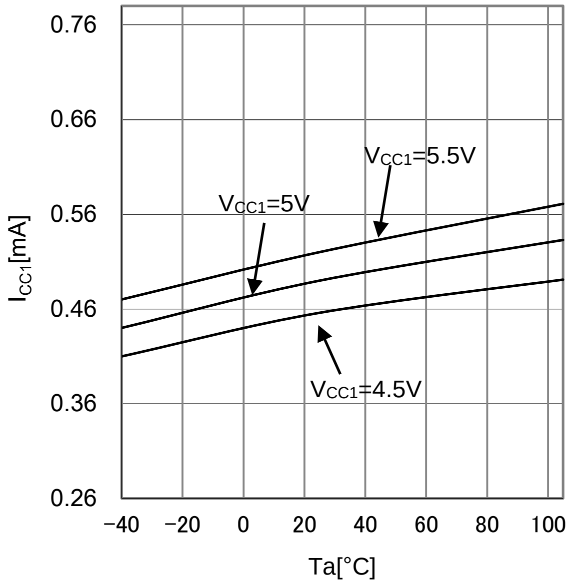


Figure 8. Input side circuit current 3
(INA=20kHz, Duty=50%)

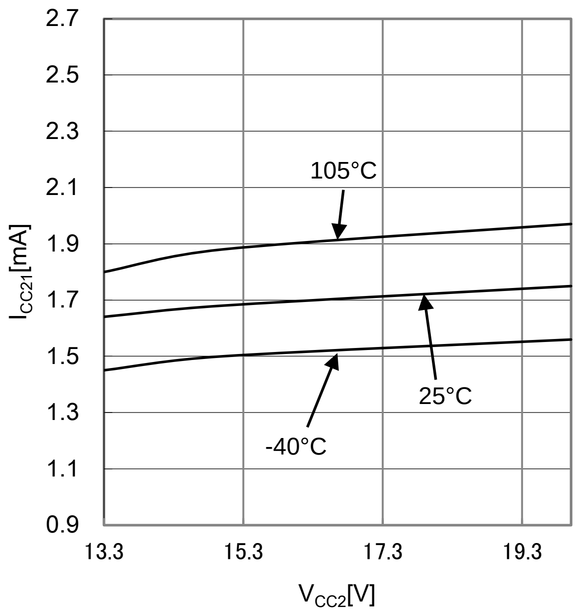


Figure 9. Output side circuit current 1
(V_{EE2}=0V, OUT=L)

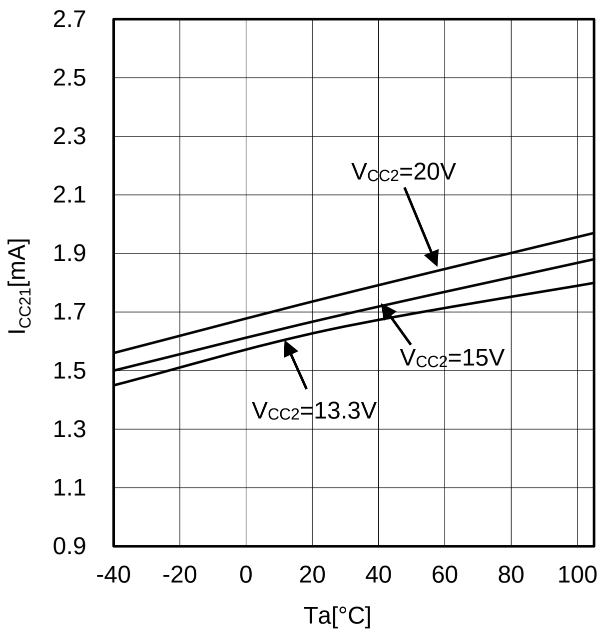


Figure 10. Output side circuit current 1
(V_{EE2}=0V, OUT=L)

Typical Performance Curves - continued

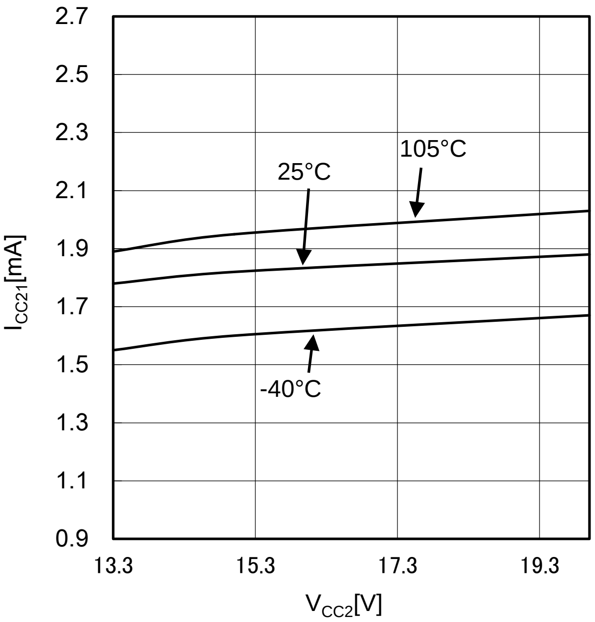


Figure 11. Output side circuit current 1
(V_{EE2}=-8V, OUT=L)

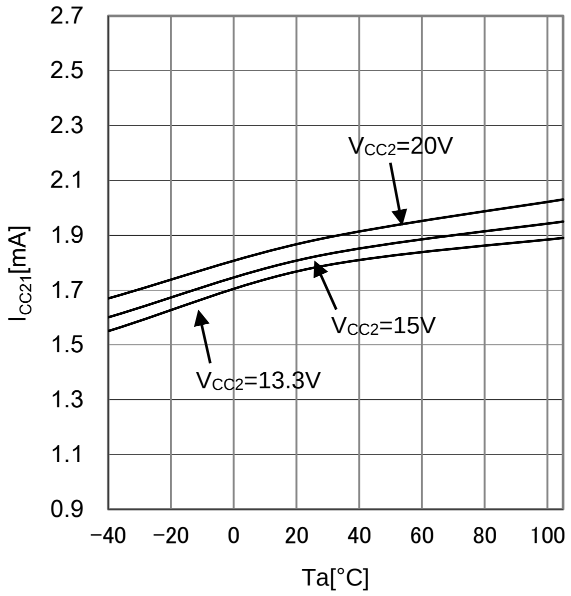


Figure 12. Output side circuit current 1
(V_{EE2}=-8V, OUT=L)

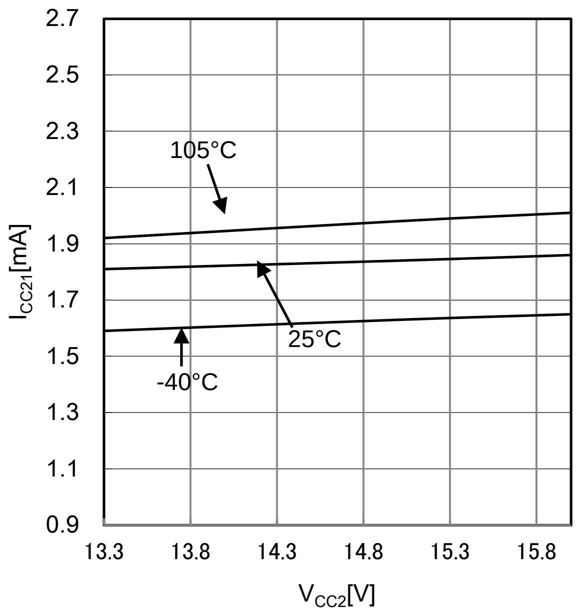


Figure 13. Output side circuit current 1
(V_{EE2}=-12V, OUT=L)

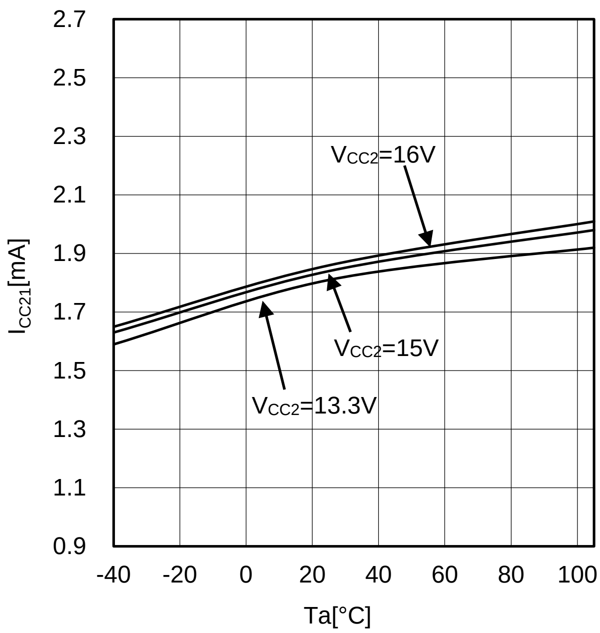


Figure 14. Output side circuit current 1
(V_{EE2}=-12V, OUT=L)

Typical Performance Curves - continued

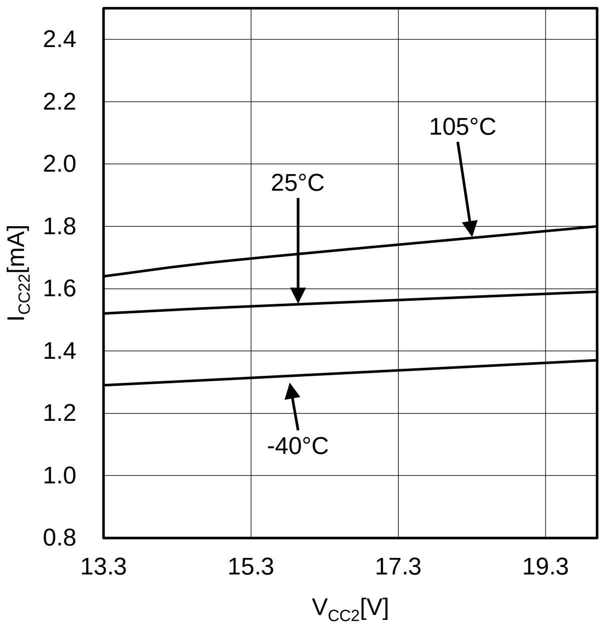


Figure 15. Output side circuit current 2
(V_{EE2}=0V, OUT=H)

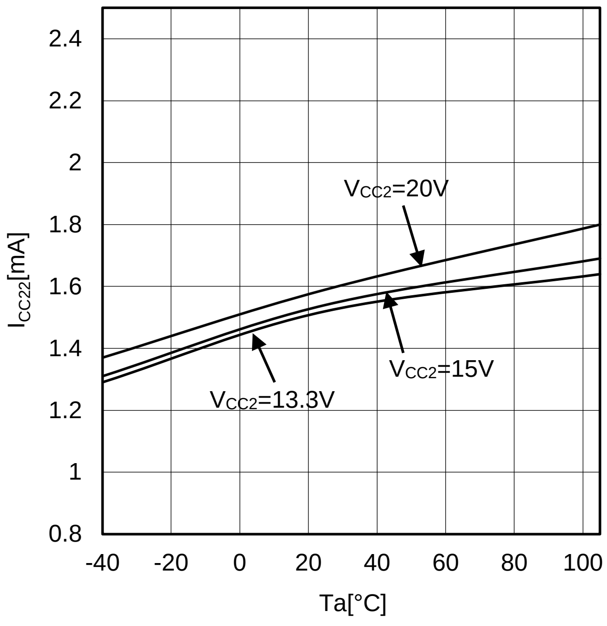


Figure 16. Output side circuit current 2
(V_{EE2}=0V, OUT=H)

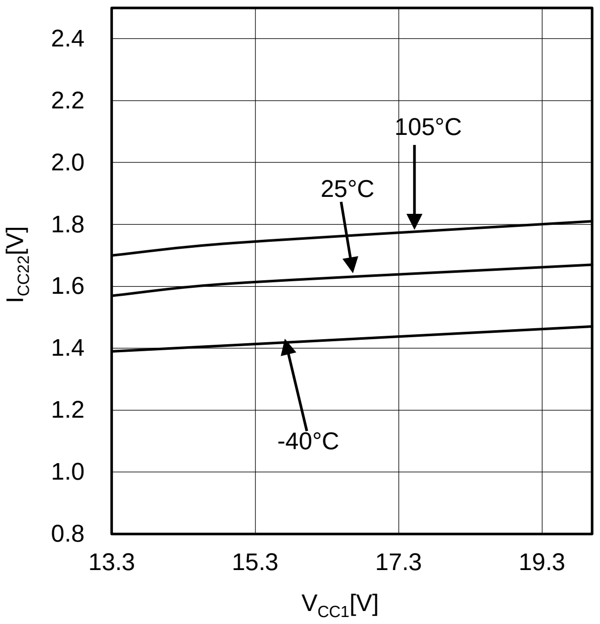


Figure 17. Output side circuit current 2
(V_{EE2}=-8V, OUT=H)

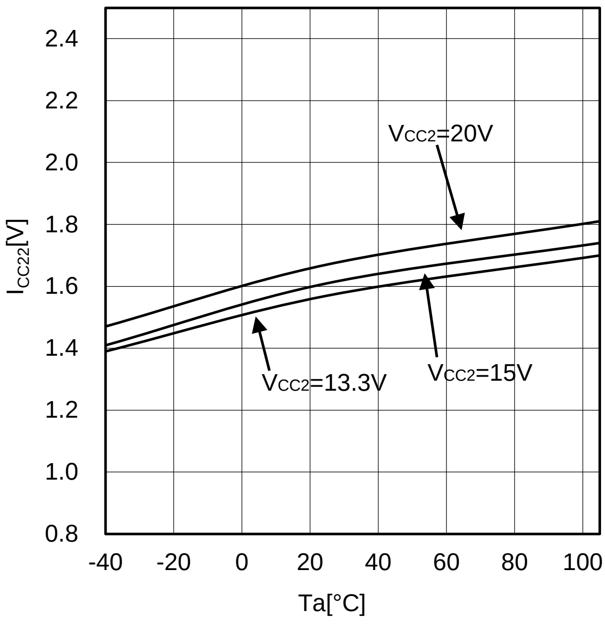


Figure 18. Output side circuit current 2
(V_{EE2}=-8V, OUT=H)

Typical Performance Curves - continued

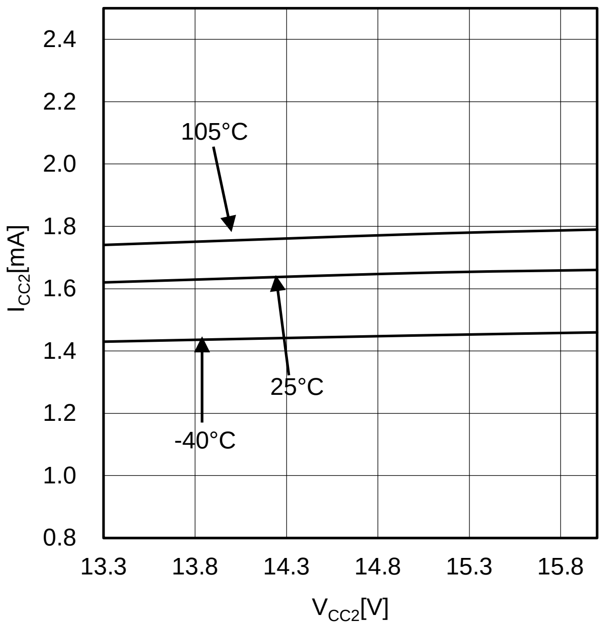


Figure 19. Output side circuit current 2
(V_{EE2}=-12V, OUT=H)

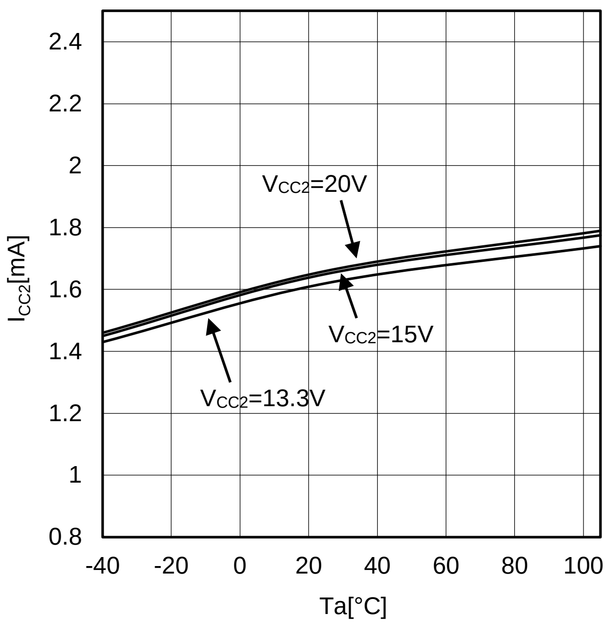


Figure 20. Output side circuit current 2
(V_{EE2}=-12V, OUT=H)

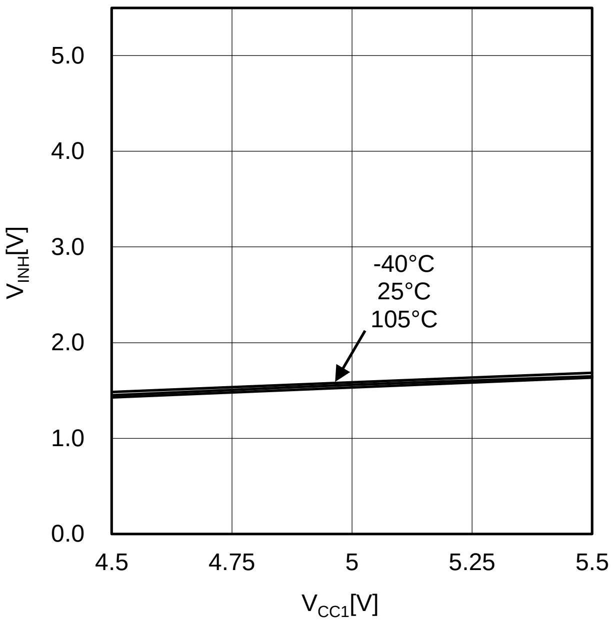


Figure 21. Logic high level input voltage

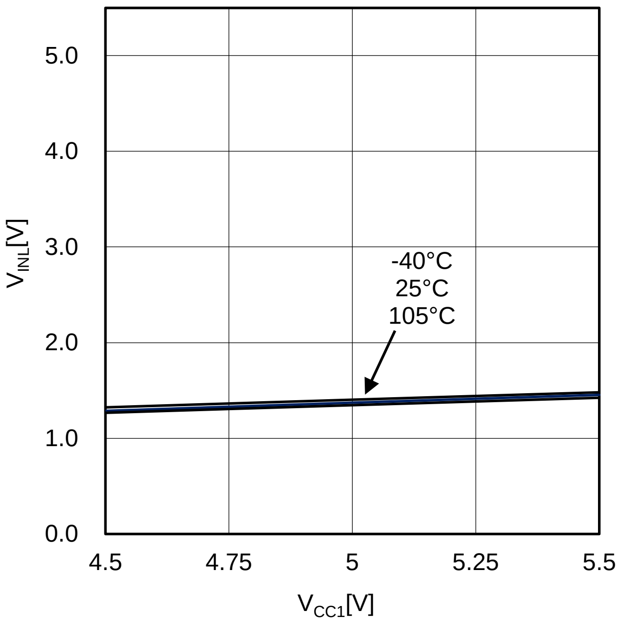


Figure 22. Logic Low level input voltage

Typical Performance Curves - continued

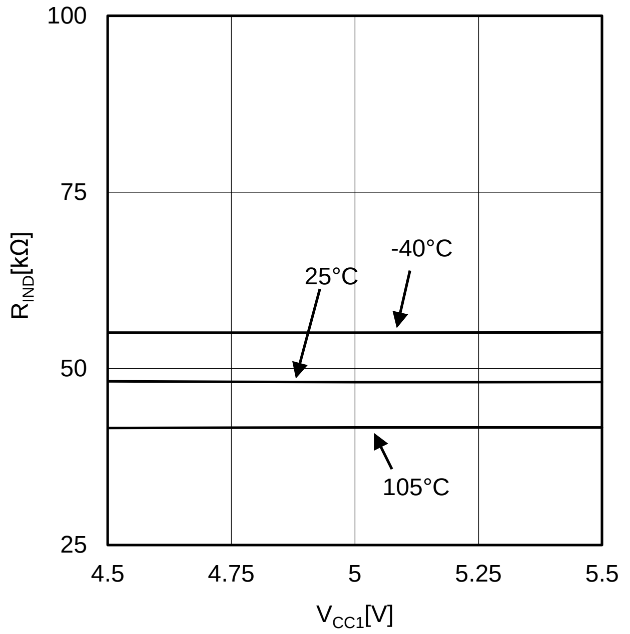


Figure 23. Logic pull-down resistance

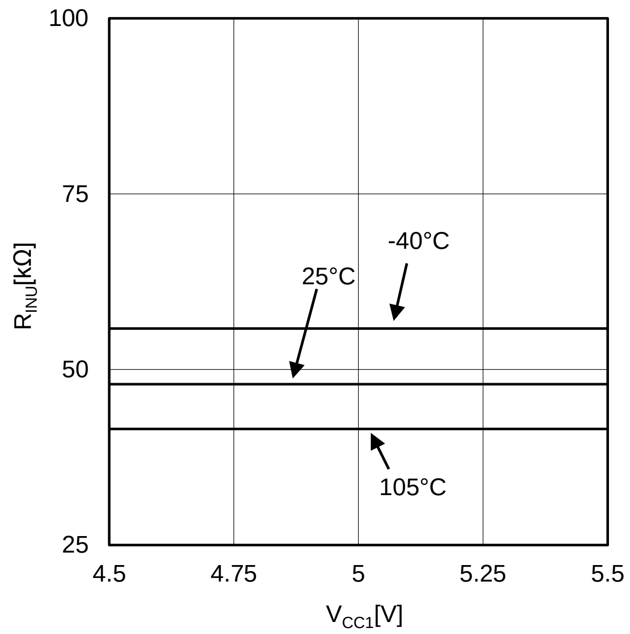


Figure 24. Logic pull-up resistance

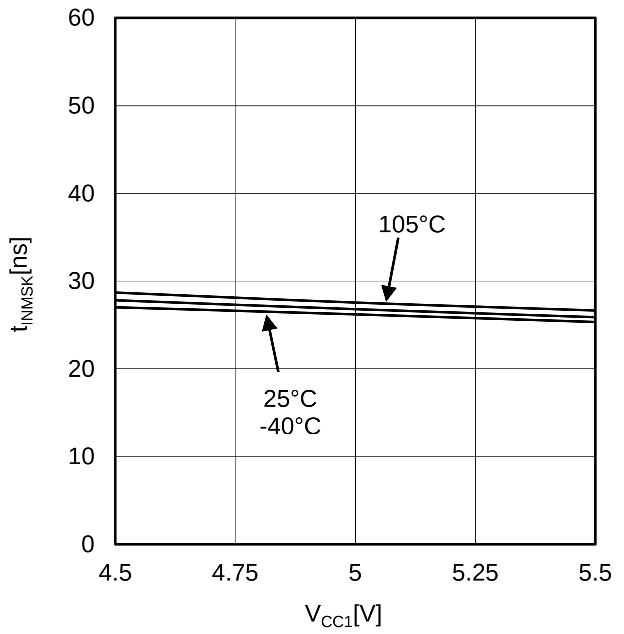


Figure 25. Logic input mask time

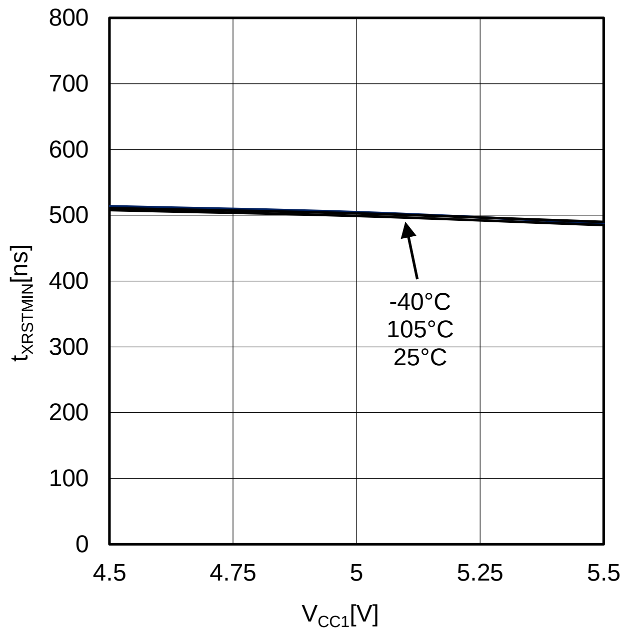


Figure 26. Minimum XRST pulse width

Typical Performance Curves - continued

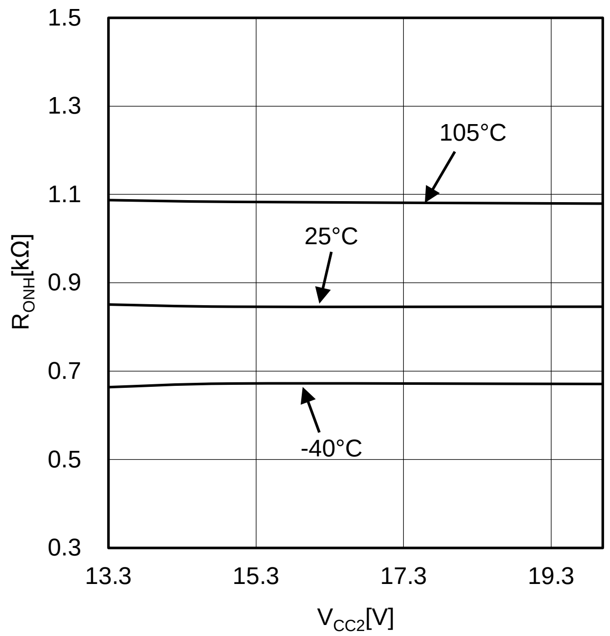


Figure 27. OUT ON resistance (Source)

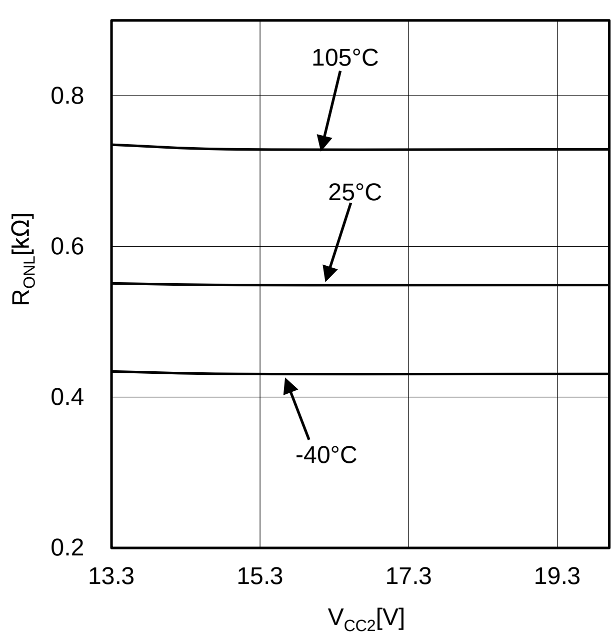


Figure 28. OUT ON resistance (Sink)

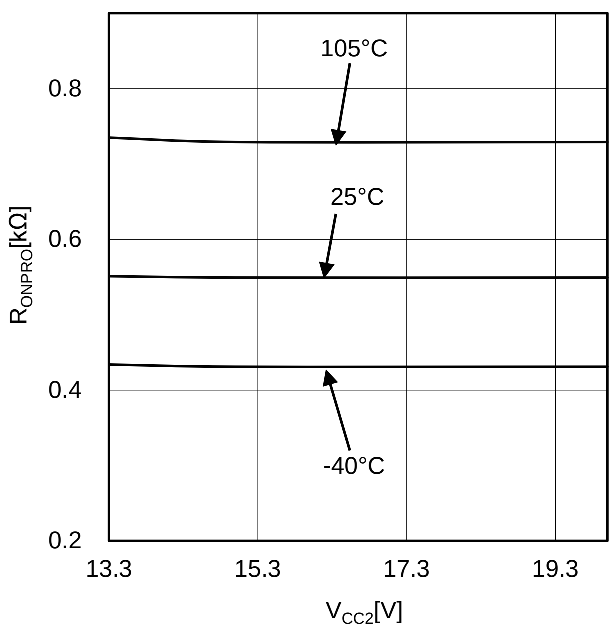


Figure 29. CLAMP ON resistance

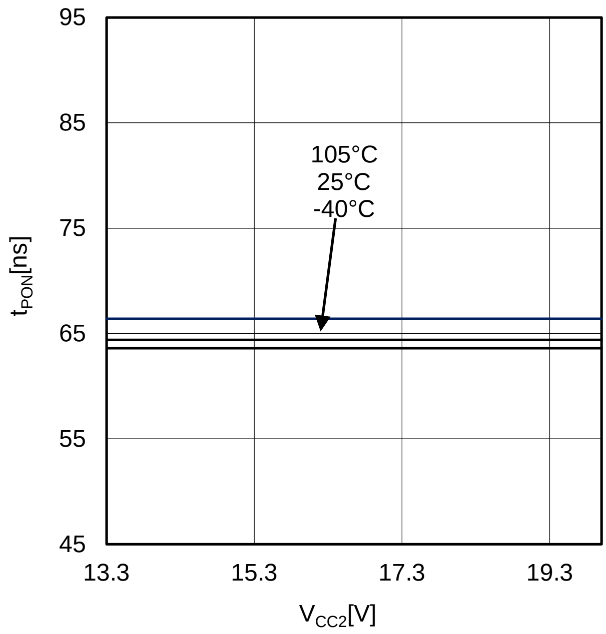


Figure 30. Turn ON time

Typical Performance Curves - continued

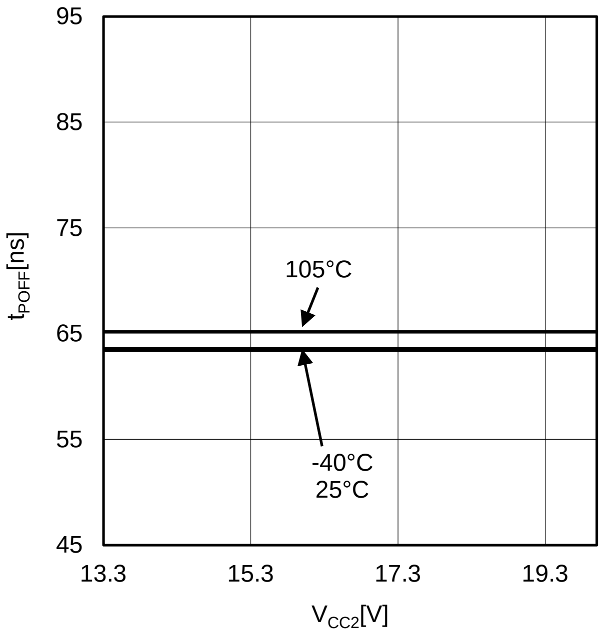


Figure 31. Turn OFF time

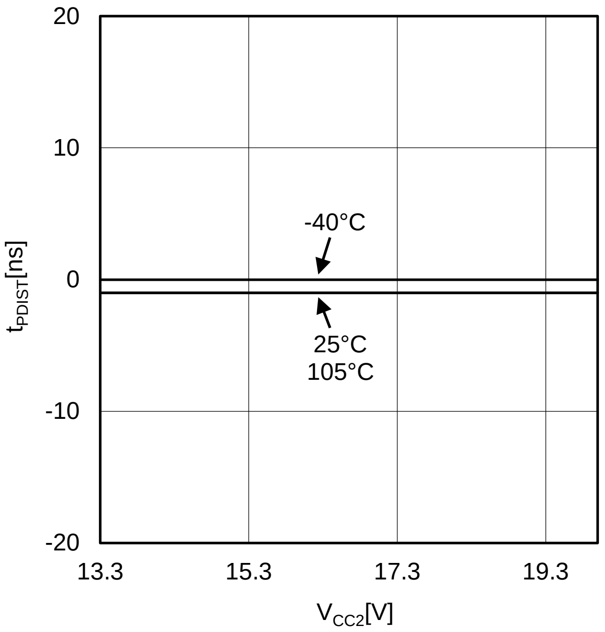


Figure 32. Propagation distortion

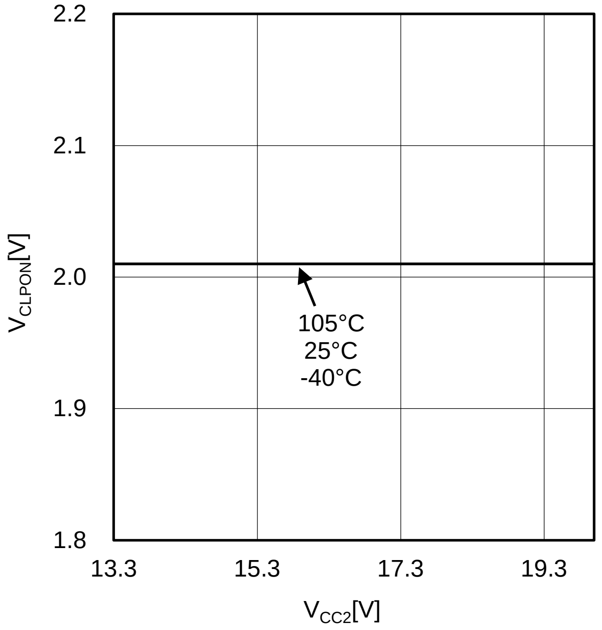


Figure 33. CLAMP ON threshold voltage

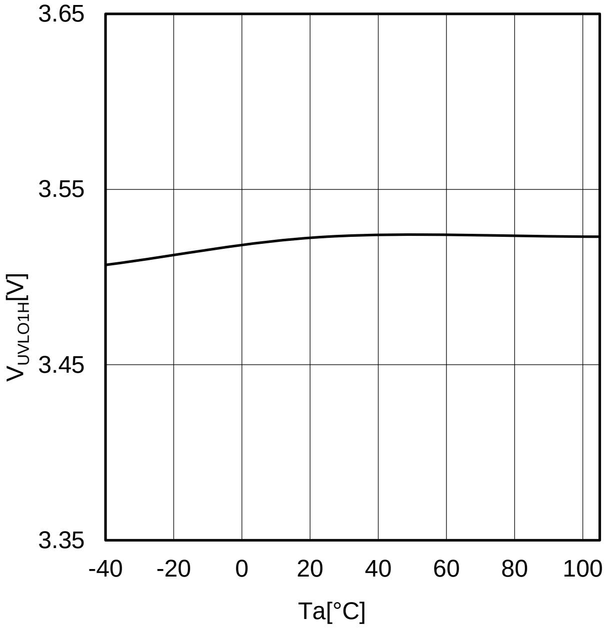


Figure 34. VCC1 UVLO OFF voltage

Typical Performance Curves - continued

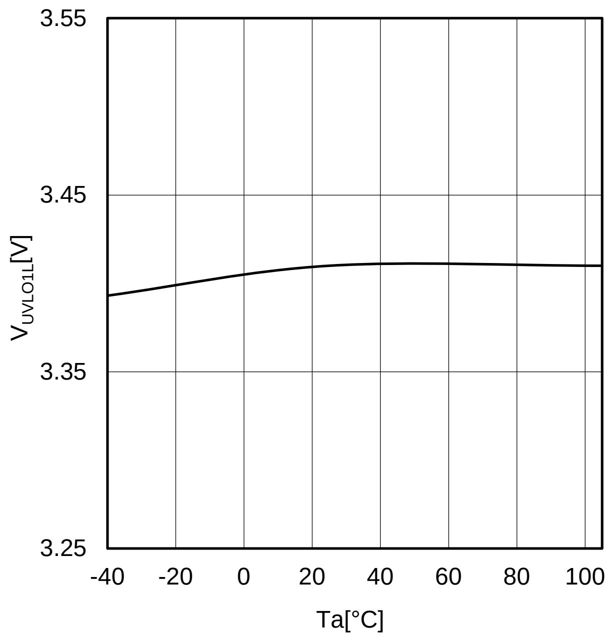


Figure 35. VCC1 UVLO ON voltage

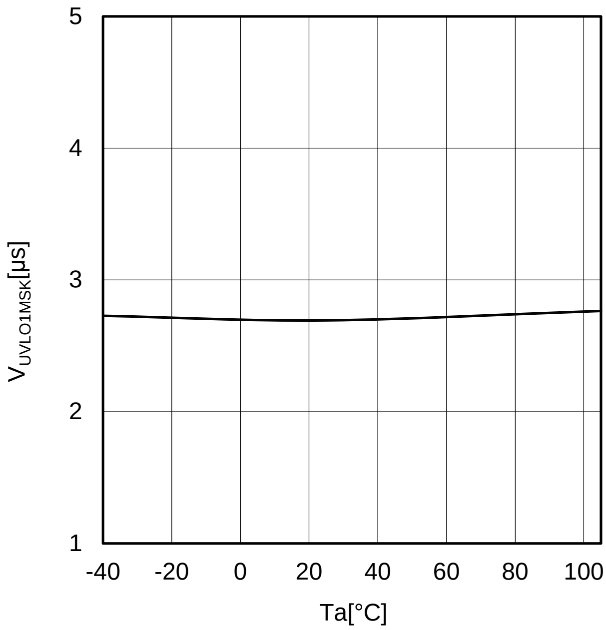


Figure 36. VCC1 UVLO mask time

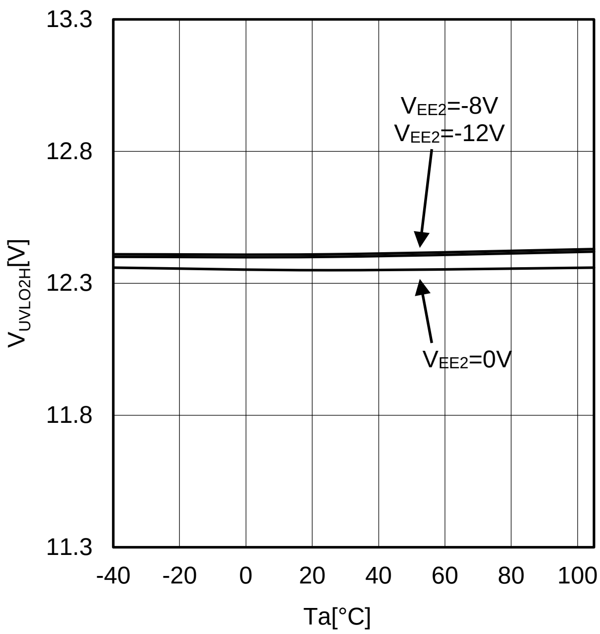


Figure 37. VCC2 UVLO OFF voltage

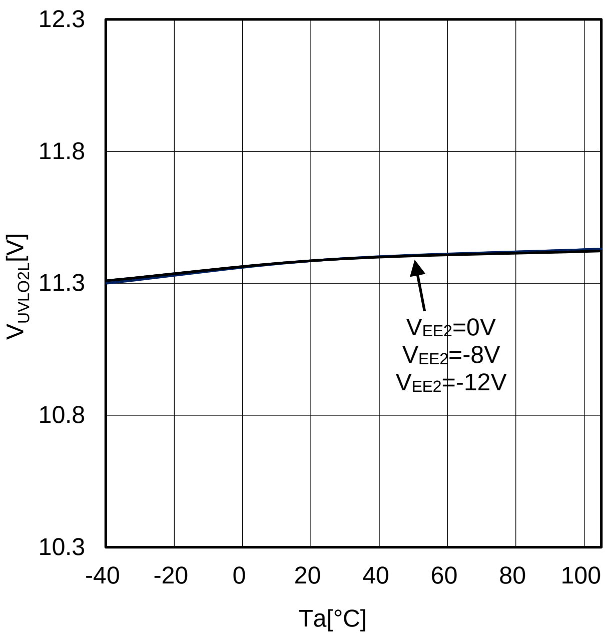


Figure 38. VCC2 UVLO ON voltage

Typical Performance Curves - continued

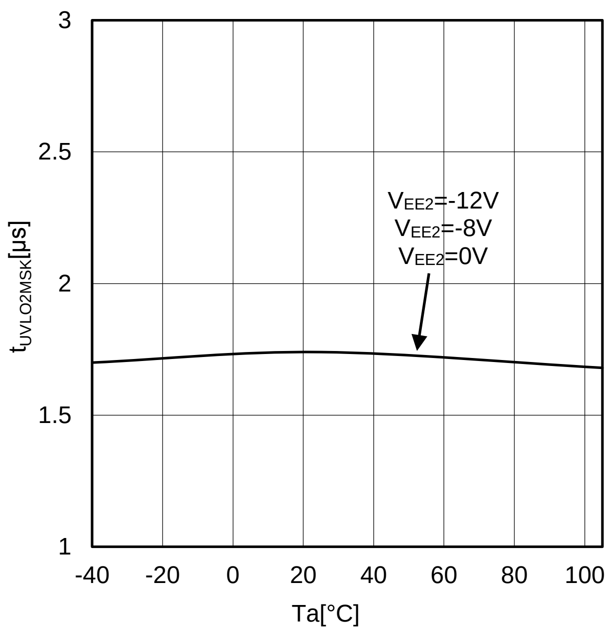


Figure 39. VCC2 UVLO mask time

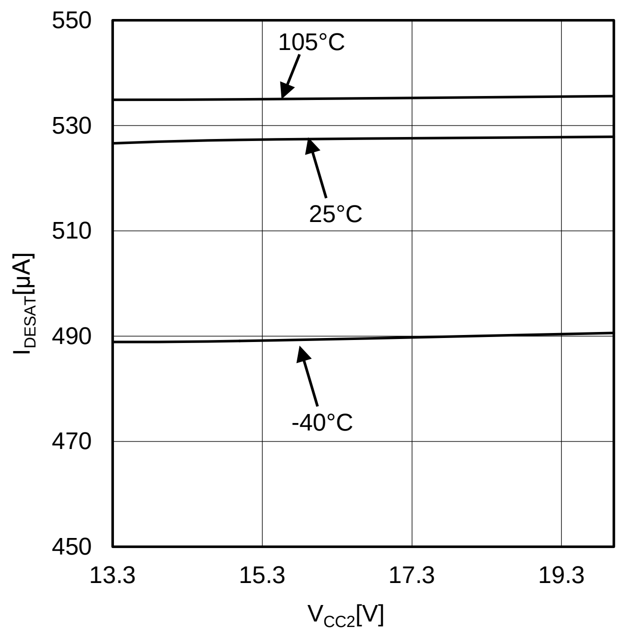


Figure 40. DESAT source current

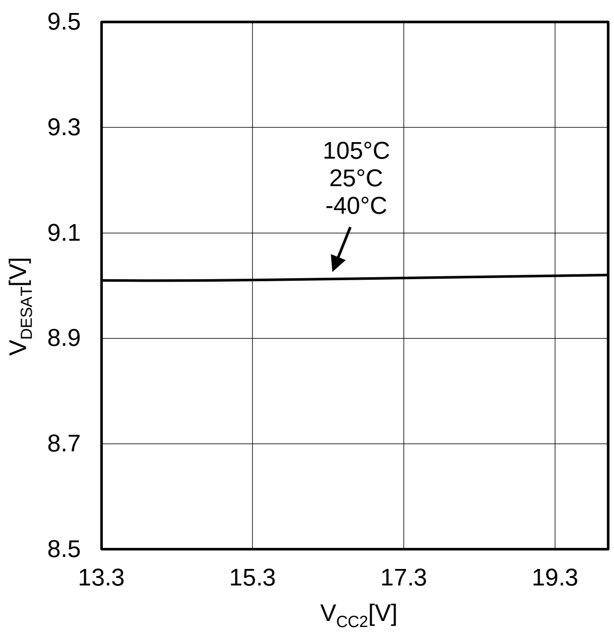


Figure 41. DESAT threshold voltage

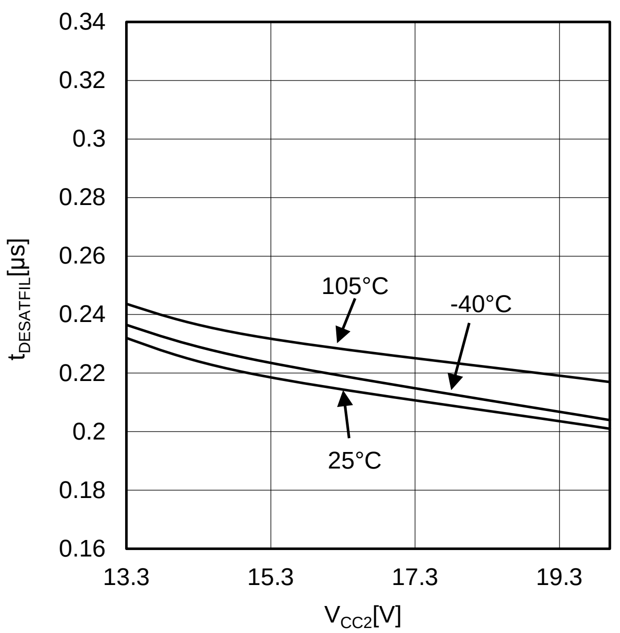


Figure 42. DESAT filter time

Typical Performance Curves - continued

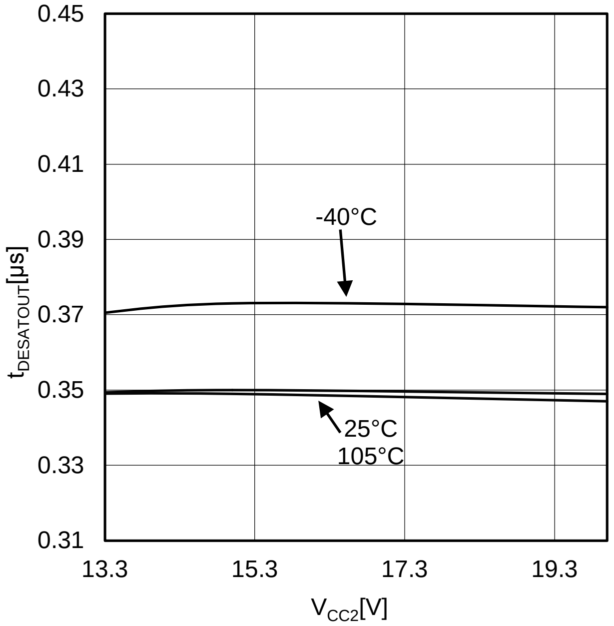


Figure 43. DESAT delay time (OUT)

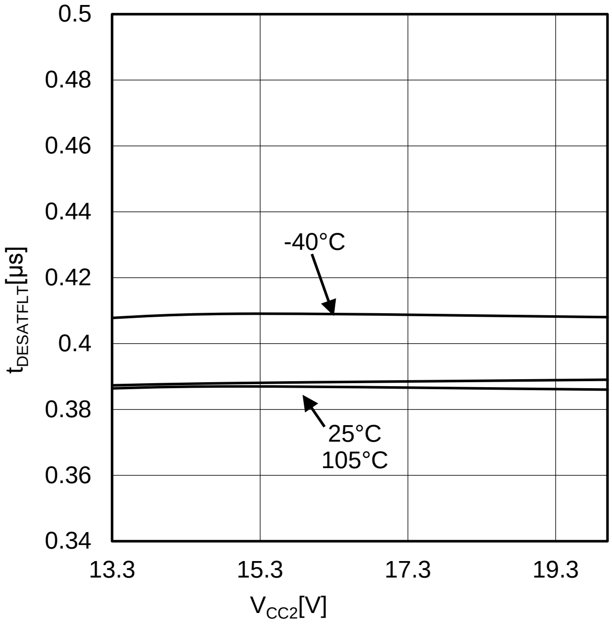


Figure 44. DESAT delay time (FLT)

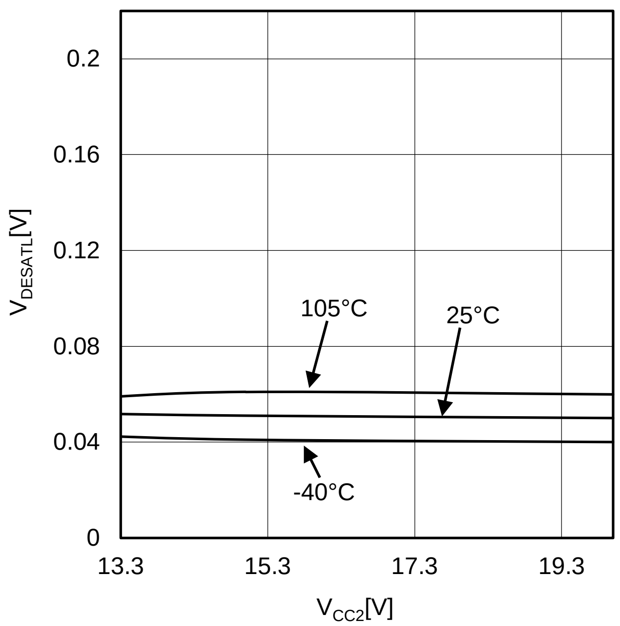


Figure 45. DESAT low voltage

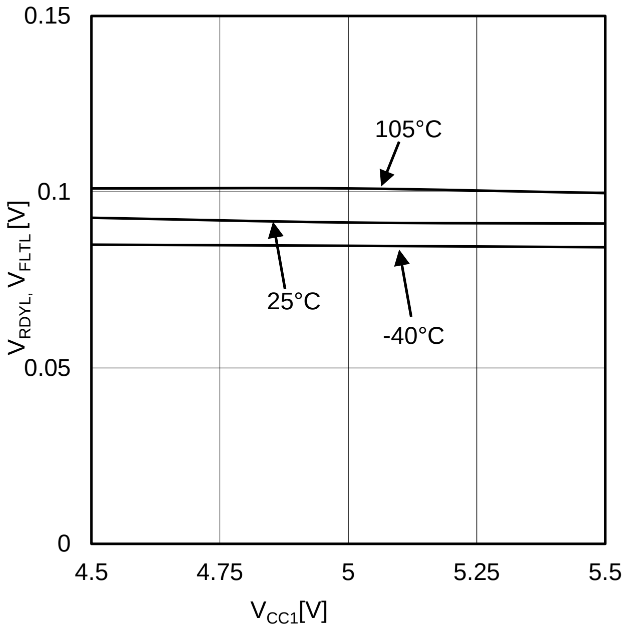


Figure 46. RDY output low voltage
FLT output low voltage

Description of pins and cautions on layout of board

1. VCC1 (Input-side power supply pin)
   The VCC1 pin is a power supply pin on the input side. To suppress voltage fluctuations due to the current to drive internal transformers, connect a bypass capacitor between the VCC1 and the GND1 pins.

2. GND1 (Input-side ground pin)
   The GND1 pin is a ground pin on the input side.

3. VCC2 (Output-side positive power supply pin)
   The VCC2 pin is a positive power supply pin on the output side. To reduce voltage fluctuations due to OUT pin output current and due to the current to drive internal transformers, connect a bypass capacitor between the VCC2 and the GND2 pins.

4. VEE2 (Output-side negative power supply pin)
   The VEE2 pin is a power supply pin on the output side. To suppress voltage fluctuations due to OUT pin output current and due to the current to drive internal transformers, connect a bypass capacitor between the VEE2 and the GND2 pins. To use no negative power supply, connect the VEE2 pin to the GND2 pin.

5. GND2 (Output-side ground pin)
   The GND2 pin is a ground pin on the output side. Connect the GND2 pin to the emitter / source of a power device.

6. INA, INB and XRST (Control input terminal)
   The INA, INB and XRST pin is a pin used to determine output logic. And XRST is in charge of setting back the FLT pin.

XRST	INB	INA	OUT
L	X	X	L
H	H	X	L
H	L	L	L
H	L	H	H

7. FLT (Fault output pin)
   The FLT pin is an open drain pin used to output a fault signal when desaturation function is activated, and will be cleared at the rising edge of FLT.

Status	FLT
While in normal operation	H
When desaturation function is activated	L

8. RDY (Ready output pin)
   The RDY pin shows the status of three internal protection features which are VCC1 UVLO, VCC2 UVLO, and output state feedback (OSFB). The term ‘output state feedback’ shows whether output internal logic is high or low corresponds to input logic or not.

Status	RDY
While in normal operation	H
VCC1 UVLO or VCC2 UVLO or Output internal logic feedback	L

9. OUT (Output pin)
   The OUT pin is a pin used to drive the gate of a power device.

10. CLAMP (Miller clamp pin)
    The CLAMP pin is a pin for preventing increase in gate voltage due to the miller current of the power device connected to OUT pin. CLAMP should be disconnected when miller clamp function is not used.

11. DESAT (Desaturation protection pin)
    The DESAT pin is a pin used to detect desaturation of IGBT/MOSFET. When the DESAT pin voltage exceeds V_{DESAT}, the DESAT function will be activated. This may cause the IC to malfunction in an open state. To avoid such trouble, short-circuit the DESAT pin to the GND2 pin if the desaturation protection is not used. In order to prevent the wrong detection due to noise, the noise mask time $t_{DESATFIL}$ is set.

Description of functions and examples of constant setting

1. Miller clamp function

If OUT=L and the CLAMP pin voltage < V_{CLPON}, the internal MOSFET of the CLAMP pin turns on.

OUT	CLAMP	Internal MOSFET of the CLAMP pin
L	Less than V_{CLPON}	ON
L	Not less than V_{CLPON}	OFF
H	X	OFF

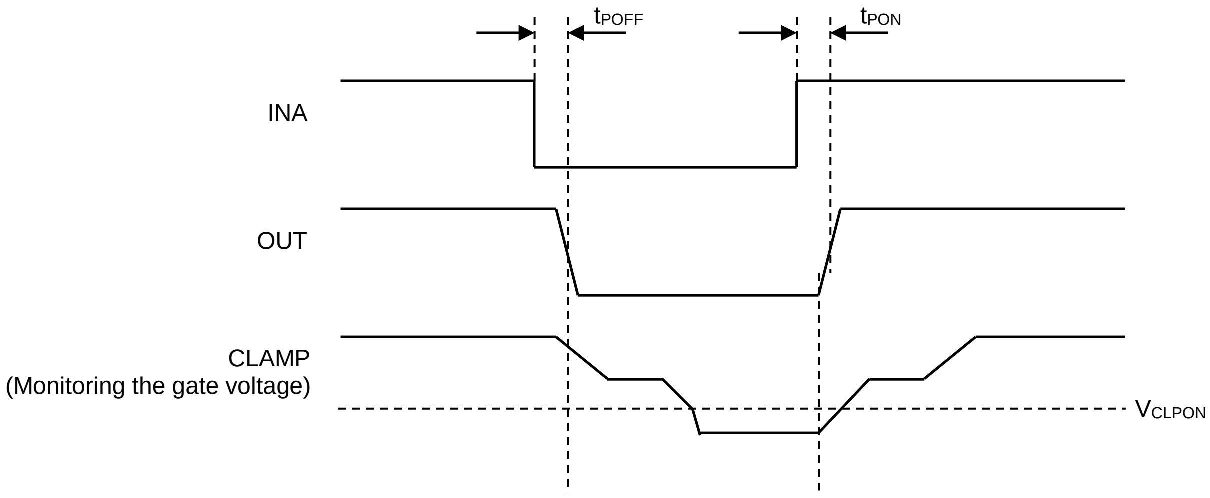


Figure 47. Timing chart of Miller clamp function

2. Fault status output

This function is used to output a fault signal from the FLT pin when the desaturation protection function is activated and hold the Fault signal until rising edge of XRST is put in.

3. Undervoltage Lockout (UVLO) function

The BM6105FW-LBZ incorporates the undervoltage lockout (UVLO) function both on the input and the output sides. When the power supply voltage drops to the UVLO ON voltage, the OUT pin and the RDY pin both will output the “L” signal. When the power supply voltage rises to the UVLO OFF voltage, these pins will be reset. To prevent malfunctions due to noises, mask time $t_{UVLO1MSK}$ and $t_{UVLO2MSK}$ are set on both input and output sides.

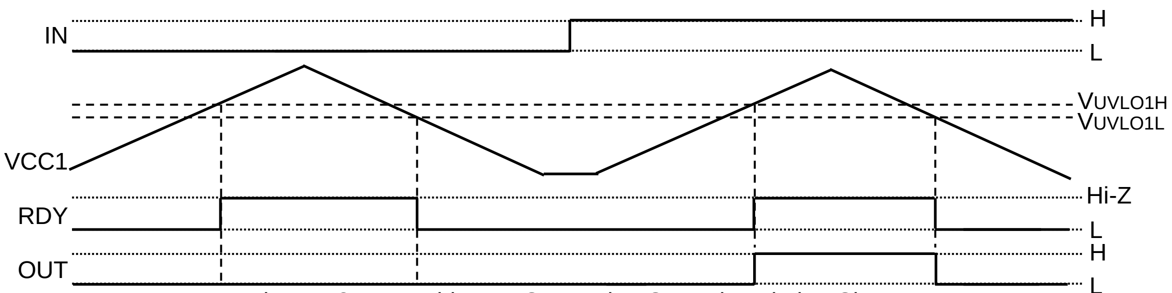


Figure 48. Input-side UVLO Function Operation Timing Chart

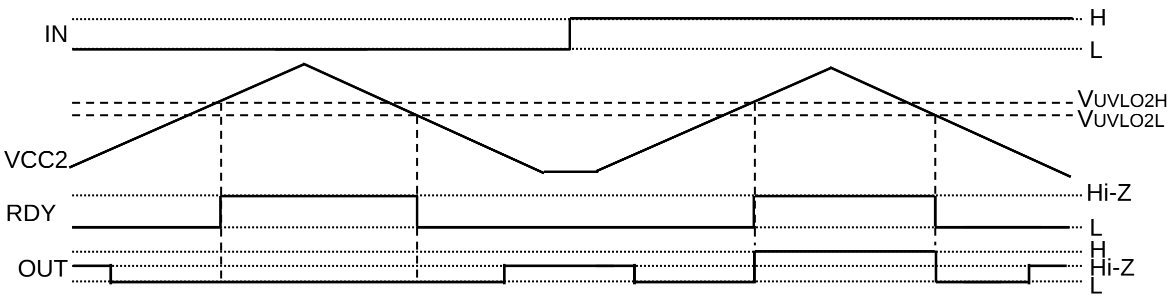


Figure 49. Output-side UVLO Operation Timing Chart

4. Desaturation protection function (DESAT)

When the DESAT pin voltage exceeds V_{DESAT}, the DESAT function will be activated. When the DESAT function is activated, the OUT pin voltage will be set to the “L” level, and then the FLT pin voltage to the “L” level. When the rising edge is put in the XRST pin, the DESAT function will be released.

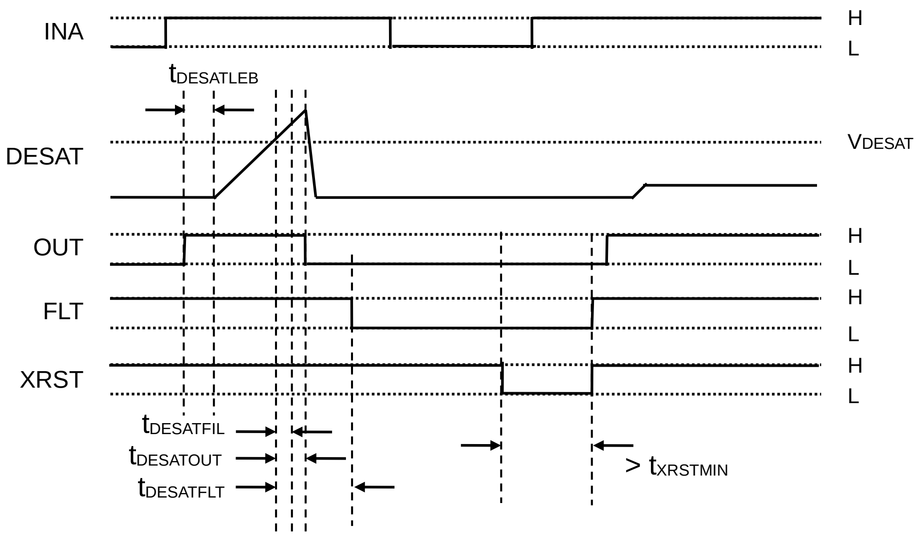


Figure 50. DESAT Operation Timing Chart

5.I/O condition table

No.	Status	Input							Output			
		VCC1	VCC2	DESAT	XRST	INB	INA	CLAMP	OUT	CLAMP	FLT	RDY
1	VCC1UVLO	UVLO	X	X	X	X	X	H	L	Hi-Z	H	L
2		UVLO	X	X	X	X	X	L	L	L	H	L
3	VCC2UVLO	○	UVLO	L	X	X	X	H	L	Hi-Z	H	L
4		○	UVLO	L	X	X	X	L	L	L	H	L
5		○	UVLO	H	X	X	X	H	L	Hi-Z	L	L
6		○	UVLO	H	X	X	X	L	L	L	L	L
7	DESAT	○	○	H	X	X	X	H	L	Hi-Z	L	H(*)
8		○	○	H	X	X	X	L	L	L	L	H(*)
9	XRST	○	○	L	L	X	X	H	L	Hi-Z	H	H(*)
10		○	○	L	L	X	X	L	L	L	H	H(*)
11	Normal operation	○	○	L	H	H	X	H	L	Hi-Z	H	H(*)
12		○	○	L	H	H	X	L	L	L	H	H(*)
13		○	○	L	H	L	L	H	L	Hi-Z	H	H(*)
14		○	○	L	H	L	L	L	L	L	H	H(*)
15		○	○	L	H	L	H	X	H	Hi-Z	H	H(*)

○: VCC1 or VCC2 > UVLO, X:Don't care

(*) If the internal logic of high voltage side doesn’t become the expected value, the RDY pin will become “L”. And this stage is cleared automatically if the internal logic of high voltage side becomes the expected value.

Power Dissipation

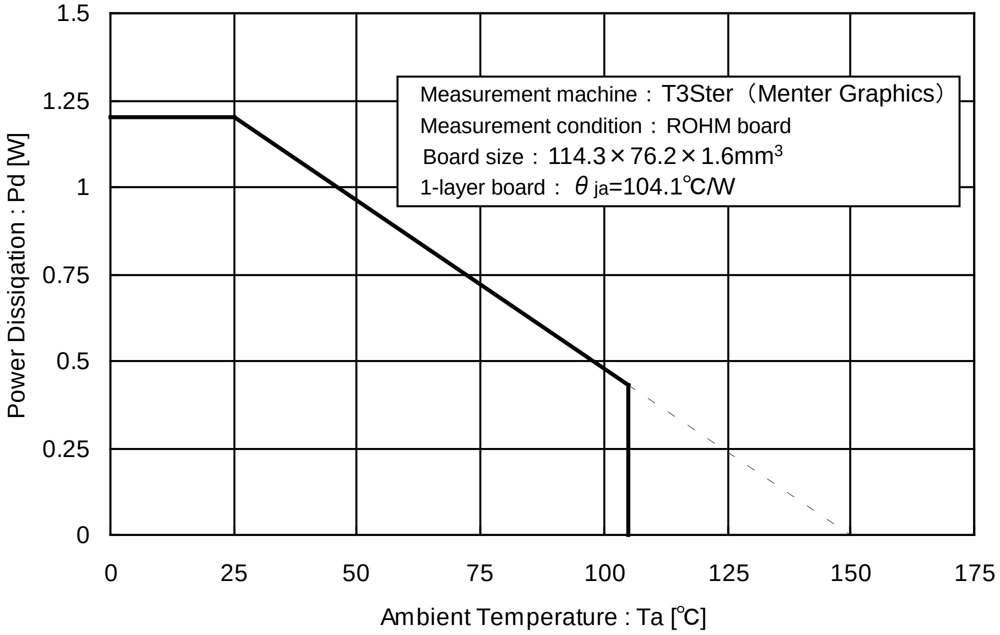
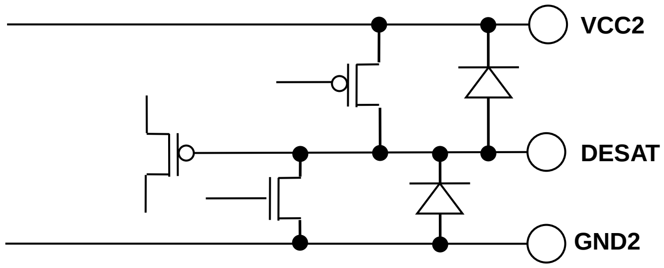
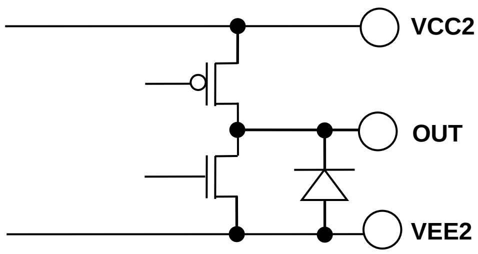
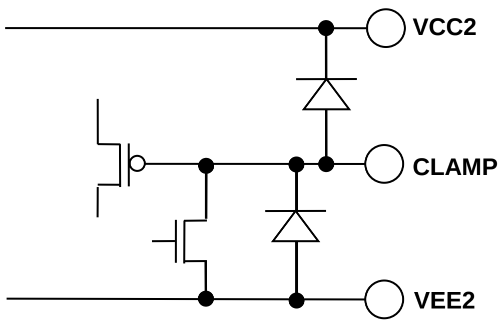


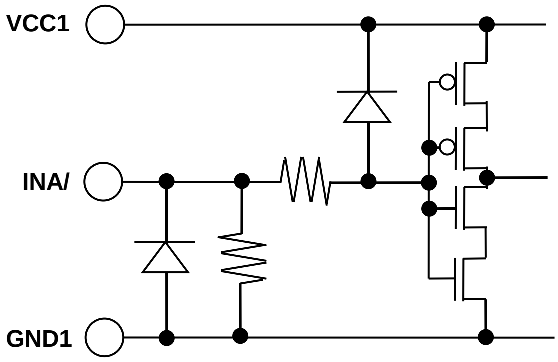
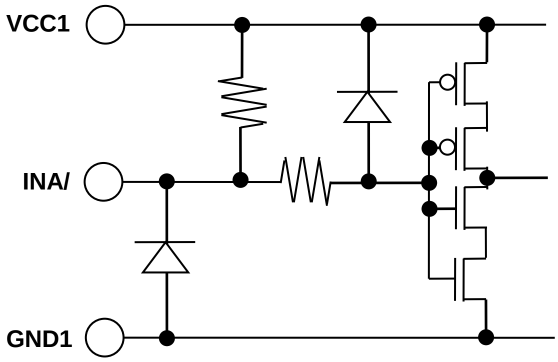
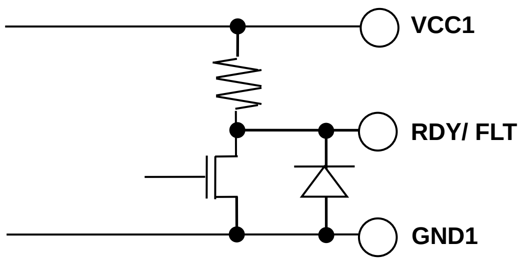
Figure 51. SOP16WM Derating Curve

Thermal design

Please confirm that the IC's chip temperature Tj is not over 150°C, while considering the IC's power consumption (W), package power (Pd) and ambient temperature (Ta). When Tj=150°C is exceeded the functions as a semiconductor do not operate and some problems (ex. Abnormal operation of various parasitic elements and increasing of leak current) occur. Constant use under these circumstances leads to deterioration and eventually IC may destruct. Tjmax=150°C must be strictly obeyed under all circumstances.

I/O equivalence circuits

Pin No.	Name	Function	I/O equivalence circuits
2	DESAT	Desaturation protection pin	
6	OUT	Output pin	
7	CLAMP	Miller clamp pin	

Pin No.	Name Function	I/O equivalence circuits
10	INA Control input pin	
11	INB Opposite driver's control input pin	
14	XRST Reset input pin	
12	RDY Ready output pin	
13	FLT Fault output pin	

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins of input side (9pin to 16pin) are at a voltage below that of the GND1 pin at any time, even during transient condition.
   Ensure that no pins of output side (1pin to 8pin) are at a voltage below that of the VEE2 pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes – continued

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

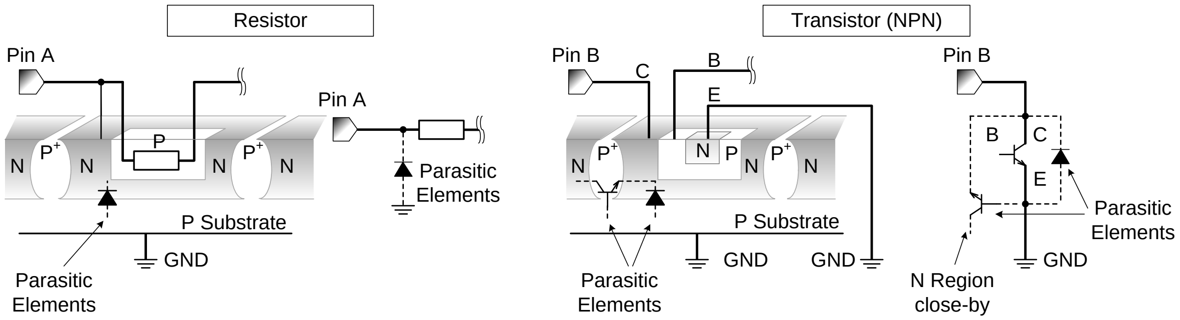


Figure 52. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

Ordering Information

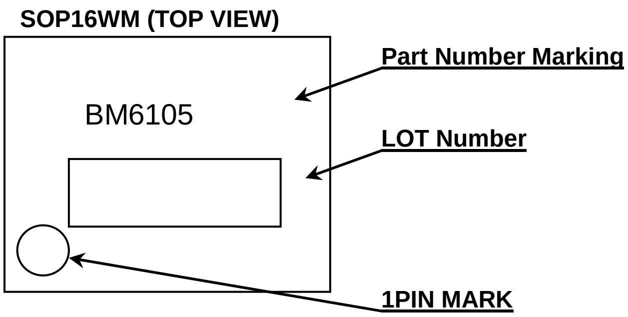
B M 6 1 0 5 F W - L B Z E 2

Part Number

Package
FW:SOP16WM

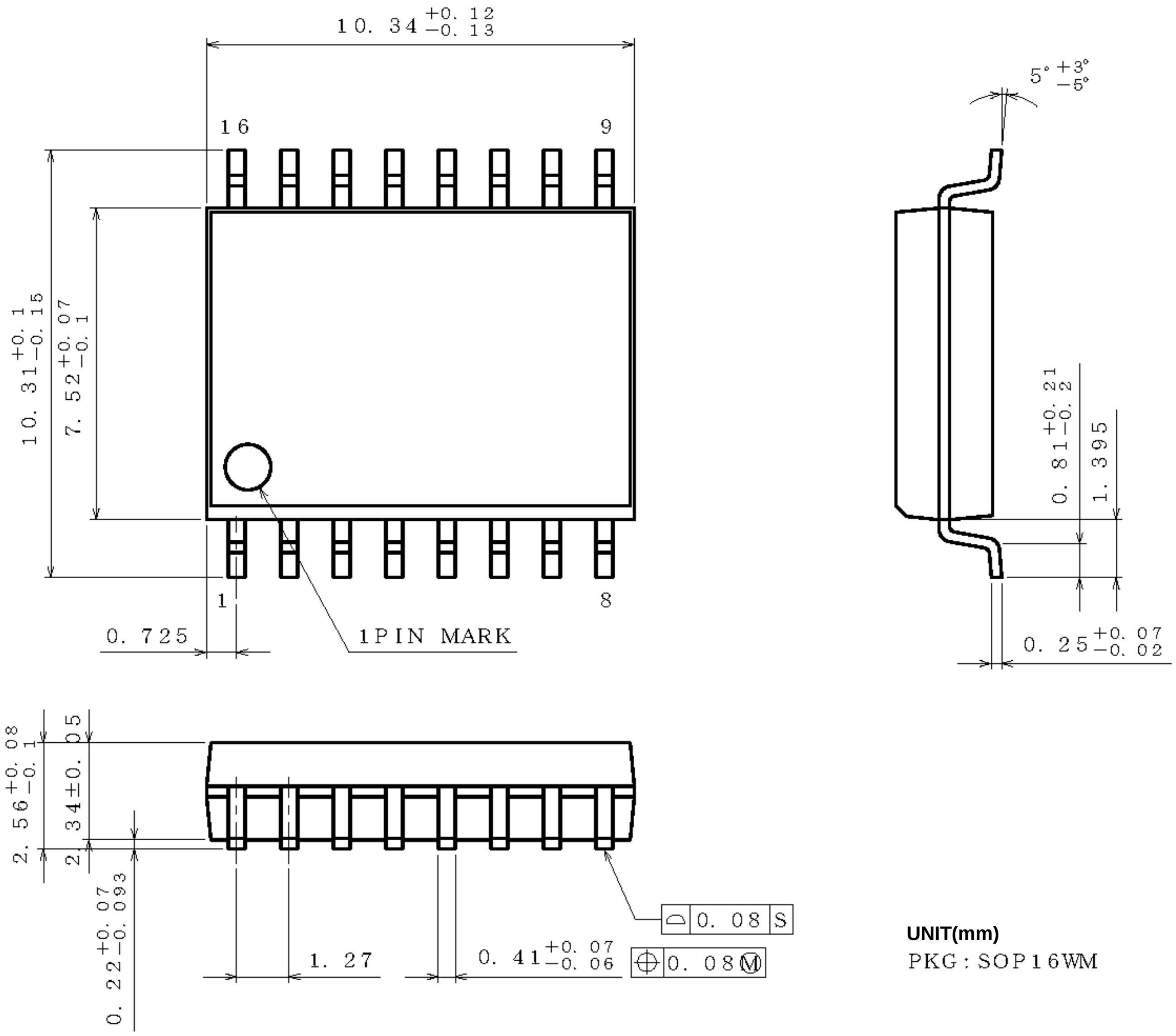
Product class
LB for Industrial applications
Packaging and forming specification
E2: Embossed tape and reel

Marking Diagram(TOP VIEW)



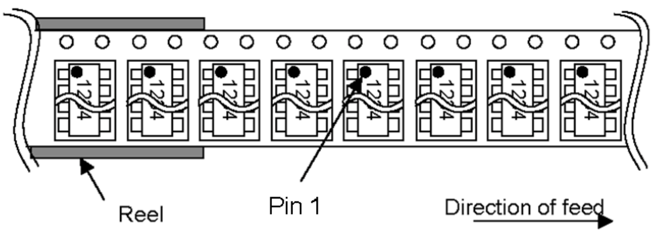
Physical Dimension Tape and Reel Information

Package Name	**SOP16WM**



< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	1500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
22.Sep.2014	001	New Release
07.Nov.2014	002	Page 4 : Add “Common Mode Transient Immunity”

Notice

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(Note1) Medical Equipment Classification of the Specific Applications

<table>
<tr><th>JAPAN</th><th>USA</th><th>EU</th><th>CHINA</th></tr>
<tr><td>CLASSⅢ</td><td rowspan="2">CLASSⅢ</td><td>CLASSⅡb</td><td rowspan="2">CLASSⅢ</td></tr>
<tr><td>CLASSⅣ</td><td>CLASSⅢ</td></tr>
</table>

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   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

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1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
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   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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