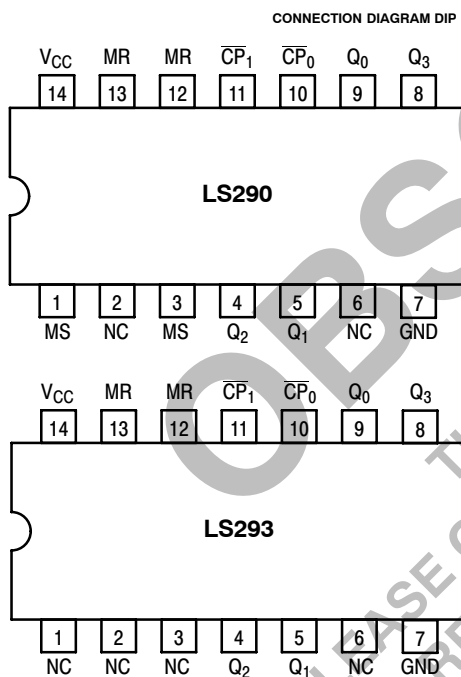


# SN74LS290

## DECADE COUNTER; 4-BIT BINARY COUNTER

The SN54/74LS290 and SN54/74LS293 are high-speed 4-bit ripple type counters partitioned into two sections. Each counter has a divide-by-two section and either a divide-by-five (LS290) or divide-by-eight (LS293) section which are triggered by a HIGH-to-LOW transition on the clock inputs. Each section can be used separately or tied together (Q to  $\overline{CP}$ ) to form BCD, Bi-quinary, or Modulo-16 counters. Both of the counters have a 2-input gated Master Reset (Clear), and the LS290 also has a 2-input gated Master Set (Preset 9).

- Corner Power Pin Versions of the LS90 and LS93
- Low Power Consumption . . . Typically 45 mW
- High Count Rates . . . Typically 42 MHz
- Choice of Counting Modes . . . BCD, Bi-Quinary, Binary
- Input Clamp Diodes Limit High Speed Termination Effects



NOTE:  
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

### PIN NAMES

|                   |  |
|-------------------|--|
| $\overline{CP}_0$ | Clock (Active LOW going edge) Input to +2 Section.         |
| $\overline{CP}_1$ | Clock (Active LOW going edge) Input to +5 Section (LS290). |
| $\overline{CP}_1$ | Clock (Active LOW going edge) Input to +8 Section (LS293). |
| MR1, MR2          | Master Reset (Clear) Inputs                                |
| MS1, MS2          | Master Set (Preset-9, LS290) Inputs                        |
| Q0                | Output from +2 Section (Notes b & c)                       |
| Q1, Q2, Q3        | Outputs from +5 & +8 Sections (Note b)                     |

### NOTES:

- 1 TTL Unit Load (U.L.) = 40  $\mu$ A HIGH/1.6 mA LOW.
- The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.
- The Q<sub>0</sub> Outputs are guaranteed to drive the full fan-out plus the  $\overline{CP}_1$  Input of the device.

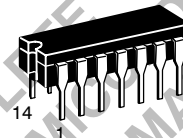


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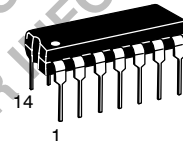
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## DECADE COUNTER; 4-BIT BINARY COUNTER

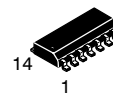
### LOW POWER SCHOTTKY



**J SUFFIX**  
CERAMIC  
CASE 632-08



**N SUFFIX**  
PLASTIC  
CASE 646-06



**D SUFFIX**  
SOIC  
CASE 751A-02

### ORDERING INFORMATION

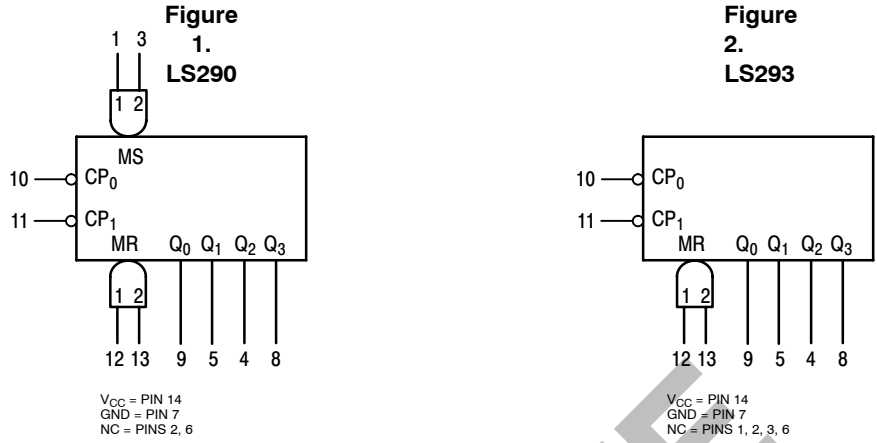
|            |         |
|------------|---------|
| SN54LSXXXJ | Ceramic |
| SN74LSXXXN | Plastic |
| SN74LSXXXD | SOIC    |

### LOADING (Note a)

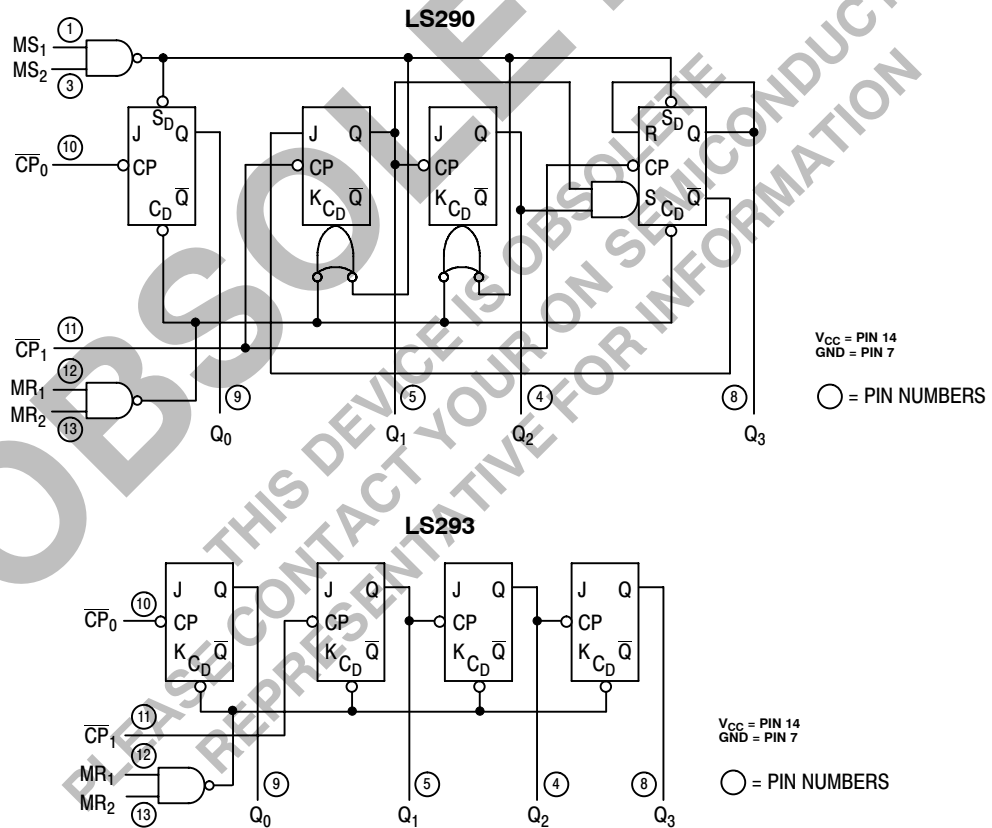
| HIGH      | LOW          |
|-----------|--------------|
| 0.05 U.L. | 1.5 U.L.     |
| 0.05 U.L. | 2.0 U.L.     |
| 0.05 U.L. | 1.0 U.L.     |
| 0.5 U.L.  | 0.25 U.L.    |
| 0.5 U.L.  | 0.25 U.L.    |
| 10 U.L.   | 5 (2.5) U.L. |
| 10 U.L.   | 5 (2.5) U.L. |

# SN74LS290

## LOGIC SYMBOL



## LOGIC DIAGRAMS



**FUNCTIONAL DESCRIPTION**

The LS290 and LS293 are 4-bit ripple type Decade, and 4-Bit Binary counters respectively. Each device consists of four master/slave flip-flops which are internally connected to provide a divide-by-two section and a divide-by-five (LS290) or divide-by-eight (LS293) section. Each section has a separate clock input which initiates state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes. The Q<sub>0</sub> output of each device is designed and specified to drive the rated fan-out plus the  $\overline{CP}_1$  input of the device.

A gated AND asynchronous Master Reset (MR<sub>1</sub> · MR<sub>2</sub>) is provided on both counters which overrides the clocks and resets (clears) all the flip-flops. A gated AND asynchronous Master Set (MS<sub>1</sub> · MS<sub>2</sub>) is provided on the LS290 which overrides the clocks and the MR inputs and sets the outputs to nine (HLLH).

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the devices may be operated in various counting modes:

**LS290**

A. BCD Decade (8421) Counter — the  $\overline{CP}_1$  input must be externally connected to the Q<sub>0</sub> output. The  $\overline{CP}_0$  input

receives the incoming count and a BCD count sequence is produced.

B. Symmetrical Bi-quinary Divide-By-Ten Counter — The Q<sub>3</sub> output must be externally connected to the  $\overline{CP}_0$  input. The input count is then applied to the  $\overline{CP}_1$  input and a divide-by-ten square wave is obtained at output Q<sub>0</sub>.

C. Divide-By-Two and Divide-By-Five Counter — No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function ( $\overline{CP}_0$  as the input and Q<sub>0</sub> as the output). The  $\overline{CP}_1$  input is used to obtain binary divide-by-five operation at the Q<sub>3</sub> output.

**LS293**

A. 4-Bit Ripple Counter — The output Q<sub>0</sub> must be externally connected to input  $\overline{CP}_1$ . The input count pulses are applied to input  $\overline{CP}_0$ . Simultaneous division of 2, 4, 8, and 16 are performed at the Q<sub>0</sub>, Q<sub>1</sub>, Q<sub>2</sub>, and Q<sub>3</sub> outputs as shown in the truth table.

B. 3-Bit Ripple Counter — The input count pulses are applied to input  $\overline{CP}_1$ . Simultaneous frequency divisions of 2, 4, and 8 are available at the Q<sub>1</sub>, Q<sub>2</sub>, and Q<sub>3</sub> outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.

**LS290 MODE SELECTION**

| RESET/SET INPUTS |                 |                 |                 | OUTPUTS        |                |                |                |
|------------------|-----------------|-----------------|-----------------|----------------|----------------|----------------|----------------|
| MR <sub>1</sub>  | MR <sub>2</sub> | MS <sub>1</sub> | MS <sub>2</sub> | Q <sub>0</sub> | Q <sub>1</sub> | Q <sub>2</sub> | Q <sub>3</sub> |
| H                | H               | L               | X               | L              | L              | L              | L              |
| H                | H               | X               | L               | L              | L              | L              | L              |
| X                | X               | H               | H               | H              | L              | L              | H              |
| L                | X               | L               | X               |                |                |                | Count          |
| X                | L               | X               | L               |                |                |                | Count          |
| L                | X               | X               | L               |                |                |                | Count          |
| X                | L               | L               | X               |                |                |                | Count          |

**LS290**

**BCD COUNT SEQUENCE**

| COUNT | OUTPUT         |                |                |                |
|-------|----------------|----------------|----------------|----------------|
|       | Q <sub>0</sub> | Q <sub>1</sub> | Q <sub>2</sub> | Q <sub>3</sub> |
| 0     | L              | L              | L              | L              |
| 1     | H              | L              | L              | L              |
| 2     | L              | H              | L              | L              |
| 3     | H              | H              | L              | L              |
| 4     | L              | L              | H              | L              |
| 5     | H              | L              | H              | L              |
| 6     | L              | H              | H              | L              |
| 7     | H              | H              | H              | L              |
| 8     | L              | L              | L              | H              |
| 9     | H              | L              | L              | H              |

NOTE: Output Q<sub>0</sub> is connected to Input CP<sub>1</sub> for BCD count.

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Don't Care

LS293 MODE SELECTION

| RESET INPUTS    |                 | OUTPUTS        |                |                |                |
|-----------------|-----------------|----------------|----------------|----------------|----------------|
| MR <sub>1</sub> | MR <sub>2</sub> | Q <sub>0</sub> | Q <sub>1</sub> | Q <sub>2</sub> | Q <sub>3</sub> |
| H               | H               | L              | L              | L              | L              |
| L               | H               |                |                |                | Count          |
| H               | L               |                |                |                | Count          |
| L               | L               |                |                |                | Count          |

TRUTH TABLE

| COUNT | OUTPUT         |                |                |                |
|-------|----------------|----------------|----------------|----------------|
|       | Q <sub>0</sub> | Q <sub>1</sub> | Q <sub>2</sub> | Q <sub>3</sub> |
| 0     | L              | L              | L              | L              |
| 1     | H              | L              | L              | L              |
| 2     | L              | H              | L              | L              |
| 3     | H              | H              | L              | L              |
| 4     | L              | L              | H              | L              |
| 5     | H              | L              | H              | L              |
| 6     | L              | H              | H              | L              |
| 7     | H              | H              | H              | L              |
| 8     | L              | L              | L              | H              |
| 9     | H              | L              | L              | H              |
| 10    | L              | H              | L              | H              |
| 11    | H              | H              | L              | H              |
| 12    | L              | L              | H              | H              |
| 13    | H              | L              | H              | H              |
| 14    | L              | H              | H              | H              |
| 15    | H              | H              | H              | H              |

Note: Output Q<sub>0</sub> connected to input CP<sub>1</sub>.

GUARANTEED OPERATING RANGES

| Symbol          | Parameter                           |          | Min         | Typ        | Max         | Unit |
|-----------------|-------------------------------------|----------|-------------|------------|-------------|------|
| V <sub>CC</sub> | Supply Voltage                      | 54<br>74 | 4.5<br>4.75 | 5.0<br>5.0 | 5.5<br>5.25 | V    |
| T <sub>A</sub>  | Operating Ambient Temperature Range | 54<br>74 | -55<br>0    | 25<br>25   | 125<br>70   | °C   |
| I <sub>OH</sub> | Output Current — High               | 54, 74   |             |            | -0.4        | mA   |
| I <sub>OL</sub> | Output Current — Low                | 54<br>74 |             |            | 4.0<br>8.0  | mA   |

# SN74LS290

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

| Symbol          | Parameter  |        | Limits |       |      | Unit | Test Conditions   |
|-----------------|--|--------|--------|-------|------|------|---|
|                 |  |        | Min    | Typ   | Max  |      |   |
| V <sub>IH</sub> | Input HIGH Voltage   |        | 2.0    |       |      | V    | Guaranteed Input HIGH Voltage for All Inputs  |
| V <sub>IL</sub> | Input LOW Voltage  | 54     |        |       | 0.7  | V    | Guaranteed Input LOW Voltage for All Inputs   |
|                 |  | 74     |        |       | 0.8  |      |   |
| V <sub>IK</sub> | Input Clamp Diode Voltage  |        |        | -0.65 | -1.5 | V    | V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA   |
| V <sub>OH</sub> | Output HIGH Voltage  | 54     | 2.5    | 3.5   |      | V    | V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table                      |
|                 |  | 74     | 2.7    | 3.5   |      | V    |   |
| V <sub>OL</sub> | Output LOW Voltage   | 54, 74 |        | 0.25  | 0.4  | V    | I <sub>OL</sub> = 4.0 mA<br>V <sub>CC</sub> = V <sub>CC</sub> MIN, V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> per Truth Table |
|                 |  | 74     |        | 0.35  | 0.5  | V    |   |
| I <sub>IH</sub> | Input HIGH Current   |        |        |       | 20   | μA   | V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V  |
|                 |  |        |        |       | 0.1  | mA   | V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V  |
| I <sub>IL</sub> | Input LOW Current<br>MS, MR<br>CP <sub>0</sub><br>CP <sub>1</sub> (LS290)<br>CP <sub>1</sub> (LS293) |        |        |       | -0.4 | mA   | V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V  |
|                 |  |        |        |       | -2.4 |      |   |
|                 |  |        |        |       | -3.2 |      |   |
|                 |  |        |        |       | -1.6 |      |   |
| I <sub>OS</sub> | Short Circuit Current (Note 1)   |        | -20    |       | -100 | mA   | V <sub>CC</sub> = MAX   |
| I <sub>CC</sub> | Power Supply Current   |        |        |       | 15   | mA   | V <sub>CC</sub> = MAX   |

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

# SN74LS290

## AC CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ , $V_{CC} = 5.0\text{ V}$ , $C_L = 15\text{ pF}$ )

| Symbol                               | Parameter  | Limits |          |          |       |          |          | Unit |
|--------------------------------------|--|--------|----------|----------|-------|----------|----------|------|
|                                      |  | LS290  |          |          | LS293 |          |          |      |
|                                      |  | Min    | Typ      | Max      | Min   | Typ      | Max      |      |
| $f_{\text{MAX}}$                     | $\overline{\text{CP}}_0$ Input Clock Frequency                       | 32     |          |          | 32    |          |          | MHz  |
| $f_{\text{MAX}}$                     | $\overline{\text{CP}}_1$ Input Clock Frequency                       | 16     |          |          | 16    |          |          | MHz  |
| $t_{\text{PLH}}$<br>$t_{\text{PHL}}$ | Propagation Delay,<br>$\overline{\text{CP}}_0$ Input to $Q_0$ Output |        | 10<br>12 | 16<br>18 |       | 10<br>12 | 16<br>18 | ns   |
| $t_{\text{PLH}}$<br>$t_{\text{PHL}}$ | $\overline{\text{CP}}_0$ Input to $Q_3$ Output                       |        | 32<br>34 | 48<br>50 |       | 46<br>46 | 70<br>70 | ns   |
| $t_{\text{PLH}}$<br>$t_{\text{PHL}}$ | $\overline{\text{CP}}_1$ Input to $Q_1$ Output                       |        | 10<br>14 | 16<br>21 |       | 10<br>14 | 16<br>21 | ns   |
| $t_{\text{PLH}}$<br>$t_{\text{PHL}}$ | $\overline{\text{CP}}_1$ Input to $Q_2$ Output                       |        | 21<br>23 | 32<br>35 |       | 21<br>23 | 32<br>35 | ns   |
| $t_{\text{PLH}}$<br>$t_{\text{PHL}}$ | $\overline{\text{CP}}_1$ Input to $Q_3$ Output                       |        | 21<br>23 | 32<br>35 |       | 34<br>34 | 51<br>51 | ns   |
| $t_{\text{PHL}}$                     | MS Input to $Q_0$ and $Q_3$ Outputs                                  |        | 20       | 30       |       |          |          | ns   |
| $t_{\text{PHL}}$                     | MS Input to $Q_1$ and $Q_2$ Outputs                                  |        | 26       | 40       |       |          |          | ns   |
| $t_{\text{PHL}}$                     | MR Input to Any Output   |        | 26       | 40       |       | 26       | 40       | ns   |

## AC SETUP REQUIREMENTS ( $T_A = 25^\circ\text{C}$ , $V_{CC} = 5.0\text{ V}$ )

| Symbol           | Parameter                                  | Limits |     |       |     | Unit |
|------------------|--|--------|-----|-------|-----|------|
|                  |  | LS290  |     | LS293 |     |      |
|                  |  | Min    | Max | Min   | Max |      |
| $t_W$            | $\overline{\text{CP}}_0$ Pulse Width       | 15     |     | 15    |     | ns   |
| $t_W$            | $\overline{\text{CP}}_1$ Pulse Width       | 30     |     | 30    |     | ns   |
| $t_W$            | MS Pulse Width                             | 15     |     |       |     | ns   |
| $t_W$            | MR Pulse Width                             | 15     |     | 15    |     | ns   |
| $t_{\text{rec}}$ | Recovery Time MR to $\overline{\text{CP}}$ | 25     |     | 25    |     | ns   |

RECOVERY TIME ( $t_{\text{rec}}$ ) is defined as the minimum time required between the end of the reset pulse and the clock transition from HIGH-to-LOW in order to recognize and transfer HIGH data to the Q outputs.

## AC WAVEFORMS

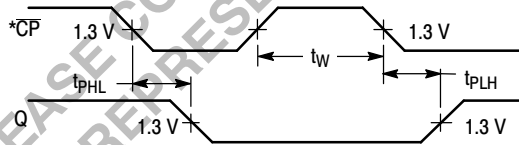


Figure 1

\*The number of Clock Pulses required between the  $t_{\text{PHL}}$  and  $t_{\text{PLH}}$  measurements can be determined from the appropriate Truth Tables.

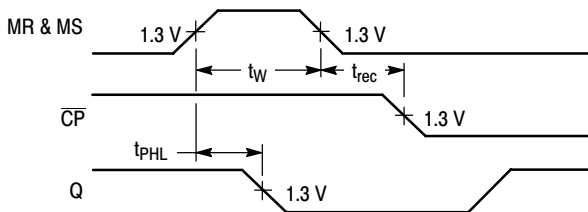


Figure 2

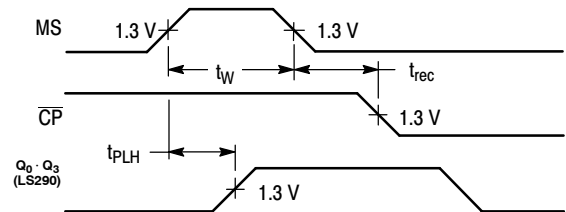



Figure 3

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