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Simplifying System Integration™

# **73S8009CN**

## **Demo Board User Manual**

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**UM\_8009C\_060**

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Teridian Semiconductor Corp., 6440 Oak Canyon, Suite 100, Irvine, CA 92618  
TEL (714) 508-8800, FAX (714) 508-8877, <http://www.teridian.com>

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## 1 Introduction

The Teridian Semiconductor Corporation 73S8009CN Demo Board is a platform for evaluating the Teridian 73S8009CN 32-pin QFN Smart Card Interface IC. It incorporates the 73S8009CN integrated circuit, and it is designed to operate either as a standalone platform (to be used in conjunction with an external microcontroller) or as a daughter card to be used in conjunction with the 73S12xxF evaluation platform. The 73S8009CN Demo Board supports the ability to connect the C4/C8 pins of a smart card/SIM to the USB D+/D- interface.

### 1.1 Package Contents

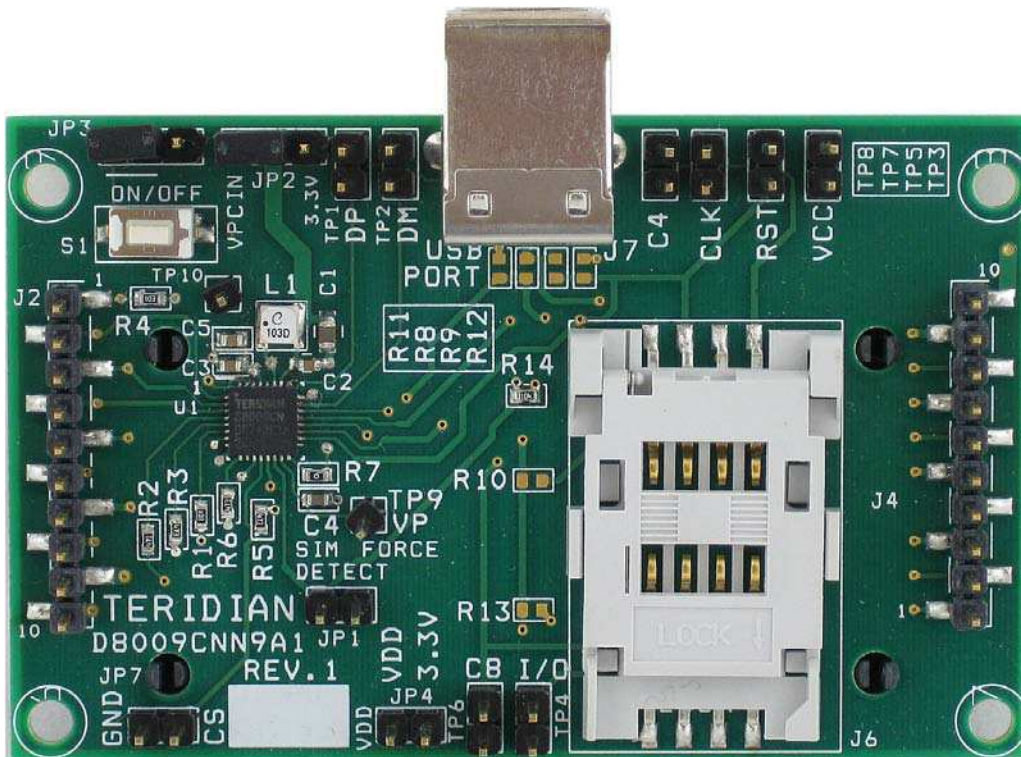


Figure 1: 73S8009CN Demo Board

The 73S8009CN Demo Board Kit includes:

- A 73S9008C Demo Board (Rev. 1)
- The following documents:
  - *73S8009CN Data Sheet*
  - *73S8009CN Demo Board User Manual* (this document)

### 1.2 Safety and ESD Notes

Connecting live voltages to the 73S8009CN Demo Board system will result in potentially hazardous voltages on the boards.



**Extreme caution should be taken when handling the 73S8009CN Demo Board after connection to live voltages!**



**The 73S8009CN Demo Board is ESD sensitive! ESD precautions should be taken when handling this board!**

### 1.3 Recommended Operating Conditions and Absolute Maximum Ratings

**Table 1: Recommended Operating Conditions**

Parameter	Rating
Supply Voltage $V_{PC}$	2.7 to 6.5 VDC
Ambient Operating Temperature	-40 °C to +85 °C

**Table 2: Absolute Maximum Ratings**

Parameter	Rating
Supply Voltage $V_{PC}$	-0.5 to 6.6 VDC
Input Voltage for Digital Inputs	-0.3 to ( $V_{DD}+0.5$ ) VDC
Storage Temperature	-60 to 150 °C
Pin Voltage (except card interface)	-0.3 to ( $V_{DD}+0.5$ ) VDC
Pin Voltage (card interface)	-0.3 to ( $V_{CC}+0.3$ ) VDC
Pin Voltage, LIN pin	0.3 to 6.5 VDC
ESD Tolerance – Card interface pins	± 6 kV
ESD Tolerance – Other pins	± 2 kV
Pin Current	± 200 mA

Operation outside these rating limits may cause permanent damage to the device.

ESD testing on Card pins is HBM condition, 3 pulses, each polarity referenced to ground.

### 1.4 Notes When Using a 73S12xxF Evaluation Board

The 73S12xxF Evaluation Board has two power supplies; 3.3 V and 5.0 V. Normally, the 5.0 V supply is tied to VPC IN on the 73S8009CN board. The 73S8009CN can supply the 3.3 V to the remainder of the system by configuring the jumpers accordingly. The 73S8009CN VDD output can be disconnected from the rest of the evaluation board if desired and the 3.3 V supply on the 73S12xxF Evaluation Board can be used. See the jumper descriptions for more details.

## 2 Connections

This section describes the 73S8009CN Demo Board external connectors. All the digital signals and power supply connections are made through 10-pin header connectors labeled J2 and J4 in Figure 2.

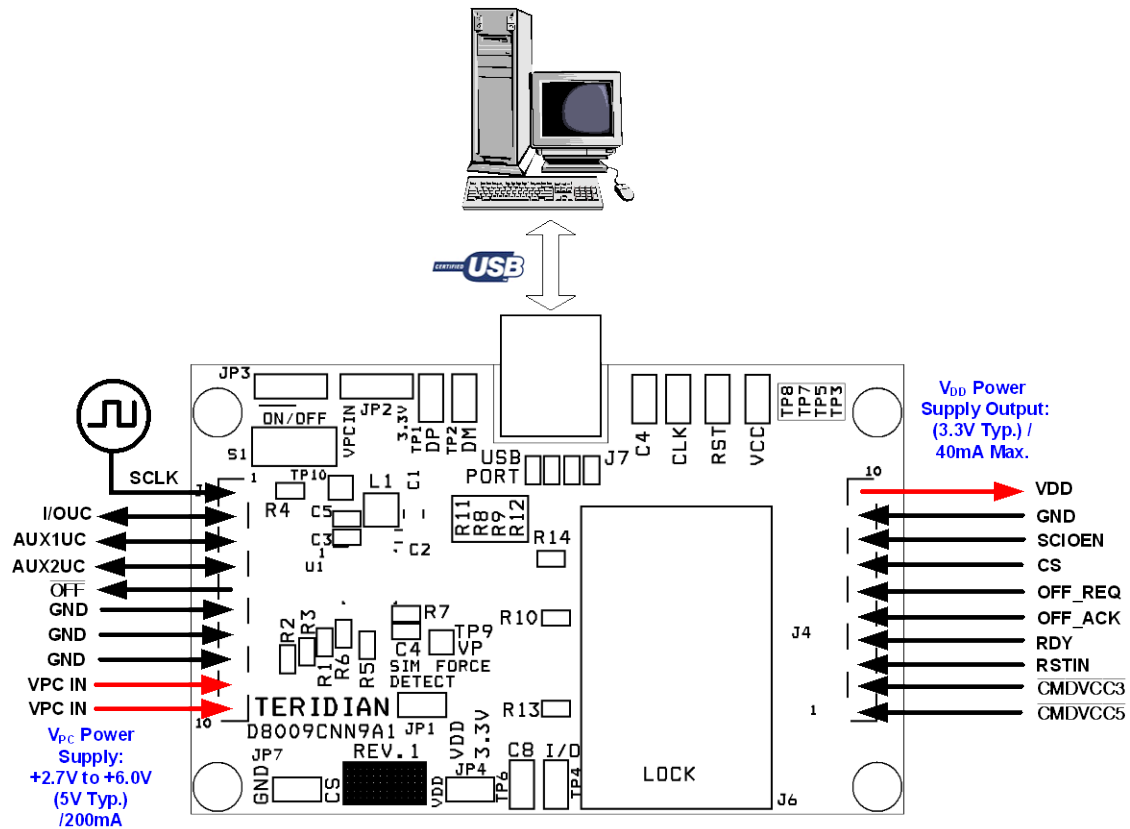


Figure 2: 73S8009CN Demo Board External Connectors

Table 3 describes the pins for the J4 connector. Reset is on pin 3. There are two power pins on pins 1 and 2 and one ground pin on pin 9.

Table 3: J4 Pin Descriptions

Pin	Pin Name	Function
1	CMDVCC5	Controls the turn-on, output voltage value, and turn-off of $V_{CC}$ .
2	CMDVCC3	
3	RSTIN	Controls the card reset signal.
4	RDY	Indicates when smart card power supply is stable and ready.
5	OFF_ACK	Setting OFF_ACK high powers "off" all analog functions and disconnects the 73S8009CN from $V_{PC}$ .
6	OFF_REQ	Digital output. Request to the host system controller to turn the 73S8009CN off.
7	CS	Chip Select – active high.
8	SCIOEN	Smart card to enable. When set high, C4/C8 signals are routed to AUX1UC and AUX2UC respectively. When set low, C4/C8 are routed to DP and DM respectively. AUX1UC and AUX2UC are tri-stated.
9	GND	Ground.
10	VDD	System interface supply voltage and supply voltage for companion controller circuitry.

Table 4 describes the J2 connector pins.

**Table 4: J2 Pin Descriptions**

Pin	Name	Function
1	SCLK	Clock source input.
2	I/OUC	System controller data I/O to/from the card.
3	AUX1UC	System controller auxiliary data C4 to/from the card when SCIOEN is high.
4	AUX2UC	System controller auxiliary data C8 to/from the card when SCIOEN is high.
5	$\overline{\text{OFF}}$	Interrupt signal to the processor. Indicator of card presence and any card fault conditions.
6	GND	Ground.
7	GND	Ground.
8	GND	Ground.
9	VPC IN	Must be between 2.7 V and 6.5 V.
10	VPC IN	Must be between 2.7 V and 6.5 V.

Connections should be made in this order:

- Power Supplies: Apply 3.3 V to pin 10 of J4 or 5 V to pin 10 of J2 depending on the setting of JP2.
- Press the ON/OFF button.
- Control signals to the device can be connected through J2 and J4. See Figure 2 and Figure 4.
- Apply the clock signal.





**Table 5: 73S8009CN Demo Board Description**

Item # (Figure 3)	Electrical Schematic & PCB Silkprint Reference	Name	Use
1	S1	ON/OFF switch	Push-button switch to turn on/off the 73S8009CN. Note: OFF_ACK must be set high to turn off.
2	JP3	ON_OFF Jumper	When set to 1-2, the ON_OFF input is set to ground which turns on the 73S8009CN when power is applied. When set to 2-3, the push button switch is connected to the ON_OFF pin.
3	JP2	VPC Select	The VPC input can select between the VPC_IN and the 3.3 V inputs. When selecting the VPC_IN, the VDD output can source the 3.3 V supply on the evaluation board. See the description for JP4.
4	TP1	Test Points: DP Test point	USB DP
5	TP2	DM Test point	USB DM
7	TP8	C4	
8	TP7	CLK	
9	TP5	RST	Two-pin test points for each respective smart card signal. The pin label name is the respective signal (i.e. VCC, CLK) and the other pin is GND.
10	TP3	VCC	
13	TP4	I/O	
14	TP6	C8	
6	J7	USB Connector	USB Connector for USB enabled smart cards.
11	J4	Board 3.3 V supply and digital control signals	Connector that either gathers or supplies the 3.3 V supply. It includes the 73S8009CN host control signal pins RDY, CS, OFF_REQ, OFF_ACK, CMDVCC5, CMDVCC3, SCIOEN and RSTIN.
12	J6	Smart Card Connector	SIM/SAM smart card format connector. Note that J6 is wired in parallel to the smart card connector J5 (underneath the PCB). J5 and J6 are never to be used at the same time.
15	JP4	VDD Select	When the jumper is inserted, the 73S8009CN VDD output is connected to the 3.3 V power plane. When using in conjunction with a 73S12xxF Evaluation Board or other host, it supplies the 3.3 V source on the platform if it is so configured. Caution must be taken as damage could occur if the 73S12xxF Evaluation Board or host is sourcing 3.3 V with this jumper inserted. Removal of the jumper provides proper isolation with any host platform.
16	J5	Smart Card Connector	Smart card connector. When inserting a card (credit card size format), contacts must face up.
17	JP7	CS Disable	CS Disable Jumper. Insertion of jumper disables the 73S8009CN. The state of the CMDVCC3, CMDVCC5 and RSTIN inputs are latched and the I/OUC, AUX1UC and AUX2UC are tri-stated. The OFF and RDY outputs are also tri-stated.

Item # (Figure 3)	Electrical Schematic & PCB Silkprint Reference	Name	Use
18	JP1	SIM Force Detect	The SIM card connector does not contain a detection switch so the jumper must be installed when using a SIM card. This allows the PRES input to be overridden so VCC can be turned on.
19	TP9	Vp Test Point	Test point to monitor the internal intermediate voltage regulator. This regulator output takes the VPC voltage and steps it up to more than 5 V (if necessary) as the input source for the VCC and VDD output regulators.
20	J3	Board VPC_IN supply, smart card data signals and $\overline{\text{OFF}}$	Connector that supplies the VPC input supply voltage, the smart card data interface signals and the $\overline{\text{OFF}}$ interrupt output.
21	TP10	ON/OFF Test Point	Test point to monitor the ON/OFF input pin.

## 4 Design Considerations

### 4.1 General Layout Rules

Follow these layout rules:

- Route I/O and auxiliary signals away from card interface signals.
- Keep CLK trace as short as possible and with minimal bends in the trace. Keep route of the CLK trace to one layer (avoid vias to other layers). Keep CLK trace away from other traces especially RST, I/O and VCC. Filtering of the CLK trace is allowed for noise purpose. Up to 30 pF to ground is allowed at the CLK pin of the smart card connector. Also, the zero ohm series resistor, R7, can be replaced with a small resistor for additional filtering (no more than 100  $\Omega$ ).
- Keep VCC trace as short as possible. Make trace a minimum of 0.5 mm thick. Also, keep VCC away from other traces especially RST and CLK.
- Keep RST trace away from VCC and CLK traces. Up to 30 pF to ground is allowed for filtering.
- Keep 0.1  $\mu$ F close to VDD pin of the device and directly take other end to ground.
- Keep 0.1  $\mu$ F and 10  $\mu$ F close to VPC pin of the device and directly take other end to ground.
- Keep 4.7  $\mu$ F close to VP pin of the device and directly take other end to ground.
- Keep 0.47  $\mu$ F close to VCC pin of the smart card connector and directly take other end to ground.
- The AUX1, AUX2, DP and DM signals should be isolated as much as possible as they can be used as fast data signaling for USB operation. The DP and DM signals should be routed in parallel as much as possible.

### 4.2 Optimization for Compliance with EMV

Default configuration of the Demo Board contains a 27 pF capacitor (C12) from the CLK pin of the smart connector to ground and a 27 pF capacitor (C13) from the RST pin of the smart connector to ground. These capacitors serve as filters for CLK and RST signals in the case of long traces or test equipment perturbations. The capacitor on CLK reduces ringing on the trace, reduces coupling to other traces and slows down the edge of the CLK signal. The capacitor on RST helps the perturbation specification in a noisy environment. The filter capacitors can be useful in the EMV test environment and have no effect on NDS testing

C9 and C12 are represented on both schematic and BOM. These capacitors are optional filter capacitors on the smart card lines CLK and RST, respectively for each card interface. These capacitors may be adjusted (value, not to exceed 30 pF) or removed to optimize performance in each specific application (PCB, card clock frequency, compliance with applicable standards etc).

### 4.3 Power Supply Configurations

#### 4.3.1 Single Supply Input Power

The single supply configuration should only connect the input power supply to VPC (2.7 V to 6.0 V).

#### 4.3.2 Output Supply Power

The VDD output can be used to power other 3.3 V circuits (40 mA max).

#### 4.4 ON/OFF Switch Operation

The ON/OFF switch uses a pushbutton to toggle between turning the 73S8009CN on and off. The switch input contains a debounce circuit for protection. The 73S8009CN defaults to the OFF state when the power source is applied. When the 8009C is in the OFF state, a switch closure turns on the 73S8009CN. When the 73S8009CN is ON, a switch closure does not turn off the 73S8009CN by itself, but it activates the OFF\_REQ signal by setting it high. The 73S8009CN does not shut off until the OFF\_ACK is set high. The purpose of this sequence is to allow the host processor to perform any necessary shut down tasks before losing power. When the host is finished, it can set the OFF\_ACK signal high to shut off the 73S8009CN. If there is no need for the host to perform any shutdown tasks, the OFF\_ACK pin can be left open and it follows the state of the OFF\_REQ output by means of an internal resistor connection between the OFF\_REQ and OFF\_ACK pins.

# 5 73S8009CN Demo Board Schematics, PCB Layouts and Bill of Materials

## 5.1 Schematics

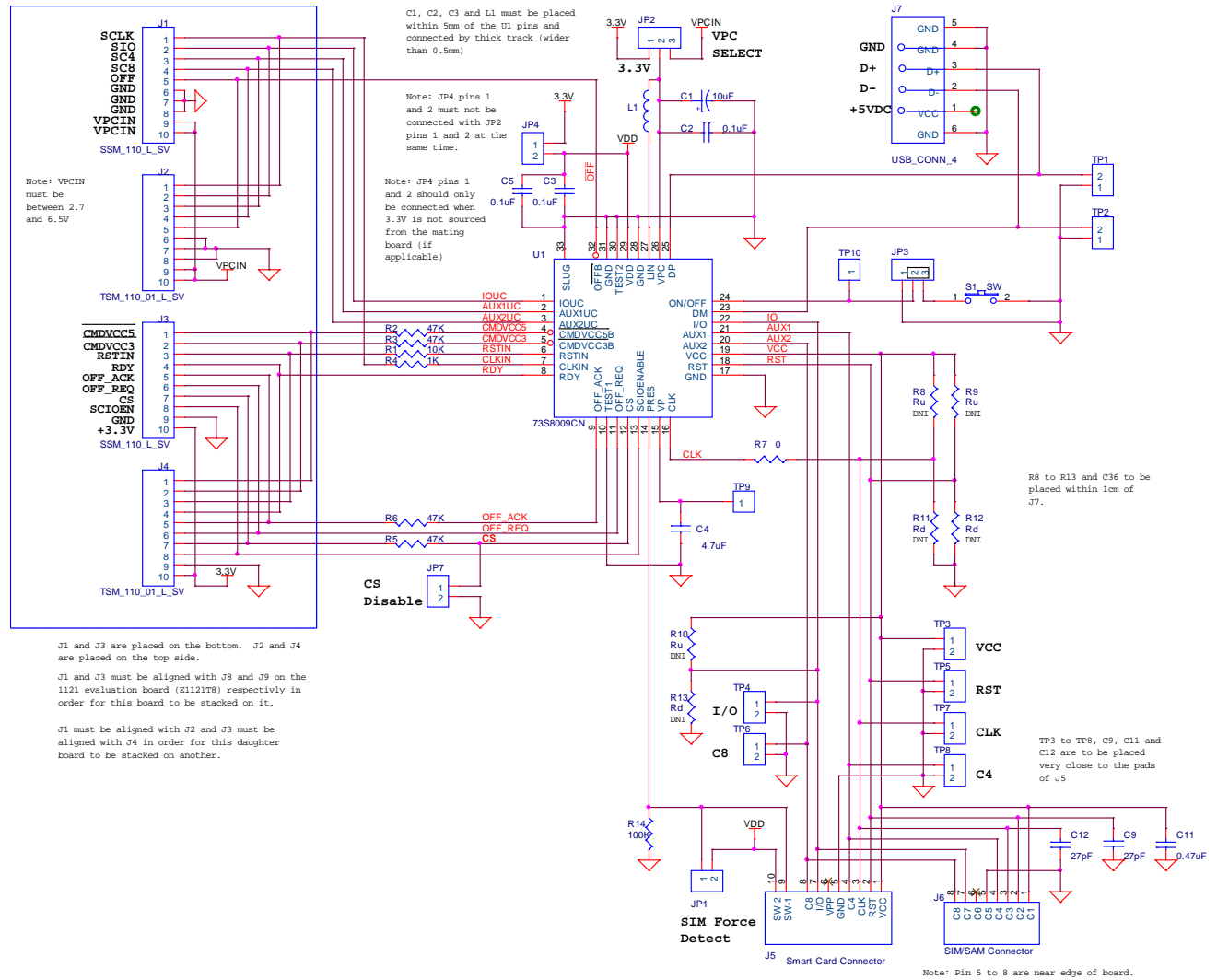


Figure 4: 73S8009CN Electrical Schematic

### 5.2 73S8009CN PCB Layouts

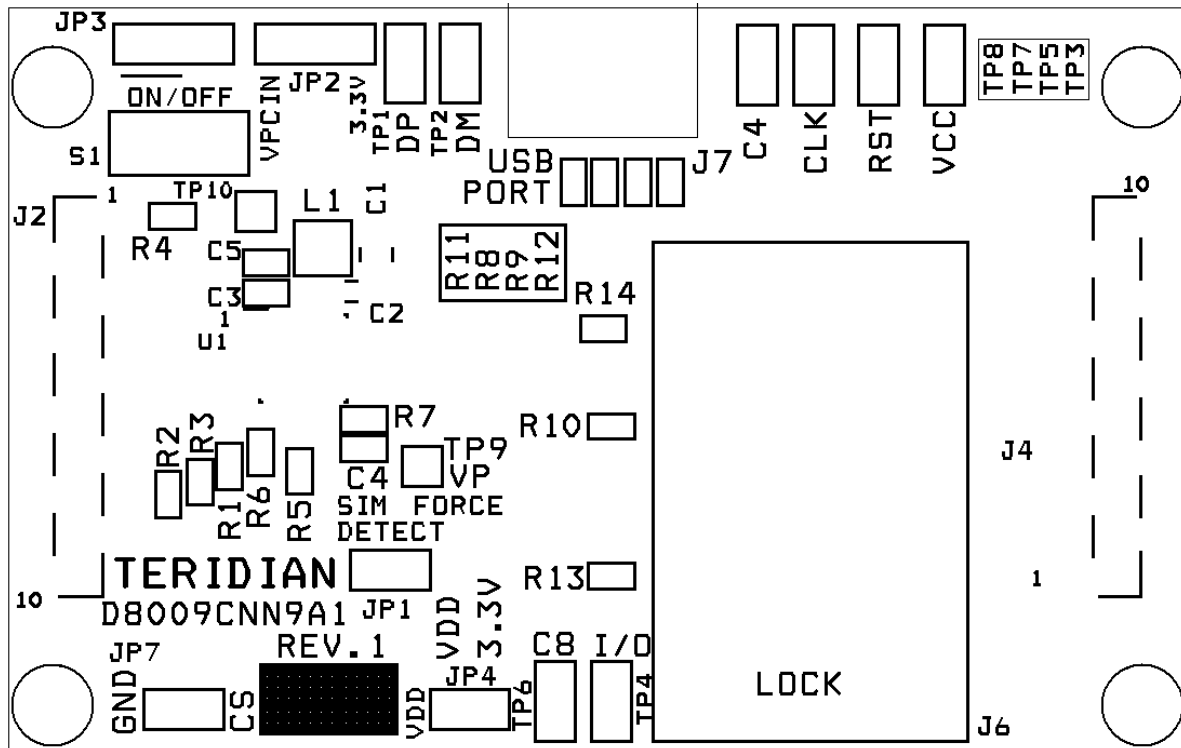


Figure 5: 73S8009CN Demo Board: Top View

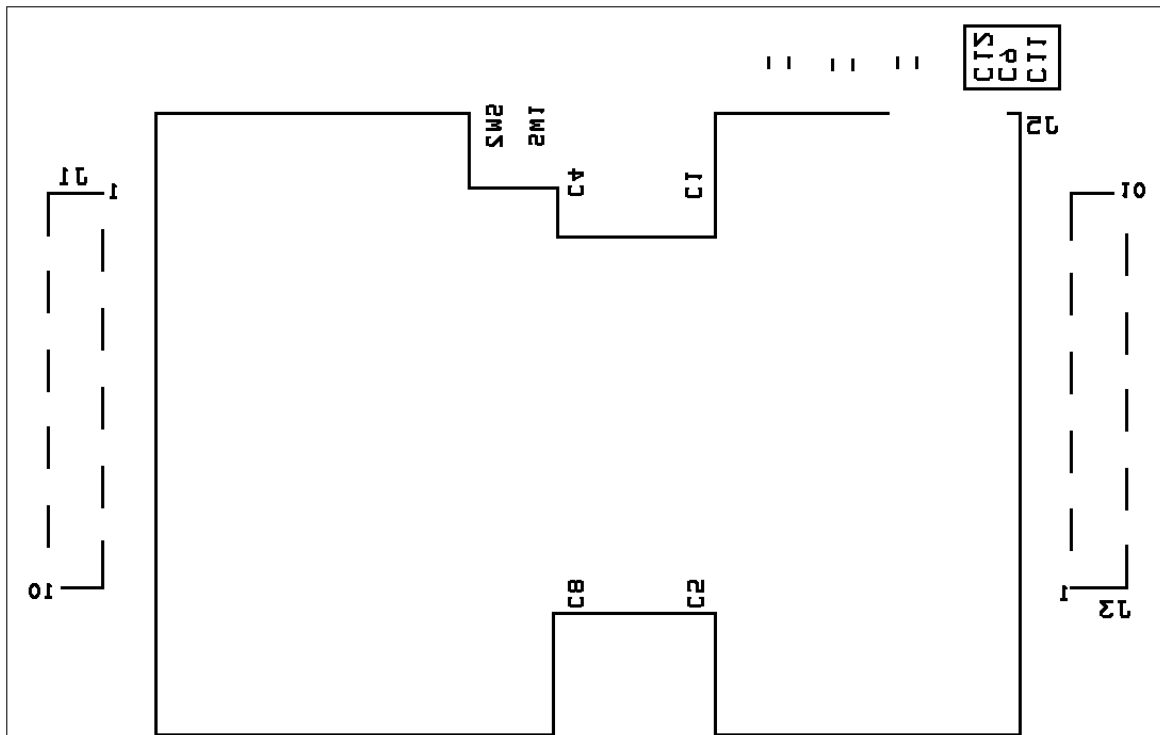


Figure 6: 73S8009CN Demo Board: Bottom View

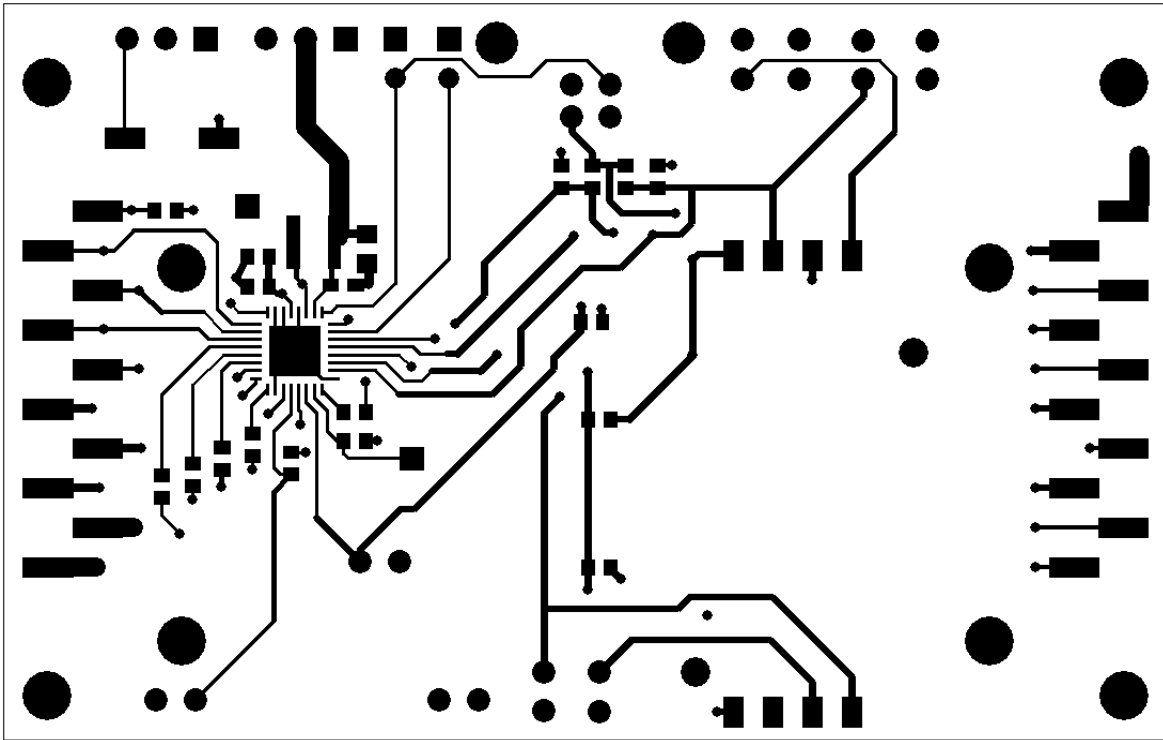


Figure 7: 73S8009CN Demo Board: Top Signal Layer

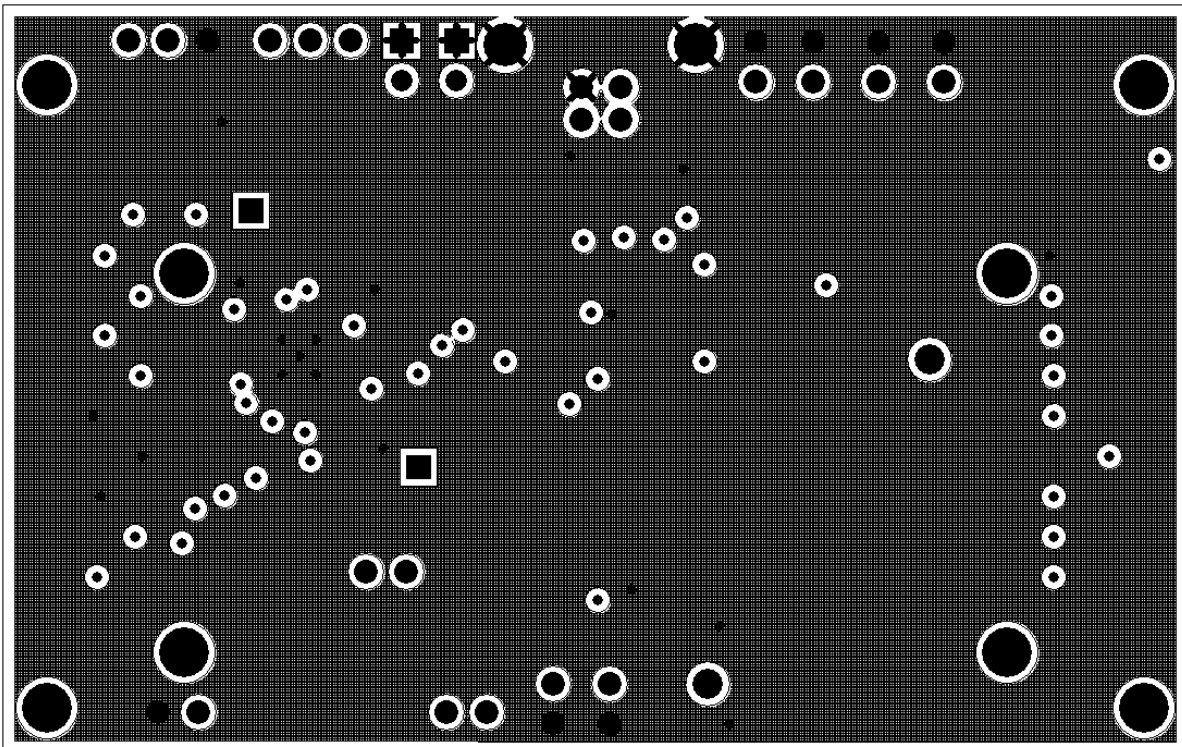


Figure 8: 73S8009CN Demo Board: Middle Layer 1, Ground Plane



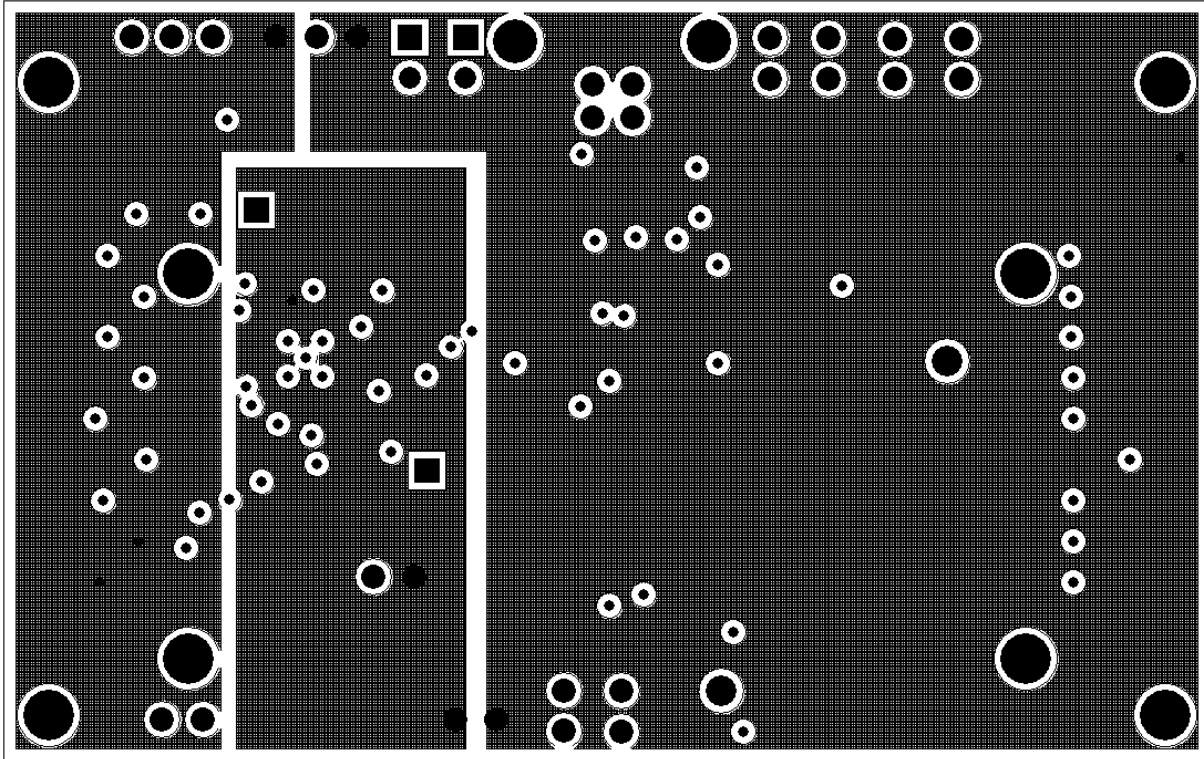


Figure 9: 73S8009CN Demo Board: Middle Layer 2, Supply Plane

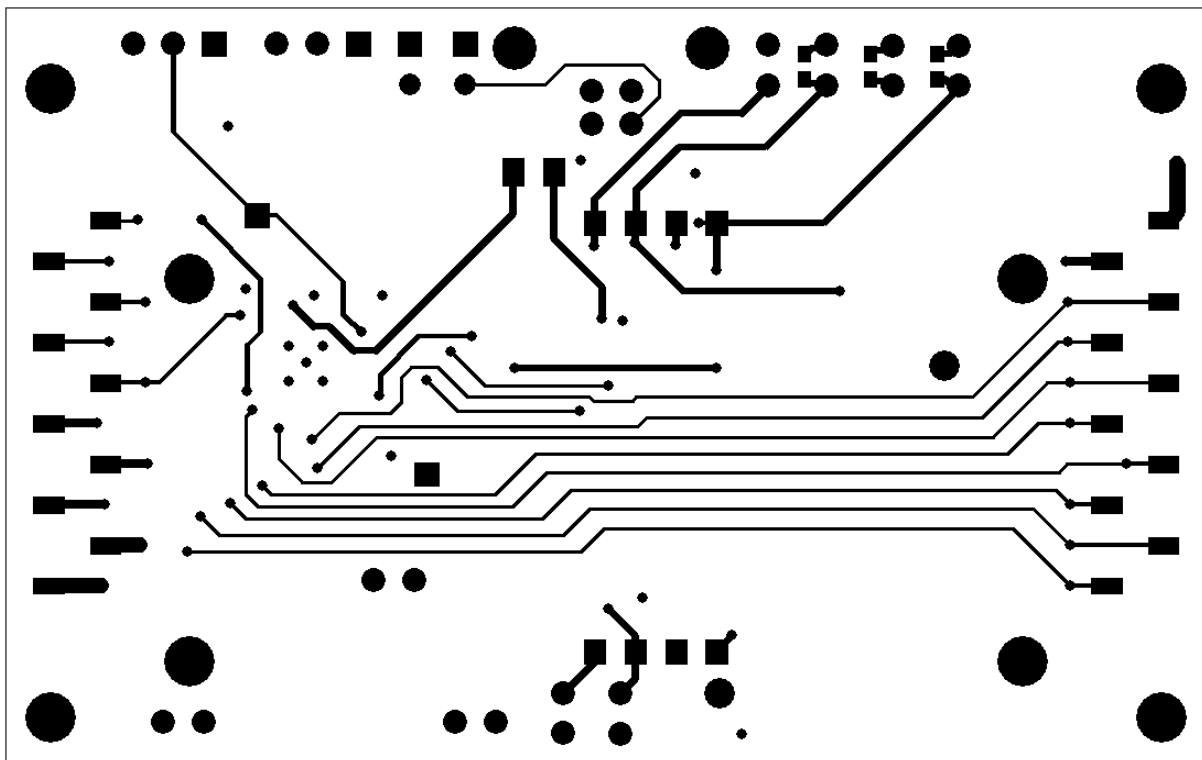


Figure 10: 73S8009CN Demo Board: Bottom Signal Layer

### 5.3 73S8009CN Demo Board Bill of Materials

**Table 6: 73S8009CN Demo Board Bill of Materials**

Qnt	Reference	Part	Digikey Part Number	Part Number	Manufacturer
1	C1	10 $\mu$ F	PCC2225CT-ND	ECJ-2FB0J106M	Panasonic
3	C2, C3, C5	0.1 $\mu$ F	PCC1762CT-ND	ECJ-1VB1C104K	Panasonic
1	C4	4.7 $\mu$ F	PCC2396CT-ND	ECJ-1VB0J475K	Panasonic
2	C9, C12	27 pF	PCC270ACVCT-ND	ECJ-1VC1H270J	Panasonic
1	C11	0.47 $\mu$ F	PCC2275CT-ND	ECJ-1VB0J475K	Panasonic
2	JP2, JP3	Header 3	S1011E-36-ND	PBC36SAAN	Sullins
2	JP1, JP4, JP7	Header 2	S1011E-36-ND	PBC36SAAN	Sullins
2	J1, J3	SSM_110_L_SV	X	SSM_110_L_SV	Samtec
2	J2, J4	TSM_110_01_L_SV	X	TSM_110_01_L_SV	Samtec
1	J5	Smart Card Connector	401-1715-ND	CCM02-2504LFT	ITTCannon
1	J6	SIM/SAM Connector	609-1403-1-ND	7112S0825X01LF	FCI
1	J7	USB Connector	ED90064-ND	897-43-004-90-000000	Mill-Max
1	L1	Inductor	X	LP 03010-103MLB	Coilcraft
1	R1	1 K	P1.0KGCT-ND	ERJ-3GEYJ102V	Panasonic
4	R2, R3, R5, R6	47 K	P47KGCT-ND	ERJ-3GEYJ473V	Panasonic
1	R4	10 K	P10KGCT-ND	ERJ-3GEYJ103V	Panasonic
2	R7	0	P0.0GCT-ND	ERJ-3GEY0R00V	Panasonic
1	R14	100 K	P100KGCT-ND	ERJ-3GEYJ104V	Panasonic
1	S1	Switch	P8051SCT	EVQ-PJX05M	Panasonic
2	TP9, TP10	TP1	S1011E-36-ND	PBC36SAAN	Sullins
8	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8	TP2	S1011E-36-ND	PBC36SAAN	Sullins
1	U1	73S8009CN	X	73S8009CN	Teridian

Note: The resistors noted Ru and Rd in the schematic are not populated on the board. They can be implemented to adjust the features of the smart card reader.

## 6 Ordering Information

Table 7 lists the order number used to identify the 73S8009CN Demo Board.

**Table 7: 73S8009CN Demo Board Order Number**

Part Description	Order Number
73S8009CN 32-Pin QFN Demo Board	73S8009CN-DB

## 7 Related Documentation

The following 73S8009CN documents are available from Teridian Semiconductor Corporation:

*73S8009CN Data Sheet*

*73S8009CN Demo Board User Manual*

## 8 Contact Information

For more information about Teridian Semiconductor products or to check the availability of the 73S8009CN, contact us at:

6440 Oak Canyon Road  
Suite 100  
Irvine, CA 92618-5201

Telephone: (714) 508-8800  
FAX: (714) 508-8878  
Email: [scr.support@teridian.com](mailto:scr.support@teridian.com)

For a complete list of worldwide sales offices, go to <http://www.teridian.com>.

## Revision History

Revision	Date	Description
1.0	9/11/2007	First publication.
1.1	2/10/2010	Formatted in the new Teridian style. Added Section 1.1, Package Contents. Added Section 1.2, Safety and ESD Notes. Added Table 3: J4 Pin Descriptions. Added Table 4: J2 Pin Descriptions. Added Section 6, Ordering Information. Added Section 7, Related Documentation. Added Section 8, Contact Information. Miscellaneous editorial corrections.