ZARLINK SEMICONDUCTOR

ZL50017
1 K Digital Switch

Data Sheet

October 2004

Features

- 1024 channel x 1024 channel non-blocking digital Time Division Multiplex (TDM) switch at 4.096, 8.192 or 16.384 Mbps
- 16 serial TDM input, 16 serial TDM output streams
- Output streams can be configured as bi-directional for connection to backplanes
- Exceptional input clock cycle to cycle variation tolerance (20 ns for all rates)
- Per-stream input bit delay with flexible sampling point selection
- Per-stream output bit and fractional bit advancement
- Per-channel constant or variable throughput delay for frame integrity and low latency applications
- Per-channel high impedance output control
- Per-channel message mode
- Input clock: 4.096 MHz, 8.192 MHz, 16.384 MHz
- Input frame pulses:61 ns, 122 ns, 244 ns
- Control interface compatible with Intel and Motorola 16-bit non-multiplexed buses

Ordering Information

ZL50017GAC 256-ball PBGA
ZL50017QCC 256-lead LQFP

-40°C to +85°C

- Connection memory block programming
- Supports ST-BUS and GCI-Bus standards for input and output timing
- IEEE-1149.1 (JTAG) test port
- 3.3 V I/O with 5 V tolerant inputs; 1.8 V core voltage

Applications

- PBX and IP-PBX
- Small and medium digital switching platforms
- Remote access servers and concentrators
- Wireless base stations and controllers
- Multi service access platforms
- Digital Loop Carriers
- Computer Telephony Integration

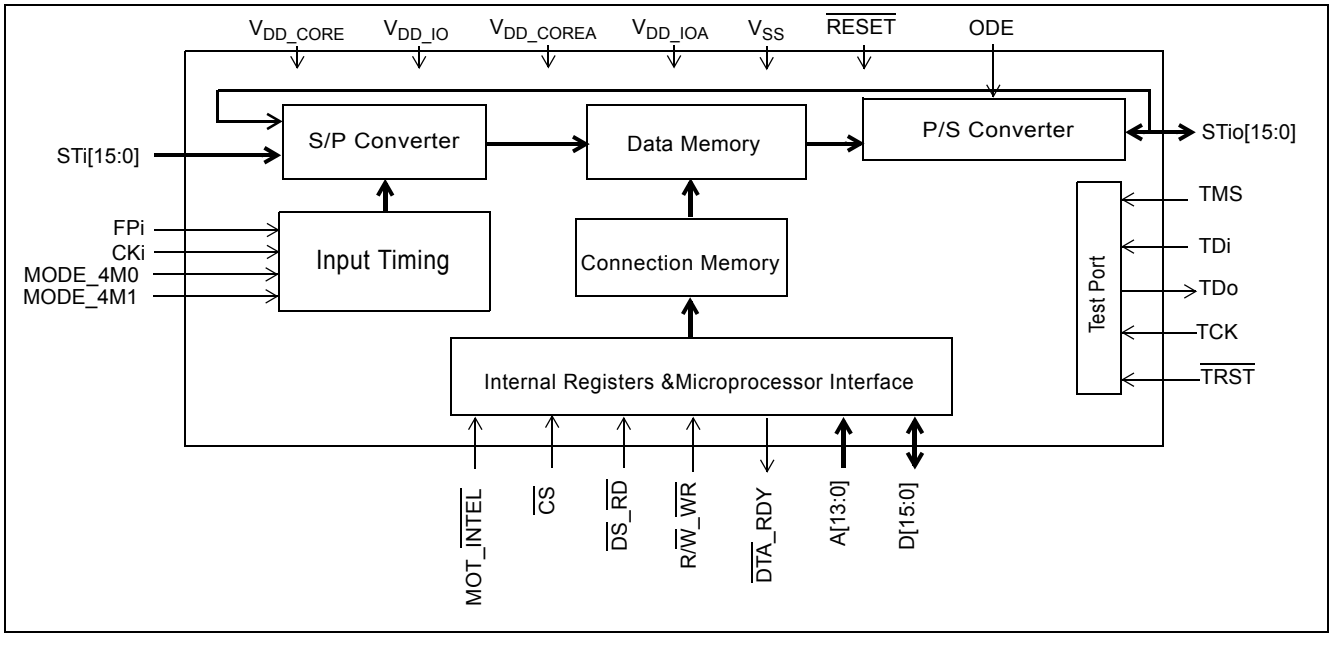

Figure 1 - ZL50017 Functional Block Diagram

Description

The ZL50017 is a maximum 1024 x 1024 channel non-blocking digital Time Division Multiplex (TDM) switch. It has sixteen input streams (STi0 - 15) and sixteen output streams (STio0 - 15). The device can switch 64 kbps and Nx64 kbps TDM channels from any input stream to any output stream. All of the input and output streams operate at the same data rate and can be programmed at any of the following data rates: 2.048 Mbps, 4.096 Mbps, 8.192 Mbps or 16.384 Mbps. The output streams can be configured to operate in bi-directional mode, in which case STi0 - 15 will be ignored.

The device contains two types of internal memory - data memory and connection memory. There are three modes of operation - Connection Mode, Message Mode and high impedance mode. In Connection Mode, the contents of the connection memory define, for each output stream and channel, the source stream and channel (the actual data to be output is stored in the data memory). In Message Mode, the connection memory is used for the storage of microprocessor data. Using Zarlink's Message Mode capability, microprocessor data can be broadcast to the data output streams on a per-channel basis. This feature is useful for transferring control and status information for external circuits or other TDM devices. In high impedance mode the selected output channel can be put into a high impedance state.

The configurable non-multiplexed microprocessor port allows users to program various device operating modes and switching configurations. Users can employ the microprocessor port to perform register read/write, connection memory read/write and data memory read operations. The port is configurable to interface with either Motorola or Intel-type microprocessors.

The device also supports the mandatory requirements of the IEEE-1149.1 (JTAG) standard via the test port.

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8	Figure 3, “ZL50017 256-Lead 28 mm x 28 mm LQFP (top view)	• Re-labeled IC_OPEN to MODE_4M0 Location: Pin 46 • Re-labeled IC_OPEN to MODE_4M1 Location: Pin 48
9	3.0, “Pin Description“	• Added MODE_4M0 & MODE_4M1 descriptions
27	13.0, “Register Address Mapping“	• Added Reg 0010H to list
28	14.0, “Detailed Register Description“	• Changed Bits 6-5 Description - Added MODE 4M0/1 reference

2.0 Pinout Diagrams

2.1 BGA Pinout

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	V_{SS}	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	V_{SS}	A
B	NC	STi10	STi5	STi4	NC	STi0	NC	NC	V_{DD_COREA}	FPi	CKi	IC_Open	IC_Open	IC_GND	ODE	NC	B
C	NC	STi9	V_{SS}	STi7	STi6	STi1	NC	NC	V_{SS}	IC_Open	IC_Open	IC_Open	IC_GND	V_{SS}	STio15	NC	C
D	NC	STi11	V_{DD_IO}	STi3	STi2	NC	NC	NC	NC	V_{SS}	NC	IC_GND	STio13	V_{DD_IO}	STio14	NC	D
E	NC	STi14	STi8	V_{DD_IO}	V_{SS}	V_{DD_CORE}	NC	NC	NC	NC	V_{DD_CORE}	V_{SS}	V_{DD_IO}	STio12	NC	NC	E
F	NC	STi15	STi12	STi13	V_{DD_IO}	V_{DD_CORE}	V_{DD_CORE}	V_{SS}	V_{SS}	V_{DD_CORE}	V_{DD_CORE}	V_{DD_IO}	IC_Open	NC	NC	NC	F
G	NC	$\overline{RESET}$	IC_GND	IC_Open	TDo	V_{DD_IO}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD_IO}	A12	A13	NC	NC	NC	G
H	NC	V_{SS}	V_{SS}	V_{DD_COREA}	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	A7	A9	A10	NC	A11	NC	H
J	NC	V_{DD_IOA}	V_{DD_IOA}	V_{SS}	V_{SS}	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	A3	A4	A5	A8	A6	NC	J
K	NC	V_{SS}	TMS	V_{SS}	V_{DD_COREA}	V_{DD_IO}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD_IO}	IC_Open	A0	A2	A1	NC	K
L	NC	V_{DD_COREA}	$\overline{TRST}$	TCK	V_{DD_IO}	V_{DD_CORE}	V_{DD_CORE}	V_{SS}	V_{SS}	V_{DD_CORE}	V_{DD_CORE}	V_{DD_IO}	STio10	STio11	STio9	NC	L
M	NC	NC	TDi	D0	V_{SS}	V_{DD_CORE}	V_{DD_CORE}	D6	D10	V_{DD_CORE}	V_{DD_CORE}	V_{SS}	$\overline{MOT\_INTEL}$	MODE_4M0	STio8	NC	M
N	NC	NC	V_{DD_IO}	STio0	NC	D1	D5	D7	D11	D13	$R/\overline{W}\_WR$	$\overline{DTA}\_RDY$	STio4	V_{DD_IO}	NC	NC	N
P	NC	NC	V_{SS}	STio1	STio3	NC	D3	D8	D14	NC	STio5	NC	NC	V_{SS}	NC	NC	P
R	NC	NC	NC	STio2	NC	D2	D4	D9	D12	D15	$\overline{CS}$	$\overline{DS}\_\overline{RD}$	MODE_4M1	STio6	STio7	NC	R
T	V_{SS}	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	V_{SS}	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Note: A1 corner identified by metallized marking.
Note: Pinout is shown as viewed through top of package.

Figure 2 - ZL50017 256-Ball 17 mm x 17 mm PBGA (as viewed through top of package)

2.2 QFP Pinout

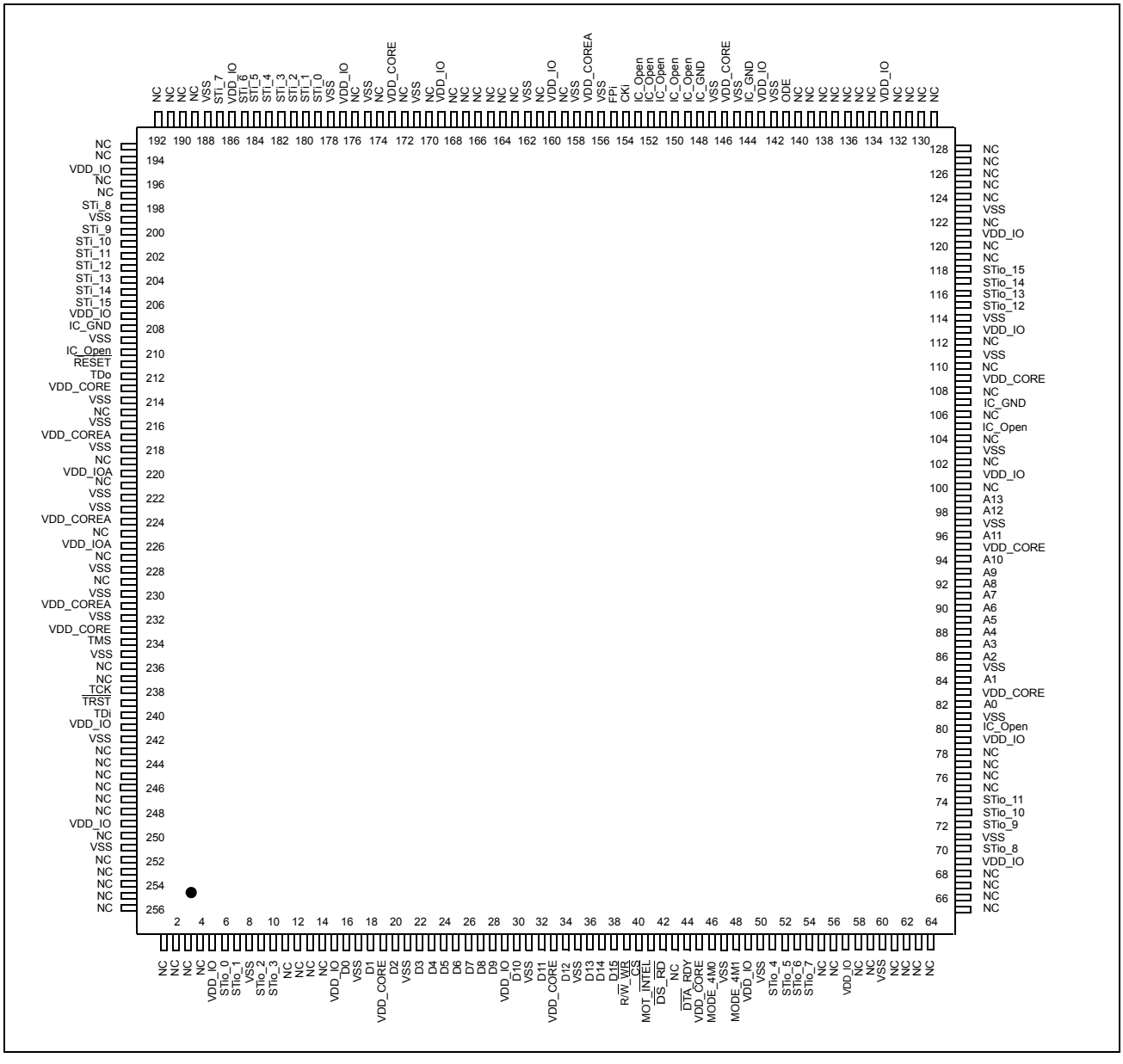


Figure 3 - ZL50017 256-Lead 28 mm x 28 mm LQFP (top view)

3.0 Pin Description

PBGA Pin Number	LQFP Pin Number	Pin Name	Description
E6, E11, F6, F7, F10, F11, L6, L7, L10, L11, M6, M7, M10, M11	19, 33, 45, 83, 95, 109, 146, 173, 213, 233	V_{DD_CORE}	**Power Supply for the core logic:** +1.8 V
H4, K5, B9, L2	217, 231, 157, 224	V_{DD_COREA}	**Power Supply for analog circuitry:** +1.8 V
D3, D14, E4, E13, F5, F12, G6, G11, K6, K11, L5, L12, N3, N14	5, 15, 29, 49, 57, 69, 79, 101, 113, 121, 133, 143, 160, 169, 177, 186, 195, 207, 241, 249	V_{DD_IO}	**Power Supply for I/O:** +3.3 V
J2, J3	220, 226	V_{DD_IOA}	**Power Supply for the CKo5 and CKo3 outputs:** +3.3 V
A1, A16, C3, C9, C14, D10, E5, E12, F8, F9, G7, G8, G9, G10, H2, H3, H6, H7, H8, H9, H10, J4, J5, J7, J8, J9, J10, K2, K4, K7, K8, K9, K10, L8, L9, M5, M12, P3, P14, T1, T16	8, 17, 21, 31, 35, 47, 50, 60, 71, 81, 85, 97, 103, 111, 114, 123, 142, 145, 147, 156, 158, 162, 171, 175, 178, 188, 199, 209, 214, 216, 218, 222, 223, 228, 230, 232, 235, 242, 251	V_{SS}	**Ground**

PBGA Pin Number	LQFP Pin Number	Pin Name	Description
K3	234	TMS	**Test Mode Select (5 V-Tolerant Input with Internal Pull-up)** JTAG signal that controls the state transitions of the TAP controller. This pin is pulled high by an internal pull-up resistor when it is not driven.
L4	238	TCK	**Test Clock (5 V-Tolerant Schmitt-Triggered Input with Internal Pull-up)** Provides the clock to the JTAG test logic.
L3	239	$\overline{\text{TRST}}$	**Test Reset (5 V-Tolerant Input with Internal Pull-up)** Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-Reset state. This pin should be pulsed low during power-up to ensure that the device is in the normal functional mode. When JTAG is not being used, this pin should be pulled low during normal operation.
M3	240	TDi	**Test Serial Data In (5 V-Tolerant Input with Internal Pull-up)** JTAG serial test instructions and data are shifted in on this pin. This pin is pulled high by an internal pull-up resistor when it is not driven.
G5	212	TDo	**Test Serial Data Out (5 V-Tolerant Three-state Output)** JTAG serial data is output on this pin on the falling edge of TCK. This pin is held in high impedance state when JTAG is not enabled.
B12, B13, C10, C11, F13, G4, K12, C12,	80, 105, 150, 151, 152, 153, 210, 149	IC_Open	**Internal Test Mode (5 V-Tolerant Input with Internal Pull-down)** These pins may be left unconnected.
G3, D12, C13, B14	144, 107, 148, 208	IC_GND	**Internal Test Mode Enable (5 V-Tolerant Input)** These pins **MUST** be low.

PBGA Pin Number	LQFP Pin Number	Pin Name	Description
A8, A9, A14, A15, E10, M2, N2, P2, P16, R2, R16, T6, T7, T8, T9, T10, T11, T12, T13, T14, T15, D16, E16, C16, B16, A13, A12, A10, A11, N1, M1, P1, R1, T2, T3, T5, T4, N16, M16, L16, K16, H16, J16, G16, F16,D9, E8, C8, E7, D6, H5, P10, G15, G14, E15, F14, H14, D11, F15, B7, C7, B5, J6, R3, P6, R5, N5, P12, N15, P13, P15, E1, D1, G1, F1, J1, H1, K1, L1, A7, A5, A6, A4, A3, A2, C1, B1, E9, D8, B8, D7	61, 62, 63, 64, 65, 66, 67, 68, 134, 135, 136, 137, 138, 139, 140, 215, 219, 225, 229, 236, 237, 125, 126, 127, 128, 129, 130, 131, 132, 253, 254, 255, 256, 1, 2, 3, 4, 75, 76, 77, 78, 119, 120, 122, 124,159, 163, 165, 167, 176, 221, 43, 102, 106, 110, 112, 100, 104, 108, 170, 172, 174, 227, 11, 12, 13, 14, 55, 56, 58, 59, 243, 244, 245, 246, 247, 248, 250, 252, 189, 190, 191, 192, 193, 194, 196, 197, 161, 164, 166, 168	NC	**No Connect** These pins **MUST** be left unconnected.

<table>
<tr><th>PBGA Pin Number</th><th>LQFP Pin Number</th><th>Pin Name</th><th>Description</th></tr>
<tr><td>M14, R13</td><td>46, 48</td><td>MODE_4M0, MODE_4M1</td><td>4 M Input Clock Mode 0 to 1 (5 V-Tolerant Input with internal pull-down) These two pins should be tied together.
<table><tr><th>MODE _4M1</th><th>MODE _4M0</th><th>Operation</th></tr><tr><td>0</td><td>0</td><td>CKi = 8.192 MHz or 16.384 MHz</td></tr><tr><td>1</td><td>1</td><td>CKi = 4.096 MHz</td></tr><tr><td>0</td><td>1</td><td>Reserved</td></tr><tr><td>1</td><td>0</td><td>Reserved</td></tr></table>See Table 5, “Control Register (CR) Bits” on page 28 for CKi and FPi selection using the CKIN1 - 0 bits.</td></tr>
<tr><td>B10</td><td>155</td><td>FPi</td><td>ST-BUS/GCI-Bus Frame Pulse Input (5 V-Tolerant Schmitt-Triggered Input)
This pin accepts the frame pulse which stays active for 61 ns, 122 ns or 244 ns at the frame boundary. The frame pulse frequency is 8 kHz. The frame pulse associated with the CKi must be applied to this pin. By default, the device accepts a negative frame pulse in ST-BUS format, but it can accept a positive frame pulse instead if the FPINP bit is set high in the Control Register (CR). It can accept a GCI-formatted frame pulse by programming the FPINPOS bit in the Control Register (CR) to high.</td></tr>
<tr><td>B11</td><td>154</td><td>CKi</td><td>ST-BUS/GCI-Bus Clock Input (5 V-Tolerant Schmitt-Triggered Input)
This pin accepts a 4.096 MHz, 8.192 MHz or 16.384 MHz clock. The clock frequency applied to this pin must be twice the highest input or output data rate. The exception is, when data is running at 16.384 Mbps, a 16.384 MHz clock must be used.
By default, the clock falling edge defines the input frame boundary, but the device allows the clock rising edge to define the frame boundary by programming the CKINP bit in the Control Register (CR).</td></tr>
<tr><td>B6, C6, D5, D4, B4, B3, C5, C4, E3, C2, B2, D2, F3, F4, E2, F2</td><td>179, 180, 181, 182, 183, 184, 185, 187, 198, 200, 201, 202, 203, 204, 205, 206</td><td>STi0 - 15</td><td>Serial Input Streams 0 to 15 (5 V-Tolerant Inputs with Internal Pull-downs)
The data rate of all the input streams are programmed through the “Data Rate Selection Register” on page 31. In the 2.048 Mbps mode, these pins accept serial TDM data streams at 2.048 Mbps with 32 channels per frame. In the 4.096 Mbps mode, these pins accept serial TDM data streams at 4.096 Mbps with 64 channels per frame. In the 8.192 Mbps mode, these pins accept serial TDM data streams at 8.192 Mbps with 128 channels per frame. In the 16.384 Mbps mode, these pins accept serial TDM data streams at 16.384 Mbps with 256 channels per frame.</td></tr>
</table>

PBGA Pin Number	LQFP Pin Number	Pin Name	Description
N4, P4, R4, P5, N13, P11, R14, R15, M15, L15, L13, L14, E14, D13, D15, C15	6, 7, 9, 10, 51, 52, 53, 54, 70, 72, 73, 74, 115, 116, 117, 118	STio 0 - 15	**Serial Output Streams 0 to 15 (5 V-Tolerant Slew-Rate-Limited Three-state I/Os with Enabled Internal Pull-downs)** The data rate of all the output streams are programmed through the “Data Rate Selection Register” on page 31. In the 2.048 Mbps mode, these pins output serial TDM data streams at 2.048 Mbps with 32 channels per frame. In the 4.096 Mbps mode, these pins output serial TDM data streams at 4.096 Mbps with 64 channels per frame. In the 8.192 Mbps mode, these pins output serial TDM data streams at 8.192 Mbps with 128 channels per frame. In the 16.384 Mbps mode, these pins output serial TDM data streams at 16.384 Mbps with 256 channels per frame.These output streams can be used as bi-directionals by programming BDH (bit 7) and BDL (bit 6) of Internal Mode Selection (IMS) register.
B15	141	ODE	**Output Drive Enable (5 V-Tolerant Input with Internal Pull-up)** This is the output enable control for STio0 - 15. When it is high, STio0 - 15 are enabled. When it is low, STio0 - 15 are tristated.
M4, N6, R6, P7, R7, N7, M8, N8, P8, R8, M9, N9, R9, N10, P9, R10	16, 18, 20, 22, 23, 24, 25, 26, 27, 28, 30, 32, 34, 36, 37, 38	D0 - 15	**Data Bus 0 to 15 (5 V-Tolerant Slew-Rate-Limited Three-state I/Os)** These pins form the 16-bit data bus of the microprocessor port.
N12	44	$\overline{\text{DTA}}$_RDY	**Data Transfer Acknowledgment_Ready (5 V-Tolerant Three-state Output)** This active low output indicates that a data bus transfer is complete for the Motorola interface. For the Intel interface, it indicates a transfer is completed when this pin goes from low to high. An external pull-up resistor **MUST** hold this pin at HIGH level for the Motorola mode. An external pull-down resistor **MUST** hold this pin at LOW level for the Intel mode.
R11	40	$\overline{\text{CS}}$	**Chip Select (5 V-Tolerant Input)** Active low input used by the Motorola or Intel microprocessor to enable the microprocessor port access.
N11	39	R/$\overline{\text{W}}$_$\overline{\text{WR}}$	**Read/Write_Write (5 V-Tolerant Input)** This input controls the direction of the data bus lines (D0 - 15) during a microprocessor access. For the Motorola interface, this pin is set high and low for the read and write access respectively. For the Intel interface, a write access is indicated when this pin goes low.
R12	42	$\overline{\text{DS}}$_$\overline{\text{RD}}$	**Data Strobe_Read (5 V-Tolerant Input)** This active low input works in conjunction with $\overline{\text{CS}}$ to enable the microprocessor port read and write operations for the Motorola interface. A read access is indicated when it goes low for the Intel interface.

PBGA Pin Number	LQFP Pin Number	Pin Name	Description
K13, K15, K14, J11, J12, J13, J15, H11, J14, H12, H13, H15, G12, G13	82, 84, 86, 87, 88, 89, 90, 91, 92, 93, 94, 96, 98, 99	A0 - 13	**Address 0 to 13 (5 V-Tolerant Inputs)** These pins form the 14-bit address bus to the internal memories and registers.
M13	41	MOT_$\overline{\text{INTEL}}$	**Motorola_Intel (5 V-Tolerant Input with Internal Pull-up)** This pin selects the Motorola or Intel microprocessor interface to be connected to the device. When this pin is unconnected or connected to high, Motorola interface is assumed. When this pin is connected to ground, Intel interface should be used.
G2	211	$\overline{\text{RESET}}$	**Device Reset (5 V-Tolerant Input with Internal Pull-up)** This input (active LOW) puts the device in its reset state that disables the STio0 - 15 drivers. It also preloads registers with default values and clears all internal counters. To ensure proper reset action, the reset pin must be low for longer than 1 μs. Upon releasing the reset signal to the device, the first microprocessor access cannot take place for at least 500 μs due to the time required to stabilize the device from the power-down state. Refer to Section Section 11.2 on page 25 for details.

4.0 Device Overview

The device has sixteen ST-BUS/GCI-Bus inputs (STi0 - 15) and sixteen ST-BUS/GCI-Bus outputs (STio0 - 15). STio0 - 15 can also be configured as bi-directional pins, in which case STi0 - 15 will be ignored. It is a non-blocking digital switch with 1024 64 kbps channels. The ST-BUS/GCI-Bus inputs and outputs accept serial input data streams with data rates of 2.048 Mbps, 4.096 Mbps, 8.192 Mbps and 16.384 Mbps.

By using Zarlink's message mode capability, microprocessor data stored in the connection memory can be broadcast to the output streams on a per-channel basis. This feature is useful for transferring control and status information for external circuits or other ST-BUS/GCI-Bus devices.

The device uses the ST-BUS/GCI-Bus input frame pulse (FPi) and the ST-BUS/GCI-Bus input clock (CKi) to define the input frame boundary and timing for sampling the ST-BUS/GCI-Bus input streams with various data rates. The output data streams will be driven by and have their timing defined by FPi and CKi. A Motorola or Intel compatible non-multiplexed microprocessor port allows users to program the device to operate in various modes under different switching configurations. Users can use the microprocessor port to perform internal register and memory read and write operations. The microprocessor port has a 16-bit data bus, a 14-bit address bus and six control signals (MOT_$\overline{\text{INTEL}}$, $\overline{\text{CS}}$, $\overline{\text{DS}}$_$\overline{\text{RD}}$, R/$\overline{\text{W}}$_$\overline{\text{WR}}$ and $\overline{\text{DTA}}$_RDY).

The device supports the mandatory requirements of the IEEE-1149.1 (JTAG) standard via the test port.

5.0 Data Rates and Timing

The ZL50017 has 16 serial data inputs and 16 serial data outputs. All streams are programmed to operate at 2.048 Mbps, 4.096 Mbps, 8.192 Mbps or 16.384 Mbps. Depending on the data rate there will be 32 channels, 64 channels, 128 channels or 256 channels, respectively, during a 125 μs frame.

The output streams can be programmed to operate as bi-directional streams. By setting BDL (bit 6) in the Internal Mode Selection (IMS) register, the input streams 0 - 15 (STi0 - 15) are internally tied low, and the output streams 0 - 15 (STio0 - 15) are set to operate in a bi-directional mode.The input data rate is set on a per-stream basis by programming STIN[n]DR3 - 0 (bits 3 - 0) in the Stream Input Control Register 0 - 15 (SICR0 - 15). The output data rate is set on a per-stream basis by programming STO[n]DR3 - 0 (bits 3 - 0) in the Stream Output Control Register 0 - 15 (SOCR0 - 15). The output data rates do not have to match or follow the input data rates. The maximum number of channels switched is limited to 1024 channels. If all 16 input streams were operating at 8.192 Mbps (128 channels per stream), this would result in 2048 channels. Memory limitations prevent the device from operating at this capacity. A maximum capacity of 1024 channels will occur if four streams are operating at 16.384 Mbps, eight streams are operating at 8.192 Mbps or all sixteen streams are operating at 4.096 Mbps. With all streams operating at 2.048 Mbps, the capacity will be reduced to 512 channels. It should be noted that only full streams can be enabled, the device does not allow partial streams configuration (i.e., cannot have all the streams operating at 16.384 Mbps but only access the half the channels).

5.1 Input Clock (CKi) and Input Frame Pulse (FPi) Timing

The frequency of the input clock (CKi) for the ZL50017 must be at least twice the input/output data rate. For example, if the input/output data rate is 8.192 Mbps, the input clock, CKi, must be 16.384 MHz. Following the example above, if the input/output data rate is 4.096 Mbps, the input clock, CKi, must be 8.192 MHz.The only exception to this is for 16.384 Mbps input/output data. In this case, the input clock, CKi, is equal to the data rate. The input frame pulse, FPi, must always follow CKi. CKIN1 - 0 (bits 6 - 5) in the Control Register (CR) are used to program the width of the input frame pulse and the frequency of the input clock supplied to the device.

Highest *Input or Output* Data Rate	CKIN 1-0 Bits	Input Clock Rate (CKi)	Input Frame Pulse (FPi)
16.384 Mbps or 8.192 Mbps	00	16.384 MHz	8 kHz (61 ns wide pulse)
4.096 Mbps	01	8.192 MHz	8 kHz (122 ns wide pulse)
2.048 Mbps	10	4.096 MHz	8 kHz (244 ns wide pulse)

Table 1 - CKi and FPi Configurations

The ZL50017 accepts positive and negative ST-BUS/GCI-Bus input clock and input frame pulse formats via the programming of CKINP (bit 8) and FPINP (bit 7) in the Control Register (CR). By default, the device accepts the negative input clock format and ST-BUS format frame pulses. However, the switch can also accept a positive-going clock format by programming CKINP (bit 8) in the Control Register (CR). A GCI-Bus format frame pulse can be used by programming FPINPOS (bit 9) and FPINP (bit 7) in the Control Register (CR).

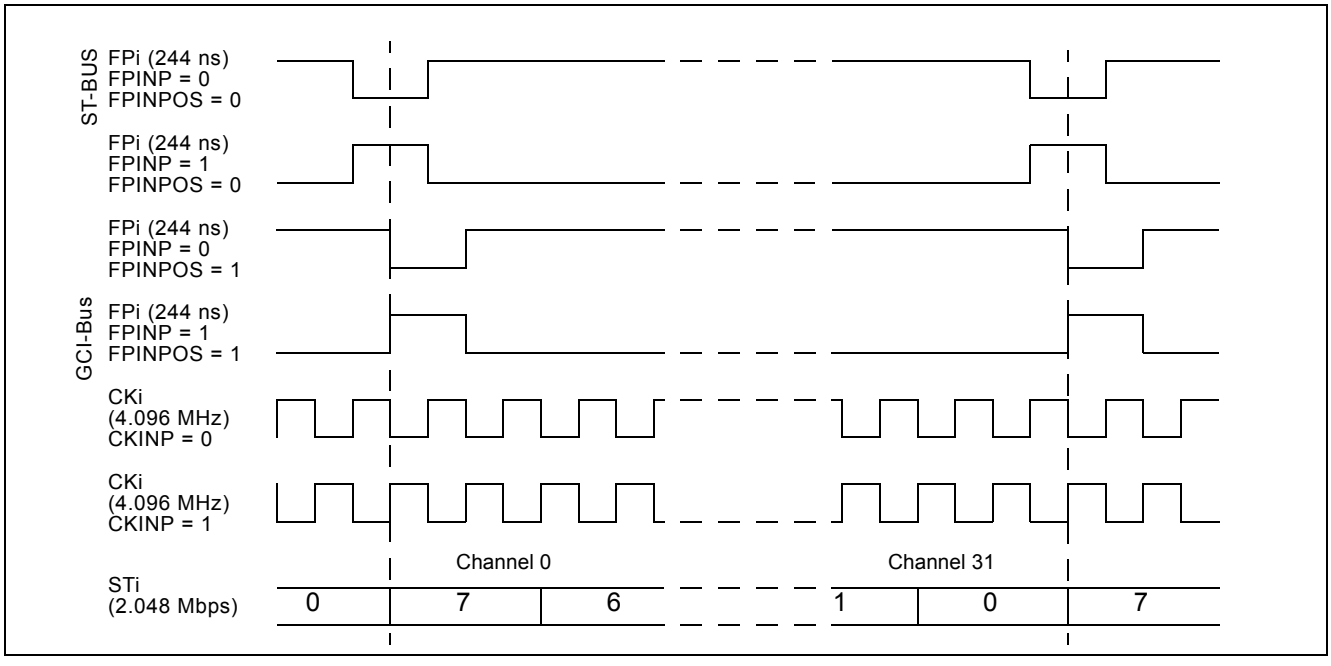


Figure 4 - Input Timing when CKIN1 - 0 bits = “10” in the CR

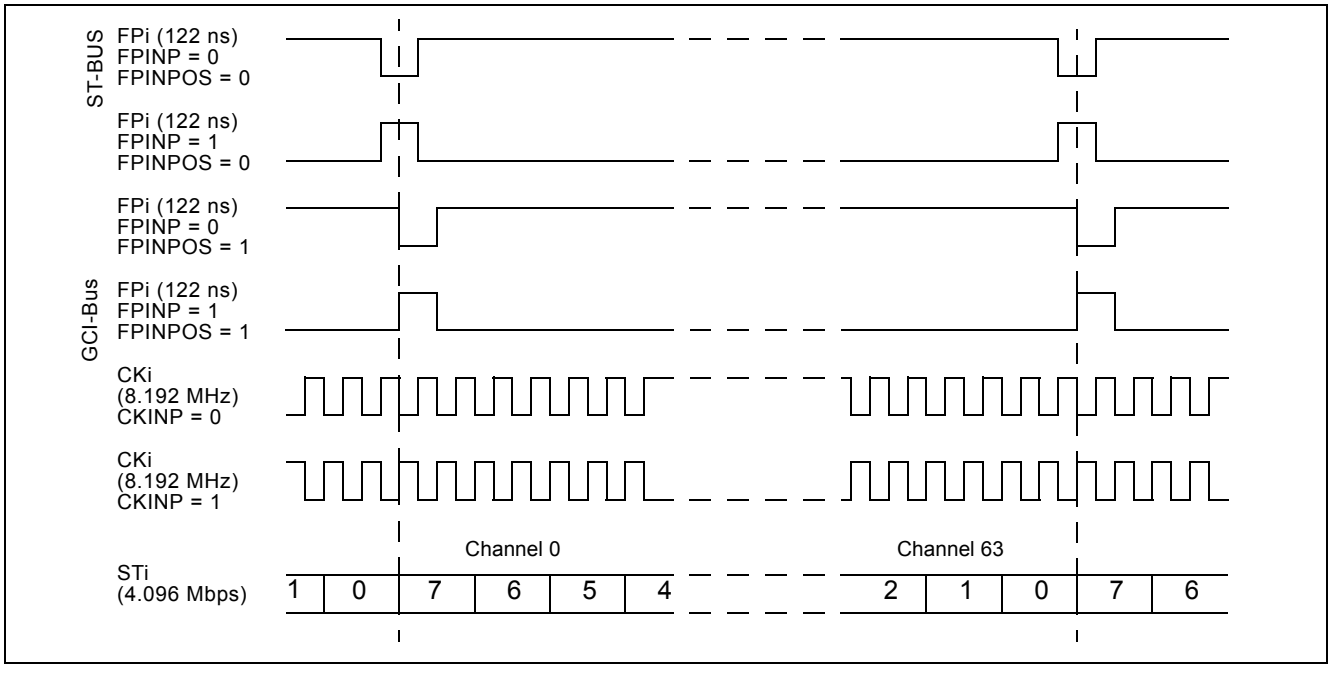


Figure 5 - Input Timing when CKIN1 - 0 bits = “01” in the CR

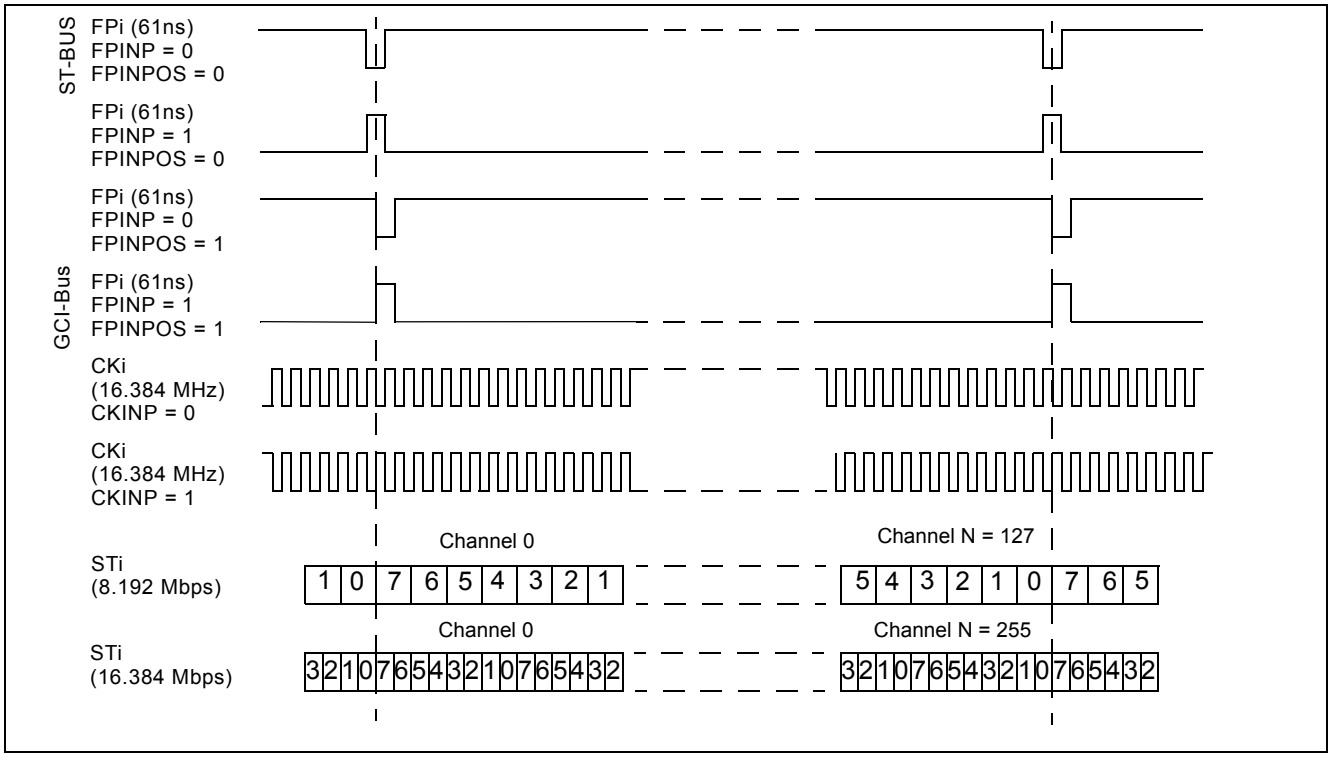


Figure 6 - Input Timing when CKIN1 - 0 = “00” in the CR

5.2 ST-BUS and GCI-Bus Timing

The ZL50017 is capable of operating using either the ST-BUS or GCI-Bus standards. By default, the ZL50017 is configured for ST-BUS input and output timing. To set the input timing to conform to the GCI-Bus standard, FPINPOS (bit 9) and FPINP (bit 7) in the Control Register (CR) must be set.

6.0 Data Input Delay and Data Output Advancement

Various registers are provided to adjust the input delay and output advancement for each input and output data stream. The input bit delay and output bit advancement can vary from 0 to 7 bits for each individual stream.

If input delay of less than a bit is desired, different sampling points can be used to handle the adjustments. The sampling point can vary from 1/4 to 4/4 with a 1/4-bit increment for all input streams. By default, the sampling point is set to the 3/4-bit location.

The fractional output bit advancement can vary from 0 to 3/4 bits, again with a 1/4 bit increment. By default, there is 0 output bit advancement.

Although input delay or output advancement features are available on streams which are operating in bi-directional mode it is not recommended, as it can easily cause bus contention. If users require this function, special attention must be given to the timing to ensure contention is minimized.

6.1 Input Bit Delay Programming

The input bit delay programming feature provides users with the flexibility of handling different wire delays when designing with source streams for different devices.

By default, all input streams have zero bit delay, such that bit 7 is the first bit that appears after the input frame boundary (assuming ST-BUS formatting). The input delay is enabled by STIN[n]BD2-0 (bits 8 - 6) in the Stream Input Control Register 0 - 15 (SICR0 - 15) as described in Table 10 on page 32. The input bit delay can range from 0 to 7 bits.

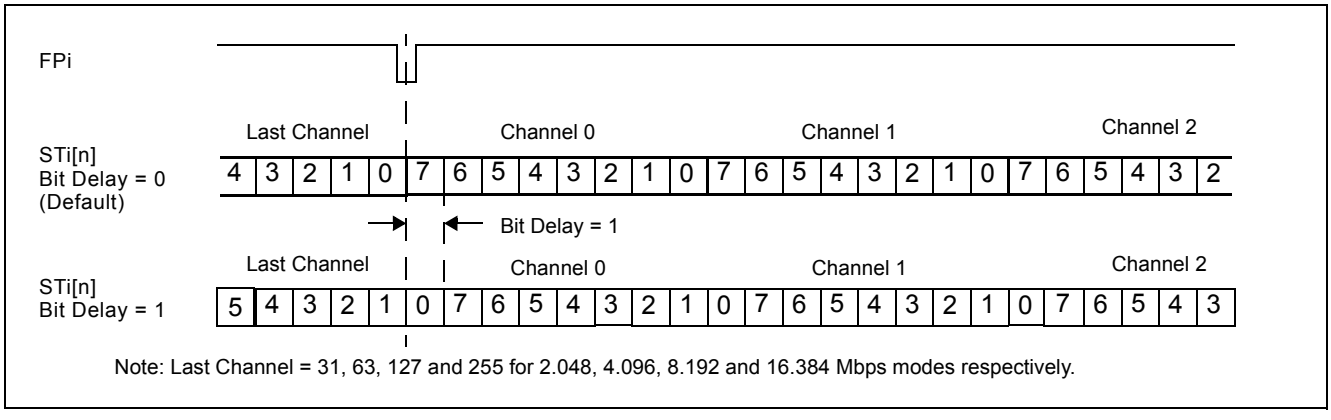


Figure 7 - Input Bit Delay Timing Diagram (ST-BUS)

6.2 Input Bit Sampling Point Programming

In addition to the input bit delay feature, the ZL50017 allows users to change the sampling point of the input bit by programming STIN[n]SMP 1-0 (bits 5 - 4) in the Stream Input Control Register 0 - 15 (SICR0 - 15). For input streams the default sampling point is at 3/4 bit and users can change the sampling point to 1/4, 1/2, 3/4 or 4/4 bit position.

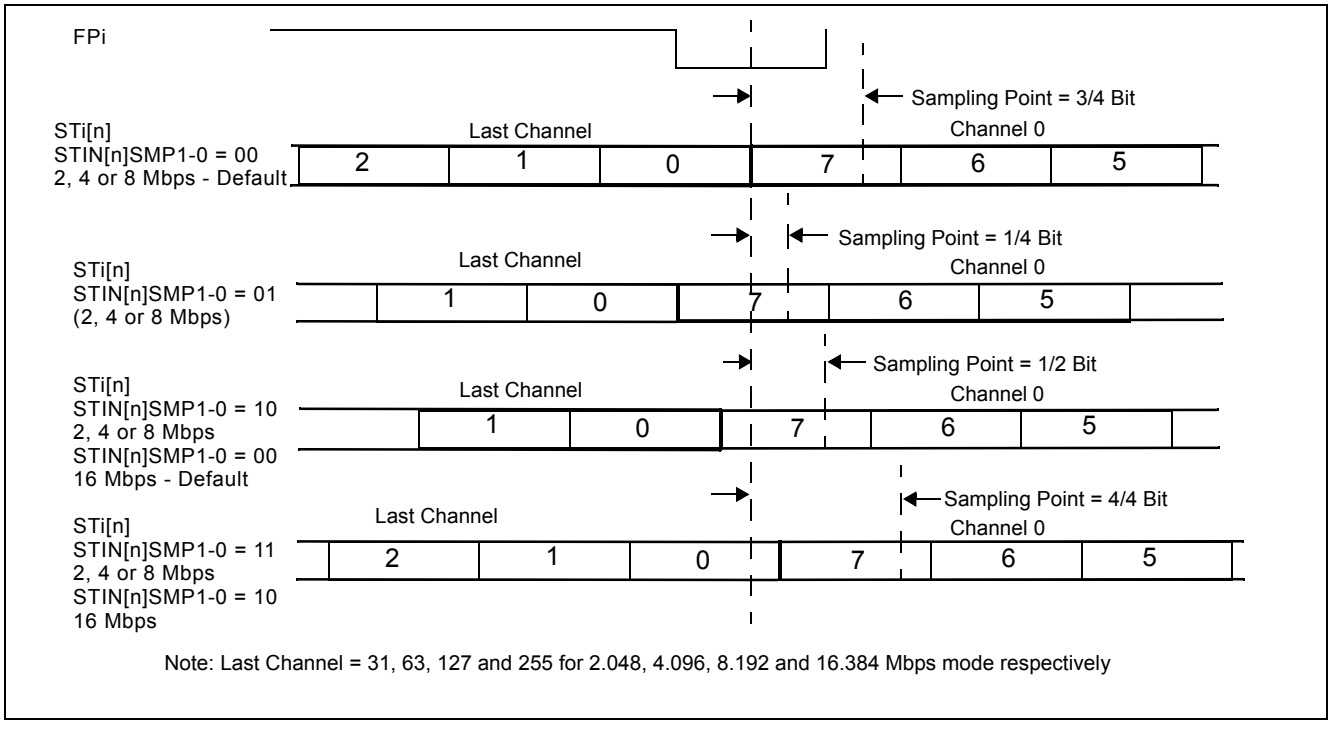


Figure 8 - Input Bit Sampling Point Programming

The input delay is controlled by STIN[n]BD2-0 (bits 8 - 6) to control the bit shift and STIN[n]SMP1 - 0 (bits 5 - 4) to control the sampling point in the Stream Input Control Register 0 - 15 (SICR0 - 15).

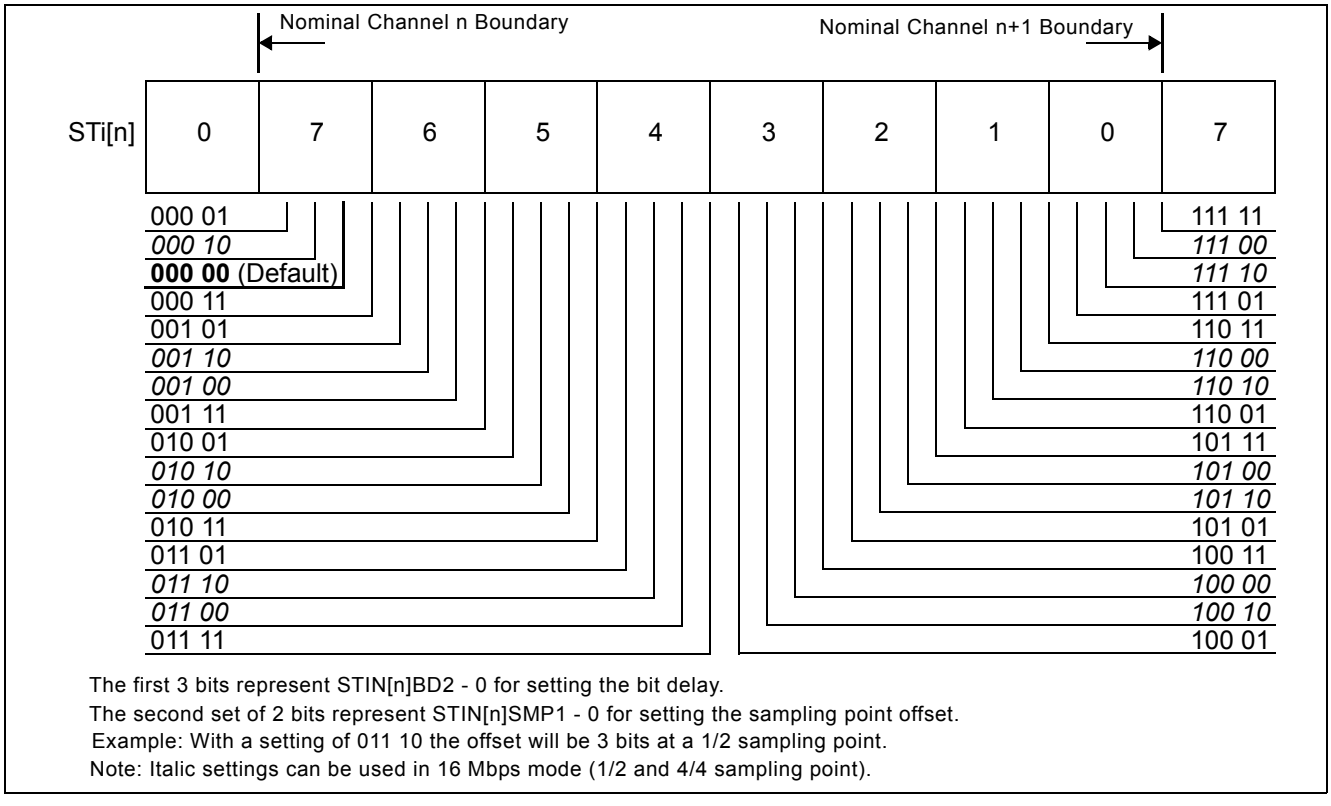


Figure 9 - Input Bit Delay and Factional Sampling Point

6.3 Output Advancement Programming

This feature is used to advance the output data of individual output streams with respect to the input frame boundary. Each output stream has its own bit advancement value which can be programmed in the Stream Output Control Register 0 - 15 (SOCR0 - 15).

By default, all output streams have zero bit advancement such that bit 7 is the first bit that appears after the input frame boundary (assuming ST-BUS formatting). The output advancement is enabled by STO[n]AD 2 - 0 (bits 6 - 4) of the Stream Output Control Register 0 - 15 (SOCR0 - 15) as described in Table 11 on page 33. The output bit advancement can vary from 0 to 7 bits.

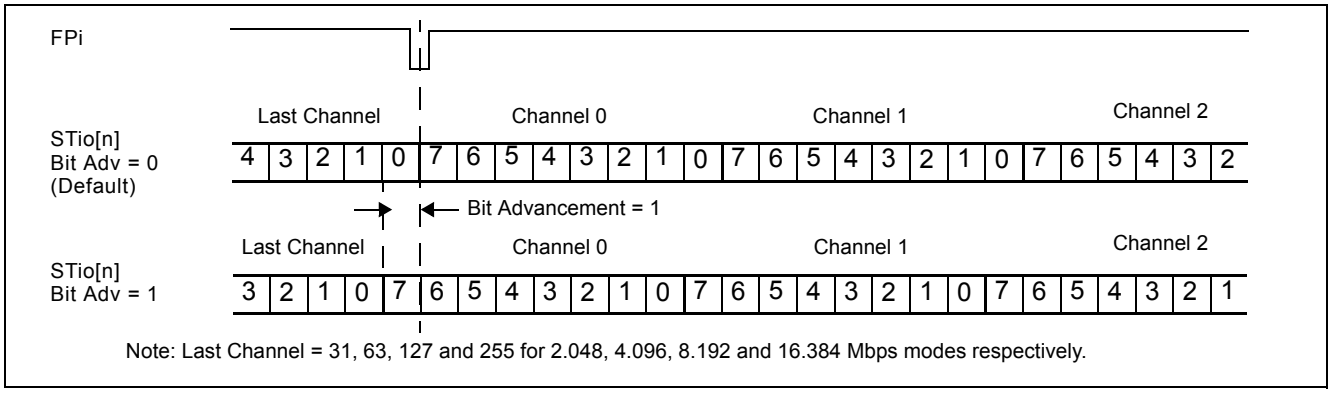


Figure 10 - Output Bit Advancement Timing Diagram (ST-BUS)

6.4 Fractional Output Bit Advancement Programming

In addition to the output bit advancement, the device has a fractional output bit advancement feature that offers better resolution. The fractional output bit advancement is useful in compensating for varying parasitic load on the serial data output pins.

By default all of the streams have zero fractional bit advancement such that bit 7 is the first bit that appears after the output frame boundary. The fractional output bit advancement is enabled by STO[n]FA 1 - 0 (bits 8 - 7) in the Stream Output Control Register 0 - 15 (SOCR0 - 15). For all streams the fractional bit advancement can vary from 0, 1/4, 1/2 to 3/4 bits.

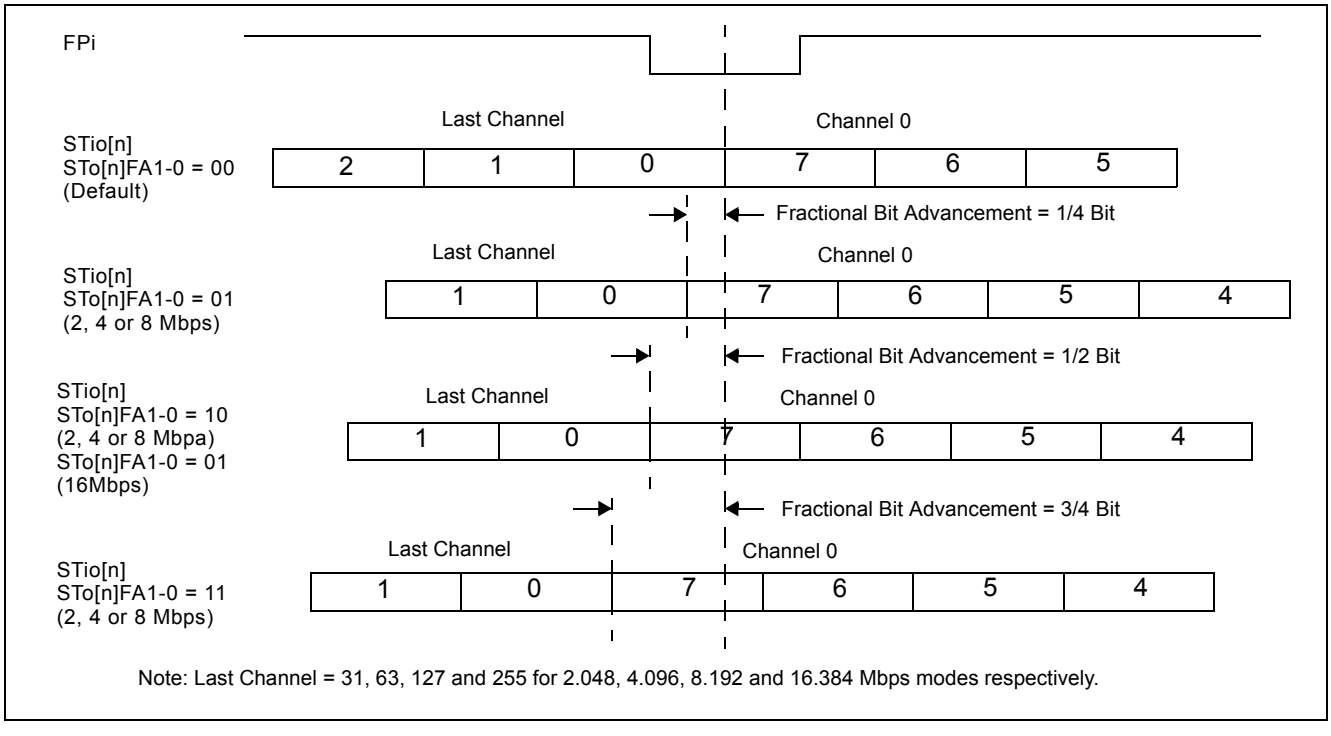


Figure 11 - Output Fractional Bit Advancement Timing Diagram (ST-BUS)

7.0 Data Delay Through the Switching Paths

The switching of information from the input serial streams to the output serial streams results in a throughput delay. The device can be programmed to perform timeslot interchange functions with different throughput delay capabilities on a per-channel basis. For voice applications, select variable throughput delay to ensure minimum delay between input and output data. In wideband data applications, select constant delay to maintain the frame integrity of the information through the switch. The delay through the device varies according to the type of throughput delay selected by the V/$\overline{C}$ (bit 14) in the Connection Memory Low when CMM = 0.

7.1 Variable Delay Mode

Variable delay mode causes the output channel to be transmitted as soon as possible. This is a useful mode for voice applications where the minimum throughput delay is more important than frame integrity. The delay through the switch can vary from 7 channels to 1 frame + 7 channels. To set the device into variable delay mode, VAREN (bit 4) in the Control Register (CR) must be set before V/$\overline{C}$ (bit 14) in the Connection Memory Low when CMM = 0. If the VAREN bit is not set and the device is programmed for variable delay mode, the information read on the output stream will not be valid.

In variable delay mode, the delay depends on the combination of the source and destination channels of the input and output streams.

m = input channel number n = output channel number	n-m <= 0	0 < n-m < 7	n-m = 7		n-m > 7
			STio < STi	STio >= STi	
T = Delay between input and output	1 frame - (m-n)	1 frame + (n-m)		n-m	

Table 2 - Delay for Variable Delay Mode

For example, if Stream 4 Channel 2 is switched to Stream 5 Channel 9 with variable delay, the data will be output in the same 125 μs frame. Contrarily, if Stream 6 Channel 1 is switched to Stream 9 Channel 3, the information will appear in the following frame.

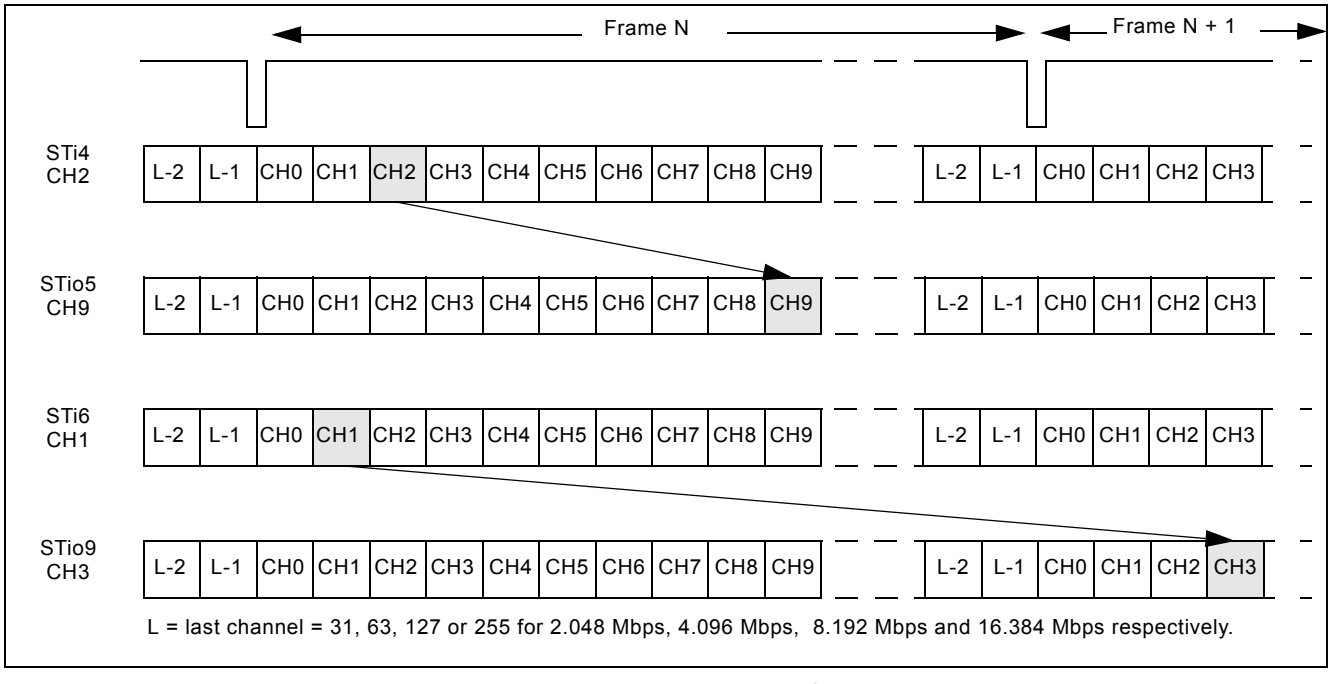


Figure 12 - Data Throughput Delay for Variable Delay

7.2 Constant Delay Mode

In this mode, frame integrity is maintained in all switching configurations. The delay though the switch is 2 frames - Input Channel + Output Channel. This can result in a minimum of 1 frame + 1 channel delay if the last channel on a stream is switched to the first channel of a stream. The maximum delay is 3 frames - 1 channel. This occurs when the first channel of a stream is switched to the last channel of a stream. The constant delay mode is available for all output channels.

The data throughput delay is expressed as a function of ST-BUS/GCI-Bus frames, input channel number (m) and output channel number (n). The data throughput delay (T) is:

T = 2 frames + (n - m)

The constant delay mode is controlled by V/$\overline{C}$ (bit 14) in the Connection Memory Low when CMM = 0. When this bit is set low, the channel is in constant delay mode. If VAREN (bit 4) in the Control Register (CR) is set (to enable variable throughput delay on a chip-wide basis), the device can still be programmed to operate in constant delay mode.

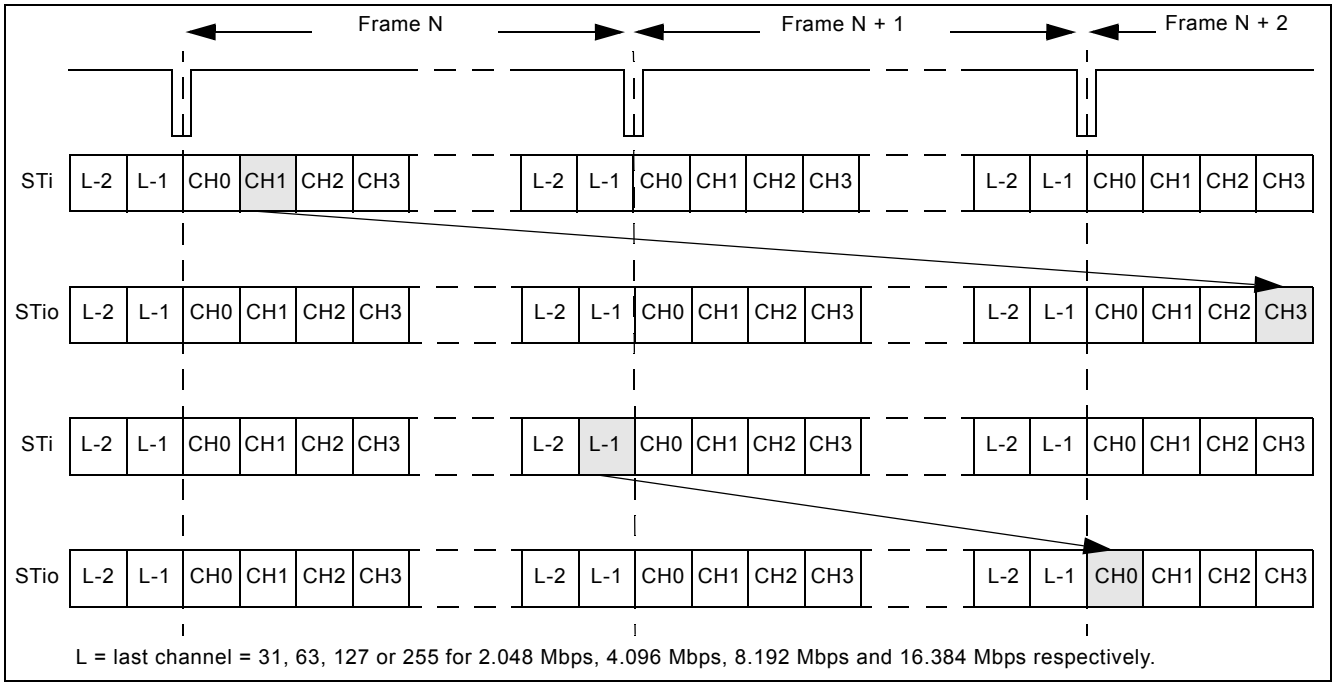


Figure 13 - Data Throughput Delay for Constant Delay

8.0 Connection Memory Description

The connection memory consists of two blocks, Connection Memory Low (CM_L). The CM_L is 16 bits wide and is used for channel switching and other special modes. Each connection memory location of the CM_L or CM_H can be read or written via the 16 bit microprocessor port within one microprocessor access cycle. See Table 12 on page 34 for the address mapping of the connection memory. Any unused bits will be reset to zero on the 16-bit data bus.

For the normal channel switching operation, CMM (bit 0) of the Connection Memory Low (CM_L) is programmed low. SCA7 - 0 (bits 8 - 1) indicate the source (input) channel address and SSA4 - 0 (bits 13 - 9) indicate the source (input) stream address. When CMM (bit 0) of the Connection Memory Low (CM_L) is programmed high, the ZL50017 will operate in one of the special modes described in Table 14 on page 36. When the per-channel message mode is enabled, MSG7 - 0 (bit 10 - 3) in the Connection Memory Low (CM_L) will be output via the serial data stream as message output data.

9.0 Connection Memory Block Programming

This feature allows for fast initialization of the connection memory after power up.

9.1 Memory Block Programming Procedure

1. Set MBPE (bit 3) in the Control Register (CR) from low to high.
2. Configure BPD2 - 0 (bits 3 - 1) in the Internal Mode Selection (IMS) register to the desired values to be loaded into CM_L.
3. Start the block programming by setting MBPS (bit 0) in the Internal Mode Selection Register (IMS) high. The values stored in BPD2 - 0 will be loaded into bits 2 - 0 of all CM_L positions. The remaining CM_L locations (bits 15 - 3).

The following tables show the resulting values that are in the CM_L and CM_H connection memory locations.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	0	0	0	0	0	0	0	0	0	0	0	0	0	BPD2	BPD1	BPD0

Table 3 - Connection Memory Low After Block Programming

It takes at least two frame periods (250 μs) to complete a block program cycle.

MBPS (bit 0) in the Control Register (CR) will automatically reset to a low position after the block programming process has completed.

MBPE (bit 3) in the Internal Mode Selection (IMS) register must be cleared from high to low to terminate the block programming process. This is not an automatic action taken by the device and must be performed manually.

Note: Once the block program has been initiated, it can be terminated at any time prior to completion by setting MBPS (bit 0) in the Control Register (CR) or MBPE (bit 3) in the Internal Mode Selection (IMS) register to low.

10.0 Microprocessor Port

The device provides access to the internal registers, connection memories and data memories via the microprocessor port. The microprocessor port is capable of supporting both Motorola and Intel non-multiplexed microprocessors. The microprocessor port consists of a 16-bit parallel data bus (D15 - 0), 14 bit address bus (A13 - 0) and six control signals (MOT_INTEL, $\overline{CS}$, $\overline{DS}$_$\overline{RD}$, R/$\overline{W}$_$\overline{WR}$ and $\overline{DTA}$_RDY).

The data memory can only be read from the microprocessor port. For a data memory read operation, D7 - 0 will be used and D15 - 8 will output zeros.

For a CM_L read or write operation, all bits (D15 - 0) of the data bus will be used. For a CM_H write operation, D4 - 0 of the data bus must be configured and D15 - 5 are ignored. D15 - 5 must be driven either high or low. For a CM_H read operation, D4 - 0 will be used and D15 - 5 will output zeros.

Refer to Figure 15 on page 39, Figure 16 on page 40, Figure 17 on page 41 and Figure 18 on page 42 for the microprocessor timing.

11.0 Device Reset and Initialization

The $\overline{\text{RESET}}$ pin is used to reset the ZL50017. When this pin is low, the following functions are performed:

- synchronously puts the microprocessor port in a reset state
- tristates the STio0 - 15 outputs
- preloads all internal registers with their default values (refer to the individual registers for default values)
- clears all internal counters

11.1 Power-up Sequence

The recommended power-up sequence is for the V_{DD_IO} supply (normally +3.3 V) to be established before the power-up of the V_{DD_CORE} supply (normally +1.8 V). The V_{DD_CORE} supply may be powered up at the same time as V_{DD_IO}, but should not “lead” the V_{DD_IO} supply by more than 0.3 V.

11.2 Device Initialization on Reset

Upon power up, the ZL50017 should be initialized as follows:

- Set the ODE pin to low to disable the STio0 - 15 outputs
- Set the $\overline{\text{TRST}}$ pin to low to disable the JTAG TAP controller
- Reset the device by pulsing the $\overline{\text{RESET}}$ pin to zero for longer than 1 μs
- After releasing the $\overline{\text{RESET}}$ pin from low to high, wait for a certain period of time (see Note below) for the device to stabilize from the power down state before the first microprocessor port access can occur
- Wait at least 500 μs prior to the next microport access (see Note below)
- Use the block programming mode to initialize the connection memory
- Release the ODE pin from low to high after the connection memory is programmed

Note: If CKi is 16.384 MHz, the waiting time is 500 μs; if CKi is 8.192 MHz, the waiting time is 1 ms; if CKi is 4.096 MHz, the waiting time is 2 ms.

11.3 Software Reset

In addition to the hardware reset from the $\overline{\text{RESET}}$ pin, the device can also be reset by using software reset SRSTSW (bit 1) in the Software Reset Register (SRR).

12.0 JTAG Port

The JTAG test port is implemented to meet the mandatory requirements of the IEEE-1149.1 (JTAG) standard. The operation of the boundary-scan circuitry is controlled by an external Test Access Port (TAP) Controller.

12.1 Test Access Port (TAP)

The Test Access Port (TAP) accesses the ZL50017 test functions. It consists of three input pins and one output pin as follows:

- **Test Clock Input (TCK)** - TCK provides the clock for the test logic. TCK does not interfere with any on-chip clock and thus remains independent in the functional mode. TCK permits shifting of test data into or out of the Boundary-Scan register cells concurrently with the operation of the device and without interfering with the on-chip logic.

- **Test Mode Selection Inputs (TMS)** - The TAP Controller uses the logic signals received at the TMS input to control test operations. The TMS signals are sampled at the rising edge of the TCK pulse. This pin is internally pulled to high when it is not driven from an external source.
- **Test Data Input (TDi)** - Serial input data applied to this port is fed either into the instruction register or into a test data register, depending on the sequence previously applied to the TMS input. The registers are described in a subsequent section. The received input data is sampled at the rising edge of the TCK pulse. This pin is internally pulled to high when it is not driven from an external source.
- **Test Data Output (TDo)** - Depending on the sequence previously applied to the TMS input, the contents of either the instruction register or test data register are serially shifted out towards TDo. The data from TDo is clocked on the falling edge of the TCK pulses. When no data is shifted through the boundary scan cells, the TDo driver is set to a high impedance state.
- **Test Reset ($\overline{\text{TRST}}$)** - Resets the JTAG scan structure. This pin is internally pulled to high when it is not driven from an external source.

12.2 Instruction Register

The ZL50017 uses the public instructions defined in the IEEE-1149.1 standard. The JTAG interface contains a four-bit instruction register. Instructions are serially loaded into the instruction register from the TDi when the TAP Controller is in its shifted-OR state. These instructions are subsequently decoded to achieve two basic functions: to select the test data register that may operate while the instruction is current and to define the serial test data register path that is used to shift data between TDi and TDo during data register scanning.

12.3 Test Data Registers

As specified in the IEEE-1149.1 standard, the ZL50017 JTAG interface contains three test data registers:

- **The Boundary-Scan Register** - The Boundary-Scan register consists of a series of boundary-scan cells arranged to form a scan path around the boundary of the ZL50017 core logic.
- **The Bypass Register** - The Bypass register is a single stage shift register that provides a one-bit path from TDi to TDo.
- **The Device Identification Register** - The JTAG device ID for the ZL50017 is $0C36114B_H$

Version	<31:28>	0000
Part Number	<27:12>	1100 0011 0110 0001
Manufacturer ID	<11:1>	0001 0100 101
LSB	<0>	1

12.4 BSDL

A Boundary Scan Description Language (BSDL) file is available from Zarlink Semiconductor to aid in the use of the IEEE-1149.1 test interface.

13.0 Register Address Mapping

Address A13 - A0	CPU Access	Register Name	Abbreviation	Reset By
0000_H	R/W	Control Register	CR	Switch/Hardware
0001_H	R/W	Internal Mode Selection Register	IMS	Switch/Hardware
0002_H	R/W	Software Reset Register	SRR	Hardware Only
0008_H	R/W	Data Rate Selection Register	DRSR	Switch/Hardware
0010_H	R Only	Internal Flag Register	IFR	Switch/Hardware
0100_H - $010F_H$	R/W	Stream Input Control Registers 0 - 15	SICR0 - 15	Switch/Hardware
0200_H - $020F_H$	R/W	Stream Output Control Registers 0 - 15	SOCR0 - 15	Switch/Hardware

Table 4 - Address Map for Registers (A13 = 0)

14.0 Detailed Register Description

External Read/Write Address: 0000_H
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	FPIN POS	CKINP	FPINP	CKIN 1	CKIN 0	VAR EN	MBPE	OSB	MS1	MS0

Bit	Name	Description
15 - 10	Unused	**Reserved.** In normal functional mode, these bits **MUST** be set to zero.
9	FPINPOS	**Input Frame Pulse (FPi) Position** When this bit is low, FPi straddles frame boundary (as defined by ST-BUS). When this bit is high, FPi starts from frame boundary (as defined by GCI-Bus)
8	CKINP	**Clock Input (CKi) Polarity** When this bit is low, the CKi falling edge aligns with the frame boundary. When this bit is high, the CKi rising edge aligns with the frame boundary.
7	FPINP	**Frame Pulse Input (FPi) Polarity** When this bit is low, the input frame pulse FPi has the negative frame pulse format. When this bit is high, the input frame pulse FPi has the positive frame pulse format.
6 - 5	CKIN1 - 0	**Input Clock (CKi) and Frame Pulse (FPi) Selection** CKIN1 - 0 / FPi Active Period / CKi 00 / 61 ns / 16.384 MHz 01 / 122 ns / 8.192 MHz 10 / 244 ns / 4.096 MHz 11 / Reserved The MODE_4M0 and MODE_4M1 pins, as described in “Pin Description” on page 9, should also be set to define the input clock mode.
4	VAREN	**Variable Delay Mode Enable** When this bit is low, the variable delay mode is disabled on a device-wide basis. When this bit is high, the variable delay mode is enabled on a device-wide basis.
3	MBPE	**Memory Block Programming Enable** When this bit is high, the connection memory block programming mode is enabled to program the connection memory. When it is low, the memory block programming mode is disabled.

Table 5 - Control Register (CR) Bits

External Read/Write Address: 0000_H
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	FPIN POS	CKINP	FPINP	CKIN 1	CKIN 0	VAR EN	MBPE	OSB	MS1	MS0

Bit	Name	Description
2	OSB	**Output Stand By Bit:** This bit enables the STio0 - 1 serial outputs. The following table describes the HiZ control of the serial data outputs: $\overline{\text{RESET}}$ Pin / SRSTSW (in SRR) / ODE Pin / OSB Bit / STio0 - 15 0 / X / X / X / HiZ 1 / 1 / X / X / HiZ 1 / 0 / 0 / X / HiZ 1 / 0 / 1 / 0 / HiZ 1 / 0 / 1 / 1 / Active (Controlled by CM) Note: Unused output streams are tristated (STio = HiZ). Refer to SOCR0 - 15 (bit 2 - 0).
1 - 0	MS1 - 0	**Memory Select Bits** These two bits are used to select connection memory low, connection high or data memory for access by CPU: MS1 - 0 / Memory Selection 00 / Connection Memory Low Read/Write 01 / Reserved 10 / Data Memory Read 11 / Reserved

Table 5 - Control Register (CR) Bits (continued)

External Read/Write Address: 0001_H
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	STIO_PD_EN	0	BD	0	0	BPD 2	BPD 1	BPD 0	MBPS

Bit	Name	Description
15 - 9	Unused	**Reserved.** In normal functional mode, these bits **MUST** be set to zero.
8	STIO_PD_EN	**STio Pull-down Enable** When this bit is low, the pull-down resistors on all STio pads will be disabled. When this bit is high, the pull-down resistors on all STio pads will be enabled.
7	Unused	**Reserved.** In normal functional mode, these bits **MUST** be set to zero.
6	BD	**Bi-directional Control** **BDL** / **STio0 - 15 Operation** 0: normal operation: STi0-15 are inputs, STio0-15 are outputs 1: bi-directional operation: STi0-15 tied low internally, STio0-15 are bi-directional
5 - 4	Unused	**Reserved.** In normal functional mode, these bits **MUST** be set to zero.
3 - 1	BPD2 - 0	**Block Programming Data** These bits refer to the value to be loaded into the connection memory, whenever the memory block programming feature is activated. After the MBPE bit in the Control Register is set to high and the MBPS bit in this register is set to high, the contents of the bits BPD2 - 0 are loaded into bits 2 - 0 of the Connection Memory Low. Bits 15 - 3 of the Connection Memory Low.
0	MBPS	**Memory Block Programming Start:** A zero to one transition of this bit starts the memory block programming function. The MBPS and BPD2 - 0 bits in this register must be defined in the same write operation. Once the MBPE bit in the Control Register is set to high, the device requires two frames to complete the block programming. After the programming function has finished, the MBPS bit returns to low, indicating the operation is completed. When MBPS is high, MBPS or MBPE can be set to low to abort the programming operation. Whenever the microprocessor writes a one to the MBPS bit, the block programming function is started. As long as this bit is high, the user must maintain the same logical value to the other bits in this register to avoid any change in the device setting.

Table 6 - Internal Mode Selection Register (IMS) Bits

External Read/Write Address: 0002_H
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	SRST SW	0

Bit	Name	Description
15 - 2	Unused	**Reserved** In normal functional mode, these bits **MUST** be set to zero.
1	SRSTSW	**Software Reset Bit for Switch** When this bit is low, switching blocks are in normal operation. When this bit is high, switching blocks are in software reset state. Refer to Table 12, “Address Map for Registers (A13 = 0)” on page 32 for details regarding which registers are affected.
0	Unused	**Reserved** In normal functional mode, these bits **MUST** be set to zero.

Table 7 - Software Reset Register (SRR) Bits

External Read/Write Address: 0008_H
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	DR3	DR2	DR1	DR0

Bit	Name	Description
15 - 4	Unused	**Reserved** In normal functional mode, these bits **MUST** be set to zero.
3 - 0	DR3 - 0	**Input/Output Data Rate Selection Bits:** These bits set the data rate for both input and output streams

DR3 - 0	STio0 - 15 Operation
0000	Reserved
0001	2.048 Mbps
0010	4.096 Mbps
0011	8.192 Mbps
0100	16.384 Mbps
0101 - 1111	Reserved

Table 8 - Data Rate Selection Register

External Read Address: 0010_H
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PERR

Bit	Name	Description
15 - 1	Unused	**Reserved** In normal functional mode, these bits are zero.
0	PERR	**Program Error (Read Only)** This bit is set high when the total number of input/output channels is programmed to be more than the maximum capacity of 1024, in which case the input/output channels beyond the maximum capacity should be disabled.This bit will be cleared automatically after the total number of active streams/channels is correctly programmed to be 1024 channels or below.

Table 9 - Internal Flag Register (IFR) Bits - Read Only

External Read/Write Address: 0100_H - $010F_H$
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	STIN[n] BD2	STIN[n] BD1	STIN[n] BD0	STIN[n] SMP1	STIN[n] SMP0	0	0	0	STIN[n] EN

Bit	Name	Description
15 - 9	Unused	**Reserved** In normal functional mode, these bits **MUST** be set to zero.
8 - 6	STIN[n]BD2 - 0	**Input Stream[n] Bit Delay Bits.** The binary value of these bits refers to the number of bits that the input stream will be delayed relative to FPi. The maximum value is 7. Zero means no delay.
5 - 4	STIN[n]SMP1 - 0	**Input Data Sampling Point Selection Bits**
3 - 1	Unused	**Reserved** In normal functional mode, these bits **MUST** be set to zero.

STIN[n]SMP1-0	Sampling Point (2.048 Mbps, 4.096 Mbps, 8.192 Mbps streams)	Sampling Point 16.384 Mbps streams)
00	3/4 point	1/2 point
01	1/4 point	
10	2/4 point	4/4 point
11	4/4 point	

Table 10 - Stream Input Control Register 0 - 15 (SICR0 - 15) Bits

External Read/Write Address: 0100_H - $010F_H$
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	STIN[n] BD2	STIN[n] BD1	STIN[n] BD0	STIN[n] SMP1	STIN[n] SMP0	0	0	0	STIN[n] EN

Bit	Name	Description
0	STIN[n]EN	**Input Stream Enable Bit** When this bit is high the input stream is enabled. When this bit is low the input stream is ignored
Note: [n] denotes input stream from 0 - 15.		

Table 10 - Stream Input Control Register 0 - 15 (SICR0 - 15) Bits (continued)

External Read/Write Address: 0200_H - $020F_H$
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	STO[n] FA1	STO[n] FA0	STO[n] AD2	STO[n] AD1	STO[n] AD0	0	0	0	STO[n] EN

Bit	Name	Description
15 - 9	Unused	**Reserved** In normal functional mode, these bits **MUST** be set to zero.
8 - 7	STO[n]FA1 - 0	**Output Stream[n] Fractional Advancement Bits** STO[n]FA1-0 / Advancement (2.048 Mbps, 4.096 Mbps, 8.192 Mbps streams) / Advancement (16.384 Mbps streams) 00 / 0 / 0 01 / 1/4 bit / 2/4 10 / 2/4 bit / Reserved 11 / 3/4 bit /
6 - 4	STO[n]AD2 - 0	**Output Stream[n] Bit Advancement Selection Bits** The binary value of these bits refers to the number of bits that the output stream is to be advanced relative to FPi. The maximum value is 7. Zero means no advancement.
3 - 1	Unused	**Reserved** In normal functional mode, these bits **MUST** be set to zero.
0	STO[n]EN	**Output Stream Enable Bit** When this bit is high the output stream is enabled. When this bit is low the output stream is set to high impedance
Note: [n] denotes output stream from 0 - 15.		

Table 11 - Stream Output Control Register 0 - 15 (SOCR0 - 15) Bits

15.0 Memory

15.1 Memory Address Mappings

When A13 is high, the data or connection memory can be accessed by the microprocessor port. Bit 1 - 0 in the Control Register determine the access to the data or connection memory (CM_L or CM_H).

MSB (Note 1)	Stream Address (St0 - 15)						Channel Address (Ch0 - 255)								
A13	**A12**	**A11**	**A10**	**A9**	**A8**	**Stream [n]**	**A7**	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**	**Channel [n]**
1	0	0	0	0	0	Stream 0	0	0	0	0	0	0	0	0	Ch 0
1	0	0	0	0	1	Stream 1	0	0	0	0	0	0	0	1	Ch 1
1	0	0	0	1	0	Stream 2	.	.	.	.	.	.	.	.	.
1	0	0	0	1	1	Stream 3	.	.	.	.	.	.	.	.	.
1	0	0	1	0	0	Stream 4	0	0	0	1	1	1	1	0	Ch 30
1	0	0	1	0	1	Stream 5	0	0	0	1	1	1	1	1	Ch 31 (Note 2)
1	0	0	1	1	0	Stream 6	0	0	1	0	0	0	0	0	Ch 32
1	0	0	1	1	1	Stream 7	0	0	1	0	0	0	0	1	Ch 33
1	0	1	0	0	0	Stream 8	.	.	.		.	.		.	.
.	.	.	.	.	.	.	.	.	.		.			.	.
.	.	.	.	.	.	.	0	0	1	1	1	1	1	0	Ch 62
.	.	.	.	.	.	.	0	0	1	1	1	1	1	1	Ch 63 (Note 3)
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
1	0	1	1	1	0	Stream 14	0	1	1	1	1	1	1	0	Ch126
1	0	1	1	1	1	Stream 15	0	1	1	1	1	1	1	1	Ch 127 (Note 4)
							.	.	.	.	.	.	.	.	.
							.	.	.	.	.	.	.	.	.
							.	.	.	.	.	.	.	.	.
							.	.	.	.	.	.	.	.	.
							1	1	1	1	1	1	1	0	Ch 254
							1	1	1	1	1	1	1	1	Ch 255 (Note 5)

Notes:
1. A13 must be high for access to data and connection memory positions. A13 must be low to access internal registers.
2. Channels 0 to 31 are used when serial stream is at 2.048 Mbps.
3. Channels 0 to 63 are used when serial stream is at 4.096 Mbps.
4. Channels 0 to 127 are used when serial stream is at 8.192 Mbps.
5. Channels 0 to 255 are used when serial stream is at 16.384 Mbps.

Table 12 - Address Map for Memory Locations (A13 = 1)

15.2 Connection Memory Low (CM_L) Bit Assignment

When the CMM bit (bit 0) in the connection memory low is zero, the per-channel transmission is set to the normal channel-switching. The connection memory low bit assignment for the channel transmission mode is shown in Table 13 on page 35.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	V/$\overline{C}$	0	SSA 3	SSA 2	SSA 1	SSA 0	SCA 7	SCA 6	SCA 5	SCA 4	SCA 3	SCA 2	SCA 1	SCA 0	**CMM =0**

Bit	Name	Description
15	Unused	**Reserved** In normal functional mode, these bits **MUST** be set to zero.
14	V/$\overline{C}$	**Variable/Constant Delay Control** When this bit is low, the output data for this channel will be taken from constant delay memory. When this bit is set to high, the output data for this channel will be taken from variable delay memory. Note that VAREN must be set in Control Register first.
13	Unused	**Reserved.** In normal functional mode, this bit **MUST** be set to zero.
12 - 9	SSA3 - 0	**Source Stream Address** The binary value of these 4 bits represents the input stream number.
8 - 1	SCA7 - 0	**Source Channel Address** The binary value of these 8 bits represents the input channel number.
0	CMM = 0	**Connection Memory Mode = 0** If this is low, the connection memory is in the normal switching mode. Bit 13 - 1 are the source stream number and channel number.

Table 13 - Connection Memory Low (CM_L) Bit Assignment when CMM = 0

When CMM is one, the device is programmed to perform one of the special per-channel transmission modes. Bits PCC0 and PCC1 from connection memory are used to select the per-channel tristate or message mode as shown in Table 14 on page 36.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	MSG 7	MSG 6	MSG 5	MSG 4	MSG 3	MSG 2	MSG 1	MSG 0	PCC 1	PCC 0	**CMM =1**

Bit	Name	Description
15 - 11	Unused	**Reserved** In normal functional mode, these bits **MUST** be set to zero.
10 - 3	MSG7 - 0	**Message Data Bits** 8-bit data for the message mode. Not used in the per-channel tristate.
2 - 1	PCC1 - 0	**Per-Channel Control Bits** These two bits control the corresponding entry's value on the STio stream**.**
0	CMM = 1	**Connection Memory Mode = 1** If this is high, the connection memory is in the per-channel control mode which is per-channel tristate or per-channel message mode.

PCC1	PCC0	Channel Output Mode
0	0	Per Channel Tristate
0	1	Message Mode
1	0	Reserved
1	1	Reserved

Table 14 - Connection Memory Low (CM_L) Bit Assignment when CMM = 1

16.0 DC Parameters

Absolute Maximum Ratings*

	Parameter	Symbol	Min.	Max.	Units
1	I/O Supply Voltage	V_{DD_IO}	-0.5	5.0	V
2	Core Supply Voltage	V_{DD_CORE}	-0.5	2.5	V
3	Input Voltage	V_{I_3V}	-0.5	V_{DD} + 0.5	V
4	Input Voltage (5 V-tolerant inputs)	V_{I_5V}	-0.5	7.0	V
5	Continuous Current at Digital Outputs	I_o		15	mA
6	Package Power Dissipation	P_D		1.5	W
7	Storage Temperature	T_S	- 55	+125	°C

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units
1	Operating Temperature	T_{OP}	-40	25	+85	°C
2	Positive Supply	V_{DD_IO}	3.0	3.3	3.6	V
3	Positive Supply	V_{DD_CORE}	1.71	1.8	1.89	V
4	Input Voltage	V_I	0	3.3	V_{DD_IO}	V
5	Input Voltage on 5 V-Tolerant Inputs	V_{I_5V}	0	5.0	5.5	V

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics† - Voltages are with respect to ground (V_{ss}) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Supply Current - V_{DD_CORE}	I_{DD_CORE}			75	mA	
2	Supply Current - V_{DD_IO}	I_{DD_IO}			40	mA	C_L=30pF
3	Input High Voltage	V_{IH}	2.0			V	
4	Input Low Voltage	V_{IL}			0.8	V	
5	Input Leakage (input pins) Input Leakage (bi-directional pins)	I_{IL} I_{BL}			5 5	µA µA	$0 \le < V_{IN} \le V_{DD\_IO}$ See Note 1
6	Weak Pullup Current	I_{PU}		-33		µA	Input at 0 V
7	Weak Pulldown Current	I_{PD}		33		µA	Input at V_{DD_IO}
8	Input Pin Capacitance	C_I		3		pF	
9	Output High Voltage	V_{OH}	2.4			V	I_{OH} = 8 mA
10	Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 8 mA
11	Output High Impedance Leakage	I_{OZ}			5	µA	$0 < V < V_{DD}$
12	Output Pin Capacitance	C_O		5	10	pF	

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C, VDD_CORE at 1.8 V and VDD_IO at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

* Note 1: Maximum leakage on pins (output or I/O pins in high impedance state) is over an applied voltage (V_{IN}).

17.0 AC Parameters

AC Electrical Characteristics† - Timing Parameter Measurement Voltage Levels

	Characteristics	Sym.	Level	Units	Conditions
1	CMOS Threshold	V_{CT}	0.5 V_{DD_IO}	V	
2	Rise/Fall Threshold Voltage High	V_{HM}	0.7 V_{DD_IO}	V	
3	Rise/Fall Threshold Voltage Low	V_{LM}	0.3 V_{DD_IO}	V	

† Characteristics are over recommended operating conditions unless otherwise stated.

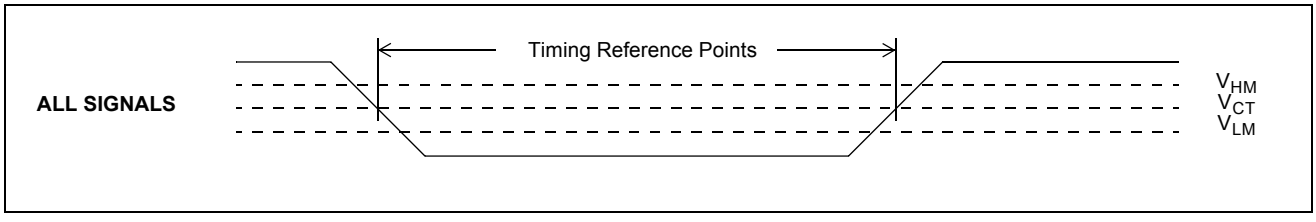


Figure 14 - Timing Parameter Measurement Voltage Levels

AC Electrical Characteristics† - Motorola Non-Multiplexed Bus Mode - Read Access

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions[2]
1	$\overline{CS}$ de-asserted time	t_{CSD}	15			ns	
2	$\overline{DS}$ de-asserted time	t_{DSD}	15			ns	
3	$\overline{CS}$ setup to $\overline{DS}$ falling	t_{CSS}	0			ns	
4	R/$\overline{W}$ setup to $\overline{DS}$ falling	t_{RWS}	10			ns	
5	Address setup to $\overline{DS}$ falling	t_{AS}	5			ns	
6	$\overline{CS}$ hold after $\overline{DS}$ rising	t_{CSH}	0			ns	
7	R/$\overline{W}$ hold after $\overline{DS}$ rising	t_{RWH}	0			ns	
8	Address hold after $\overline{DS}$ rising	t_{AH}	0			ns	
9	Data setup to $\overline{DTA}$ Low	t_{DS}	8			ns	C_L = 50 pF
10	Data Active to High Impedance	t_{DHZ}			8	ns	C_L = 50 pF, R_L = 1 K (Note 1)
11	Acknowledgement delay time. From $\overline{DS}$ low to $\overline{DTA}$ low: Registers Memory	t_{AKD}			75 185	ns ns	C_L = 50 pF C_L = 50 pF
12	Acknowledgement hold time. From $\overline{DS}$ high to $\overline{DTA}$ high	t_{AKH}	4		12	ns	C_L = 50 pF, R_L = 1 K (Note 1)
13	$\overline{DTA}$ drive high to HiZ	t_{AKZ}			8	ns	

Note 1: High impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel time taken to discharge C_L.

Note 2: A delay of 500 µs to 2 ms (see Section 11.2 on page 25) must be applied before the first microprocessor access is performed after the $\overline{RESET}$ pin is set high.

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C, VDD_CORE at 1.8 V and VDD_IO at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

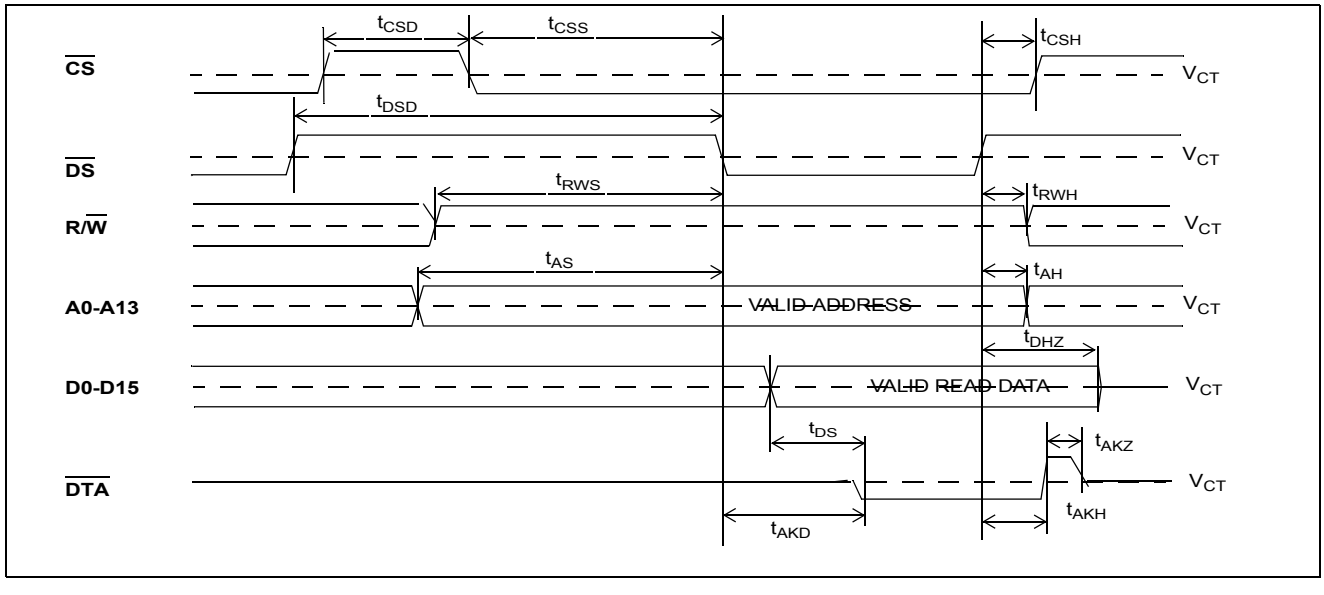


Figure 15 - Motorola Non-Multiplexed Bus Timing - Read Access

AC Electrical Characteristics† - Motorola Non-Multiplexed Bus Mode - Write Access

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions[2]
1	$\overline{CS}$ de-asserted time	t_{CSD}	15			ns	
2	$\overline{DS}$ de-asserted time	t_{DSD}	15			ns	
3	$\overline{CS}$ setup to $\overline{DS}$ falling	t_{CSS}	0			ns	
4	R/$\overline{W}$ setup to $\overline{DS}$ falling	t_{RWS}	10			ns	
5	Address setup to $\overline{DS}$ falling	t_{AS}	5			ns	
6	Data setup to $\overline{DS}$ falling	t_{DS}	0			ns	C_L = 50 pF
7	$\overline{CS}$ hold after $\overline{DS}$ rising	t_{CSH}	0			ns	
8	R/$\overline{W}$ hold after $\overline{DS}$ rising	t_{RWH}	0			ns	
9	Address hold after $\overline{DS}$ rising	t_{AH}	0			ns	
10	Data hold from $\overline{DS}$ rising	t_{DH}	5			ns	C_L = 50 pF, R_L = 1 K (Note 1)
11	Acknowledgement delay time. From $\overline{DS}$ low to $\overline{DTA}$ low: Registers Memory	t_{AKD}			 55 150	 ns ns	 C_L = 50 pF C_L = 50 pF
12	Acknowledgement hold time. From $\overline{DS}$ high to $\overline{DTA}$ high	t_{AKH}	4		12	ns	C_L = 50 pF, R_L = 1 K (Note 1)
13	$\overline{DTA}$ drive high to HiZ	t_{AKZ}			8	ns	

Note 1: High impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel time taken to discharge C_L.

Note 2: A delay of 500 µs to 2 ms (see Section 11.2 on page 25) must be applied before the first microprocessor access is performed after the $\overline{RESET}$ pin is set high.

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C, VDD_CORE at 1.8 V and VDD_IO at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

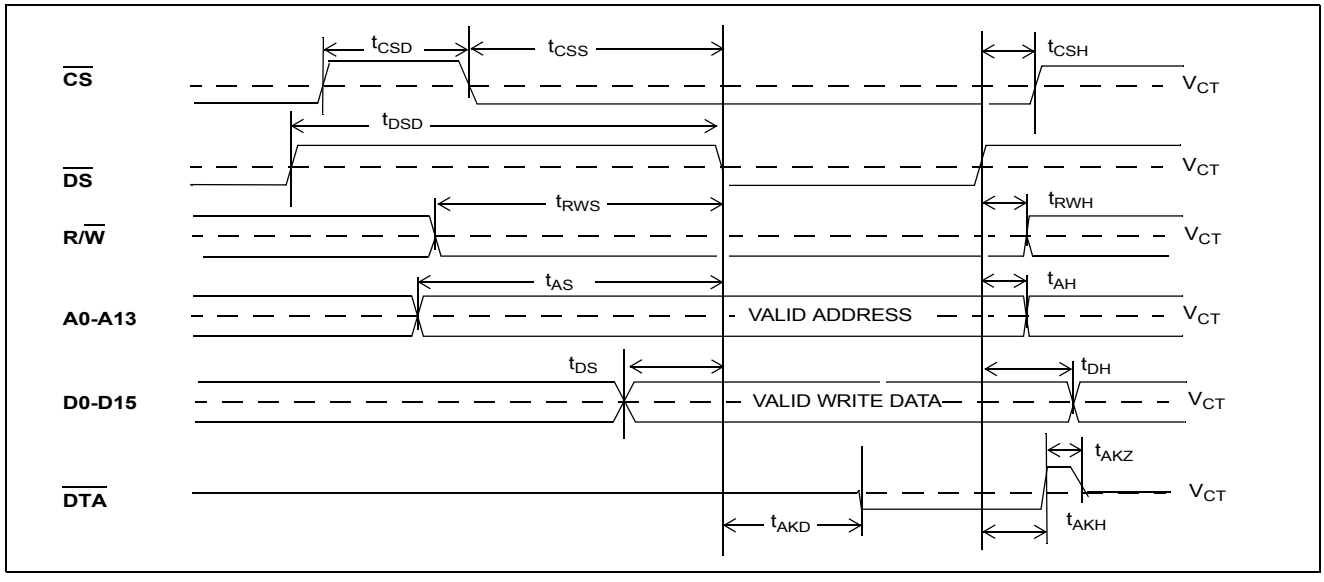


Figure 16 - Motorola Non-Multiplexed Bus Timing - Write Access

AC Electrical Characteristics† - Intel Non-Multiplexed Bus Mode - Read Access

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions[2]
1	$\overline{CS}$ de-asserted time	t_{CSD}	15			ns	
2	$\overline{RD}$ setup to $\overline{CS}$ falling	t_{RS}	10			ns	
3	$\overline{WR}$ setup to $\overline{CS}$ falling	t_{WS}	10			ns	
4	Address setup to $\overline{CS}$ falling	t_{AS}	5			ns	
5	$\overline{RD}$ hold after $\overline{CS}$ rising	t_{RH}	0			ns	
6	$\overline{WR}$ hold after $\overline{CS}$ rising	t_{WH}	0			ns	
7	Address hold after $\overline{CS}$ rising	t_{AH}	0			ns	
8	Data setup to RDY high	t_{DS}	8			ns	C_L = 50 pF
9	Data Active to High Impedance	t_{CSZ}	7			ns	C_L = 50 pF, R_L = 1 K (Note 1)
10	Acknowledgement delay time. From $\overline{CS}$ low to RDY high: Registers Memory	t_{AKD}			 175 185	 ns ns	 C_L = 50 pF C_L = 50 pF
11	Acknowledgement hold time. From $\overline{CS}$ high to RDY low	t_{AKH}	4		12	ns	C_L = 50 pF, R_L = 1 K (Note 1)
12	RDY drive low to HiZ	t_{AKZ}			8	ns	

Note 1: High impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel time taken to discharge C_L.

Note 2: A delay of 500 μs to 2 ms (see Section 11.2 on page 25) must be applied before the first microprocessor access is performed after the $\overline{RESET}$ pin is set high.

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C, VDD_CORE at 1.8 V and VDD_IO at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

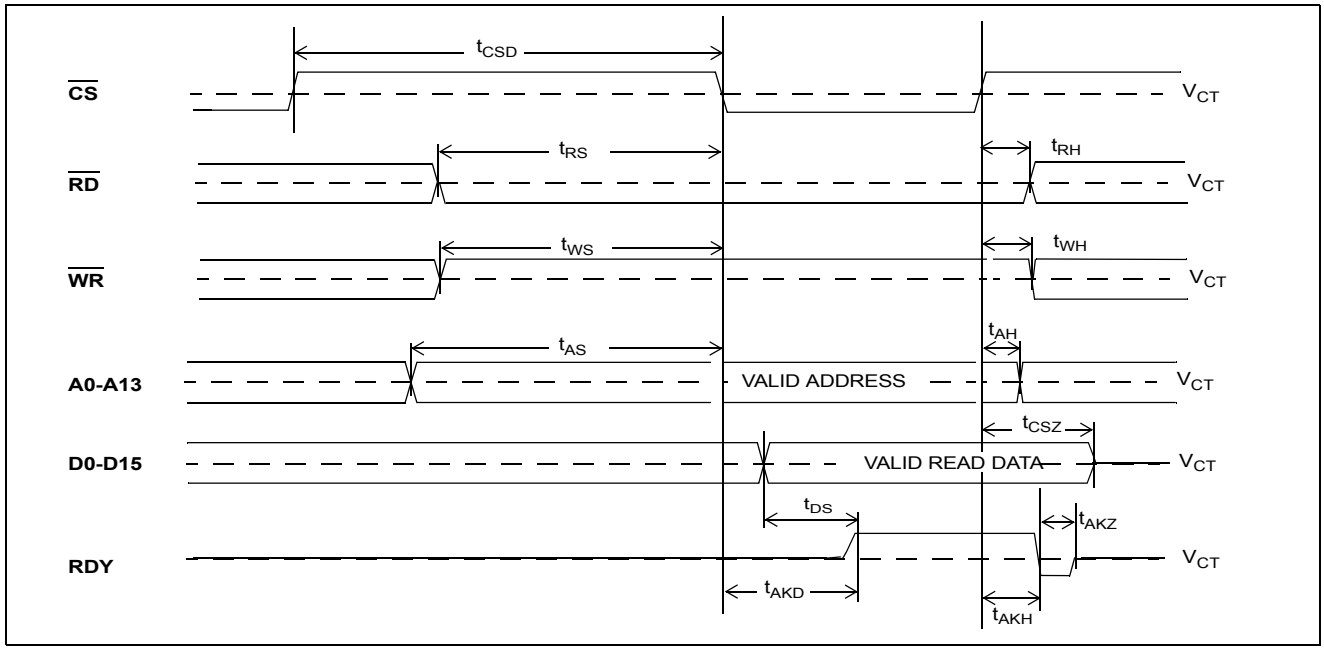


Figure 17 - Intel Non-Multiplexed Bus Timing - Read Access

AC Electrical Characteristics† - Intel Non-Multiplexed Bus Mode - Write Access

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions[2]
1	$\overline{CS}$ de-asserted time	t_{CSD}	15			ns	
2	$\overline{WR}$ setup to $\overline{CS}$ falling	t_{WS}	10			ns	
3	$\overline{RD}$ setup to $\overline{CS}$ falling	t_{RS}	10			ns	
4	Address setup to $\overline{CS}$ falling	t_{AS}	5			ns	
5	Data setup to $\overline{CS}$ falling	t_{DS}	0			ns	C_L = 50 pF
6	$\overline{WR}$ hold after $\overline{CS}$ rising	t_{WH}	0			ns	
7	$\overline{RD}$ hold after $\overline{CS}$ rising	t_{RH}	0			ns	
8	Address hold after $\overline{CS}$ rising	t_{AH}	10			ns	
9	Data hold after $\overline{CS}$ rising	t_{DH}	5			ns	C_L = 50 pF, R_L = 1 K (Note 1)
10	Acknowledgement delay time. From $\overline{CS}$ low to RDY high: Registers Memory	t_{AKD}			 55 150	 ns ns	 C_L = 50 pF C_L = 50 pF
11	Acknowledgement hold time. From $\overline{CS}$ high to RDY low	t_{AKH}	4		12	ns	C_L = 50 pF, R_L = 1 K (Note 1)
12	RDY drive low to HiZ	t_{AKZ}			8	ns	

Note 1: High impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel time taken to discharge C_L.

Note 2: A delay of 500 µs to 2 ms (Section 11.2 on page 25) must be applied before the first microprocessor access is performed after the $\overline{RESET}$ pin is set high.

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C, VDD_CORE at 1.8 V and VDD_IO at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

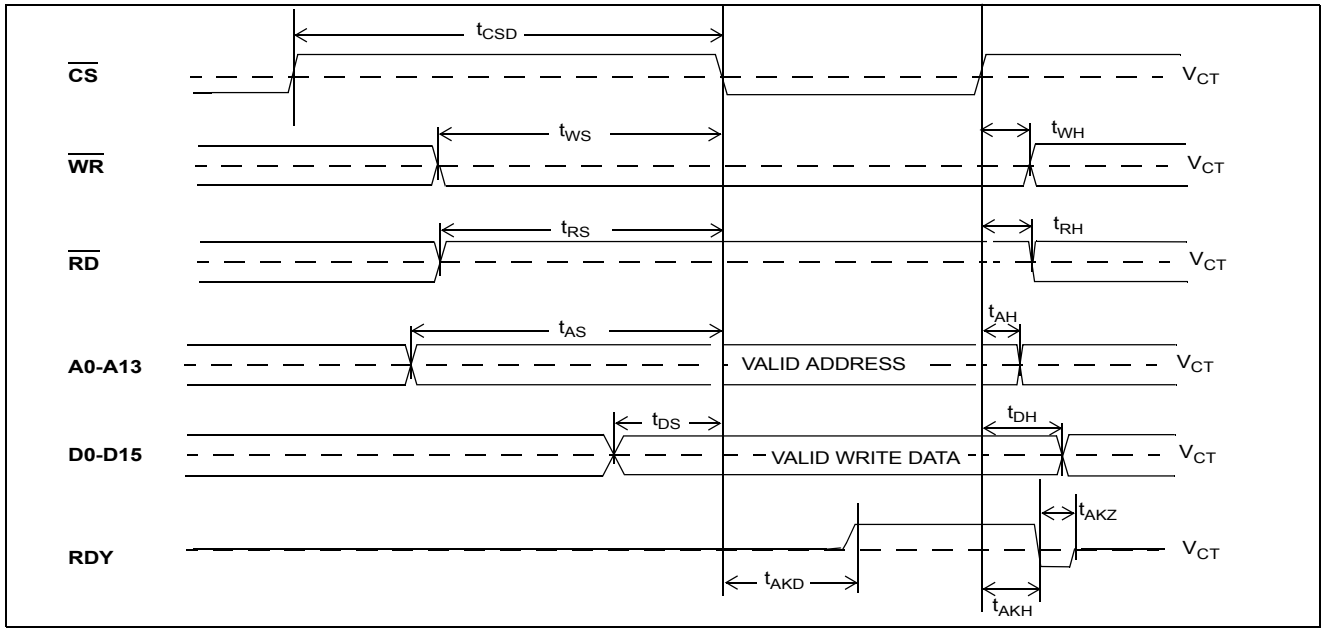


Figure 18 - Intel Non-Multiplexed Bus Timing - Write Access

AC Electrical Characteristics† - JTAG Test Port Timing

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	TCK Clock Period	t_{TCKP}	100			ns	
2	TCK Clock Pulse Width High	t_{TCKH}	20			ns	
3	TCK Clock Pulse Width Low	t_{TCKL}	20			ns	
4	TMS Set-up Time	t_{TMSS}	10			ns	
5	TMS Hold Time	t_{TMSH}	10			ns	
6	TDi Input Set-up Time	t_{TDIS}	20			ns	
7	TDi Input Hold Time	t_{TDIH}	60			ns	
8	TDo Output Delay	t_{TDOD}			30	ns	C_L = 30 pF
9	$\overline{\text{TRST}}$ pulse width	t_{TRSTW}	200			ns	

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C, VDD_CORE at 1.8 V and VDD_IO at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

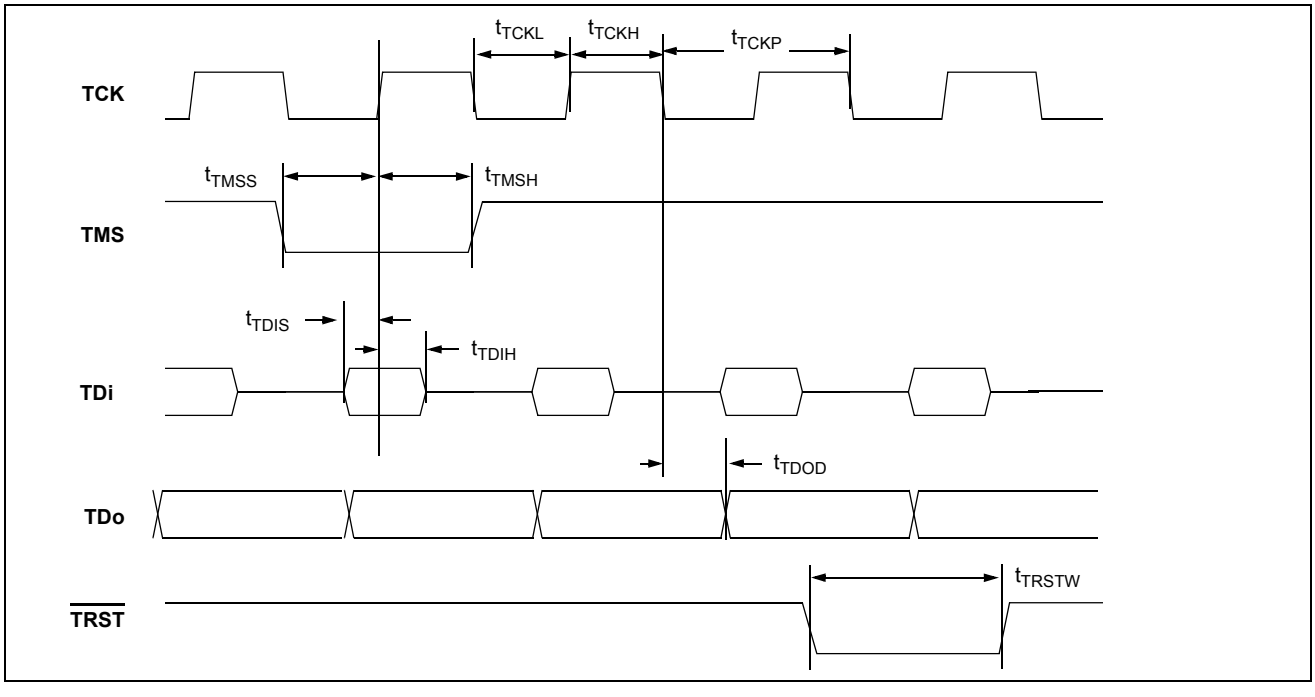


Figure 19 - JTAG Test Port Timing Diagram

AC Electrical Characteristics† - FPi and CKi Timing when CKIN1-0 bits = 00 (16.384 MHz)

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	FPi Input Frame Pulse Width	t_{FPIW}	40	61	115	ns	
2	FPi Input Frame Pulse Setup Time	t_{FPIS}	20			ns	
3	FPi Input Frame Pulse Hold Time	t_{FPIH}	20			ns	
4	CKi Input Clock Period	t_{CKIP}	55	61	67	ns	
5	CKi Input Clock High Time	t_{CKIH}	27		34	ns	
6	CKi Input Clock Low Time	t_{CKIL}	27		34	ns	
7	CKi Input Clock Rise/Fall Time	t_rCKi, t_fCKi			3	ns	
8	CKi Input Clock Cycle to Cycle Variation	t_{CVC}	0		20	ns	

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C, VDD_CORE at 1.8 V and VDD_IO at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics† - FPi and CKi Timing when CKIN1-0 bits = 01 (8.192 MHz)

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	FPi Input Frame Pulse Width	t_{FPIW}	90	122	220	ns	
2	FPi Input Frame Pulse Setup Time	t_{FPIS}	45			ns	
3	FPi Input Frame Pulse Hold Time	t_{FPIH}	45			ns	
4	CKi Input Clock Period	t_{CKIP}	110	122	135	ns	
5	CKi Input Clock High Time	t_{CKIH}	55		69	ns	
6	CKi Input Clock Low Time	t_{CKIL}	55		69	ns	
7	CKi Input Clock Rise/Fall Time	t_rCKi, t_fCKi			3	ns	
8	CKi Input Clock Cycle to Cycle Variation	t_{CVC}	0		20	ns	

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C, VDD_CORE at 1.8 V and VDD_IO at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics† - FPi and CKi Timing when CKIN1-0 bits = 10 (4.096 MHz)

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	FPi Input Frame Pulse Width	t_{FPIW}	90	244	420	ns	
2	FPi Input Frame Pulse Setup Time	t_{FPIS}	110			ns	
3	FPi Input Frame Pulse Hold Time	t_{FPIH}	110			ns	
4	CKi Input Clock Period	t_{CKIP}	220	244	270	ns	
5	CKi Input Clock High Time	t_{CKIH}	110		135	ns	
6	CKi Input Clock Low Time	t_{CKIL}	110		135	ns	
7	CKi Input Clock Rise/Fall Time	t_rCKi, t_fCKi			3	ns	
8	CKi Input Clock Cycle to Cycle Variation	t_{CVC}	0		20	ns	

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C, VDD_CORE at 1.8 V and VDD_IO at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

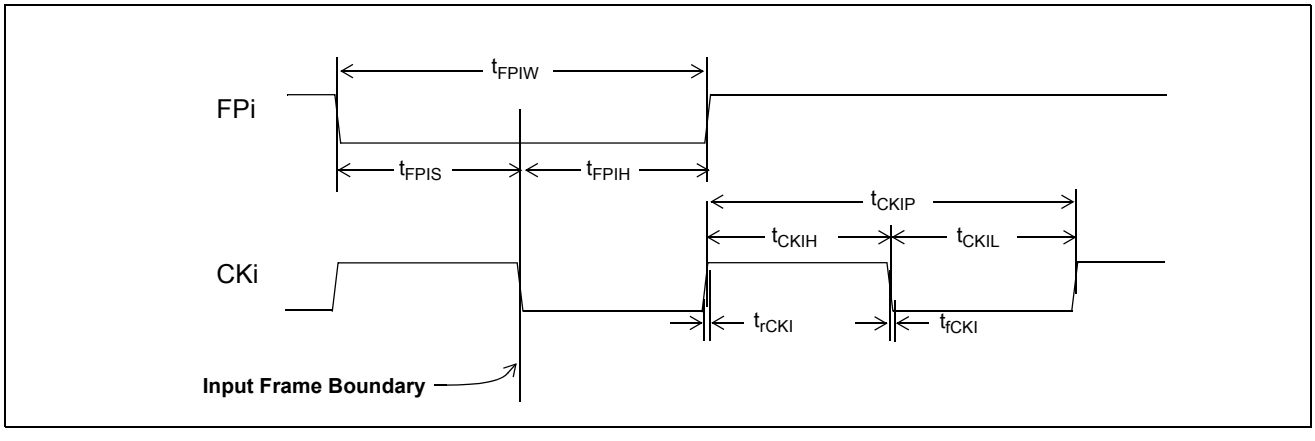


Figure 20 - Frame Pulse Input and Clock Input Timing Diagram (ST-BUS)

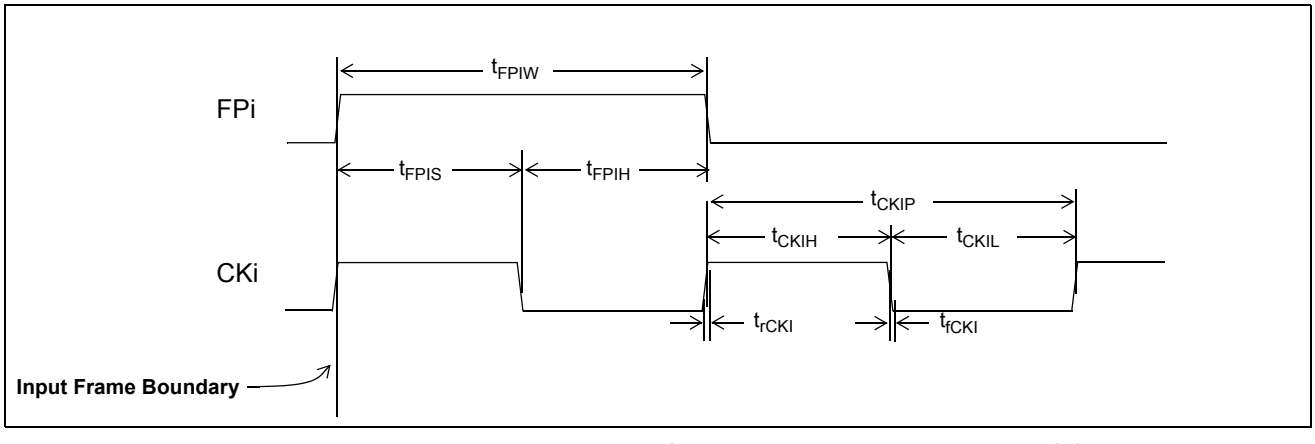


Figure 21 - Frame Pulse Input and Clock Input Timing Diagram (GCI-Bus)

AC Electrical Characteristics† - ST-BUS/GCI-Bus Input Timing

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	STi Setup Time 2.048 Mbps 4.096 Mbps 8.192 Mbps 16.384 Mbps	 t_{SIS2} t_{SIS4} t_{SIS8} t_{SIS16}	 5 5 5 5			 ns ns ns ns	
2	STi Hold Time 2.048 Mbps 4.096 Mbps 8.192 Mbps 16.384 Mbps	 t_{SIH2} t_{SIH4} t_{SIH8} t_{SIH16}	 8 8 8 8			 ns ns ns ns	
3	STio Delay - Active to Active @2.048 Mbps @4.096 Mbps @8.192 Mbps @16.384 Mbps	 t_{SOD2} t_{SOD4} t_{SOD8} t_{SOD16}	 -6 -6 -6 -6		 0 0 0 0	 ns ns ns ns	C_L = 30 pF
4	STio Delay - Active to High-Z STio Delay - High-Z to Active 2.048 Mbps 4.096 Mbps 8.192 Mbps 16.384 Mbps	t_{DZ} t_{ZD}	 -8 -8 -8 -8		 0 0 0 0	 ns ns ns ns	R_L = 1 k, C_L = 30 pF, See Note 1.
5	Output Drive Enable (ODE) Delay - High-Z to Active	t_{ZD_ODE}			260	ns	
6	Output Drive Enable (ODE) Delay - Active to High-Z	t_{DZ_ODE}			260	ns	

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C, VDD_CORE at 1.8 V and VDD_IO at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

Note 1: High impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel the time taken to discharge C_L.

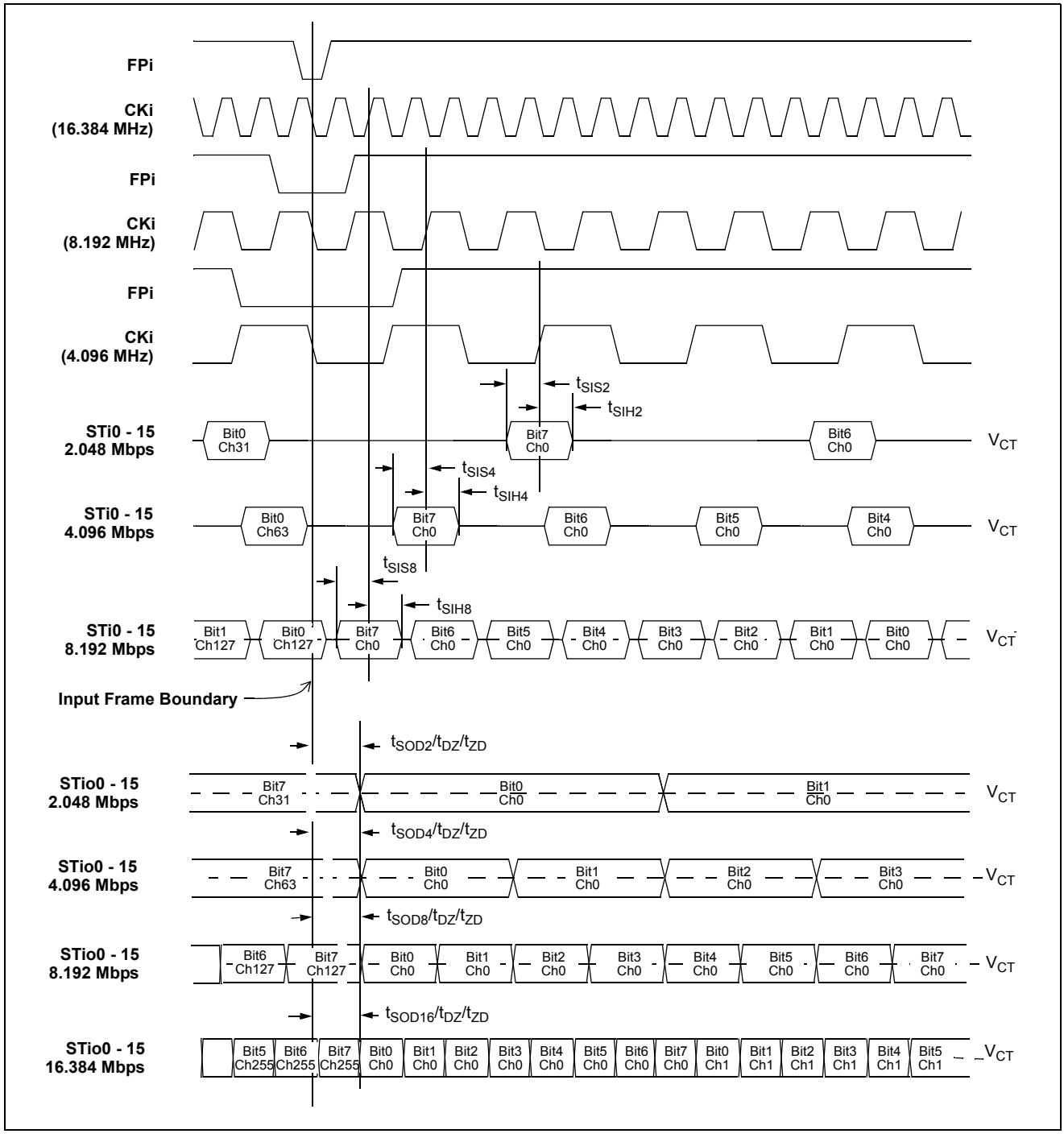


Figure 22 - ST-BUS Input and Output Timing Diagram when Operated at 2, 4, 8 and 16 Mbps

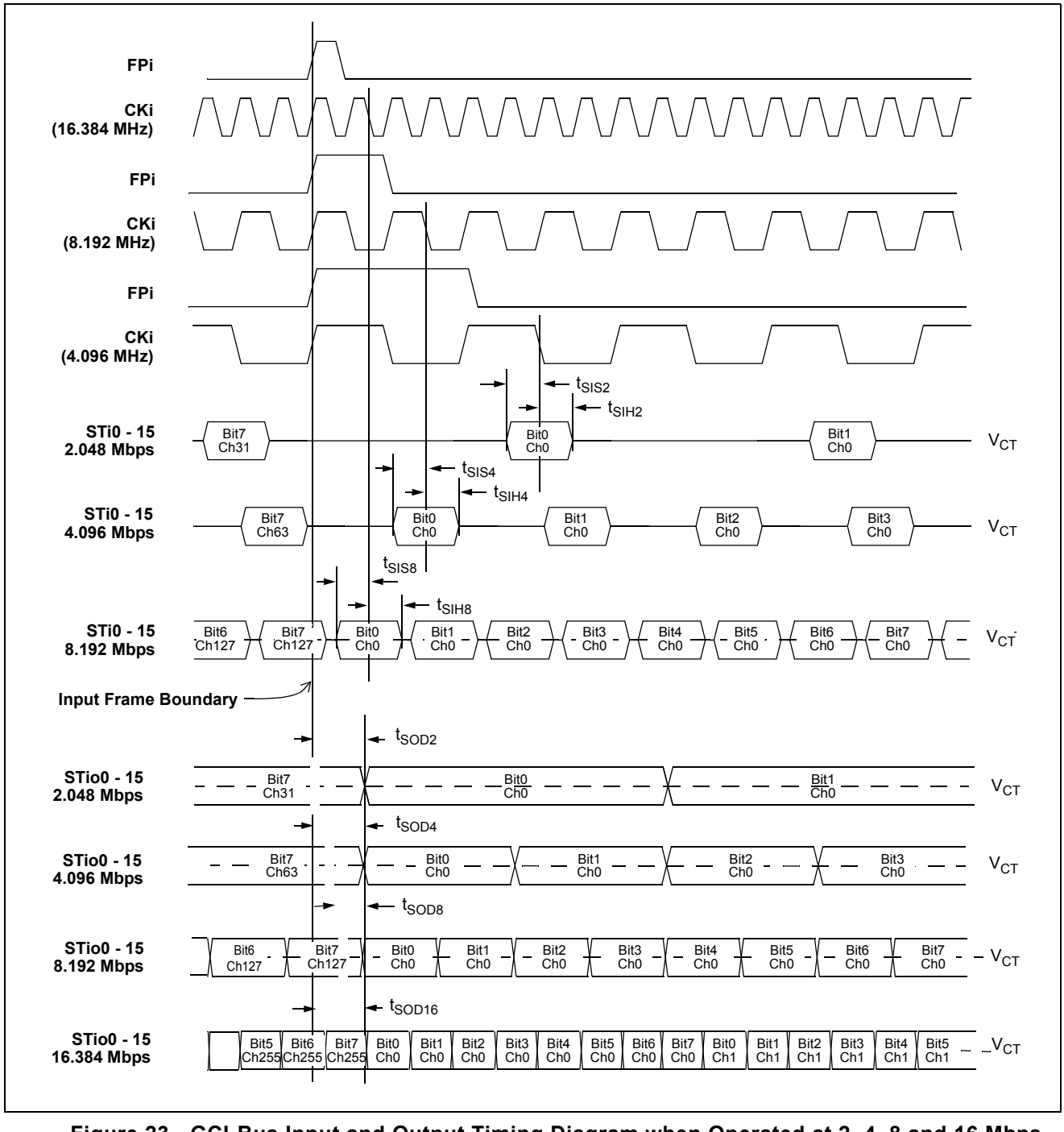
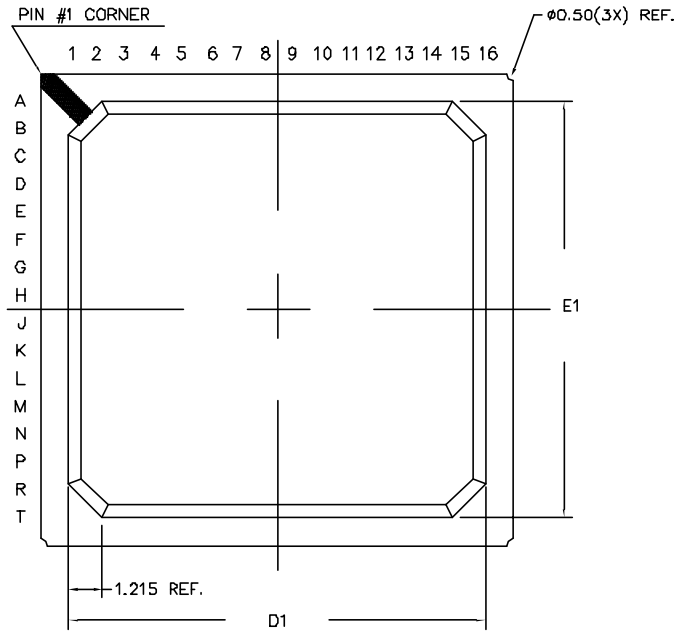
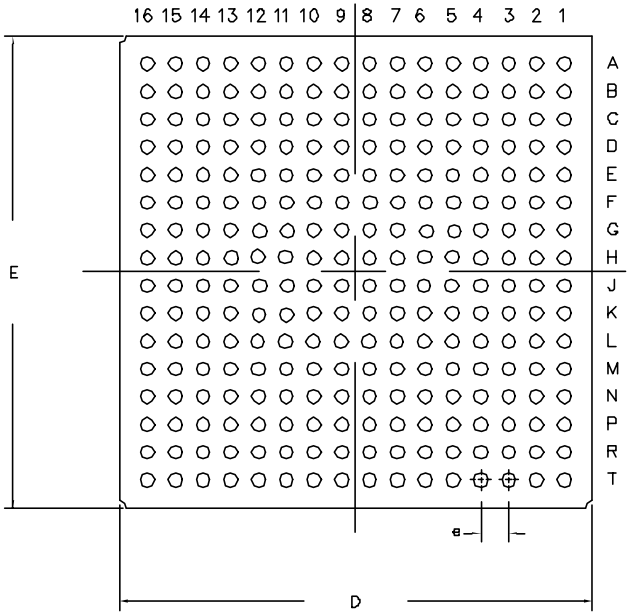


Figure 23 - GCI-Bus Input and Output Timing Diagram when Operated at 2, 4, 8 and 16 Mbps

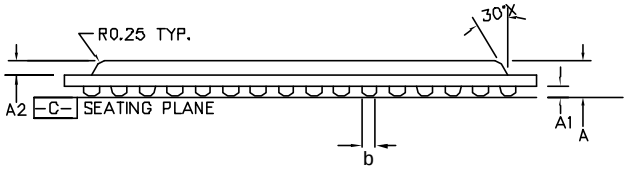
TOP VIEW



BOTTOM VIEW



DIMENSION	MIN	MAX
A	1.42	1.80
A1	0.30	0.50
A2	0.85 REF	
D	16.80	17.20
D1	14.80	15.20
E	16.80	17.20
E1	14.80	15.20
b	0.40	0.60
e	1.00	
N	256	
Conforms to JEDEC MS-034		



SIDE VIEW

NOTES: –
1. Controlling dimensions are in MM.
2. Seating plane is defined by the spherical crown of the solder balls.
3. Not to scale.
4. N is the number of solder balls
5. Substrate thickness is 0.36 MM.

ISSUE	1			
ACN	214440			
DATE	26June03			
APPRD.				

ZARLINK SEMICONDUCTOR

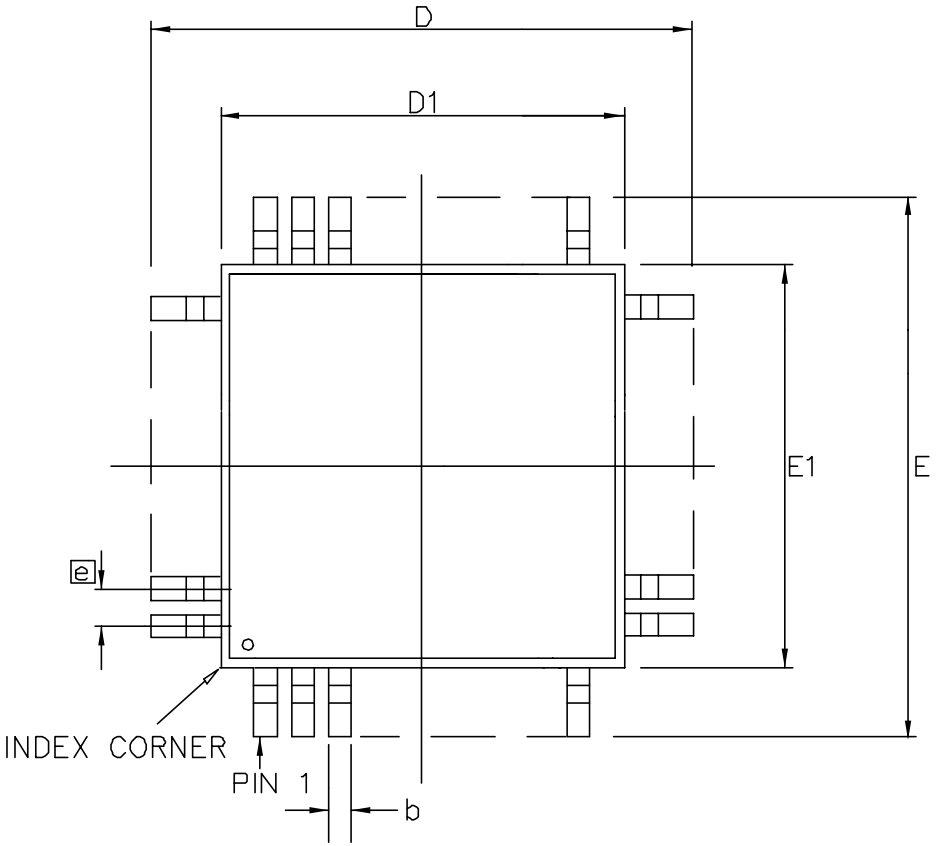
Previous package codes

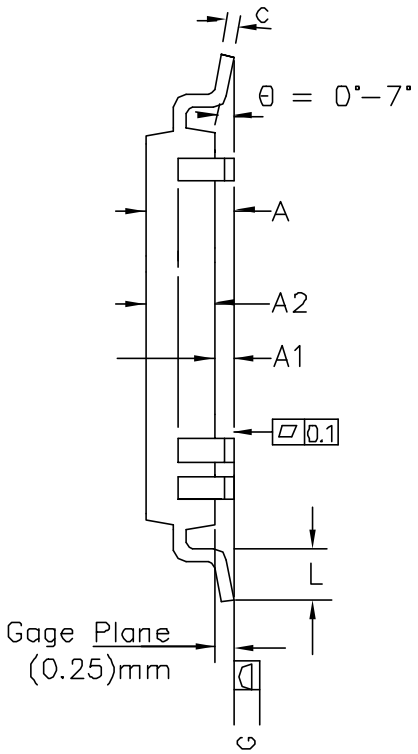
BP/G

Package Code GA

Package Outline for
256ball BGA
17x17x1.61mm

GPD00842





Symbol	Control Dimensions in millimetres			Altern. Dimensions in inches	
	MIN	MAX		MIN	MAX
A	—	1.60		—	0.063
A1	0.05	0.15		0.002	0.006
A2	1.35	1.45		0.053	0.057
D	30.00 BSC			1.181 BSC	
D1	28.00 BSC			1.102 BSC	
E	30.00 BSC			1.181 BSC	
E1	28.00 BSC			1.102 BSC	
L	0.45	0.75		0.018	0.029
e	0.40 BSC			0.016 BSC	
b	0.13	0.23		0.005	0.009
c	0.09	0.20		0.003	0.008
	Pin features				
N	256				
ND	64				
NE	64				
NOTE	SQUARE				

Conforms to JEDEC MS–026 BJC Iss. D

Notes:
1. Pin 1 indicator may be a corner chamfer, dot or both, located within a zone of dimension E1/4 x D1/4 from the index corner
2. All dimensioning and tolerancing conform to ANSI Y14.5–1982.
3. Dimensions D1 and E1 do not include mold protrusion – allowable mold protrusion is 0.254 mm on D1 and E1 dimensions.
4. "N" is the total number of terminals
5. Package top dimensions are smaller than bottom dimensions and top of package will not overhang bottom of package
6. Dimension b does not include Dambar protrusion.
7. Controlling Dimensions are in Millimeter
8. A1 is defined as the distance from the seating plane to the lowest point of the package body

ISSUE	1	2	3	4
ACN	214172	214382		
DATE	27Mar03	12June03		
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes

GP

Package Code QC

Package Outline for 256 lead LQFP (28 x 28 x 1.4mm) 2.0mm Footprint

GPD00837

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www.zarlink.com

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