AH125

½ W High Linearity InGaP HBT Amplifier

Applications

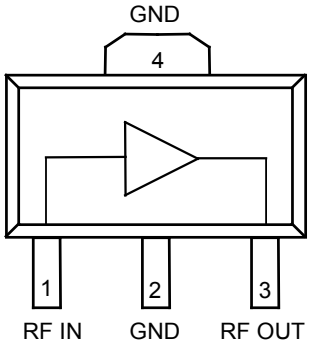
- Repeaters
- Mobile Infrastructure
- LTE / WCDMA / EDGE / CDMA

3-pin SOT-89 Package

Product Features

- 400 − 3600 MHz
- +28 dBm P1dB
- +45 dBm Output IP3
- 16.2 dB Gain @ 2140 MHz
- 150 mA current draw
- +5 V Single Supply
- MTTF > 100 Years
- Lead-free/Green/RoHS-compliant SOT-89 Package
- Class 2 HBM ESD rating (>2kV)

Functional Block Diagram



General Description

The AH125 is a high dynamic range driver amplifier in a low-cost surface mount package. The InGaP/GaAs HBT is able to achieve high performance across a broad range with +45 dBm OIP3 and +28 dBm of compressed 1dB power while drawing 150 mA current. The AH125 is available in a lead-free/green/RoHS-compliant SOT-89 package. All devices are 100% RF and DC tested.

The AH125 is targeted for use as a driver amplifier in wireless infrastructure where high linearity, medium power, and high efficiency are required. Internal biasing allows the AH125 to maintain high linearity over temperature and operate directly off a single +5V supply. This combination makes the device an excellent candidate for transceiver line cards in current and next generation multi-carrier 3G base stations or repeaters.

Pin Configuration

Pin No.	Symbol
1	Vbias
3	RFin
2,4	RFout/Vcc

Not Recommended for New Designs

Recommended Replacement Part: TQP7M9102

Ordering Information

Part No.	Description
AH125-89G	½W High Linearity Amplifier

Standard T/R size = 1000 pieces on a 7” reel.

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−65 to 150°C
RF Input Power, CW, 50Ω, T=25°C	Input P_{10}dB
Device Voltage	+6 V

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Case Temperature	−40		+85	°C
Tj for >10^6 hours MTTF			+200	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: V_{SUPPLY}=+5 V, I_{CQ}=150 mA (typ.), Temp= +25°C, tuned application circuit

Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		400		3600	MHz
Test Frequency			2140		MHz
Gain		14	16.2	18	dB
Input Return Loss			12		dB
Output Return Loss			12		dB
W-CDMA Channel Power	At -50dBc ACLR, Note 1		+19		dBm
Output P1dB			+28		dBm
Output IP3	Pout=+12 dBm/tone, Δf=1 MHz	+41	+45		dBm
Noise Figure			4.4		dB
Quiescent Collector Current		130	150	170	mA
Thermal Resistance, θ_{JC}	Junction to case			64.3	°C / W

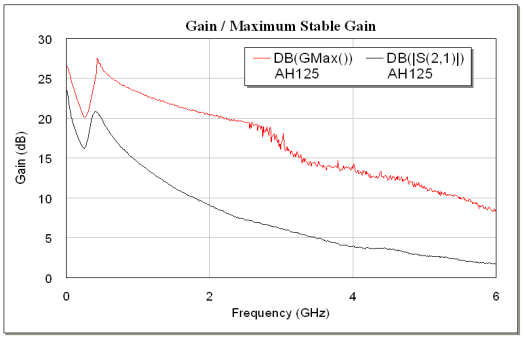
Performance Summary Table

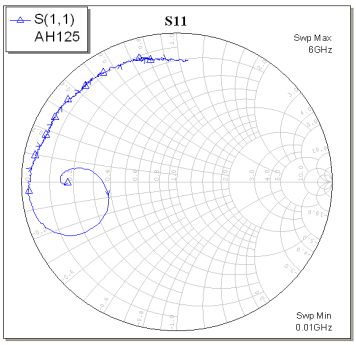
Test conditions unless otherwise noted: V_{SUPPLY}=+5 V, I_{CQ}=150 mA (typ.), Temp= +25°C, tuned application circuit

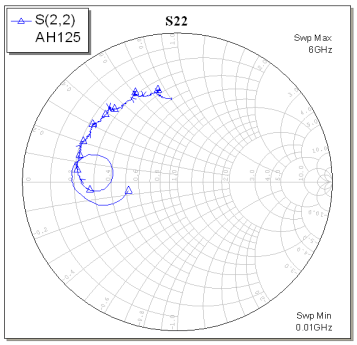
Parameter	Conditions	Typical			Units
Frequency		920	1960	2140	MHz
Gain		20	17	16.2	dB
Input Return Loss		20	16	12	dB
Output Return Loss		9.9	9	12	dB
W-CDMA Channel Power	At -50 dBc ACLR, Note 1	+19	+19	+19	dBm
Output P1dB		+28.1	+27.8	+28.0	dBm
Output IP3	Note 2	+47	+47	+45	dBm
Noise Figure		7.7	4.6	4.4	dB

Notes:
1. W-CDMA 3GPP Test Model 1+64 DPCH, PAR = 10.3 dB at 0.01% Probability, 3.84 MHz.
2. OIP3 is measured with two tones separated by 1 MHz.
   Measured at Pout=+17dBm/tone for 900 MHz, +14 dBm/tone for 1960 MHz, and +12 dBm/tone for 2140 MHz.

Device Characterization Data







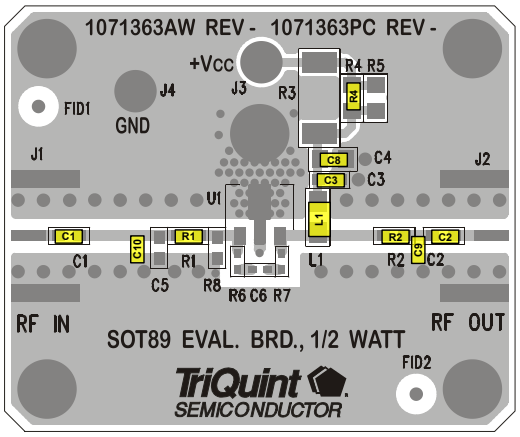
Note:
The gain for the unmatched device in 50 ohm system is shown as the trace in black color. For a tuned circuit for a particular frequency, it is expected that actual gain will be higher, up to the maximum stable gain. The maximum stable gain is shown in the dashed red line.

S-Parameters

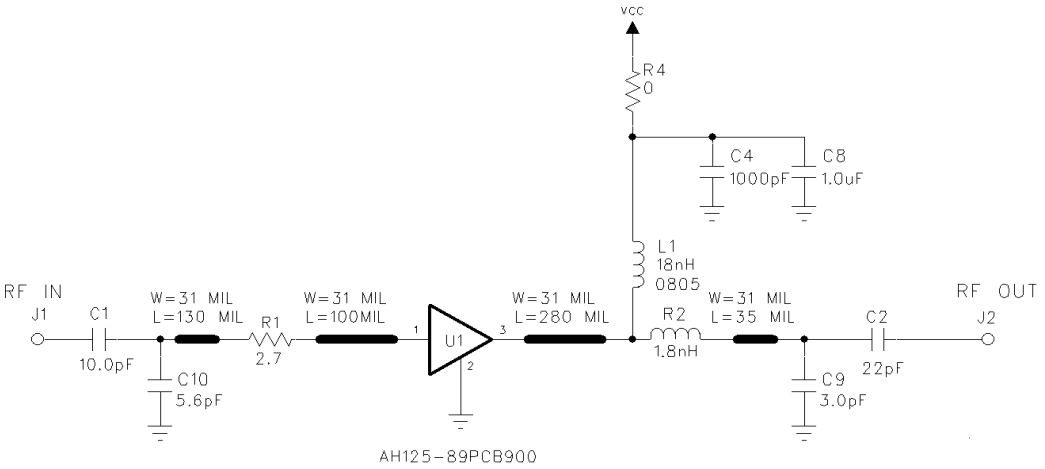
Test Conditions: V_{DEVICE}=+5 V, I_{CQ}=150 mA, T=+25°C, unmatched 50 ohm system

Freq (MHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
100	-2.51	176.96	19.12	153.71	-33.85	-7.98	-4.58	-168.55
300	-6.65	-179.55	16.82	171.45	-41.51	-51.50	-3.50	167.66
500	-0.47	-166.72	19.86	129.11	-32.54	37.90	-6.46	-173.90
700	-0.50	179.58	16.95	110.14	-32.11	15.12	-4.57	-177.11
900	-0.56	173.91	15.09	99.64	-32.29	6.66	-4.14	177.58
1100	-0.65	170.52	13.68	91.32	-32.15	2.53	-3.89	173.40
1300	-0.78	166.87	12.37	83.49	-32.04	-2.50	-3.71	169.83
1500	-0.82	163.90	11.21	76.80	-32.11	-4.03	-3.64	167.10
1700	-0.93	161.34	10.11	71.12	-31.97	-7.89	-3.70	164.08
1900	-0.93	157.61	9.40	64.93	-31.94	-9.93	-3.64	160.19
2100	-0.94	154.21	8.47	58.83	-31.97	-10.87	-3.54	156.60
2300	-0.91	151.59	7.66	53.42	-31.80	-14.20	-3.48	153.92
2500	-0.93	149.24	7.06	49.26	-32.04	-16.18	-3.67	152.18
2700	-0.90	145.94	6.70	43.87	-31.63	-16.91	-3.72	147.67
2900	-0.96	143.87	6.12	39.45	-31.18	-18.50	-3.54	143.63
3100	-1.07	139.90	5.74	34.00	-31.37	-23.47	-3.52	141.32
3300	-1.18	136.50	5.09	29.36	-31.25	-20.88	-3.70	140.24
3500	-1.18	133.80	4.62	24.20	-31.12	-27.12	-3.72	135.07
3700	-1.11	132.39	4.12	20.26	-31.25	-26.33	-3.64	130.47

869-960 MHz Application Circuit



Notes:
1. The primary RF microstrip line is 50 Ω.
2. Components shown on the silkscreen but not on the schematic are not used.
3. 0 Ω jumpers can be replaced with copper trace in target application.
4. The edge of R2 is placed at 280 mil from AH125 RFout pin. (14.3° at 920 MHz)
5. The edge of C9 is placed 35 mil from the edge of R2. (1.8° at 920 MHz)
6. The edge of R1 is placed at 100 mil from AH125 RFin pin. (5.1° at 920 MHz)
7. The edge of C10 is placed 130 mil from the edge of R1. (6.6° at 920 MHz)



Typical Performance 869-960 MHz

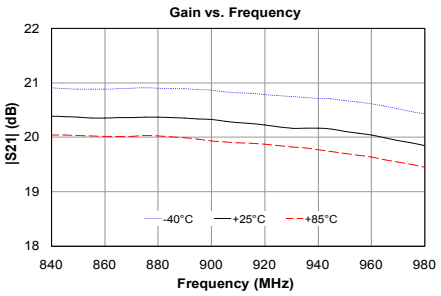
Test conditions unless otherwise noted: V_{SUPPLY}=+5 V, I_{CQ}=150 mA (typ.), Temp= +25°C, tuned application circuit

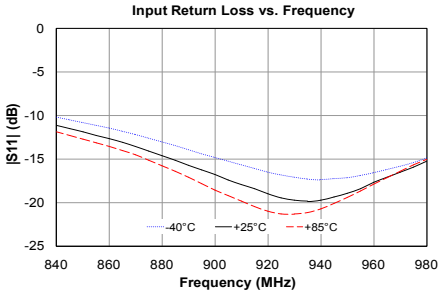
Frequency	Conditions	869	920	960	MHz
Gain		20	20	20	dB
Input Return Loss		14	20	22	dB
Output Return Loss		10	9.9	9.9	dB
ACLR	Pout = +18 dBm, Note 1	-52	-52.5	-52	dBc
Output P1dB		+27.4	+28.1	+27.9	dBm
Output IP3	Pout=+17 dBm/tone, Δf=1 MHz	+44	+47	+49	dBm
Noise Figure		7.9	7.7	7.5	dB

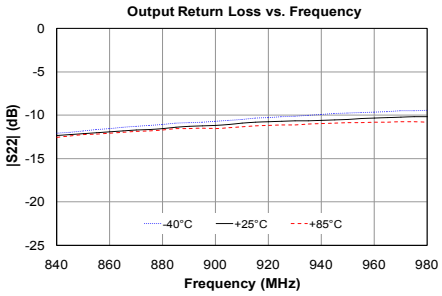
Notes:
1. W-CDMA 3GPP Test Model 1+64 DPCH, PAR = 10.3 dB at 0.01% Probability, 3.84 MHz.

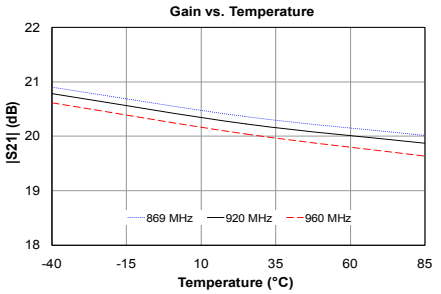
Performance Plots 869-960 MHz

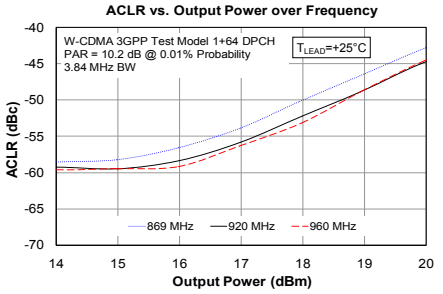
Test conditions unless otherwise noted: V_{SUPPLY}=+5 V, I_{CQ}=150 mA (typ.), Temp= +25°C, tuned application circuit

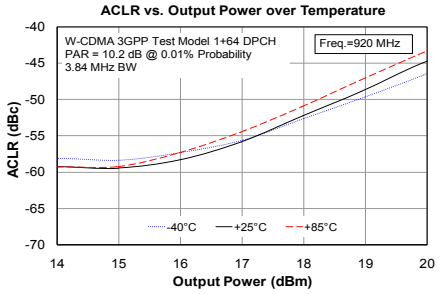


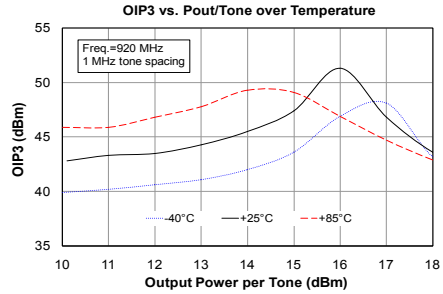


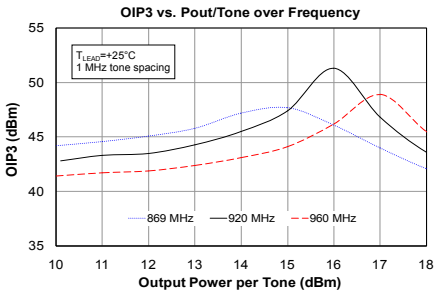


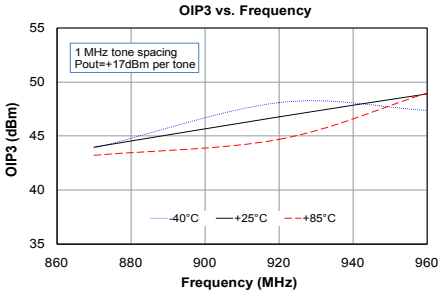


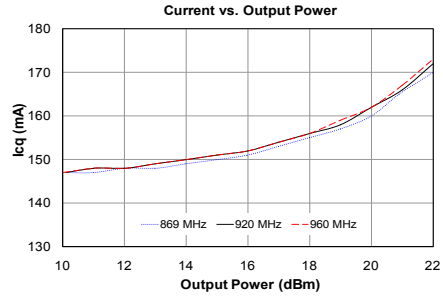


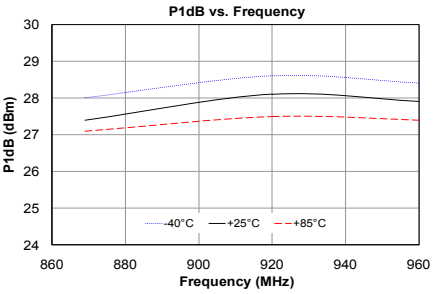


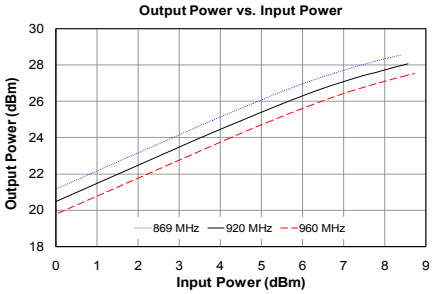


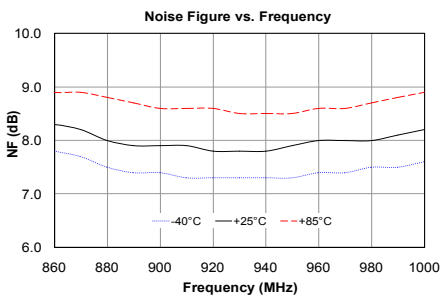




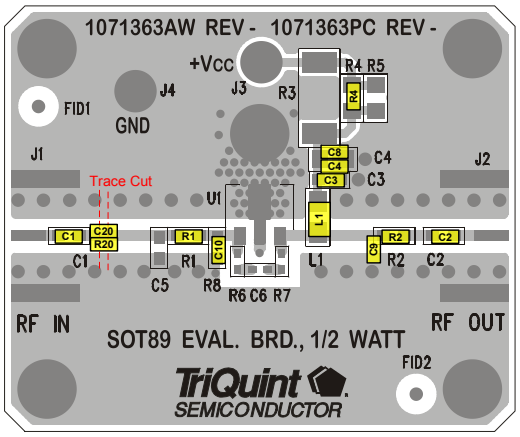




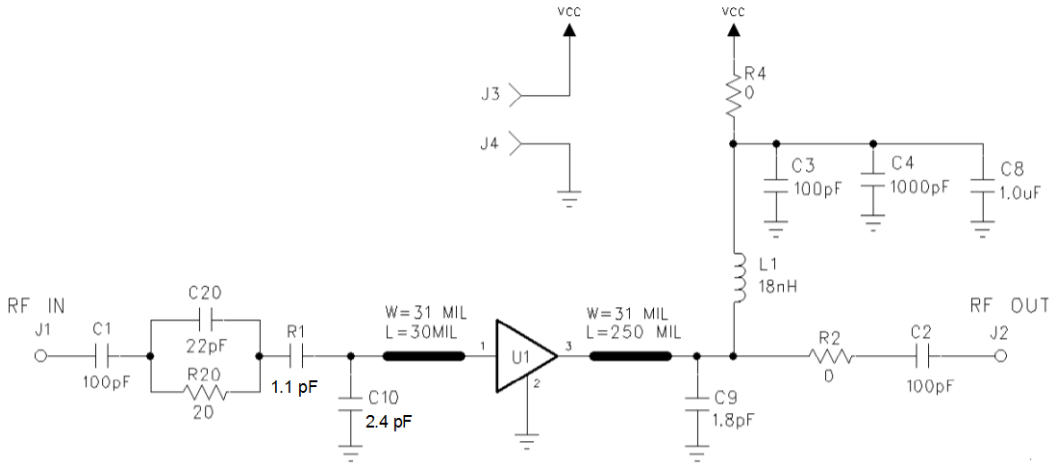




1805-1880 MHz Application Circuit



Notes:
1. The primary RF microstrip line is 50 Ω.
2. Components shown on the silkscreen but not on the schematic are not used.
3. 0 Ω jumpers can be replaced with copper trace in target application.
4. The edge of C9 is placed at 250 mil from AH125 RFout pin. (25.5° at 1845 MHz)
5. The edge of R1 is placed against the edge of C10.
6. The edge of C10 is placed at 30 mil from AH125 RFin pin. (3.1° at 1845 MHz)



Typical Performance 1805-1880 MHz

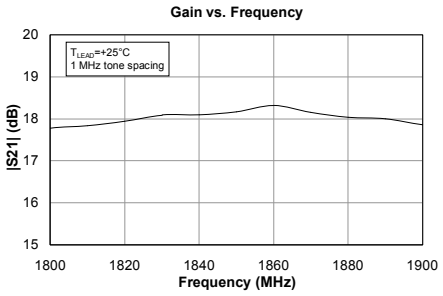
Test conditions unless otherwise noted: V_{SUPPLY}=+5 V, I_{CQ}=150 mA (typ.), Temp= +25°C, tuned application circuit

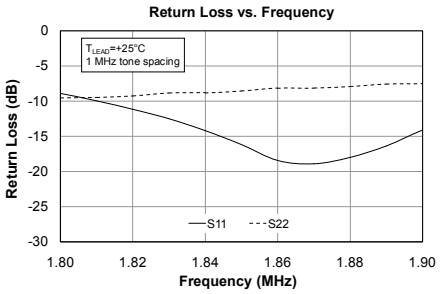
Frequency	Conditions	1805	1842	1880	MHz
Gain		17.8	18.2	18.1	dB
Input Return Loss		9.5	16.5	17.0	dB
Output Return Loss		9.4	8.4	7.8	dB
ACLR	Pout = +18 dBm, Note 1	-51	-51	-49	dBc
Output P1dB		+28	+27.9	+27.8	dBm
Output IP3	Pout=+14 dBm/tone, Δf=1 MHz	+44	+45	+43.5	dBm

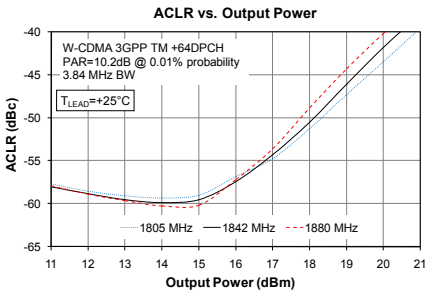
Notes:
1. W-CDMA 3GPP Test Model 1+64 DPCH, PAR = 10.3 dB at 0.01% Probability, 3.84 MHz.

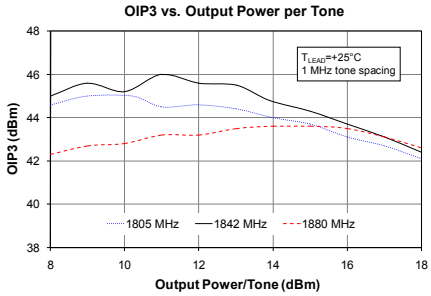
Performance Plots 1805-1880 MHz

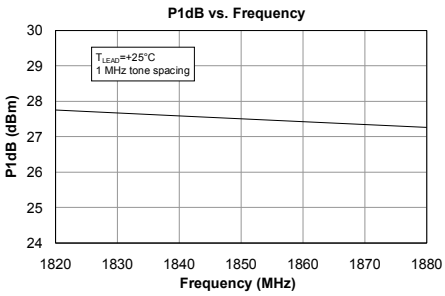
Test conditions unless otherwise noted: V_{SUPPLY}=+5 V, I_{CQ}=150 mA (typ.), Temp= +25°C, tuned application circuit



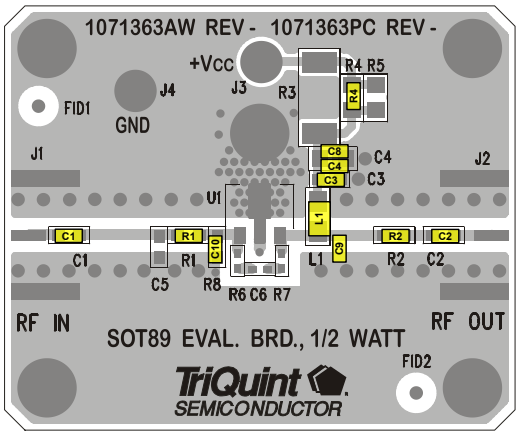




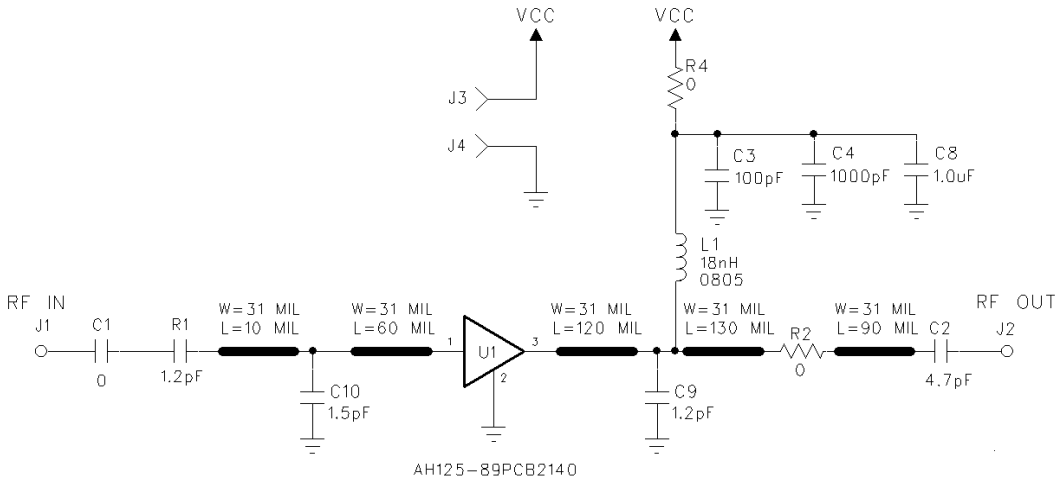




2110-2170 MHz Application Circuit



Notes:
1. The primary RF microstrip line is 50 Ω.
2. Components shown on the silkscreen but not on the schematic are not used.
3. 0 Ω jumpers can be replaced with copper trace in target application.
4. The edge of C9 is placed at 120 mils from AH125 RFout pin. (14.2° at 2140 MHz)
5. The edge of C2 is placed at 280 mils from the edge of C9. (33.2° at 2140 MHz)
6. The edge of C10 is placed at 60 mils from AH125 RFin pin. (7.1° at 2140 MHz)
7. The edge of R1 is placed 10 mils from the edge of C10. (1.2° at 2140 MHz)



Typical Performance 2110-2170 MHz

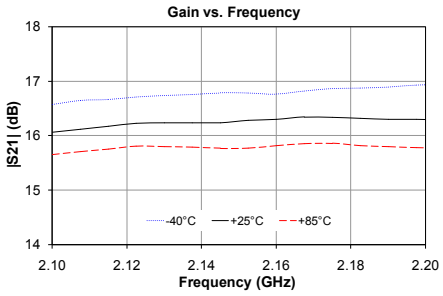
Test conditions unless otherwise noted: V_{SUPPLY}=+5 V, I_{CQ}=150 mA (typ.), Temp= +25°C, tuned application circuit

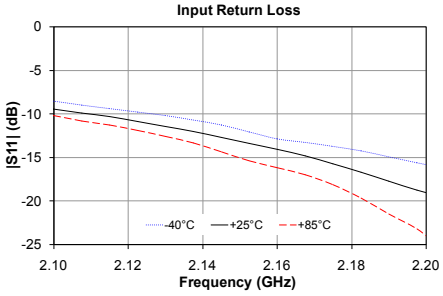
Frequency	Conditions	2110	2140	2170	MHz
Gain		16.1	16.2	16.3	dB
Input Return Loss		10	12	15	dB
Output Return Loss		13	12	11	dB
ACLR	Pout = +18 dBm	-52	-52	-52	dBc
Output P1dB		+28	+28	+28	dBm
Output IP3	Pout=+12 dBm/tone, Δf=1 MHz	+49	+45	+47	dBm
Noise Figure		4.3	4.4	4.4	dB

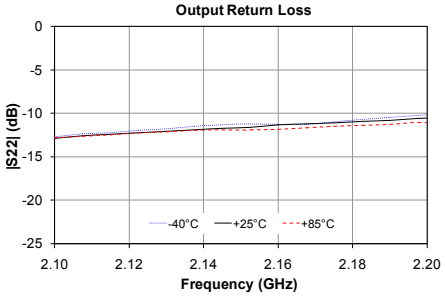
Notes:
1. TD-SCDMA 3 Carrier, PAR = 10 dB @ 0.01% Probability, 1.28 MHz BW

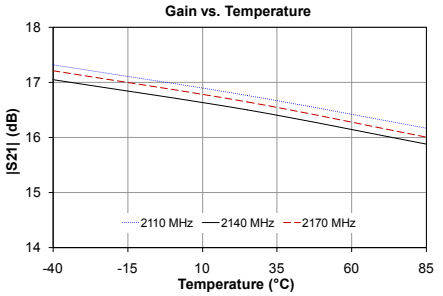
Performance Plots 2110-2170 MHz

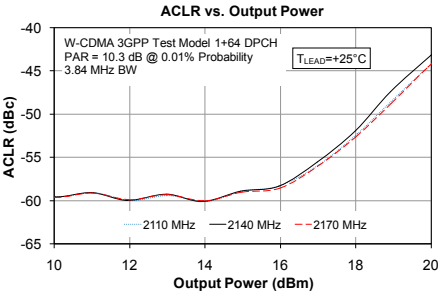
Test conditions unless otherwise noted: V_{SUPPLY}=+5 V, I_{CQ}=150 mA (typ.), Temp= +25°C, tuned application circuit

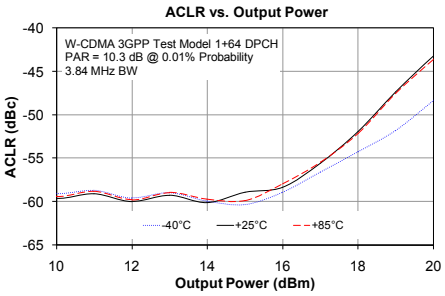


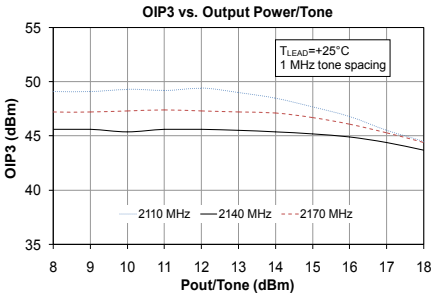


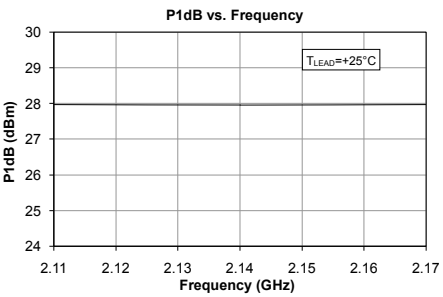


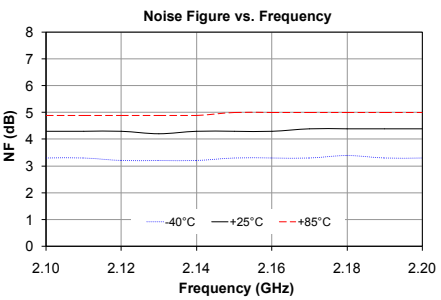




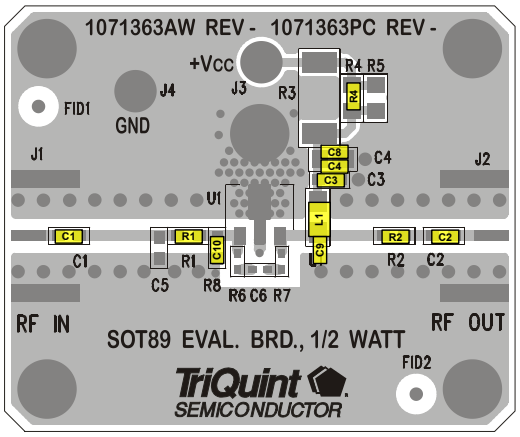






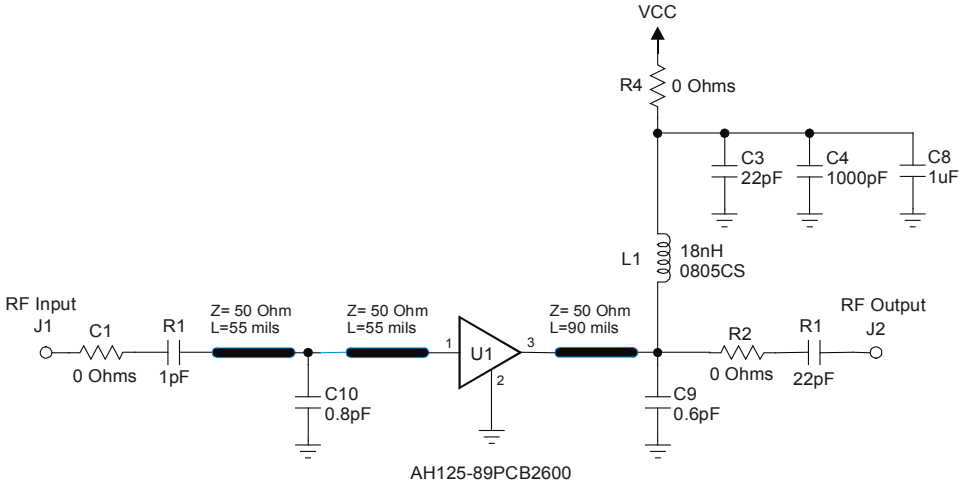


2500-2700 MHz Application Circuit



Notes:

1. The primary RF microstrip line is 50 Ω.
2. Components shown on the silkscreen but not on the schematic are not used.
3. 0 Ω jumpers can be replaced with copper trace in target application.
4. Distance from side edge of C10 to side edge of U1 pin 1 is 55 mils (7.9° at 2600 MHz).
5. Distance from end edge of R1 to side edge of U1 pin 1 is 110 mils (15.8° at 2600 MHz).
6. Distance from side edge of C9 to side edge of U1 pin 3 is 90 mils (13.0° at 2600 MHz).



AH125-89PCB2600

Typical Performance 2500-2700 MHz

Test conditions unless otherwise noted: V_{SUPPLY}=+5 V, I_{CQ}=150 mA (typ.), Temp= +25°C, tuned application circuit

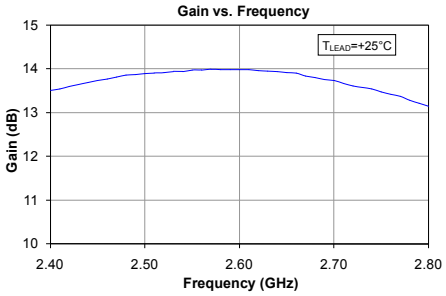
Frequency	Conditions	2500	2600	2700	MHz
Gain		13.9	14.0	13.7	dB
Input Return Loss		9.5	13.1	12.9	dB
Output Return Loss		9.4	8.7	8.2	dB
EVM	Pout = +19 dBm	1.5	1.25	1.3	%
Output P1dB		+28	+28	+28	dBm
Output IP3	Pout=+16 dBm/tone, Δf=1 MHz	+49	+48	+47	dBm

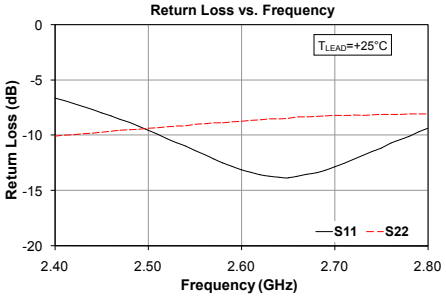
Notes:

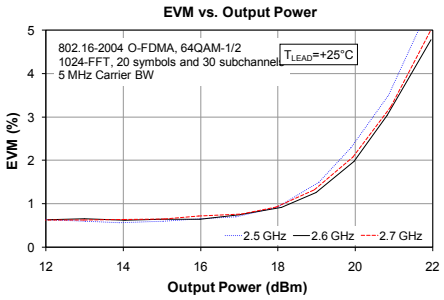
1. 802.16-2004 O-FDMA, 64QAM-1/2, 1024-FFT, 20 symbols and 30 sub-channels, 5 MHz Carrier BW.

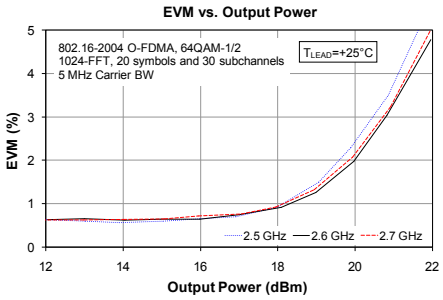
Performance Plots 2500-2700 MHz

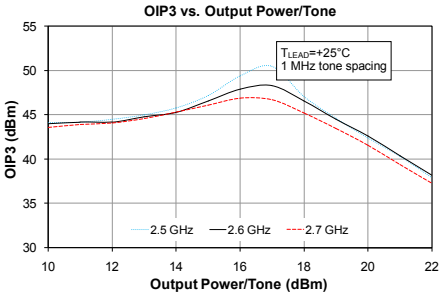
Test conditions unless otherwise noted: V_{SUPPLY}=+5 V, I_{CQ}=150 mA (typ.), Temp= +25°C, tuned application circuit



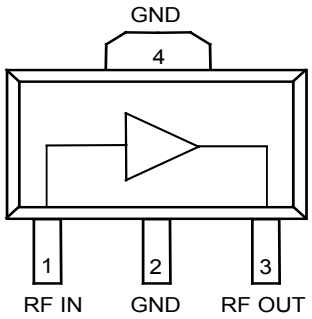








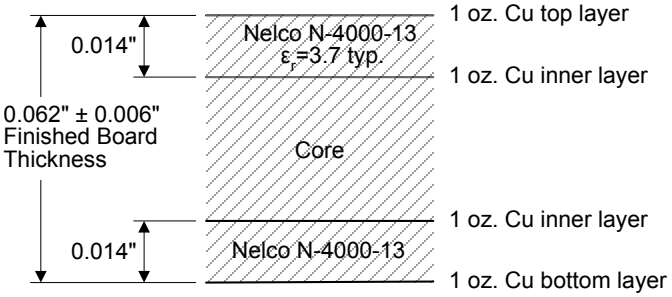
Pin Configuration and Description



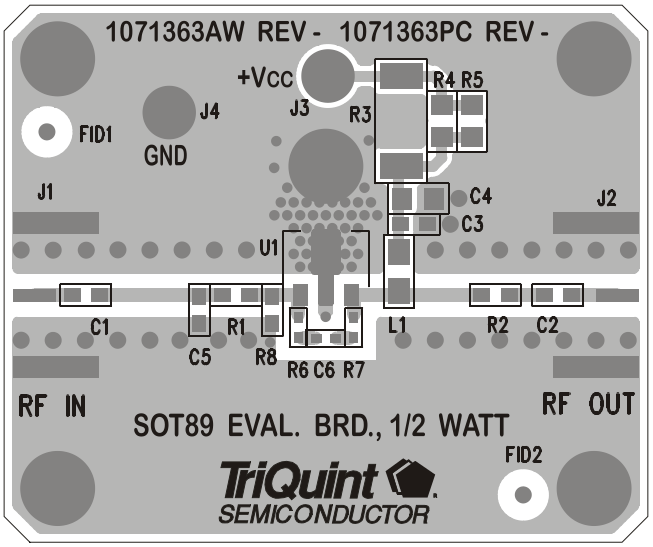
Pin No.	Symbol	Description
1	RF IN	RF Input. Requires external match for optimal performance. External DC Block required.
2, 4	GND	RF/DC Ground Connection
3	RFout / Vcc	RF Output. Requires external match for optimal performance. External DC Block and supply voltage is required.

Evaluation Board PCB Information

TriQuint PCB 1071363 Material and Stack-up

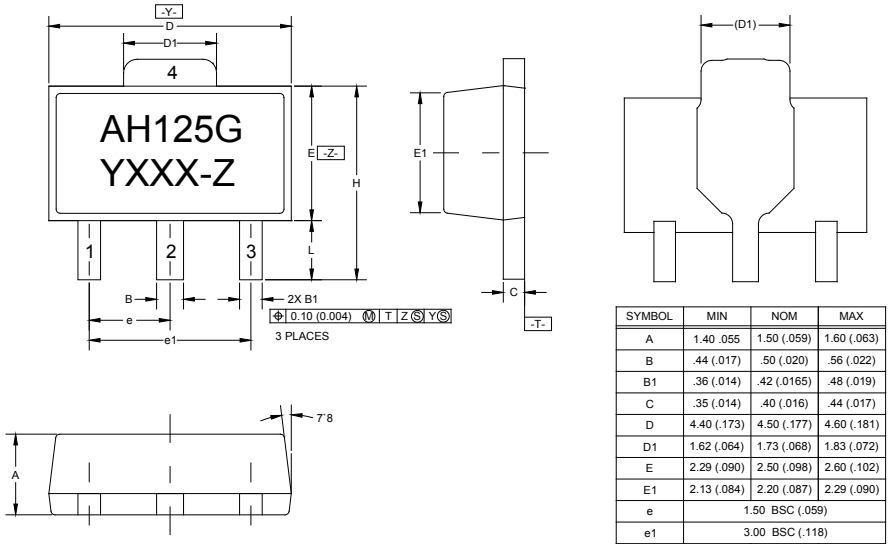


50 Ohm Lines: Width=28 mils
Spacing=28 mils



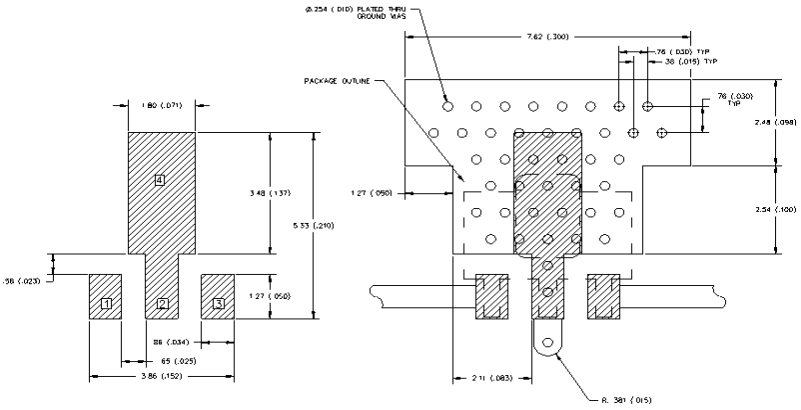
Package Marking and Dimensions

The AH125 will be marked with an "AH125G" designator with a lot code marked below the part designator. The "Y" represents the last digit of the year the part was manufactured, the "XXX" is an auto-generated number, and "Z" refers to a wafer number in a batch.



SYMBOL	MIN	NOM	MAX
A	1.40 .055	1.50 (.059)	1.60 (.063)
B	.44 (.017)	.50 (.020)	.56 (.022)
B1	.36 (.014)	.42 (.0165)	.48 (.019)
C	.35 (.014)	.40 (.016)	.44 (.017)
D	4.40 (.173)	4.50 (.177)	4.60 (.181)
D1	1.62 (.064)	1.73 (.068)	1.83 (.072)
E	2.29 (.090)	2.50 (.098)	2.60 (.102)
E1	2.13 (.084)	2.20 (.087)	2.29 (.090)
e	1.50 BSC (.059)		
e1	3.00 BSC (.118)		
H	3.94 (.155)	4.10 (.161)	4.25 (.167)
L	.89 (.035)	1.10 (.043)	1.20 (.047)

PCB Mounting Pattern



Notes:

1. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010").
2. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.
3. RF trace width depends upon the PC board material and construction.
4. Use 1 oz. Copper minimum.
5. All dimensions are in millimeters (inches). Angles are in degrees.

Product Compliance Information

ESD Sensitivity Ratings

Caution! ESD-Sensitive Device

ESD Rating: Class 2
Value: ⩾2000V to <4000V
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

ESD Rating: Class IV
Value: Passes ≥ 2000V min
Test: Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101

MSL Rating

MSL Rating: 3
Test: +260°C convection reflow
Standard: JEDEC standard IPC/JEDEC J-STD-020

Solderability

Compatible with both lead-free (maximum 260 °C reflow temperature) and leaded (maximum 245 °C reflow temperature) soldering processes.

Package lead plating: NiPdAu

RoHs Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

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Email: info-sales@triquint.com **Fax:** +1.503.615.8902

For technical questions and application information:

Email: sjcapplications.engineering@triquint.com

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