AN11054

GreenChip III+ SSL4101 integrated PFC and flyback controller

Rev. 1 — 13 May 2011 Application note

Document information

Info	Content
Keywords	GreenChip III+, SSL4101, PFC, flyback, high-efficiency, LED driver, adapter, notebook, PC Power, low THD, high Power Factor (PF).
Abstract	The SSL4101 is a member of the new generation of combined PFC and flyback controller ICs for efficient switched mode power supplies. It has a high level of integration which allows the design of a cost effective power supply with a very low number of external components. The SSL4101 is fabricated in a Silicon On Insulator (SOI) process. The NXP Semiconductors SOI process makes a wide voltage range possible.

Revision history

Rev	Date	Description
v.1	20110513	first issue

Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

1. Introduction

The SSL4101 is a combination IC with both a Power Factor Controller (PFC) and a flyback controller integrated into an SO16 package. Both controllers operate in Quasi-Resonant (QR) or Discontinuous Conduction Mode (DCM) mode with valley detection. Switching is independent for each controller.

The PFC output power is an on-time controlled for simplicity. It is not necessary to sense the phase of the mains voltage. The flyback output power is Current Controlled Mode (CCM) ensuring good suppression of the input voltage ripple.

The communication circuitry between both controllers is integrated and no adjustment is needed.

The voltage and current levels mentioned in this application note are typical values. A detailed description of the pin level spreading can be found in the *SSL4101 data sheet*.

1.1 Scope

This application note describes the functionality and the control functions of SSL4101 and the adjustments needed within the power controller application.

The design and data for the inductor and transformer for the large signal parts of the PFC and flyback power stages are dealt with in a separate application note.

1.2 The SSL4101 GreenChip III+ controller

The features of the GreenChip III+ allow the power supply engineer to design a reliable, cost-effective and efficient Switched Mode Power Supply (SMPS) with the minimum number of external components.

1.2.1 Key features

- PFC and flyback controller integrated in one SO16 package
- Switching frequency of PFC and flyback are independent of each other
- No external hardware required for communication between the two controllers
- High level of integration, resulting in a very low external component count
- Integrated Mains voltage enable and brown-out protection
- Fast latch reset function

1.2.2 System features

- Safe Restart mode for system fault conditions
- High voltage start-up current source (5.4 mA)
- Reduction of HV current source (1 mA) in Safe restart mode
- Wide V_{CC} range (up to 38 V)
- MOSFET driver voltage limited
- Easily controlled start-up behavior and V_{CC} circuit
- General purpose input for latched protection
- Internal IC OverTemperature Protection (OTP)

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

- Two high voltage spacers between the HV pin and the next active pin
- Open pin protection on the VINSENSE, VOSENSE, PFCAUX, FBCTRL and FBAUX pins

1.2.3 PFC features

- QR/DCM operation with valley switching
- t_{on} controlled
- Mains input voltage compensation of the control loop for good transient response
- OverCurrent Protection (OCP)
- Soft-start and soft-stop
- Open/short detection for PFC feedback loop: no external OVP circuit necessary

1.2.4 Flyback features

- QR/DCM operation with valley switching
- Frequency limitation (125 kHz) to reduce switching losses and EMI
- Current Controlled Mode (CCM)
- OverCurrent Protection (OCP)
- Frequency reduction with fixed minimum peak current to maintain high-efficiency at low output power levels without audible noise
- Soft-start function
- Accurate OverVoltage Protection (OVP) through the auxiliary winding
- Time-out protection for output overloads and open flyback feedback loop, available as safe restart

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

1.3 Application schematic

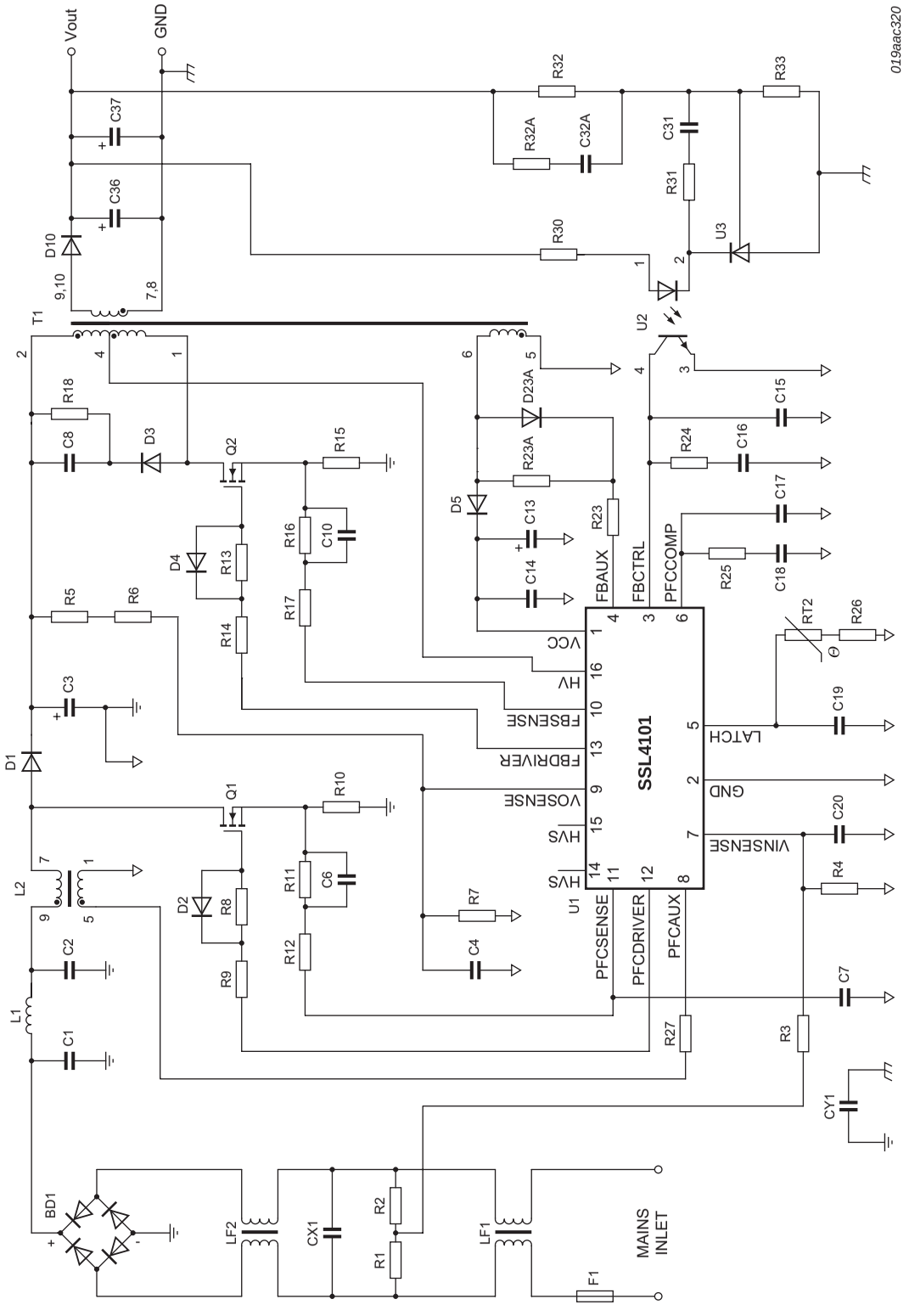


Fig 1. Application schematic

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

2. Pin description

Table 1. Pin description

Pin	Name	Functional description
1	V_{CC}	Supply voltage: $V_{startup}$ = 22 V, $V_{th(UVLO)}$ = 15 V. At mains switch-on, the capacitor connected to this pin is charged to V_{CC} start by the internal HV current source. When the pin voltage is lower than 0.65 V, the charge current is limited to 1 mA, this to prevent overheating of the IC if the V_{CC} pin is short circuited. When the pin voltage is between 0.65 V and $V_{th(UVLO)}$, the charge current is 5.4 mA to enable a fast start-up. Between $V_{th(UVLO)}$ and $V_{startup}$, the charge current is again limited to 1 mA, this to reduce the safe restart duty cycle and as a result the input power during fault conditions. At the moment $V_{startup}$ is reached the current source is pinched-off, and V_{CC} is regulated to $V_{startup}$ till the flyback starts. See chapter Section 3.2 for a complete description of the start-up sequence.
2	GND	Ground connection.
3	FBCTRL	Control input for flyback for direct connection of the optocoupler. At a control-voltage of 2 V the flyback will deliver maximum power. At a control voltage of 1.5 V the flyback will enter the frequency reduction mode and the PFC will be switched off. At 1.4 V the flyback will stop switching. Internal there is a 30 mA current source connected to the pin, which is controlled by the internal logic. This current source can be used to implement a time-out function to detect an open control-loop or a short circuit of the output-voltage. The time-out function can be disabled with a resistor of 100 kΩ between this pin and ground
4	FBAUX	Input from auxiliary winding for transformer demagnetization detection, mains dependent OverPower Protection (OPP) OverVoltage Protection (OVP) of the flyback. The combination of the demagnetization detection and the valley detection at pin HV determines the switch-on moment of the flyback in the valley. A flyback OVP is detected at a current > 300 μA into the FBAUX pin. Internal filtering is present to prevent false detection of an OVP. The flyback OPP starts at a current ≤100 μA out of the FBAUX pin.
5	LATCH	General purpose latched protection input. When $V_{startup}$ (pin 1) is reached, this pin is charged to a voltage of 1.35 V first before the PFC is enabled. To trigger the latched protection the pin has to be pulled down to below 1.25 V. An internal 80 μA current source is connected to the pin, which is controlled by the internal logic. Because of this current source, an NTC resistor for temperature protection can be directly connected to this pin.
6	PFCCOMP	Frequency compensation pin for the PFC control loop.
7	VINSENSE	Sense input for mains voltage. This pin has 5 functions: • mains enable level: $V_{start(VINSENSE)}$ = 1.15 V; • mains stop level (brown-out): $V_{stop(VINSENSE)}$ = 0.9 V; • mains voltage compensation for the PFC control-loop gain bandwidth; • fast latch reset: V_{flr} = 0.75 V The mains enable and mains stop level will enable and disable the PFC. The voltage at the VINSENSE pin must be an averaged DC value, representing the AC line voltage. The pin is not used for sensing the phase of the mains voltage.
8	PFCAUX	Input from an auxiliary winding of the PFC coil for demagnetization timing and valley detection to control the PFC switching. The auxiliary winding needs to be connected by a 5 kΩ series resistor to prevent damage of the input due to lightning surges.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

Table 1. Pin description

Pin	Name	Functional description
9	VOSENSE	Sense input for output voltage of the PFC. VOSENSE pin, open loop and short detection: $V_{th(ol)(VOSENSE)}$ = 1.15 V Regulation of PFC output voltage: $V_{reg(VOSENSE)}$ = 2.5 V PFC soft-OVP (cycle-by-cycle): $V_{ovp(VOSENSE)}$ = 2.63 V
10	FBSENSE	Current sense input for flyback. At this pin, the voltage across the flyback current sense resistor is measured. The setting of the sense level is determined by the FBCTRL voltage, using the equation: $V_{FBSENSE} = 0.75 \times V_{FBCTRL} - 1$ V. The maximum setting level for $V_{FBSENSE}$ = 0.5 V. Internal there is a 60 μA current source connected to the pin, which is controlled by the internal logic. The current source is used to implement a soft-start function for the flyback and to enable the flyback. The flyback will only start when the internal current source is able to charge the soft-start capacitor to a voltage of more than 0.5 V, therefore a minimum soft-start resistor of 12 kΩ is required to guarantee the enabling of the flyback.
11	PFCSENSE	Overcurrent protection input for PFC. This input is used to limit the maximum peak current in the PFC inductor. The PFCSENSE is a cycle by cycle protection, at 0.5 V the PFC MOSFET is switched off. There is an internal 60 μA current-source connected to the pin, which is controlled by the internal logic. This current source is used to implement a soft-start and soft-stop function. This pin is also used for enabling of the PFC. The PFC only starts when the internal current source is able to charge the soft-start capacitor to a voltage of more than 0.5 V, therefore a minimum soft-start resistor of 12 kΩ is required to guarantee the enabling of the PFC.
12	PFCDRIVER	Gate driver output for PFC MOSFET.
13	FBDRIVER	Gate driver output for flyback MOSFET.
14	HVS	High voltage safety spacer, not connected
15	HVS	High voltage safety spacer, not connected
16	HV	High voltage input for internal start-up current source (output at pin 1), and valley sensing of the flyback. The combination of the demagnetization detection at the FBAUX pin and the valley detection at the HV pin are determining the switch-on moment of the flyback in the valley.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

3. System description and calculation

3.1 PFC and flyback start conditions

In Figure 2 and Figure 3, show the conditions for enabling of the PFC and flyback are given. In case of start-up problems these condition can be checked to find the cause of the problem. Some of the conditions are dynamic signals (see Figure 4) and should be checked with an oscilloscope.

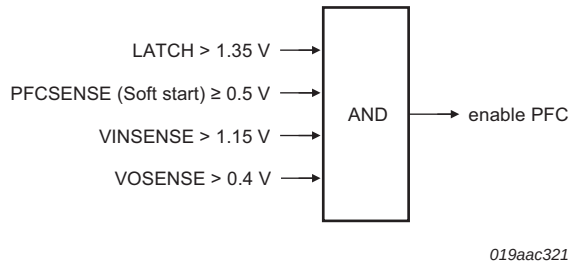


Fig 2. PFC start condition

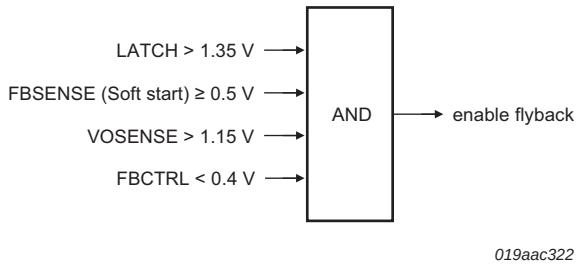


Fig 3. Flyback start conditions

3.2 Start-up sequence

At switch on with a low mains voltage, the SSL4101T power supply has the following start-up sequence (see Figure 4):

1. The HV current source is set to 0.9 mA and the V_{CC} elcap is charged to 0.65 V to detect a possible short-circuit on pin VCC.
2. At V_{CC} = 0.65 V, the HV current source is set to 5.4 mA and the V_{CC} elcap is fast charged to $V_{th(UVLO)}$.
3. At $V_{CC} = V_{th(UVLO)}$, the HV current source is set to 0.9 mA again and the V_{CC} elcap is charged further to $V_{startup}$.
4. At $V_{startup}$, the HV current source is switched off and the 80 μA LATCH pin current source is switched on to charge the LATCH pin capacitor. At the same time the PFCSENSE and FBSENSE soft-start current sources are switched on.
5. When the LATCH pin is charged up to 1.35 V and the VINSENSE pin has reached a level of 0.4 V, the PFC and flyback convertor start switching.
6. With the PFC, the soft-start capacitor connected to pin PFCSENSE must be charged up to 0.5 V and the voltage on the VOSENSE pin must be greater than 0.4 V.
7. With the flyback controller, the soft-start capacitor connected to pin FBSENSE must be charged up to 0.5 V and the voltage on the FBCTRL pin must be less than 4.5 V. Normally, the voltage on the FBCTRL pin is always less than 4.5 V on the first flyback switching cycle, unless the FBCTRL pin is open. When the flyback controller starts, the FBCTRL time out current source is switched on.
8. When the flyback has reached its nominal output voltage, the V_{CC} supply of the IC is taken over through the auxiliary winding. If the flyback feedback loop signal is missing, time-out protection on the FBCTRL pin is triggered and both controllers are switched off, V_{CC} drops to the $V_{th(UVLO)}$ value and the IC continues with step 3 of the start-up cycle. This is the safe restart cycle.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

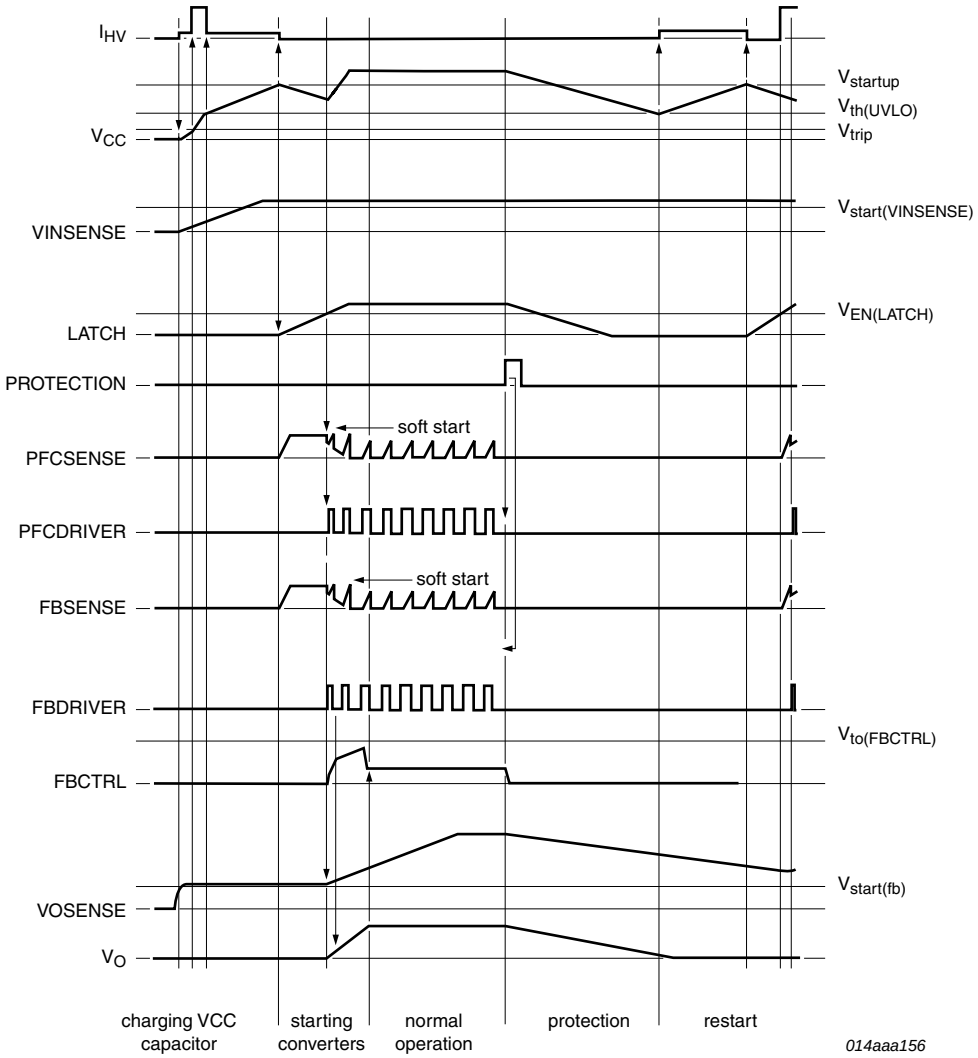


Fig 4. Start-up sequence at low mains voltage

The charge time of the soft-start capacitors is set by choosing their values independently for the PFC and the flyback controller. In this way, it can be realized that the PFC starts before the flyback.

3.3 V_{CC} cycle at safe restart protection features

In Safe restart mode the controller goes through steps 3 to 8 as described in Section 3.2.

3.4 Mains voltage sensing and brownout

The mains input voltage is measured through the VINSENSE pin. When the VINSENSE pin has reached the $V_{start(VINSENSE)}$ level of 1.15 V, the PFC can start switching but only if the other start conditions are met as well (see Section 3.1). As soon as the voltage on pin VINSENSE drops below the $V_{stop(VINSENSE)}$ level of 0.89 V, the PFC stops switching.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

The flyback however, continues switching until the flyback maximum on-time protection, $t_{on(fb)max}$ (40 µs) is triggered. When this protection is triggered, the IC stops switching and enters the safe restart mode.

The voltage on the VINSENSE pin must be an average DC value, representing the mains input voltage. The system works optimally with a time constant of approximately 150 ms on the VINSENSE pin.

The long time constant on the VINSENSE pin prevents a fast restart of the PFC after a mains drop-out, therefore the voltage at the VINSENSE pin is clamped to a level of 100 mV below the $V_{start(VINSENSE)}$ level to guarantee a fast PFC restart after recovery of the mains input voltage.

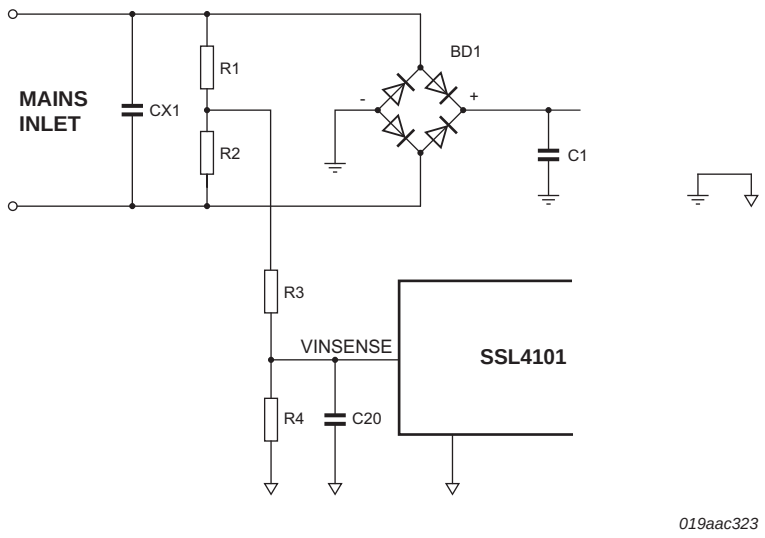


Fig 5. VINSENSE circuitry

3.4.1 Discharge of mains input capacitor

According to Ref. 1 for safety, the X-capacitors in the EMC input filtering must be discharged with a time constant $\tau < 1$ s.

The R to discharge the X-cap in the input filtering is determined by the replacement value of R1+ R2.

In a typical 90 W adapter application with Cx1 = 220 nF, the replacement value of R1 + R2 must be smaller than or equal to the following:

$$R_V \leq \frac{\tau}{C} = \frac{1}{220\ nF} = 4.55\ M\Omega \quad (1)$$

3.4.2 Brownout voltage adjustment

The rectified AC input voltage is measured via R1 and R2. Each resistor alternately senses half the sine wave, so both resistors must have the same value.
The average voltage sensed at the connection of R1 and R2 is as follows:

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

$$V_{avg} = \frac{2\sqrt{2}}{\pi} \cdot V\,(AC)_{RMS} \quad (2)$$

The V (AC) brownout RMS level is calculated as follows:

$$V_{bo} = \frac{\pi}{2\sqrt{2}} \cdot V_{stop(VINSENSE)} \cdot 2 \cdot \frac{R1 \cdot R2}{\left(\frac{R1 + R2}{R4} + 1\right)} + R3 \quad (3)$$

where: V_{bo} is the AC brownout voltage; $V_{stop(VINSENSE)}$ = 0.89 V

With an obtained brown-out threshold ($V_{th(bo)}$) of 68 V (AC) and complying with Ref. 1. Example values are shown in Table 2.

Table 2. VINSENSE component values

Cx1	R1	R2	R3	R4
220 nF	2 MΩ	2 MΩ	560 kΩ	47 kΩ
330 nF	1.5 MΩ	1.5 MΩ	820 kΩ	47 kΩ
470 nF	1 MΩ	1 MΩ	1.1 MΩ	47 kΩ

A value of 3.3 μF for capacitor C20, with 47 kΩ at R4, gives the recommended time constant of ~150 ms on the VINSENSE pin.

3.5 Internal OTP

The IC has an internal OverTemperature Protection (OTP) circuit to protect the IC from overheating by overloads on the V_{CC} pin. When the junction temperature exceeds the thermal shutdown temperature, the IC stops switching. As long as the OTP is active, the V_{CC} capacitor is not recharged from the HV mains. The OTP circuit is supplied by the HV pin if the V_{CC} supply voltage is not sufficient. OTP is a latched protection.

3.6 LATCH pin

The LATCH pin is a general purpose input pin which can be used to latch both controllers off. The pin sources a bias current $I_{o(LATCH)}$ of 80 μA for the direct connection of the Negative Temperature Coefficient (NTC) resistor. When the voltage on this pin is pulled below 1.25 V, switching of both controllers immediately stops. V_{CC} starts cycling between the $V_{th(UVLO)}$ and $V_{startup}$, without a restart. Switching off and then switching on the mains input voltage triggers the fast latch reset circuit and resets the latch.

At start-up, the latch pin must be charged above 1.35 V, before both controllers are enabled. Charging of the LATCH pin starts at $V_{startup}$.

No internal filtering is present at the LATCH pin. A 10 nF capacitor must be placed between this pin and the GND pin to prevent false triggering, also when the LATCH pin function is not used.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

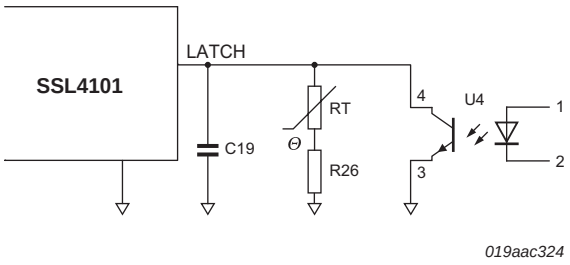


Fig 6. Usage of the LATCH pin protection

Latching on application overtemperature occurs when the total resistance value of the Negative Temperature Coefficient (NTC) and its series resistor drops below the following:

$$R_{OTP} = \frac{V_{prot(LATCH)}}{I_{O(LATCH)}} = \frac{1.25\ V}{80\ \mu A} = 15.6\ k\Omega \quad (4)$$

The optocoupler triggers the latch if the driven optotransistor conducts more than 80 μA.

3.7 Fast latch reset

Switching off and then switching on the mains input voltage, can reset the latched protection. After the mains input is switched off, the voltage on the VINSENSE pin drops below V_{FLR} (0.75 V). This triggers the fast latch reset circuit, but it does not reset the latched protection. After the mains input is switched on, the voltage on the VINSENSE pin rises again and when the level passes 0.85 V, the latch is reset. The system restarts again when the V_{CC} pin is charged to $V_{startup}$. See step 4 of Section 3.2

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

4. PFC description and calculation

The PFC operates in Quasi-Resonant (QR) or Discontinuous Conduction Mode (DCM) with valley detection to reduce the switch on losses. The maximum switching frequency of the PFC is limited to 380 kHz. One or more valleys are skipped, when necessary, to keep the frequency below 380 kHz.

At low output loads, the PFC is switched off to ensure a high-efficiency and a low no-load stand-by input power. After switch off the bulk elcap voltage drops to V (AC) × √2.

4.1 PFC output power and voltage control

The PFC of the SSL4101T is on-time controlled, therefore it is not necessary to measure the mains phase angle. The on-time is kept constant during the half sine wave to obtain a good Power Factor (PF) and a class-D Mains Harmonics Reduction (MHR) see Ref. 2.

The PFC output voltage is controlled through the VOSENSE pin. At the VOSENSE pin there is a trans-conductance error amplifier with a reference voltage of 2.5 V. The error at the VOSENSE pin is converted with 80 μA/V into a current at the PFCCOMP pin. The voltage at the PFCCOMP pin, in combination with the voltage at the VINSENSE pin, determines the PFC on-time.

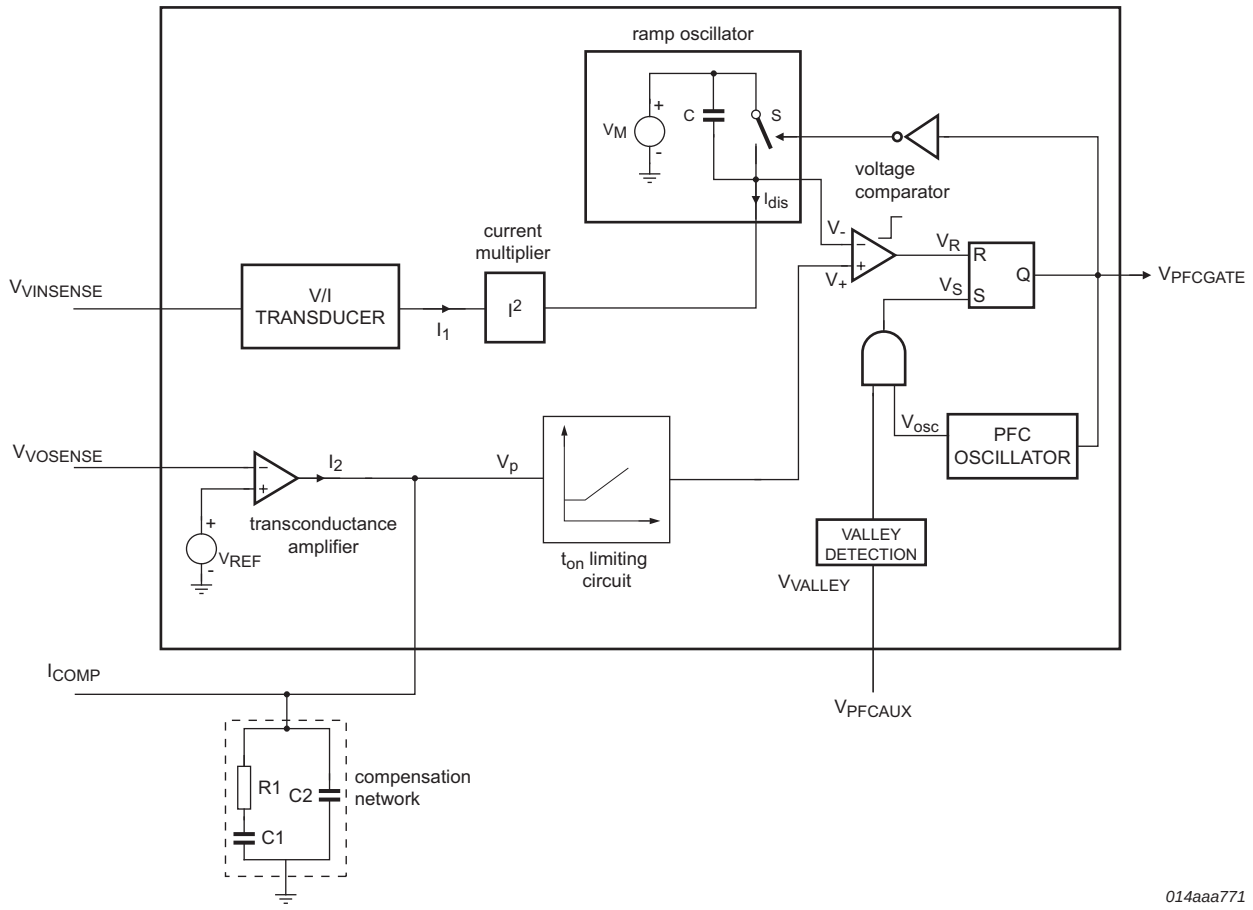


Fig 7. PFC on-time control

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

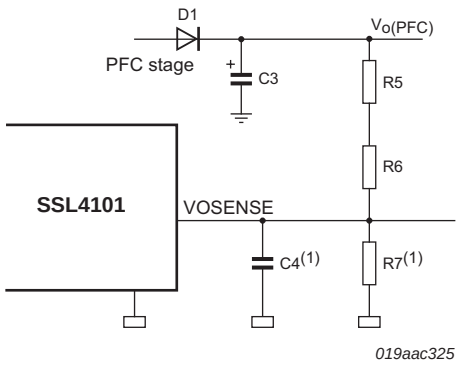
To stabilize the PFC control loop, a network with one resistor and two capacitors at the PFCCOMP pin is used. The mathematical equation for the transfer function of a boost controller contains the square of the mains input voltage. In a typical application, this results in a low regulation bandwidth for low mains input voltages and a high regulation bandwidth at high input voltages, while at high mains input voltages it can be difficult to meet the MHR requirements.

The SSL4101T uses the mains input voltage measured through the VINSENSE pin to compensate the control loop gain as function of the mains input voltage. As a result the gain is constant over the entire mains input voltage range.

The voltage at the VINSENSE pin must be an average DC value, representing the mains input voltage. The system works optimally with a time constant of approximately 150 ms on the VINSENSE pin.

4.1.1 Setting the PFC output voltage

The PFC output voltage is set with a resistor divider between the PFC output voltage and the VOSENSE pin. In PFC Normal mode, the PFC output voltage is regulated so that the voltage on the VOSENSE pin is equal to $V_{reg(VOSENSE)}$ = 2.5 V.



(1) Place C4 and R7 as close as possible to the IC.

Fig 8. PFC output voltage setting

Two resistors of 4.7 MΩ (1 %) can be used for low no-load input power placed between the bulk elcap and the VOSENSE pin. With a resistor value of 4.7 MΩ for R5 and R6 and 60 kΩ to 62 kΩ for R7, a universal mains adapter will have a PFC output voltage of approximately 380 V to 390 V at high mains and 240 V to 250 V at low mains.

The resistor R7 (1 %) between the VOSENSE pin and ground can be calculated with Equation 5:

$$R7 = \frac{(R5 + R6) \times V_{reg(VOSENSE)}}{(V_{O(PFC)} - V_{reg(VOSENSE)})} \quad (5)$$

If the regulated PFC output voltage is 382 V, then:

$$R7 = \frac{(4.7\ M\Omega + 4.7\ M\Omega) \times 2.5\ V}{(382\ V - 2.5\ V)} = 62\ K\Omega(1\ \%) \quad (6)$$

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

The function of the capacitor C4 connected to the VOSENSE pin, is to filter noise and to prevent false triggering of the protection circuits, due to MOSFET switching noise, mains surge events or ESD events.

False triggering of the $V_{ovp(VOSENSE)}$ protection can cause audible noise and disturbance of the AC mains input current. False triggering of the $V_{th(ol)(VOSENSE)}$ protection causes a safe restart cycle. A time constant of 500 ns to 1 ms, for the VOSENSE pin should be sufficient, resulting in a value of 10 nF for capacitor C4.

It is advisable to place R7 and C4 as close as possible to the IC between the VOSENSE pin and the IC ground pin.

4.1.2 Calculation of the PFC soft-start and soft-stop components

The soft-start and soft-stop are implemented through the RC network connected to the PFCSENSE pin.

R_{SS1} must have a minimum value of 12 kΩ as specified. This to ensure that the voltage $V_{start(soft)PFC}$ of 0.5 V is reached to enable start-up of the PFC. See Section 3.1 for start-up description.

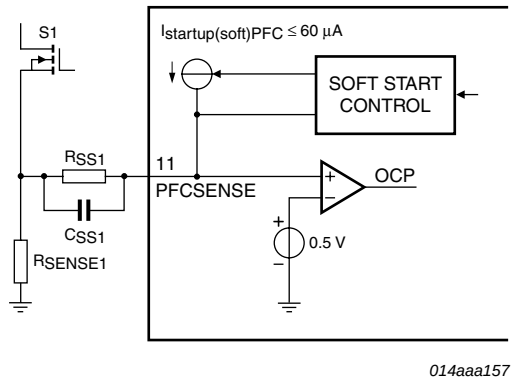


Fig 9. PFC soft-start

The total soft-start or soft-stop time is equal to: $t_{soft-start} = 3Rss1 \cdot Css1$

It is advised to keep the soft-start time of the PFC smaller than the soft-start time of the flyback controller to ensure that the PFC starts before the flyback at initial start-up. It is also advised that the soft-start time is kept within a range of 2 ms to 5 ms.

With C8 = 100 nF and R11 = 12 kΩ, the total soft-start time will be 3.6 ms.

4.2 PFC demagnetizing and valley detection

The PFC MOSFET is switched on after the transformer is demagnetized. Internal circuitry connected to the PFCAUX pin detects the end of the secondary stroke. It also detects the voltage across the PFC MOSFET. The next stroke is started if the voltage across the PFC MOSFET is at its minimum to reduce switching losses and ElectroMagnetic Interference (EMI) (valley switching).

The maximum switching frequency of the PFC is limited to 380 kHz. One or more valleys are skipped, when necessary, to keep the frequency below 380 kHz.

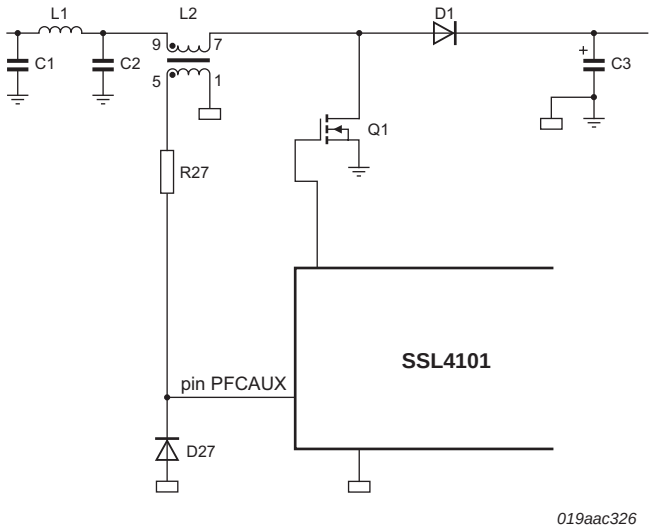
All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

If no demagnetization signal is detected on the PFCAUX pin, the controller generates a Zero Current Signal (ZCS), 50 ms after the last PFC gate signal.

If no valley signal is detected on the PFCAUX pin, the controller generates a valley signal 4 μs after demagnetization was detected.

In some applications, the PI filter before the PFC inductor can start oscillating when the PFC switching frequency is close to the third harmonic of the PI filter resonance frequency. This could lead to false PFC valley detection. As a result, the PFC can run in Continuous conduction mode. False detection can be suppressed by placing a diode between the IC ground and the PFCAUX pin.



(1) Place D27 and R27 close to the IC.

Fig 10. PFCAUX circuitry

4.2.1 Design of the PFCAUX winding and circuit

To guarantee valley detection at low ringing amplitudes, the voltage at the PFCAUX pin should be set as high as possible, taking into account its absolute maximum rating of ±25 V.

The number of turns of the PFCAUX winding can be calculated as follows:

$$N_{a\_max} = \frac{V_{PFCAUX}}{V_{L(max)}} \times N_p = \frac{25V}{V_{L(max)}} \times N_p \quad (7)$$

Where: V_{PFCAUX} is the absolute maximum rating of the PFCAUX pin and $V_{L(max)}$ is the maximum voltage load across the PFC primary winding. The PFC output voltage at the PFC OVP level determines the maximum voltage across the PFC primary winding and can be calculated with Equation 8:

$$V_{Lmax} = \frac{V_{OVP(VoSense)}}{V_{reg(VoSense)}} \times Vo_{PFC} = \frac{2.63V}{2.5V} \times Vo_{PFC} \quad (8)$$

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

When a PFC coil with a higher number of auxiliary turns is used, then a resistor voltage divider can be placed between the auxiliary winding and pin PFCAUX. The total resistive value of the divider should be less than 10 kΩ to prevent delay in the valley detection due to parasitic capacitance.

The polarity of the signal at the PFCAUX pin must be reversed compared to the PFC MOSFET drain signal.

To protect the PFCAUX pin against electrical overstress, for example during lighting surge events, it is advised to place a 5 kΩ resistor between the PFC auxiliary winding and this pin. To prevent incorrect valley switching of the PFC due to external disturbance, the resistor should be placed close to the IC.

4.3 PFC protection features

4.3.1 VOSENSE OverVoltage Protection

At start-up, a voltage overshoot can occur at the boost elcap. This overshoot is caused by the relatively slow response of the PFC control loop. The PFC control loop response must be relatively slow to guarantee a good power factor and meet the MHR requirements.

The OverVoltage Protection (OVP) at the VOSENSE pin limits the overshoot. When the $V_{OVP(VOSENSE)}$ level of 2.63 V is detected, the PFC MOSFET is immediately switched off, regardless of the on-time setting. Switching of the MOSFET remains blocked until the voltage at the VOSENSE pin drops below 2.63 V again.

When the resistor between the VOSENSE pin and ground is open, OVP is also triggered.

The peak voltage at the boost elcap generated by the PFC due to an overshoot and limited by the PFC OVP can be calculated with the Equation 9:

$$Vo_{PFC\_PEAK} = \frac{V_{ovp(VOSENSE)}}{V_{reg(VOSENSE)}} \cdot Vo_{PFC\_NOMINAL} = \frac{2.63V}{2.5V} \cdot Vo_{PFC\_NOMINAL} \quad (9)$$

4.3.2 VOSENSE open and short pin detection

The VOSENSE pin which senses the PFC output voltage, has integrated protection circuitry to detect an open and short-circuited pin. This pin can also sense if one of the resistors in the voltage divider is open. Therefore the VOSENSE pin is completely fail-safe. It is not necessary to add an external OVP circuit for the PFC.

An internal current source pulls the pin down below the $V_{th(ol)(VOSENSE)}$ detection level of 1.4 V, when the pin is open. At detection of the $V_{th(ol)(VOSENSE)}$ level switching of the PFC MOSFET is blocked until the voltage at the VOSENSE pin rises above 0.4 V again.

4.3.3 VINSENSE open pin detection

The VINSENSE pin which senses the mains input voltage, has an integrated protection circuit to detect an open pin. An internal current source pulls the pin down below the $V_{stop(VINSENSE)}$ level of 0.89 V, when the pin is open.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

4.3.4 OverCurrent Protection (OCP)

An OverCurrent Protection (OCP) limits the maximum current through the PFC MOSFET and PFC inductor. The current is measured via a current sense resistor in series with the MOSFET source. The MOSFET is immediately switched off when the voltage at pin PFCSENSE exceeds the $V_{sense(PFC)max}$ level of 0.52 V. The OCP is a switching cycle-by-switching cycle protection.

To avoid false triggering of the PFC OCP by switching of the flyback, it is advised to keep a margin of 0.1 V into account. False triggering of the $V_{OVP(VOSENSE)}$ protection can cause disturbance of the AC mains input current. It is also advised that a small capacitor of 100 pF to 220 pF is placed directly at the PFCSENSE pin to any suppress external disturbance.

The current sense resistor can be calculated using Equation 10:

$$R_{OCP(PFC)} = \frac{V_{SENSE(PFC)max} - V_{margin}}{Ip_{QR(PFC)max}} = \frac{0.52\ V - 0.1\ V}{Ip_{QR(PFC)max}} \quad (10)$$

Where: $I_{pQR(PFC)max}$ is the maximum PFC peak current at the high load and low mains.

The maximum peak current for the PFC operating in quasi-resonant mode can be calculated using Equation 11:

$$Ip_{QR(PFC)max} = \frac{2\sqrt{2} \cdot P_{i(max)} \cdot 1.1}{V\ (AC)_{min}} = \frac{2\sqrt{2} \cdot \frac{P_{o(max)}}{\eta} \cdot 1.1}{V\ (AC)_{min}} \quad (11)$$

Where:

- $P_{o(max)}$ is the maximum output power of the flyback
- 1.1 is a factor to compensate for the dead-time between zero current in the PFC inductor at the end of the secondary stroke and the detection of the first valley in QR mode
- η is the expected efficiency of the total controller at maximum output power
- $V\ (AC)_{min}$ is minimum mains input voltage.

5. Flyback description and calculation

The flyback of the SSL4101T is a variable frequency controller that can operate in Quasi Resonant (QR) or Discontinuous Conduction mode with demagnetization detection and valley switching.

The setting of the primary peak current controls the output power; the switching frequency is a result. The primary peak current is set through the voltage at the FBCTRL pin and measured back at the FBSENSE pin with the following relationship: $V_{sense(FB)} \cong 0.75 \times V_{FBCTRL} - 1\ V$.

The flyback controls the operational mode of the PFC. At low output powers, when the primary peak current, $Ip \leq 0.25 \times Ip\_max$, the PFC is switched off.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

Demagnetization of the flyback transformer is detected through pin FBAUX, connected to the auxiliary winding. The valley is detected through the HV pin which can be connected to the MOSFET drain or to the center tap of the primary winding.

The input voltage of the flyback is measured through pin FBAUX and used to implement and OverPower Protection (OPP). OPP keeps the maximum output power of the flyback controller constant over the input voltage.

The flyback has an accurate OverVoltage Protection (OVP) circuit. The overvoltage is measured, through pin FBAUX. Both controllers will be switched off in a latched protection when an overvoltage is detected.

5.1 Flyback output power control

An important aspect of the SSL4101T flyback system is, that the setting of the primary peak current controls the output power. The switching frequency is a result of external application parameters and internal IC parameters.

External application parameters are the transformer turns ratio, the primary inductance, the drain source capacitance, the input voltage, the output voltage and the feedback signal from the control loop. Internal IC parameters are the oscillator setting, the setting of the peak current and the detection of demagnetization and valley.

The output power of flyback can be described with Equation 12:

$$P_o = \frac{1}{2} \cdot Lp \cdot Ip^2 \cdot fs \cdot \eta \quad (12)$$

At initial start-up, the flyback controller always starts at maximum output power. The flyback controller will go through the three operation modes from maximum to minimum output power, as shown Figure 11.

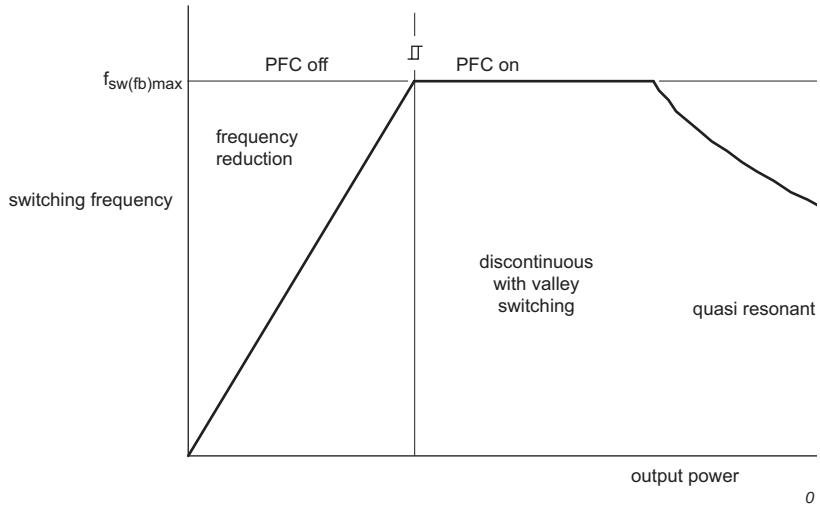


Fig 11. Operation modes flyback

At maximum output power, limited by the flyback current sense resistor, the flyback controller operates in Quasi-Resonant (QR) mode. The next primary switching cycle starts at detection of the first valley.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

By reducing the peak current, the output power is reduced and as a result the switching frequency increases. When the maximum flyback switching frequency is reached and the output power still has to be reduced, the flyback goes from QR into DCM with valley switching.

In DCM, the output power is reduced by further reduction of the peak current and at the same time skipping of one or more valleys. In this mode, the switching frequency is kept constant. The exact switching frequency however, depends on the detection of the valley but will never be higher as the maximum frequency.

The minimum flyback peak current: $Ip\_min = 0.25 \times Ip\_max$. At this point the flyback controller enters the Frequency Reduction mode. In the Frequency Reduction mode the peak current is kept constant. Increasing the off time reduces the output power.

It is advised to place a 10 nF noise filter capacitor (C15) as close as possible to the FBCTRL pin to avoid disturbance of the flyback by switching of the PFC MOSFET.

5.1.1 Calculation of the flyback current sense resistor

The current sense resistor $R_{OCP(fb)}$ can be calculated using Equation 13:

$$R_{OCP(fb)} = \frac{V_{sense(fb)max}}{Ip_{QR(fb)max}} = \frac{0.52\ V}{Ip_{QR(fb)max}} \quad (13)$$

The peak current can be calculated for the flyback controller operating in quasi-resonant mode using Equation 14:

$$Ip_{QR(fb)max} = \frac{2P_{o(max)} \cdot 1.1}{\eta \times V\ (DC)} \times \frac{V\ (DC) + \frac{Np}{Ns} \cdot V_o}{\frac{Np}{Ns} \cdot V_o} \quad (14)$$

Where:

- $P_{o(max)}$ is the maximum output power of the flyback controller
- 1.1 is a factor that compensates for the dead time between zero current in the flyback transformer at the end of the secondary stroke and the detection of the first valley in QR mode;
- η is the expected efficiency of the flyback at maximum output power
- V (DC) is the bulk elcap voltage
- V_o is the output voltage
- Np is the number of primary turns of the flyback transformer
- Ns is the number of secondary turns of the flyback transformer.

5.1.2 Calculation of the flyback soft-start components

The soft-start is implemented through the RC network at pin FBSENSE. R_{SS1} must have a minimum value of 12 kΩ as specified. This to ensure that the voltage $V_{start(soft)PFC}$ of 0.5 V is reached to enable start-up of the flyback. See Section 3.1 for start-up description.

The total soft-start or soft-stop time is equal to $t_{soft\text{-}start} = 3Rss \cdot Css$.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

It is advisable to make the soft-start time for the flyback larger than the soft-start time of the PFC, to make sure that the PFC starts before the flyback at initial start-up. It is also advisable to keep the soft-start time in a range of 5 ms to 10 ms.

With C10 = 220 nF and R16 = 12 kΩ the total soft-start time will be 8 ms.

5.2 Flyback converter protection circuits

5.2.1 Short-circuit on the FBCTRL pin

If the pin is shorted to ground, switching of the flyback controller is inhibited. This situation is equal to the minimum or a no output power situation.

5.2.2 Open the FBCTRL pin

As shown in Figure 12, the FBCTRL pin is connected to a 3.5 V internal voltage source via an internal 3 kΩ resistor. When the voltage on pin FBCTRL is above 2.5 V, this connection is disabled and the FBCTRL pin is biased with an internal 30 μA current source. When the voltage on the FBCTRL pin rises above $V_{to(FBCTRL)}$ of 4.5 V a fault is assumed. Switching of the flyback (and also the PFC) is blocked and the controller will enter the Safe Restart mode.

An internal switch pulls the FBCTRL pin down when the flyback convertor is disabled.

5.2.3 Time-out flyback control-loop

A time-out function can be realized to protect for an output short-circuit at initial start-up or for an open control loop situation. This can be done by placing a resistor in series with a capacitor between the FBCTRL pin and ground (see Figure 12).

Above 2.5 V, the switch in series with the 3 kΩ resistor is open and pin FBCTRL (and thus the RC combination) is biased with a 30 μA current source. When the voltage on FBCTRL pin rises above 4.5 V, switching of the flyback controller and the PFC is blocked causing the controller to enter the Safe Restart mode. The capacitor can be used to set the time delay to reach 4.5 V at the FBCTRL pin. The resistor is necessary to separate the relatively large time-out capacitor from the control loop response. It is advised to use a resistor of at least 30 kΩ. The resistor however, will also influence the charge time of the capacitor.

The time-out time t_{to} can be calculated using Equation 15:

$$t_{to} = \frac{C_{to} \cdot (V_{to(FBCTRL)} - (I_{0(FBCTRL)} \cdot R_{to}))}{I_{O(FBCTRL)}} \quad (15)$$

otherwise the capacitor can be calculated using Equation 16:

$$C_{to} = \frac{I_{O(FBCTRL)} \cdot t_{to}}{V_{to(FBCTRL)} - (I_{O(FBCTRL)} \cdot R_{to})} \quad (16)$$

or the resistor can be calculated using Equation 17:

$$R_{to} = \frac{V_{to(FBCRTL)}}{I_{O(FBCRTL)}} - \frac{t_{to}}{C_{to}} \quad (17)$$

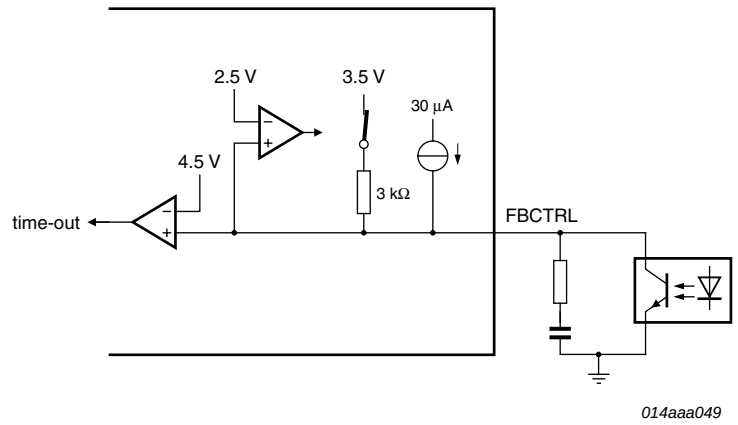
All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

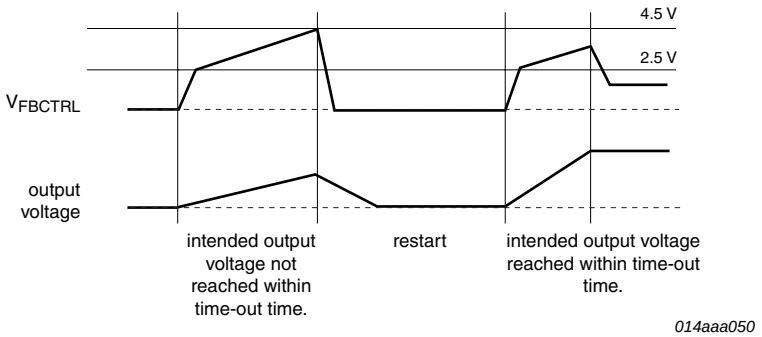
A t_{to} of 37 ms in combination with a C_{to} of 330 nF leads to a resistor value of:

$$R_{to} = \frac{4.5V}{30\mu A} - \frac{37ms}{330nF} = 37.9k\Omega \approx 39k\Omega \quad (18)$$

When the time-out protection is not required, placing a resistor of 100 kΩ between pin FBCTRL and ground can disable the time-out protection.



a. Circuit diagram



b. Timing diagram

Fig 12. Time-out protection

5.2.4 Overvoltage protection flyback

The IC has an internal OverVoltage Protection (OVP) circuit, which switches off both controllers when an overvoltage is detected at the flyback output, by a latched protection.

The IC can detect an overvoltage in a secondary winding of the flyback controller by measuring the voltage at the auxiliary winding during the secondary stroke. A series resistor between the auxiliary winding and the FBAUX pin converts this voltage to a current on the FBAUX pin.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

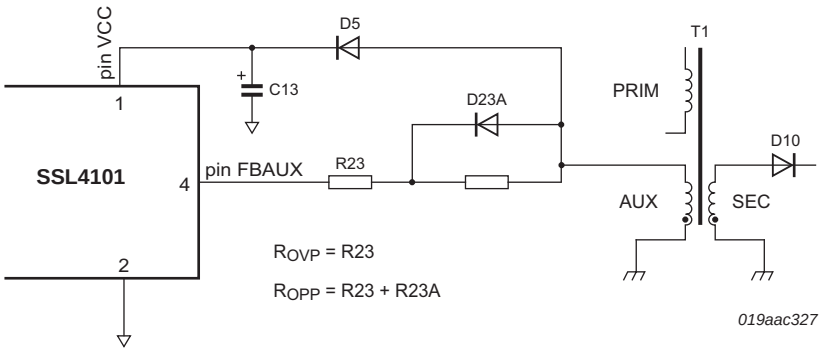


Fig 13. Flyback OVP and OPP circuit

At a current $I_{ovp(FBAUX)}$ of 300 μA on the FBAUX pin, the IC detects an overvoltage. An internal integrator filters noise and voltage spikes. The output of the integrator is used as an input for an up-down counter. The counter has been added as an extra filter to prevent false OVP detection which might occur during ESD or lightning events.

If the integrator detects an overvoltage, the counter increases its value by one. If another overvoltage is detected during the next switching cycle, the counter increases its value by one again. If no overvoltage is detected during the next switching cycle, the counter will subtract its value by two (the minimum value is 0). If the value reaches 8, the IC assumes a true overvoltage and activates the latched protection. Both controllers are immediately switched off and V_{CC} starts cycling between the $V_{th(UVLO)}$ and $V_{startup}$, without a restart.

Switching the mains input voltage off and then on triggers the fast latch reset circuit and resets the latch.

The OVP level can be set by the resistor R_{OVP}:

$$R_{OVP} = \frac{\left(\frac{N_{AUX}}{N_S} \times V_{o(OVP)}\right) - V_{clamp(FBAUX)} - V_{F(D23A)}}{I_{OVP(FBAUX)}} = \frac{\left(\frac{N_{AUX}}{N_S} \times V_{o(OVP)}\right) - 0.7_{(typ)} - V_{F(D23A)}}{300\ \mu A_{(typ)}} \quad (19)$$

Where:

- N_S is the number of turns on the secondary winding
- N_{AUX} is the number of turns on the auxiliary winding of the flyback transformer
- $V_{clamp(FBAUX)}$ is the positive clamp-voltage of the FBAUX pin.
- $V_{F(D23A)}$ is the forward voltage of D23A at a current of 300 μA

For the calculation of the $V_{o(OVP)}$ level the tolerances on $I_{ovp(FBAUX)}$ have to be taken into account, this to avoid triggering of the OVP during normal operation.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

5.2.5 OverPower Protection (OPP)

In a quasi-resonant flyback, the maximum output power is dependent on the (mains) input voltage. OPP is implemented to compensate.

During the primary stroke of the flyback the mains voltage is sensed by measuring the current drawn from pin FBAUX. With a resistor connected between the flyback auxiliary winding and pin FBAUX, the voltage at the auxiliary winding is converted into a current I_{FBAUX} (see Figure 13). The IC is using the current information to reduce the setting of the maximum flyback peak current measured through pin FBSENSE. See Figure 14 for the limitation of the maximum $V_{FBSENSE}$ level as a function of I_{FBAUX}.

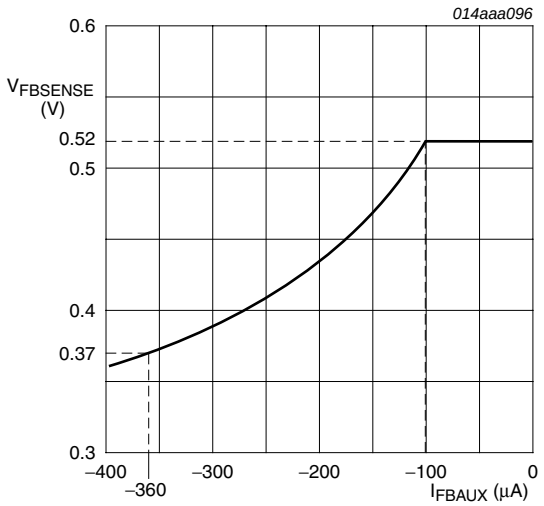


Fig 14. Operation modes flyback

The total OPP resistance determines the I_{FBAUX} current during the primary stroke of the flyback and consists of R23 + R23A (see Figure 13). First, the OVP resistor R23 has to be calculated before the remaining part of the OPP resistor R23A can be calculated.

The value of R23A can be calculated by:

$$R23A = \frac{\frac{Na}{Np} \cdot V_{o(PFC)low} - V_{clamp(FBAUX)}}{I_{start(OPP)FBAUX}} = \frac{\frac{Na}{Np} \cdot 240\ V - 0.8\ V}{100\ \mu A} - R_{OVP} \quad (20)$$

6. Summary of calculations

See Figure 1 application schematic for component reference numbers.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

7. PCB layout considerations

<tbd>

8. References

[1] **IEC-60950 —** Chapter 2.1.1.7 “discharge of capacitors in equipment”

[2] **IEC61000-3-2 —** Limits for Harmonic Current Emissions

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

9. Legal information

9.1 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

9.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

9.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

GreenChip — is a trademark of NXP B.V.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

10. Contents

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2011. **All rights reserved.**

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 13 May 2011
Document identifier: AN11054