R1EV5801MB Series

1M EEPROM (128-Kword × 8-bit)Ready/Busy and RES function

R10DS0209EJ0100
Rev.1.00
Jun 09, 2014

Description

Renesas Electronics' R1EV5801MB is an electrically erasable and programmable ROM organized as 131072-word × 8-bit. It has realized high speed, low power consumption and high reliability by employing advanced MONOS memory technology and CMOS process and circuitry technology. It also has a 128-byte page programming function to make the write operations faster.

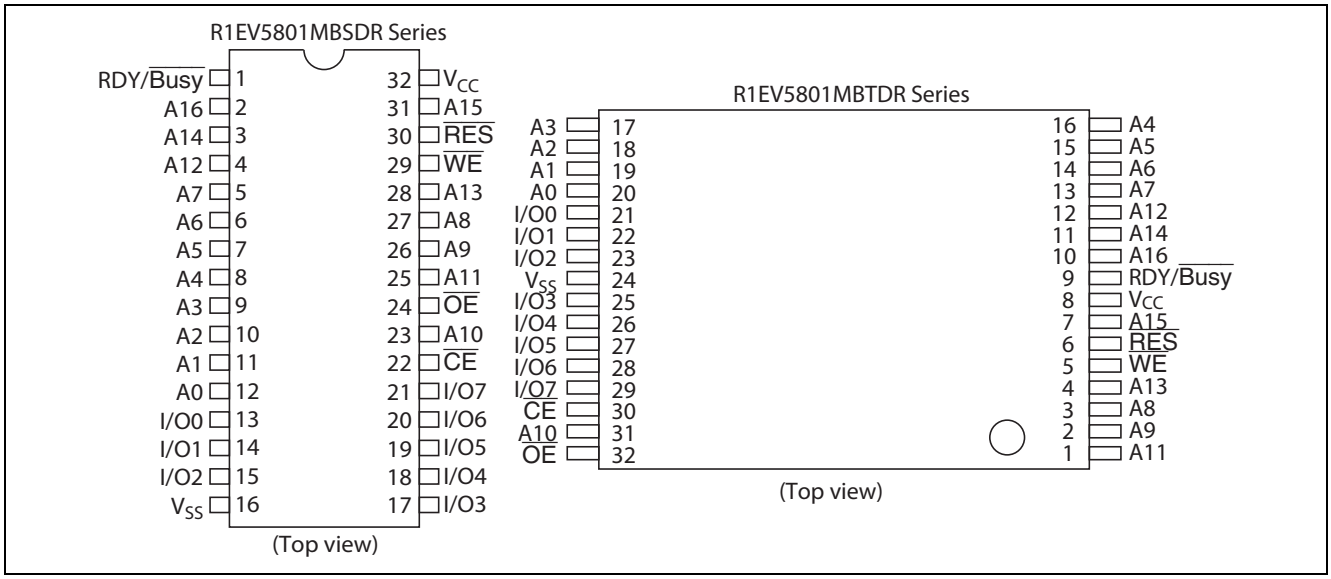
Features

- Single voltage supply: 2.7 V to 5.5 V
- Access time:
  - 150 ns (max) at Vcc=4.5 V to 5.5 V
  - 250 ns (max) at Vcc=2.7 V to 5.5 V
- Power dissipation
  - Active: 20 mW/MHz, (typ)
  - Standby: 110 µW (max)
- On-chip latches: address, data, $\overline{CE}$, $\overline{OE}$, $\overline{WE}$
- Automatic byte write: 10 ms (max)
- Automatic page write (128 bytes): 10 ms (max)
- $\overline{Data}$ polling and RDY/$\overline{Busy}$
- Data protection circuit on power on/off
- Conforms to JEDEC byte-wide standard
- Reliable CMOS with MONOS cell technology
- 10^4 or more erase/write cycles
- 10 or more years data retention
- Software data protection
- Write protection by $\overline{RES}$ pin
- Temperature range: –40 to +85°C
- There are lead free products.

Ordering Information

Orderable Part Name	Access time	Package	Shipping Container	Quality
R1EV5801MBSDRDI#B0	150ns/250ns	525mil 32-pin plastic SOP PRSP0032DC-A (FP-32DV)	Tube	Max. 22 pcs/tube Max. 880 pcs/inner box
R1EV5801MBTDRDI#B0	150ns/250ns	32-pin plastic TSOP PTSA0032KD-A (TFP-32DAV)	Tray	Max. 60 pcs/reel Max. 600 pcs/inner box

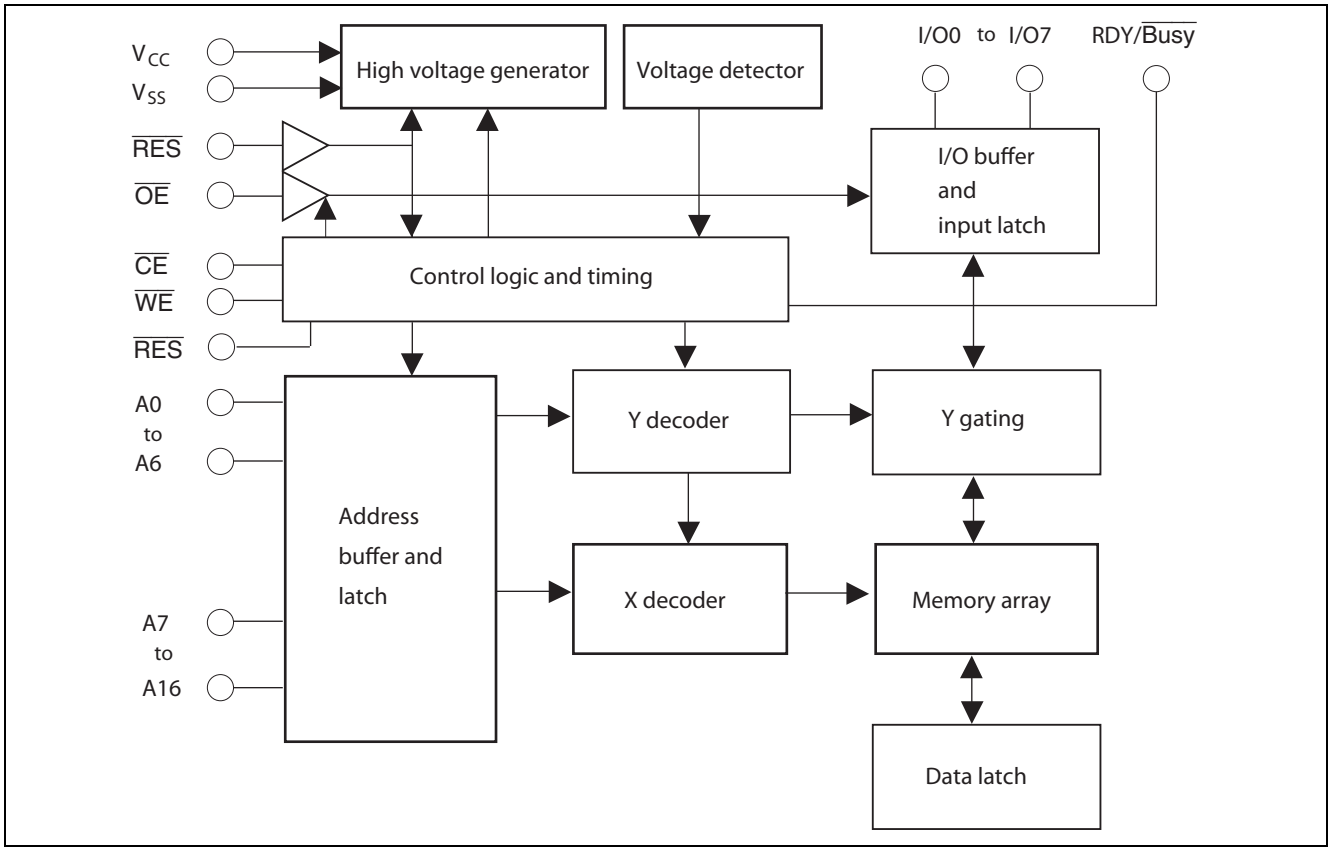
Pin Arrangement



Pin Description

Pin name	Function
A0 to A16	Address input
I/O0 to I/O7	Data input/output
$\overline{OE}$	Output enable
$\overline{CE}$	Chip enable
$\overline{WE}$	Write enable
V_{CC}	Power supply
V_{SS}	Ground
RDY/$\overline{Busy}$	Ready busy
$\overline{RES}$	Reset

Block Diagram



Operation Table

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RES}$	RDY/$\overline{Busy}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	V_H*1	High-Z	Dout
Standby	V_{IH}	×*2	×	×	High-Z	High-Z
Write	V_{IL}	V_{IH}	V_{IL}	V_H	High-Z to V_{OL}	Din
Deselect	V_{IL}	V_{IH}	V_{IH}	V_H	High-Z	High-Z
Write Inhibit	×	×	V_{IH}	×	—	—
	×	V_{IL}	×	×	—	—
$\overline{Data}$ Polling	V_{IL}	V_{IL}	V_{IH}	V_H	V_{OL}	Dout (I/O7)
Program reset	×	×	×	V_{IL}	High-Z	High-Z

Notes: 1. Refer to the recommended DC operating conditions.
2. × : Don't care

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage relative to V_{SS}	V_{CC}	–0.6 to +7.0	V
Input voltage relative to V_{SS}	Vin	–0.5*1 to +7.0	V
Operating temperature range*2	Topr	–40 to +85	°C
Storage temperature range	Tstg	–55 to +125	°C

Notes: 1. Vin min = –3.0 V for pulse width ≤ 50 ns
2. Including electrical characteristics and data retention

Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	2.7	3.0	5.5	V
	V_{SS}	0	0	0	V
Input voltage	V_{IL}	–0.3*[1]	—	0.8	V
	V_{IH}	1.9*[2]	—	V_{CC} + 0.3	V
	V_H	V_{CC} – 0.5	—	V_{CC} + 1.0	V
Operating temperature	Topr	–40	—	+85	°C

Notes: 1. V_{IL} (min): –1.0 V for pulse width ≤ 50 ns
2. V_{IH} (min): 2.2 V for V_{CC} = 3.6 to 5.5 V

DC Characteristics (Ta = -40 to +85°C, V_{CC} = 2.7 V to 5.5 V)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I_{LI}	—	—	2*[1]	µA	V_{CC} = 5.5 V, Vin =5.5 V
Output leakage current	I_{LO}	—	—	2	µA	V_{CC} = 5.5 V, Vout = 5.5/0.4 V
Standby V_{CC} current	I_{CC1}	—	—	20	µA	$\overline{CE}$ = V_{CC}
	I_{CC2}	—	—	1	mA	$\overline{CE}$ = V_{IH}
Operating V_{CC} current	I_{CC3}	—	—	15	mA	Iout = 0 mA, Duty = 100%, Cycle = 1 µs, V_{CC} = 5.5 V
		—	—	6	mA	Iout = 0 mA, Duty = 100%, Cycle = 1 µs, V_{CC} = 3.3 V
		—	—	50	mA	Iout = 0 mA, Duty = 100%, Cycle = 150 ns, V_{CC} = 5.5 V
		—	—	15	mA	Iout = 0 mA, Duty = 100%, Cycle = 250 ns, V_{CC} = 3.3 V
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
Output high voltage	V_{OH}	V_{CC} × 0.8	—	—	V	I_{OH} = –400 µA

Notes: 1. I_{LI} on $\overline{RES}$: 100 µA (max)

Capacitance (Ta = +25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance*[1]	Cin	—	—	6	pF	Vin = 0 V
Output capacitance*[1]	Cout	—	—	12	pF	Vout = 0 V

Note: 1. This parameter is periodically sampled and not 100% tested.

AC Characteristics

(Ta = -40 to +85°C, V_{CC} = 4.5 V to 5.5 V)

Test Conditions

- Input pulse levels: 0.4 V to 2.4 V, 0 V to V_{CC} ($\overline{RES}$ pin)
- Input rise and fall time: ≤ 20 ns
- Output load: 1TTL Gate +100 pF
- Reference levels for measuring timing: 0.8 V, 2.0 V

Read Cycle

Parameter	Symbol	Min	Max	Unit	Test conditions
Address to output delay	t_{ACC}	—	150	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{CE}$ to output delay	t_{CE}	—	150	ns	$\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{OE}$ to output delay	t_{OE}	10	75	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Address to output hold	t_{OH}	0	—	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{OE}$ ($\overline{CE}$) high to output float*[1]	t_{DF}	0	50	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{RES}$ low to output float*[1]	t_{DFR}	0	350	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{RES}$ to output delay	t_{RR}	0	450	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}

Write Cycle

Parameter	Symbol	Min*[2]	Typ	Max	Unit	Test conditions
Address setup time	t_{AS}	0	—	—	ns	
Address hold time	t_{AH}	150	—	—	ns	
$\overline{CE}$ to write setup time ($\overline{WE}$ controlled)	t_{CS}	0	—	—	ns	
$\overline{CE}$ hold time ($\overline{WE}$ controlled)	t_{CH}	0	—	—	ns	
$\overline{WE}$ to write setup time ($\overline{CE}$ controlled)	t_{WS}	0	—	—	ns	
$\overline{WE}$ hold time ($\overline{CE}$ controlled)	t_{WH}	0	—	—	ns	
$\overline{OE}$ to write setup time	t_{OES}	0	—	—	ns	
$\overline{OE}$ hold time	t_{OEH}	0	—	—	ns	
Data setup time	t_{DS}	100	—	—	ns	
Data hold time	t_{DH}	10	—	—	ns	
$\overline{WE}$ pulse width ($\overline{WE}$ controlled)	t_{WP}	250	—	—	ns	
$\overline{CE}$ pulse width ($\overline{CE}$ controlled)	t_{CW}	250	—	—	ns	
Data latch time	t_{DL}	300	—	—	ns	
Byte load cycle	t_{BLC}	0.55	—	30	µs	
Byte load window	t_{BL}	100	—	—	µs	
Write cycle time	t_{WC}	—	—	10*[3]	ms	
Time to device busy	t_{DB}	120	—	—	ns	
Write start time	t_{DW}	150*[4]	—	—	ns	
Reset protect time	t_{RP}	100	—	—	µs	
Reset high time*[5]	t_{RES}	1	—	—	µs	

Notes: 1. t_{DF} and t_{DFR} are defined as the time at which the outputs achieve the open circuit conditions and are no longer driven.
2. Use this device in longer cycle than this value.
3. t_{WC} must be longer than this value unless polling techniques or RDY/$\overline{Busy}$ are used. This device automatically completes the internal write operation within this value.
4. Next read or write operation can be initiated after t_{DW} if polling techniques or RDY/$\overline{Busy}$ are used.
5. This parameter is sampled and not 100% tested.
6. A7 through A16 are page addresses and these addresses are latched at the first falling edge of $\overline{WE}$.
7. A7 through A16 are page addresses and these addresses are latched at the first falling edge of $\overline{CE}$.
8. See AC read characteristics.

AC Characteristics

(Ta = -40 to +85°C, V_{CC} = 2.7 V to 5.5 V)

Test Conditions

- Input pulse levels: 0.4 V to 2.4 V, 0 V to V_{CC} ($\overline{RES}$ pin)
- Input rise and fall time: ≤ 20 ns
- Output load: 1TTL Gate +100 pF
- Reference levels for measuring timing: 0.8 V, 2.0 V

Read Cycle

Parameter	Symbol	Min	Max	Unit	Test conditions
Address to output delay	t_{ACC}	—	250	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{CE}$ to output delay	t_{CE}	—	250	ns	$\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{OE}$ to output delay	t_{OE}	10	120	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Address to output hold	t_{OH}	0	—	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{OE}$ ($\overline{CE}$) high to output float*[1]	t_{DF}	0	50	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{RES}$ low to output float*[1]	t_{DFR}	0	350	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{RES}$ to output delay	t_{RR}	0	600	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}

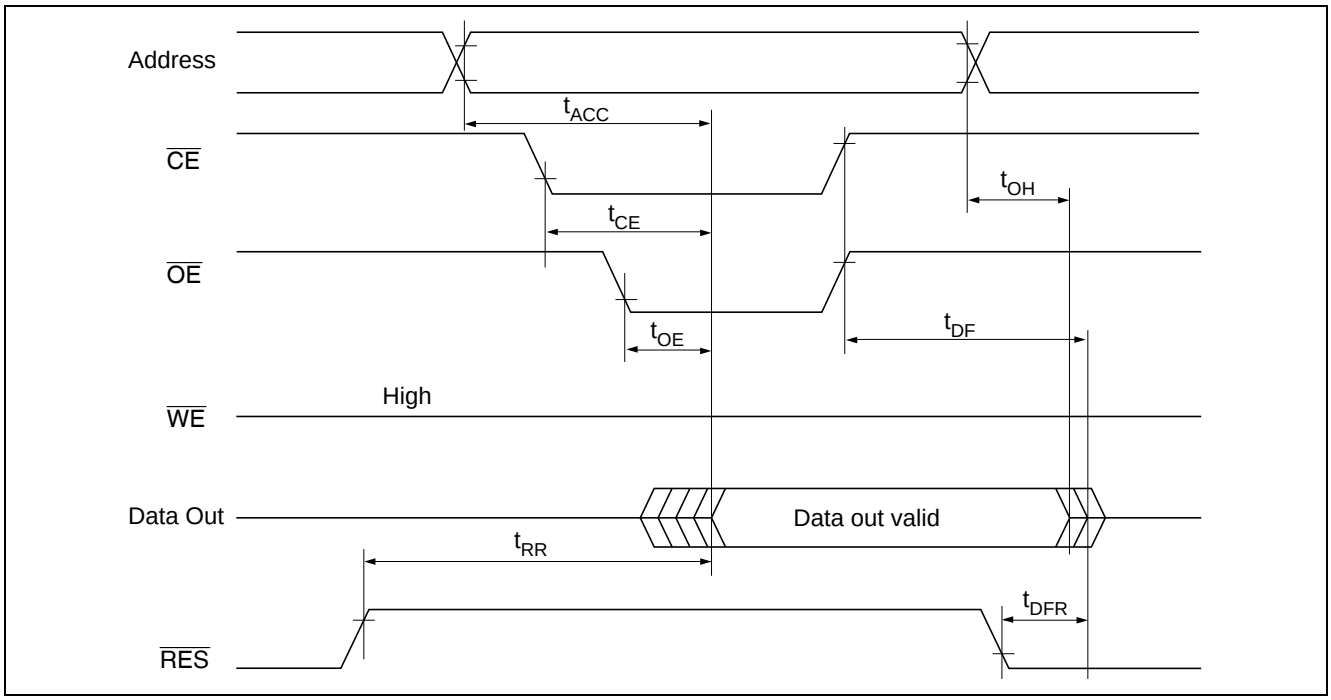
Write Cycle

Parameter	Symbol	Min*[2]	Typ	Max	Unit	Test conditions
Address setup time	t_{AS}	0	—	—	ns	
Address hold time	t_{AH}	150	—	—	ns	
$\overline{CE}$ to write setup time ($\overline{WE}$ controlled)	t_{CS}	0	—	—	ns	
$\overline{CE}$ hold time ($\overline{WE}$ controlled)	t_{CH}	0	—	—	ns	
$\overline{WE}$ to write setup time ($\overline{CE}$ controlled)	t_{WS}	0	—	—	ns	
$\overline{WE}$ hold time ($\overline{CE}$ controlled)	t_{WH}	0	—	—	ns	
$\overline{OE}$ to write setup time	t_{OES}	0	—	—	ns	
$\overline{OE}$ hold time	t_{OEH}	0	—	—	ns	
Data setup time	t_{DS}	100	—	—	ns	
Data hold time	t_{DH}	10	—	—	ns	
$\overline{WE}$ pulse width ($\overline{WE}$ controlled)	t_{WP}	250	—	—	ns	
$\overline{CE}$ pulse width ($\overline{CE}$ controlled)	t_{CW}	250	—	—	ns	
Data latch time	t_{DL}	750	—	—	ns	
Byte load cycle	t_{BLC}	1.0	—	30	µs	
Byte load window	t_{BL}	100	—	—	µs	
Write cycle time	t_{WC}	—	—	10*[3]	ms	
Time to device busy	t_{DB}	120	—	—	ns	
Write start time	t_{DW}	250*[4]	—	—	ns	
Reset protect time	t_{RP}	100	—	—	µs	
Reset high time*[5]	t_{RES}	1	—	—	µs	

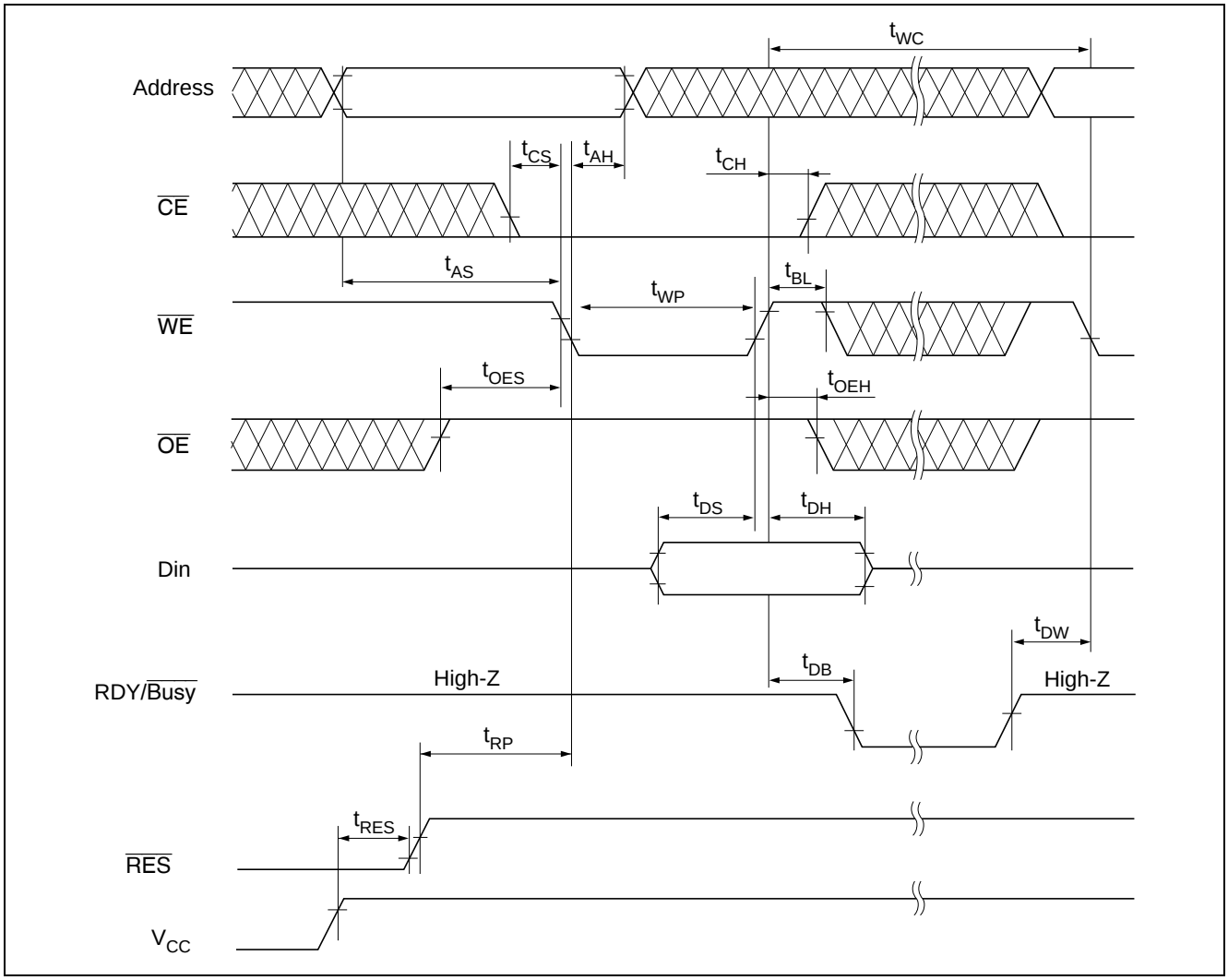
Notes: 1. t_{DF} and t_{DFR} are defined as the time at which the outputs achieve the open circuit conditions and are no longer driven.
2. Use this device in longer cycle than this value.
3. t_{WC} must be longer than this value unless polling techniques or RDY/$\overline{Busy}$ are used. This device automatically completes the internal write operation within this value.
4. Next read or write operation can be initiated after t_{DW} if polling techniques or RDY/$\overline{Busy}$ are used.
5. This parameter is sampled and not 100% tested.
6. A7 through A16 are page addresses and these addresses are latched at the first falling edge of $\overline{WE}$.
7. A7 through A16 are page addresses and these addresses are latched at the first falling edge of $\overline{CE}$.
8. See AC read characteristics.

Timing Waveforms

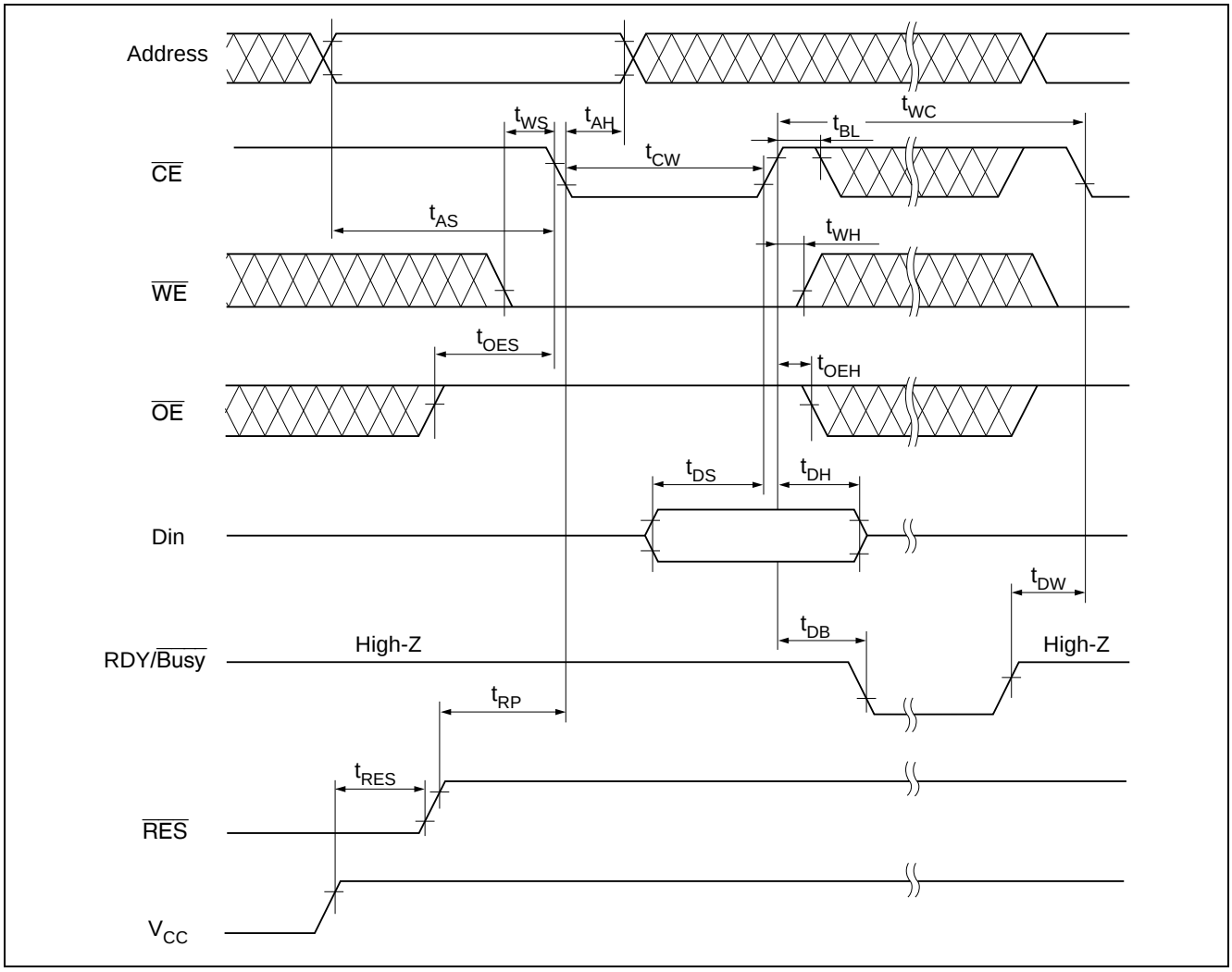
Read Timing Waveform



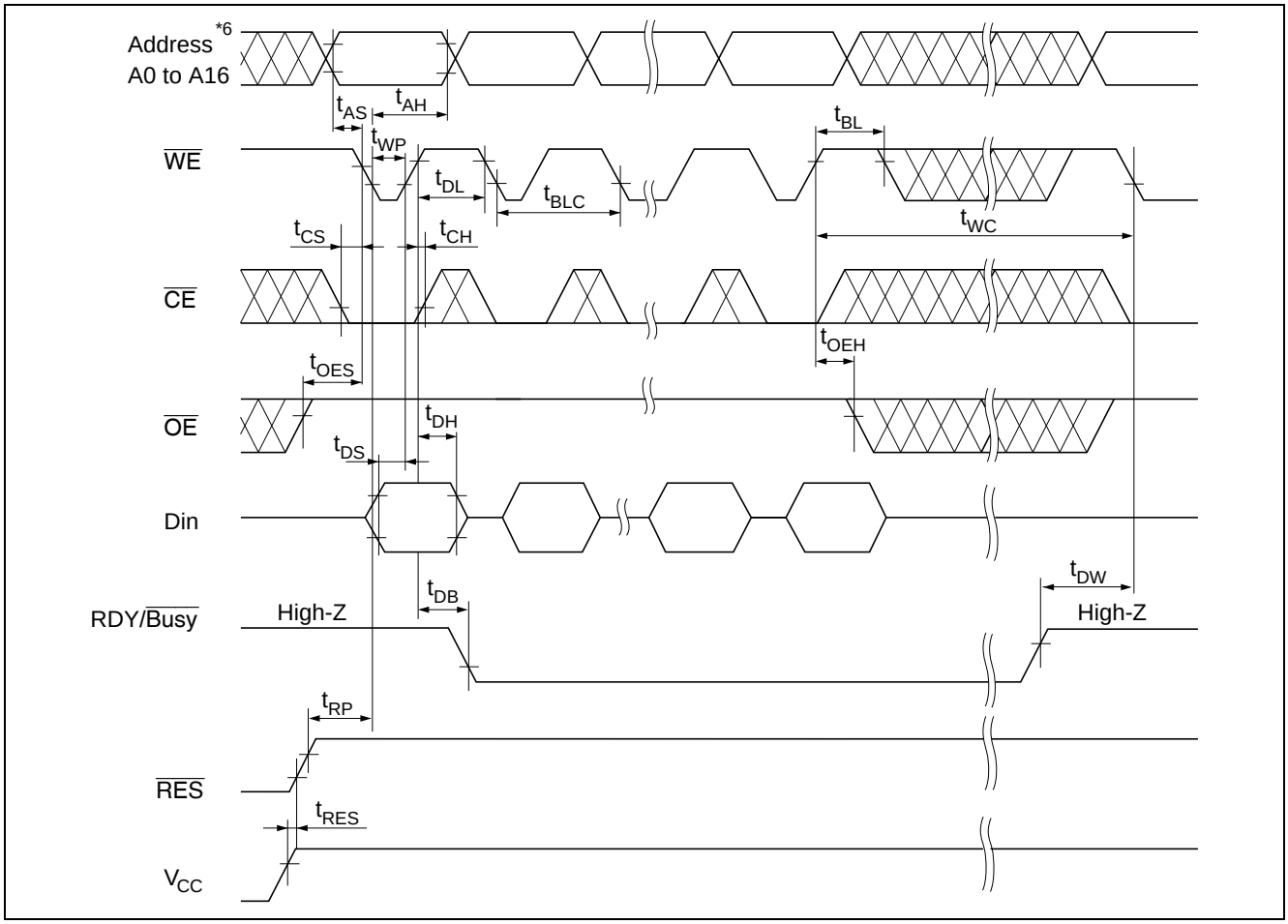
Byte Write Timing Waveform (1) ($\overline{WE}$ Controlled)



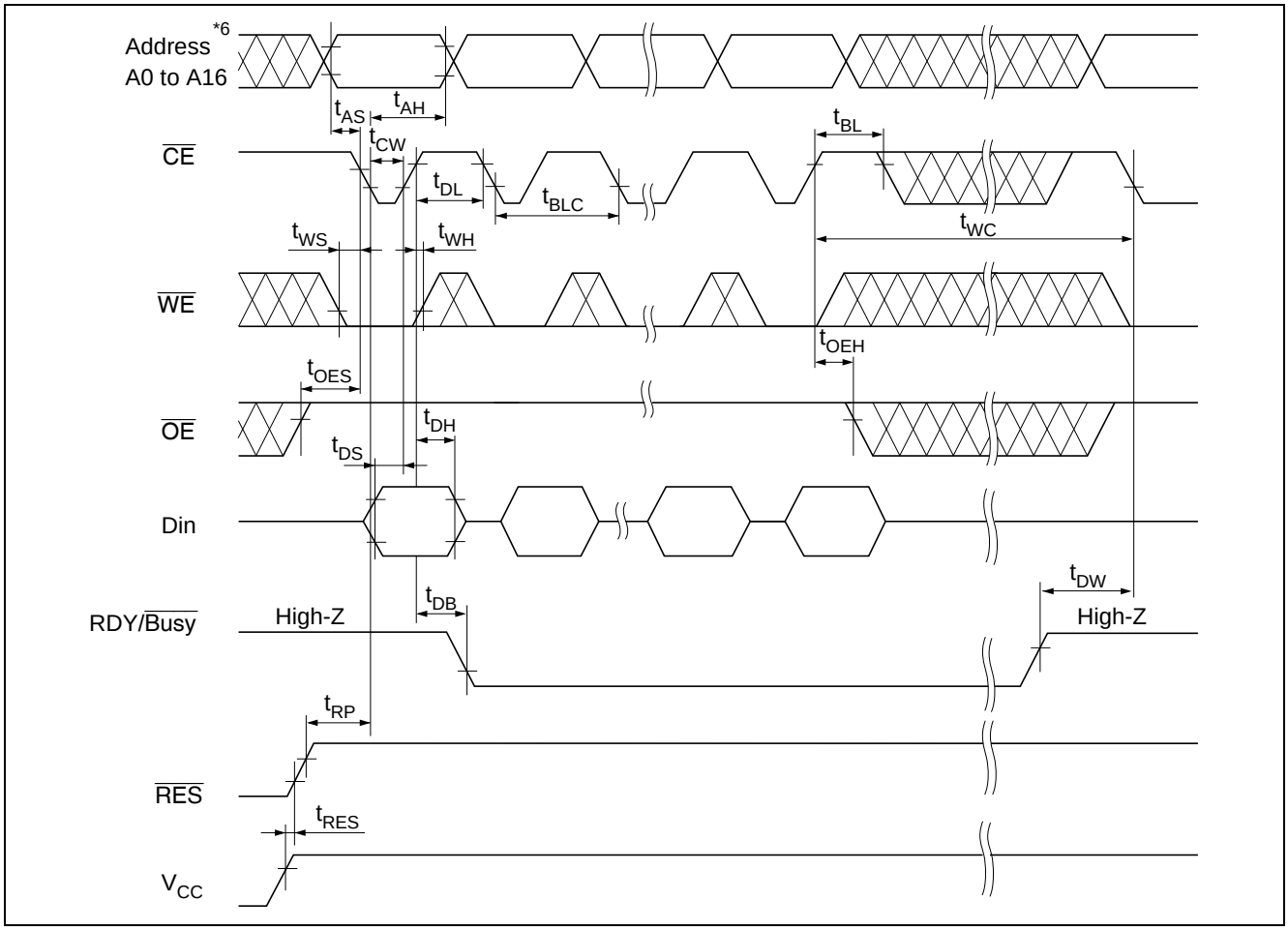
Byte Write Timing Waveform (2) ($\overline{CE}$ Controlled)



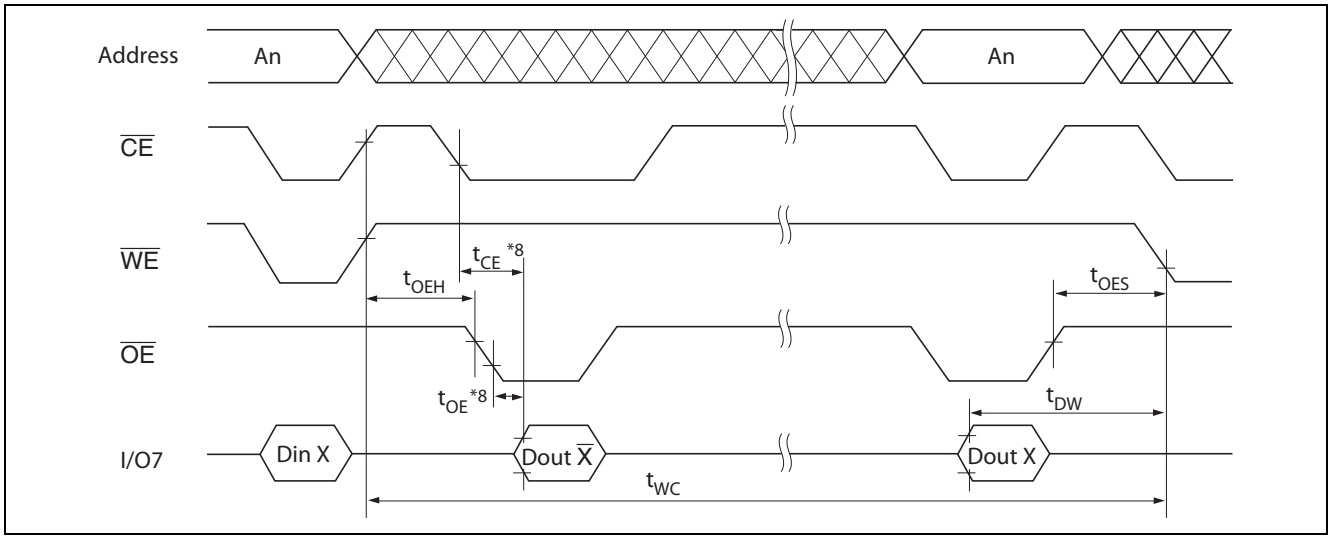
Page Write Timing Waveform (1) ($\overline{WE}$ Controlled)



Page Write Timing Waveform (2) ($\overline{CE}$ Controlled)



Data Polling Timing Waveform

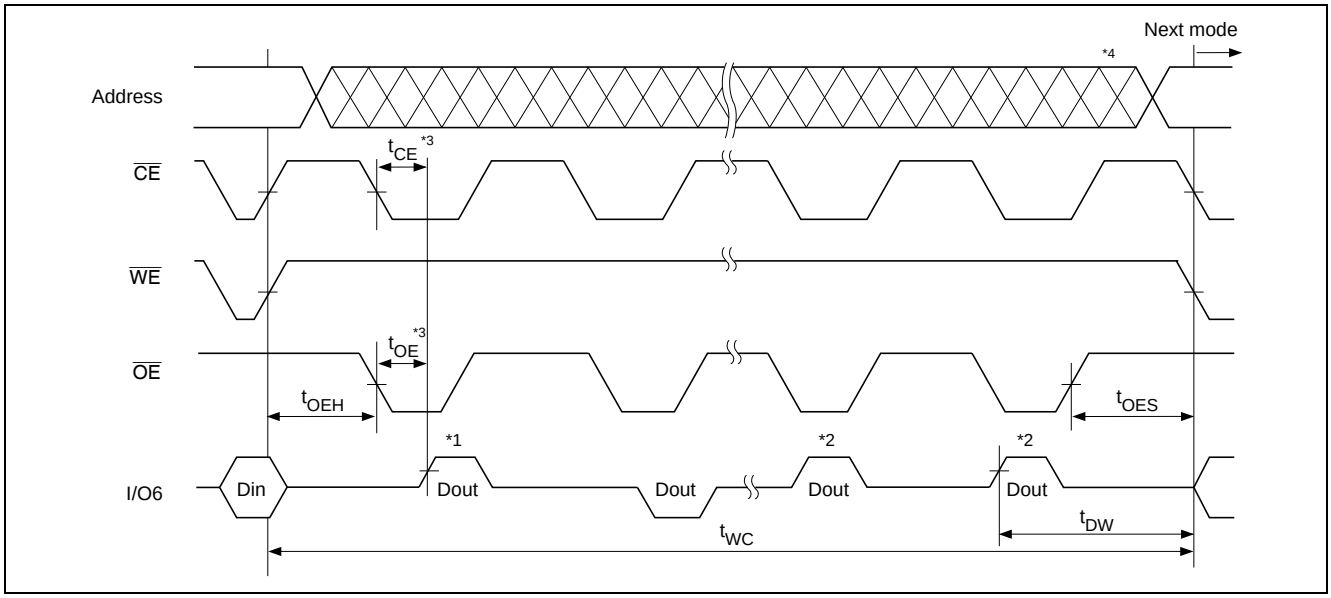


Toggle bit

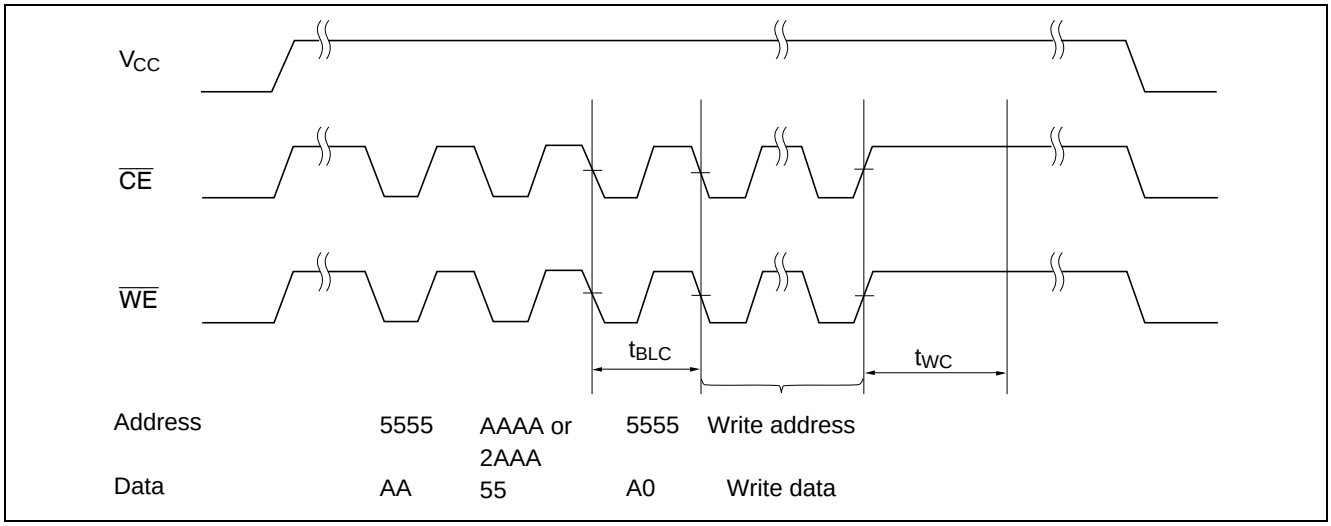
This device provide another function to determine the internal programming cycle. If the EEPROM is set to read mode during the internal programming cycle, I/O6 will charge from “1” to “0” (toggling) for each read. When the internal programming cycle is finished, toggling of I/O6 will stop and the device can be accessible for next read or program.

Notes: 1. I/O6 beginning state is “1”.
2. I/O6 ending state will vary.
3. See AC read characteristics.
4. Any location can be used, but the address must be fixed.

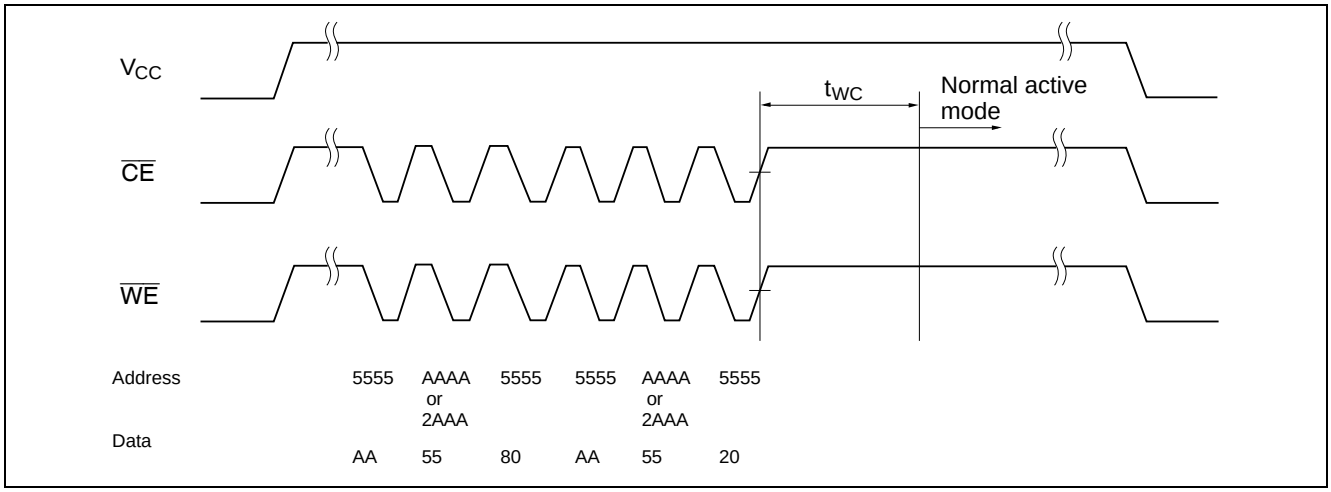
Toggle bit Waveform



Software Data Protection Timing Waveform (1) (in protection mode)



Software Data Protection Timing Waveform (2) (in non-protection mode)



Functional Description

Automatic Page Write

Page-mode write feature allows 1 to 128 bytes of data to be written into the EEPROM in a single write cycle. Following the initial byte cycle, an additional 1 to 127 bytes can be written in the same manner. Each additional byte load cycle must be started within 30 µs from the preceding falling edge of $\overline{WE}$ or $\overline{CE}$. When $\overline{CE}$ or $\overline{WE}$ is kept high for 100 µs after data input, the EEPROM enters write mode automatically and the input data are written into the EEPROM.

$\overline{Data}$ Polling

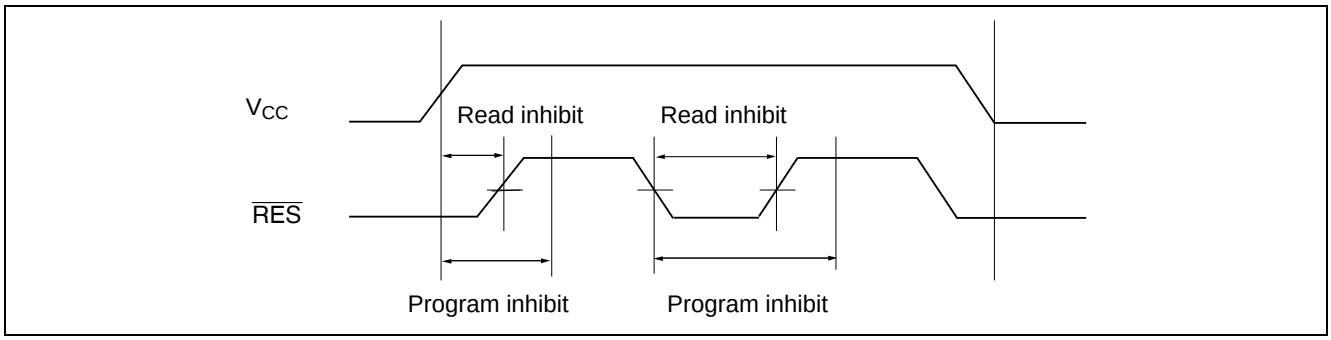
$\overline{Data}$ polling allows the status of the EEPROM to be determined. If EEPROM is set to read mode during a write cycle, an inversion of the last byte of data to be loaded outputs from I/O7 to indicate that the EEPROM is performing a write operation.

RDY/$\overline{Busy}$ Signal

RDY/$\overline{Busy}$ signal also allows status of the EEPROM to be determined. The RDY/$\overline{Busy}$ signal has high impedance except in write cycle and is lowered to V_{OL} after the first write signal. At the end of write cycle, the RDY/$\overline{Busy}$ signal changes state to high impedance.

$\overline{RES}$ Signal

When $\overline{RES}$ is low, the EEPROM cannot be read or programmed. Therefore, data can be protected by keeping $\overline{RES}$ low when V_{CC} is switched. $\overline{RES}$ should be high during read and programming because it doesn't provide a latch function.



$\overline{WE}$, $\overline{CE}$ Pin Operation

During a write cycle, addresses are latched by the falling edge of $\overline{WE}$ or $\overline{CE}$, and data is latched by the rising edge of $\overline{WE}$ or $\overline{CE}$.

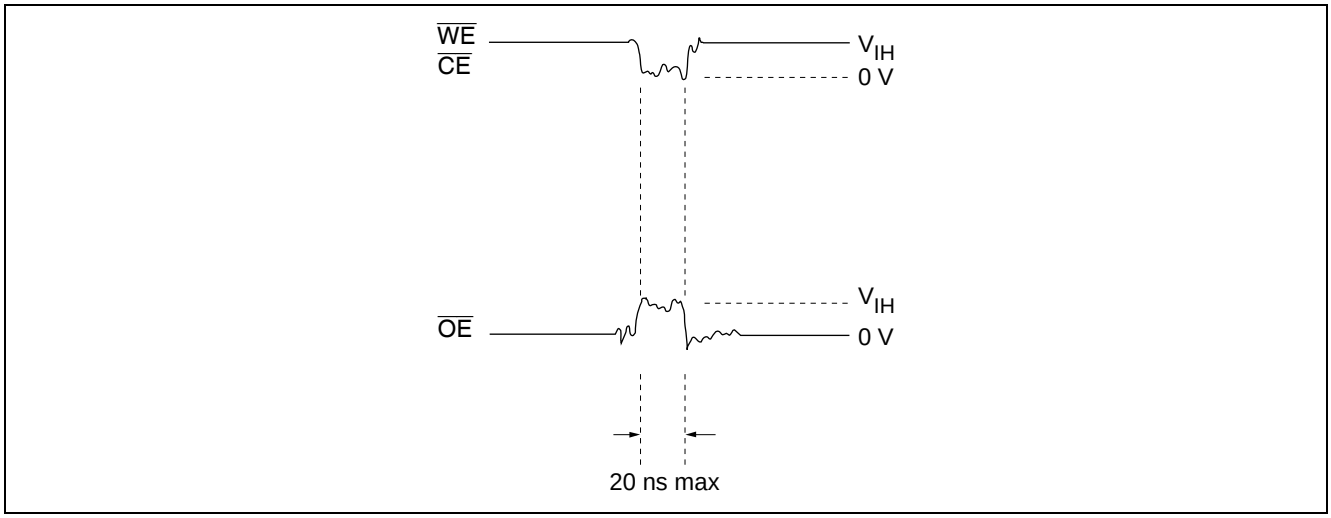
Write/Erase Endurance and Data Retention Time

The endurance is 10^4 cycles (1% cumulative failure rate). The data retention time is more than 10 years.

Data Protection

To prevent this phenomenon, this device has a noise cancellation function that cuts noise if its width is 20 ns or less in program mode.

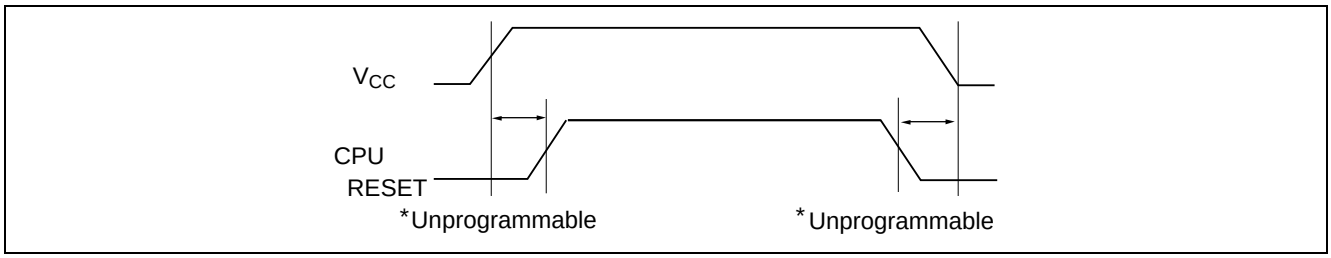
1. Data Protection against Noise on Control Pins ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) during Operation
   During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to programming mode by mistake. Be careful not to allow noise of a width of more than 20 ns on the control pins.



2. Data Protection at V_{CC} On/Off

When V_{CC} is turned on or off, noise on the control pins generated by external circuits (CPU, etc) may act as a trigger and turn the EEPROM to program mode by mistake. To prevent this unintentional programming, the EEPROM must be kept in an unprogrammable state while the CPU is in an unstable state.

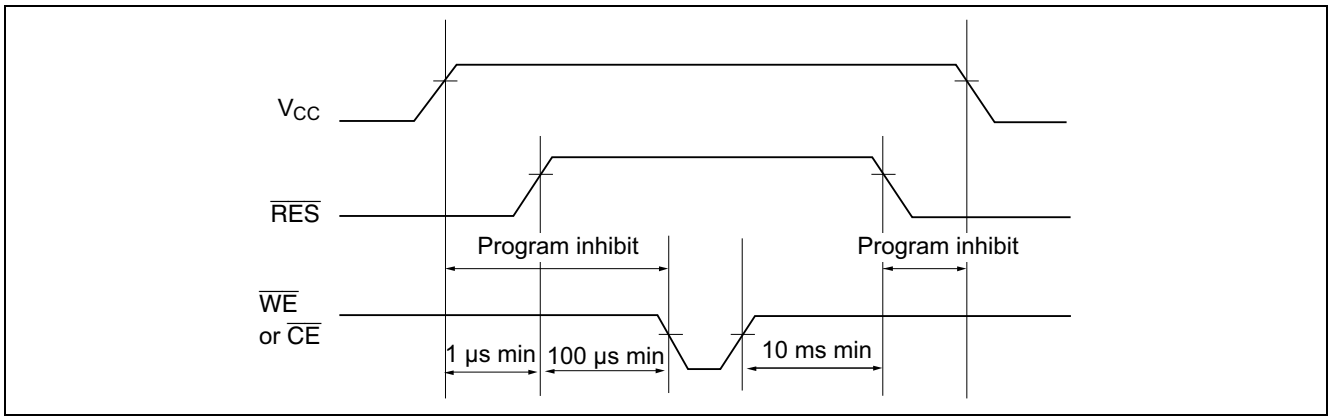
Note: The EEPROM should be kept in unprogrammable state during V_{CC} on/off by using CPU RESET signal.



2.1 Protection by $\overline{RES}$

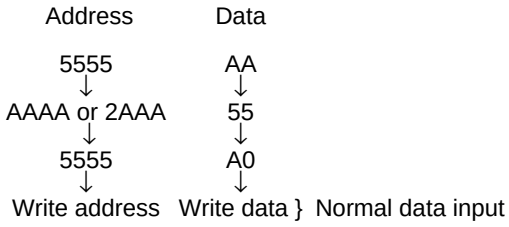
The unprogrammable state can be realized by that the CPU's reset signal inputs directly to the EEPROM's $\overline{RES}$ pin. $\overline{RES}$ should be kept V_{SS} level during V_{CC} on/off.

The EEPROM brakes off programming operation when $\overline{RES}$ becomes low, programming operation doesn't finish correctly in case that $\overline{RES}$ falls low during programming operation. $\overline{RES}$ should be kept high for 10 ms after the last data input.

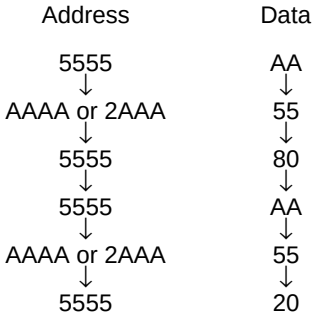


3. Software data protection

To prevent unintentional programming, this device has the software data protection (SDP) mode. The SDP is enabled by inputting the following 3 bytes code and write data. SDP is not enabled if only the 3 bytes code is input. To program data in the SDP enable mode, 3 bytes code must be input before write data.



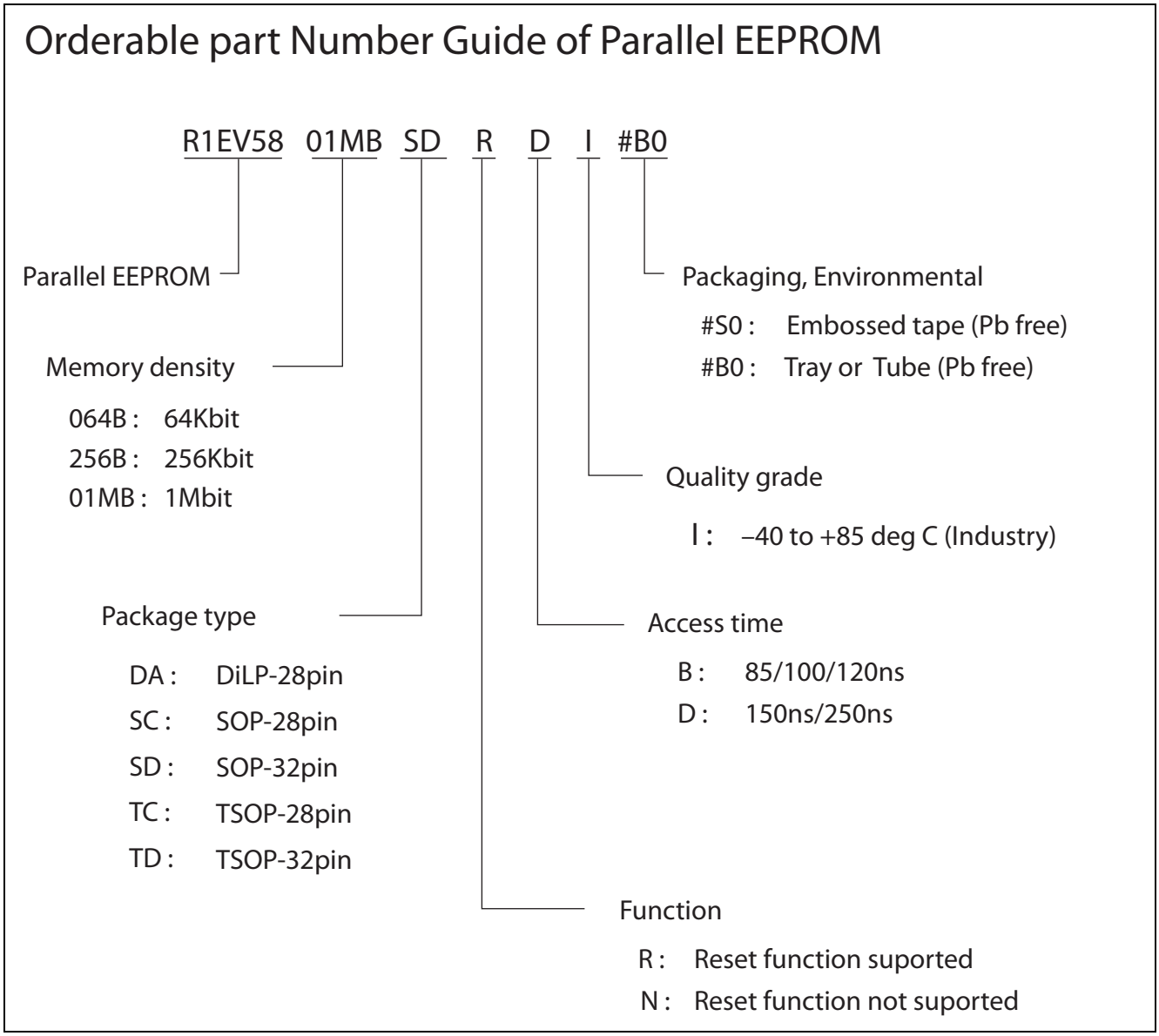
The SDP mode is disabled by inputting the following 6 bytes code. Note that, if data is input in the SDP disable cycle, data can not be written.



The software data protection is not enabled at the shipment.

Note: There are some differences between Renesas Electronics' and other company's for enable/disable sequence of software data protection. If there are any questions , please contact with Rnesas Electronics' sales offices.

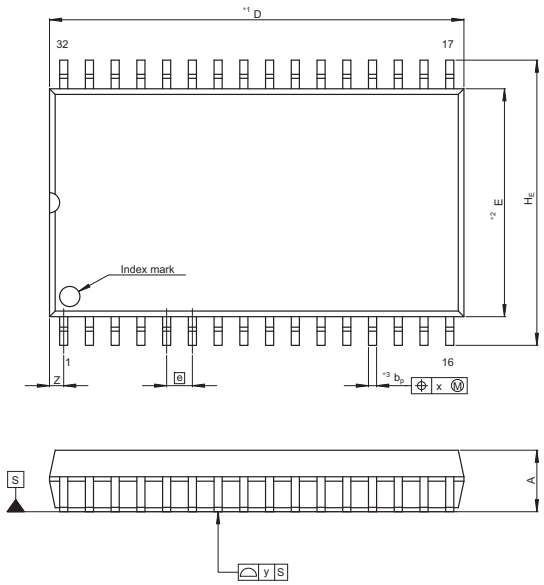
Orderable part Number Guide

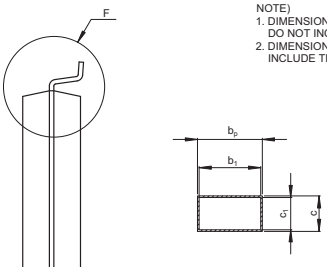


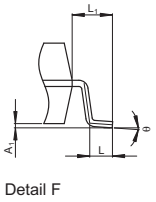
Package Dimensions

R1EV5801MBSD Series (PRSP0032DC-A / Previous code: FP-32DV)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP32-11.3x20.45-1.27	PRSP0032DC-A	FP-32D/FP-32DV	1.3g





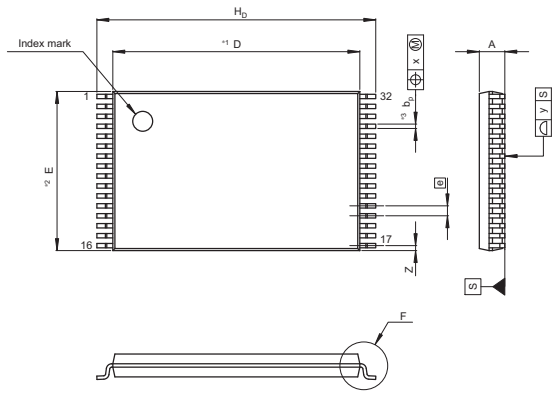


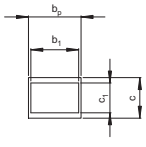
NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.

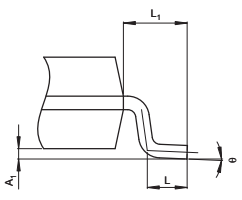
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	20.45	20.95
E	—	11.30	—
A_2	—	—	—
A_1	0.05	0.15	0.27
A	—	—	3.00
b_p	0.32	0.40	0.48
b_1	—	0.38	—
c	0.17	0.22	0.27
c_1	—	0.20	—
θ	0°	—	8°
H_E	13.84	14.14	14.44
e	—	1.27	—
x	—	—	0.15
y	—	—	0.10
Z	—	—	1.00
L	0.60	0.80	1.00
L_1	—	1.42	—

R1EV5801MBTD Series (PTSA0032KD-A / Previous Code: TFP-32DAV)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TSOP(1)32-8x12.4-0.50	PTSA0032KD-A	TFP-32DA/TFP-32DAV	0.26g







NOTE)
1. DIMENSION"*1"AND"*2(Nom)" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	12.40	—
E	—	8.00	8.20
A_2	—	—	—
A_1	0.08	0.13	0.18
A	—	—	1.20
b_p	0.14	0.22	0.30
b_1	—	0.20	—
c	0.12	0.17	0.22
c_1	—	0.125	—
θ	0	—	5
H_D	13.80	14.00	14.20
e	—	0.50	—
x	—	—	0.08
y	—	—	0.10
Z	—	—	0.45
L	0.40	0.50	0.60
L_1	—	0.80	—

Revision History	R1EV5801MB Series Data Sheet

Rev.	Date	Description	
		Page	Summary
0.01	Oct 17, 2013	—	Initial issue
0.02	Oct 18, 2013	19	Orderable part Number Guide: Deletion of A and C for access time.
1.00	Jun 09, 2014	—	Delete preliminary

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