UCS81003

Automotive USB Port Power Controller with Charger Emulation

Features:

- Port Power Switch with Two Current Limit Behaviors
  - 2.9V to 5.5V source voltage range
  - Up to 3.0A current (2.85A typical) with 55 mΩ on resistance
  - Overcurrent trip or constant current limiting
  - Soft turn-on circuitry
  - Programmable current limit
  - Dynamic thermal management
  - Under and overvoltage lockout
  - Back-Drive, back-voltage protection
  - Latch or auto-recovery (low test current) fault handling
  - Selectable active-high or -low power switch enable
  - BC1.2 V_{BUS} discharge port renegotiation function
- Selectable/Automatic Cycling of Universal Serial Bus (USB) Data Line Charger Emulation Profiles
  - USB-IF BC1.2 Charging Downstream Port (CDP) and Dedicated Charging Port (DCP) modes, Chinese Telecommunications Industry Standard YD/T 1591-2009 and most Apple® Inc. and RIM® protocols standard; others as defined via the SMBus 2.0/I^2C™ protocol
  - Supports 12W charging emulation
  - USB 2.0 compliant high-speed data switch (in data pass-through, SDP and CDP modes)
  - Nine preloaded charger emulation profiles for maximum compatibility coverage of the peripheral devices
  - One custom-programmable charger emulation profile for portable device support for fully host-controlled charger emulation
- Supports Active Cables
- Self-Contained Current Monitoring and Rationing for Power-Allocation Applications
- Low-Power Attach Detection and Open-Drain (A_DET#) Pin
- Ultra-Low Power Sleep State
- Optional Split Supply Support for V_S and V_{DD} for Low-Power in System Standby States
- Wake on Attach USB
- SMBus 2.0/I^2C Communications
  - Supports block write and read
  - Multiple SMBus addresses
- Wide Operating Temperature Range: -40°C to +85°C
- IEC61000-4-2 8/15 kV Electrostatic Discharge (ESD) Immunity

Description:

The UCS81003 provides a USB port power switch for precise control of up to 3.0A continuous current (2.85A typical) with Overcurrent Limit (OCL), dynamic thermal management, latch or auto-recovery (low-test current) fault handling, selectable active-low or -high enable, under and overvoltage lockout, back-drive protection and back-voltage protection.

Split supply support for V_S and V_{DD} is an option for low power in system standby states. This gives battery-operated applications (such as on-board computers) the ability to detect attachments from a Sleep or Off state. After the Attach Detection is flagged, the system can decide to wake up and/or provide charging.

In addition to Power Switching and Current Limiting modes, the UCS81003 will automatically charge a wide variety of portable devices, including USB-IF BC1.2, YD/T-1591 (2009), most Apple Inc. and RIM, and many others. Nine preloaded charger emulation profiles maximize the compatibility coverage of the peripheral devices. Additionally, a customizable charger emulation profile is available to accommodate unique existing and future portable device handshaking/signature requirements.

The UCS81003 also provides current monitoring to allow intelligent management of system power and charge rationing for controlled delivery of current, regardless of the host power state. This is especially important for battery-operated applications that want to provide power and do not want to drain the battery excessively.

The UCS81003 is available in a 5 mm x 5 mm 28-pin VQFN package.

Applications:

- DC Power Socket Replacement
- Consumer USB Port Protection
- Consumer Device Charging Port
- Auxiliary Box Charging Feature
- Rear Seat Entertainment Consumer Access Point

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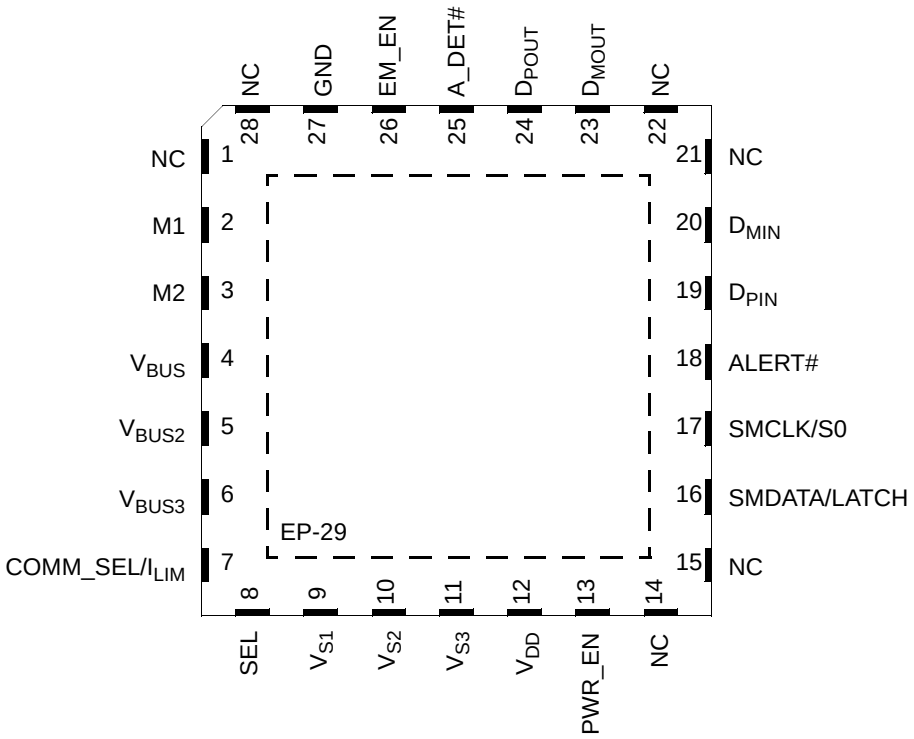
Package Type

UCS81003
5 x 5 VQFN*



* Includes Exposed Thermal Pad (EP); see Table 3-1.

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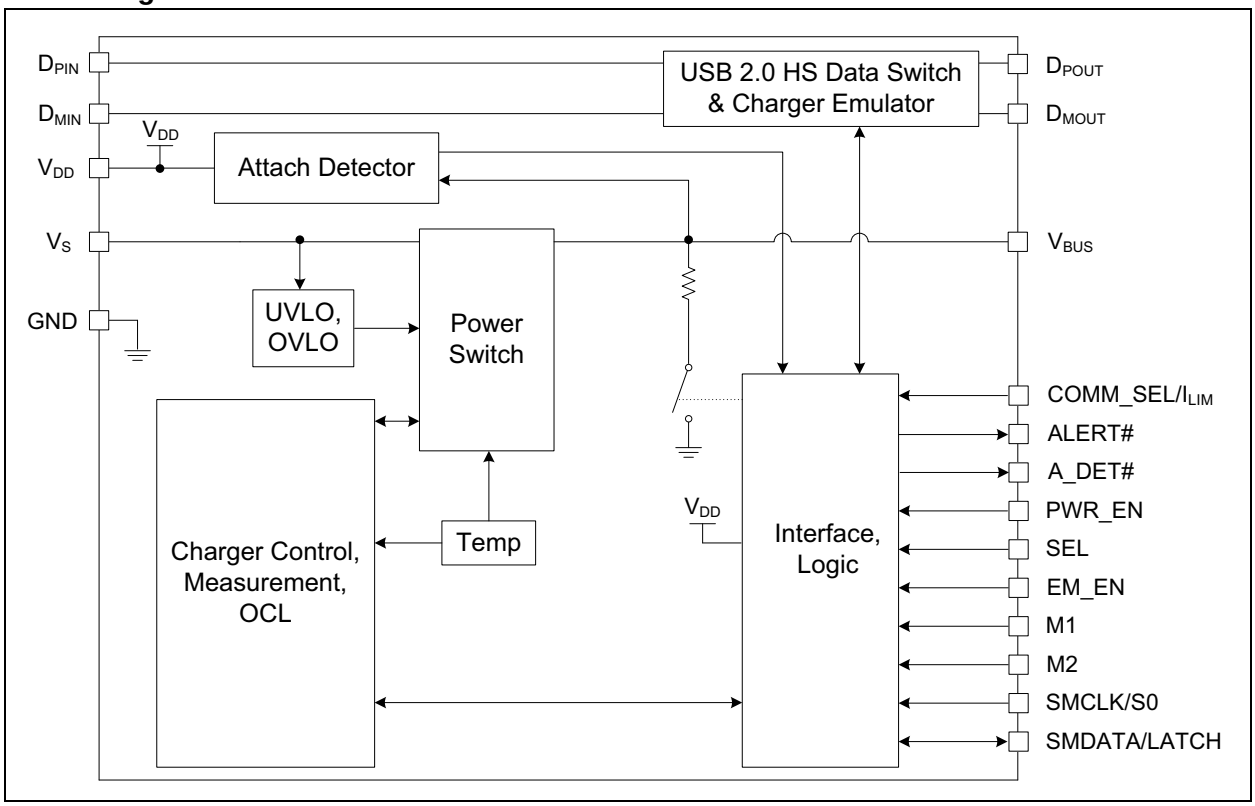
Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Voltage on V_{DD}, V_S and V_{BUS} pins ..... -0.3 to 6V

Pull-Up Voltage (V_{PULLUP}) ..... -0.3 to V_{DD} + 0.3V

Data Switch Current (I_{HSW_ON}), Switch On ..... ±50 mA

Port Power Switch Current ..... Internally limited

Data Switch Pin Voltage To Ground (D_{POUT}, D_{PIN}, D_{MOUT}, D_{MIN}); (V_{DD} powered or unpowered) ..... -0.3 to V_{DD} + 0.3V

Differential Voltage Across Open Data Switch (D_{POUT} -D_{PIN}, D_{MOUT} - D_{MIN}, D_{PIN} - D_{POUT}, D_{MIN} - D_{MOUT}) ..... V_{DD}

Voltage on any Other Pin to Ground ..... -0.3 to V_{DD} + 0.3V

Current on any Other Pin ..... ±10 mA

Package Power Dissipation ..... Table 1-1

Maximum Junction Temperature Under Bias ..... +125°C

Storage Temperature Range ..... -55°C to +150°C

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: POWER DISSIPATION SUMMARY

Board	Package	θ_{JC}	θ_{JA}	De-rating Factor Above +25°C	T_A < +25°C Power Rating	T_A < +70°C Power Rating	T_A < +85°C Power Rating
High K (see Note 1)	28-pin VQFN 5 x 5 mm	4°C/W	32°C/W	31.3 mW°/C	2470 mW	1220 mW	800 mW
Low K (see Note 1)	28-pin VQFN 5 x 5 mm	4°C/W	51°C/W	19.6 mW°/C	1620 mW	800 mW	530 mW

Note 1: Junction to ambient (θ_{JA}) is dependent on the design of the thermal vias. Without thermal vias and a thermal landing, the θ_{JA} is approximately 77°C/W, including localized PCB temperature increase. This θ_{JA} value is an estimate for a JEDEC® compliant 2S2P PCB with thermal vias.

TABLE 1-2: ELECTRICAL CHARACTERISTICS

Electrical Characteristics: Unless otherwise specified, V_{DD} = 4.5V to 5.5V, V_S = 2.9V to 5.5V, V_{PULLUP} = 3V to 5.5V, T_J = -40°C to +125°C; all Typical values at V_{DD} = V_S = 5V, T_J = +27°C.

Characteristic	Sym.	Min.	Typ.	Max.	Unit	Conditions
Power Supply						
Supply Voltage	V_{DD}	4.5	5	5.5	V	Note 1
Source Voltage	V_S	2.9	5	5.5	V	Note 1
Supply Current in Active (I_{DD_ACTIVE} + I_{VS_ACT})	I_{ACTIVE}	—	650	750	µA	Average current I_{BUS} = 0 mA, T_J < +85°C

Note 1: For split supply systems using the Attach Detection feature, V_S must not exceed V_{DD} + 150 mV.

2: This parameter is ensured by design and is not 100% tested.

3: This parameter is characterized, but not 100% production tested.

4: The current measurement full-scale range maximum value is 3.0A. However, the UCS81003 cannot report values above I_{LIM} (if $I_{BUS_R2MIN} \le I_{LIM}$) or above I_{BUS_R2MIN} (if $I_{BUS_R2MIN} > I_{LIM}$ and $I_{LIM} \le 1.68A$).

5: The Minimum and Maximum values represent the boundaries of a programmable range. Each value in the range is typical.

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TABLE 1-2: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise specified, V_{DD} = 4.5V to 5.5V, V_S = 2.9V to 5.5V, V_{PULLUP} = 3V to 5.5V, T_J = -40°C to +125°C; all Typical values at V_{DD} = V_S = 5V, T_J = +27°C.						
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
Supply Current in Sleep (I_{DD_SLEEP} + I_{VS_SLEEP})	I_{SLEEP}	—	5	15	µA	Average current $V_{PULLUP} \le V_{DD}$, T_J < +85°C
Supply Current in Detect (I_{DD_DETECT} + I_{VS_DETECT})	I_{DETECT}	—	175	—	µA	Average current, no portable device attached
Power-On Reset						
V_S Low Threshold	V_{S_UVLO}	—	2.5	—	V	V_S voltage increasing
V_S Low Hysteresis	$V_{S_UVLO_HYST}$	—	100	—	mV	V_S voltage decreasing
V_{DD} Low Threshold	V_{DD_TH}	—	4	—	V	V_{DD} voltage increasing
V_{DD} Low Hysteresis	$V_{DD_TH_HYST}$	—	500	—	mV	V_{DD} voltage decreasing
I/O Pins - SMCLK, SMDATA, EM_EN, M1, M2, PWR_EN, S0, LATCH, ALERT#, A_DET# – DC Parameters						
Output Low Voltage	V_{OL}	—	—	0.4	V	I_{SINK_IO} = 8 mA SMDATA, ALERT#, A_DET#
Input High Voltage	V_{IH}	2.1	—	—	V	PWR_EN, EM_EN, M1, M2, LATCH, S0, SMDATA, SMCLK
Input Low Voltage	V_{IL}	—	—	0.8	V	PWR_EN, EM_EN, M1, M2, LATCH, S0, SMDATA, SMCLK
Leakage Current	I_{LEAK}	—	—	±5	µA	Powered or unpowered, $V_{PULLUP} \le V_{DD}$, T_J < +85°C
Interrupt Pins - AC Parameters						
ALERT#, A_DET# Pin Blanking Time	t_{BLANK}	—	25	—	ms	
ALERT# Pin Interrupt Masking Time	t_{MASK}	—	5	—	ms	
SMBus/I²C™ Timing						
Input Capacitance	C_{IN}	—	5	—	pF	
Clock Frequency	f_{SMB}	10	—	400	kHz	
Spike Suppression	t_{SP}		—	50	ns	Note 2
Bus Free Time Stop to Start	t_{BUF}	1.3	—	—	µs	
Start Setup Time	$t_{SU:STA}$	0.6	—	—	µs	
Start Hold Time	$t_{HD:STA}$	0.6	—	—	µs	
Stop Setup Time	$t_{SU:STO}$	0.6	—	—	µs	
Data Hold Time	$t_{HD:DAT}$	0	—	—	µs	When transmitting to the master
Data Hold Time	$t_{HD:DAT}$	0.3	—	—	µs	When receiving from the master
Data Setup Time	$t_{SU:DAT}$	0.6	—	—	µs	
Clock Low Period	t_{LOW}	1.3	—	—	µs	
Clock High Period	t_{HIGH}	0.6	—	—	µs	

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Electrical Characteristics: Unless otherwise specified, V_{DD} = 4.5V to 5.5V, V_S = 2.9V to 5.5V, V_{PULLUP} = 3V to 5.5V, T_J = -40°C to +125°C; all Typical values at V_{DD} = V_S = 5V, T_J = +27°C.						
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
Propagation Delay Skew	Δt_{PD}	—	25	—	ps	R_{TERM} = 50Ω, C_{LOAD} = 5 pF
Rise/Fall Time	$t_{F/R}$	—	10	—	ns	R_{TERM} = 50Ω, C_{LOAD} = 5 pF
D_P – D_M Crosstalk	X_{TALK}	—	-40	—	dB	R_{TERM} = 50Ω, C_{LOAD} = 5 pF
Off Isolation	O_{IRR}	—	-30	—	dB	R_{TERM} = 50Ω, C_{LOAD} = 5 pF, f = 240 MHz
-3 dB Bandwidth	BW	—	1100	—	MHz	R_{TERM} = 50Ω, C_{LOAD} = 5 pF, V_{DPOUT} = V_{DMOUT} = 350 mV DC
Total Jitter	t_J	—	200	—	ps	R_{TERM} = 50Ω, C_{LOAD} = 5 pF, Rise Time = Fall Time = 500 ps at 480 Mbps (PRBS = 2^{15} – 1)
Skew of Opposite Transitions of the Same Output	$t_{SK(P)}$	—	20	—	ps	R_{TERM} = 50Ω, C_{LOAD} = 5 pF
Port Power Switch						
Port Power Switch - DC Parameter						
Overvoltage Lockout	V_{S_OV}	—	6	—	V	
On Resistance	R_{ON_PSW}	—	55	—	mΩ	4.75V < V_S < 5.25V
V_S Leakage Current	I_{LEAK_VS}	—	2.22	—	µA	Sleep state into V_S pin
Back-Voltage Protection Threshold	V_{BV_TH}	—	150	—	mV	V_{BUS} > V_S, V_S > V_{S_UVLO}
Back-Drive Current	I_{BD_1}	—	0	3	µA	V_{DD} < V_{DD_TH}, Any powered power pin to any unpowered power pin. Current out of unpowered pin (Note 3).
	I_{BD_2}	—	0	2	µA	V_{DD} < V_{DD_TH}, Any powered power pin to any unpowered power pin, except for V_{DD} to V_{BUS} in Detect power state and V_S to V_{BUS} in Active Power state. Current out of unpowered pin (Note 3).

Note 1: For split supply systems using the Attach Detection feature, V_S must not exceed V_{DD} + 150 mV.

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Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
Selectable Current Limits	I_{LIM1}	—	570	—	mA	I_{LIM} Resistor = 0 or 47 kΩ (minimum mA setting)
	I_{LIM2}	—	1000	—		I_{LIM} Resistor = 10 kΩ or 56 kΩ
	I_{LIM3}	—	1130	—		I_{LIM} Resistor = 12 kΩ or 68 kΩ
	I_{LIM4}	—	1350	—		I_{LIM} Resistor = 15 kΩ or 82 kΩ
	I_{LIM5}	—	1680	—		I_{LIM} Resistor = 18 kΩ or 100 kΩ
	I_{LIM6}	—	2050	—		I_{LIM} Resistor = 22 kΩ or 120 kΩ
	I_{LIM7}	—	2280	—		I_{LIM} Resistor = 27 kΩ or 150 kΩ
	I_{LIM8}	—	2850	3000		I_{LIM} Resistor = 33 kΩ or V_{DD}
Pin Wake Time	t_{PIN_WAKE}	—	3	—	ms	
SMBus Wake Time	t_{SMB_WAKE}	—	4	—	ms	
Idle Sleep Time	t_{IDLE_SLEEP}	—	200	—	ms	
Thermal Regulation Limit	T_{REG}	—	110	—	°C	Die Temperature at which current limit will be reduced.
Thermal Regulation Hysteresis	T_{REG_HYST}	—	10	—	°C	Hysteresis for t_{REG} functionality. Temperature must drop by this value before I_{LIM} value restored to normal operation.
Thermal Shutdown Threshold	T_{TSD}	—	135	—	°C	Die Temperature at which port power switch will turn off.
Thermal Shutdown Hysteresis	T_{TSD_HYST}	—	35	—	°C	After Shutdown due to T_{TSD} being reached, a die temperature drop is required before port power switch can be turned on again.
Auto-Recovery Test Current	I_{TEST}	—	190	—	mA	Portable device attached, V_{BUS} = 0V, Die Temp < T_{TSD}
Auto-Recovery Test Voltage	V_{TEST}	—	750	—	mV	Portable device attached, V_{BUS} = 0V before application, Die Temp < T_{TSD} Programmable, 250 - 1000 mV, default listed
Discharge Impedance	$R_{DISCHARGE}$	—	100	—	Ω	

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Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
Port Power Switch - AC Parameters						
Turn-On Delay	t_{ON_PSW}	—	0.75	—	ms	PWR_EN active toggle to switch on time, V_{BUS} discharge not active.
Turn-Off Time	$t_{OFF_PSW_INA}$	—	0.75	—	ms	PWR_EN inactive toggle to switch off time C_{BUS} = 120 µF
Turn-Off Time	$t_{OFF_PSW_ERR}$	—	1	—	ms	Overcurrent Error, V_{BUS} Min Error, or Discharge Error to switch off, C_{BUS} = 120 µF
Turn-Off Time	$t_{OFF_PSW_ERR}$	—	100	—	ns	TSD or back-drive error to switch off, C_{BUS} = 120 µF
V_{BUS} Output Rise Time	t_{R_BUS}	—	1.1	—	ms	Measured from 10% to 90% of V_{BUS}, C_{LOAD} = 220 µF, I_{LIM} = 1.0A
Soft Turn-On Rate	$\Delta I_{BUS}/\Delta_t$	—	100	—	mA/µs	
Temperature Update Time	t_{DC_TEMP}	—	200	—	ms	Programmable 200 - 1600 ms, default listed
Short-Circuit Response Time	t_{SHORT_LIM}	—	1.5	—	µs	Time from detection of short to current limit applied. No C_{BUS} applied.
Short-Circuit Detection Time	t_{SHORT}	—	6	—	ms	Time from detection of short to port power switch disconnect and ALERT# pin assertion.
Latched Mode Cycle Time	t_{UL}	—	7	—	ms	From PWR_EN edge transition from inactive to active to begin error recovery.
Auto-Recovery Mode Cycle Time	t_{CYCLE}	—	25	—	ms	Time delay before error condition check. Programmable 10-25 ms, default listed.
Auto-Recovery Delay	t_{RST}	—	20	—	ms	Portable device attached, V_{BUS} must be ≥ V_{TEST} after this time. Programmable 10-25 ms, default listed.
Discharge Time	$t_{DISCHARGE}$	—	200	—	ms	Amount of time discharge resistor applied. Programmable 100-400 ms, default listed.

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Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
Port Power Switch Operation With Trip Mode Current Limiting						
Region 2 Current Keep-Out	I_{BUS_R2MIN}	—	0.12	—	A	
Minimum V_{BUS} Allowed at Output	V_{BUS_MIN}	1.5	2.0	2.25	V	Note 5
Port Power Switch Operation with Constant Current Limiting (Variable Slope)						
Region 2 Current Keep-Out	I_{BUS_R2MIN}	—	1.68	—	A	
Minimum V_{BUS} Allowed at Output	V_{BUS_MIN}	1.5	2.0	2.25	V	Note 5
Current Measurement - DC						
Current Measurement Range	I_{BUS_M}	0	—	2988.6	mA	Range 0 – 255 LSB (see Note 4)
Reported Current Measurement Resolution	D_{IBUS_M}	—	11.72	—	mA	1 LSB
Current Measurement Accuracy		—	±2	—	%	180 mA < I_{BUS} < I_{LIM}
		—	±2	—	LSB	I_{BUS} < 180 mA
Current Measurement - AC						
Sampling Rate		—	500	—	µs	
Charge Rationing - DC						
Accumulated Current Measurement Accuracy		—	±4.5	—	%	
Charge Rationing - AC						
Current Measurement Update Time	t_{PCYCLE}	—	1	—	s	
Attach/Removal Detection						
V_{BUS} Bypass - DC						
On Resistance	R_{ON_BYP}	—	50	—	Ω	
Leakage Current	I_{LEAK_BYP}	—	—	3	µA	Switch off, T_A < +85°C, Note 2
Current Limit	I_{DET_CHG}/I_{BUS_BYP}	—	2	—	mA	V_{DD} = 5V and V_{BUS} > 4.75V
Attach/Removal Detection - DC						
Attach Detection Threshold	I_{DET_QUAL}	—	800	—	µA	Programmable 200 – 1000 µA, default listed.

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Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
Primary Removal Detection Threshold	$I_{REM_QUAL_ACT}$	—	700	—	µA	Programmable 100 – 900 µA, default listed, Active Power state
		—	800	—	µA	Programmable 200 – 1000 µA, default listed, Detect power state (see **Section 8.4 "Removal Detection"**).
Attach/Removal Detection - AC						
Attach Detection Time	t_{DET_QUAL}	—	100	—	ms	Time from Attach to A_DET# assert
Removal Detection Time	t_{REM_QUAL}	—	1000	—	ms	
Allowed Charge Time	t_{DET_CHARGE}	—	800	—	ms	C_{BUS} = 500 µF maximum, Programmable 200 – 2000 ms, default listed.
Charger Emulation Profile						
General Emulation - DC						
Charging Current Threshold	I_{BUS_CHG}	—	175.8	—	mA	Default
Charging Current Threshold Range	$I_{BUS_CHG_RNG}$	11.72	—	175.8	mA	Note 5
DP-DM Shunt Resistor Value	R_{DCP_RES}		—	200	Ω	Connected between D_{POUT} and D_{MOUT}, 0V < D_{POUT} = D_{MOUT} < 3V
Response Magnitude (voltage divider option resistance range)	SX_RXMAG_DVDR	93	—	200	kΩ	Note 5
Resistor Ratio Range (voltage divider option)	SX_RATIO	0.25	—	0.66	V/V	Note 5
Resistor Ratio Accuracy (voltage divider option)	SX_RATIO_ ACC	—	±0.5	—	%	Average over range
Response Magnitude (resistor option range)	SX_RXMAG_RES	1.8	—	150	kΩ	Note 5
Internal Resistor Tolerance (resistor option)	SX_RXMAG_RES _ACC	—	±10	—	%	Average over range
Response Magnitude (voltage option range)	SX_RXMAG_VOLT	0.4	—	2.2	V	Note 5
Voltage Option Accuracy	SX_RXMAG_VOLT _ACC	—	±1	—	%	No load, average over range
Voltage Option Accuracy	SX_RXMAG_VOLT _ACC_ 150	—	-6	—	%	150 µA load, average over range
Voltage Option Accuracy	SX_RXMAG_VOLT _ACC_ 250	—	-10	—	%	250 µA load, average over range

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2: This parameter is ensured by design and is not 100% tested.

3: This parameter is characterized, but not 100% production tested.

4: The current measurement full-scale range maximum value is 3.0A. However, the UCS81003 cannot report values above I_{LIM} (if $I_{BUS_R2MIN} \leq I_{LIM}$) or above I_{BUS_R2MIN} (if $I_{BUS_R2MIN} > I_{LIM}$ and $I_{LIM} \leq 1.68A$).

5: The Minimum and Maximum values represent the boundaries of a programmable range. Each value in the range is typical.

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TABLE 1-2: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise specified, V_{DD} = 4.5V to 5.5V, V_S = 2.9V to 5.5V, V_{PULLUP} = 3V to 5.5V, T_J = -40°C to +125°C; all Typical values at V_{DD} = V_S = 5V, T_J = +27°C.						
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
Voltage Option Output	SX_RXMAG_VOLT_BC	0.5	—	—	V	D_{MOUT} = 0.6V, 250 µA load, Note 3
Response Magnitude (Zero Volt Option Range)	SX_PUPD	10	—	150	µA	SX_RXMAG_VOLT = 0 Note 5
Pull-Down Current Accuracy	SX_PUPD_ACC_3p6	—	±5	—	%	D_{POUT} or D_{MOUT} = 3.6V Compliance voltage
Pull-Down Current	SX_PUPD_ACC_BC	50	—	—	µA	Setting = 100 µA D_{POUT} or D_{MOUT} = 0.15V Compliance voltage, Note 3
Stimulus Voltage Threshold Range	SX_TH	0.3	—	2.2	V	Note 5
Stimulus Voltage Accuracy	SX_TH_ ACC	—	±2	—	%	Average over range
Stimulus Voltage Accuracy	SX_TH_ACC_BC	0.25	—	—	V	At SX_TH = 0.3V, Note 3
General Emulation - AC						
Emulation Reset Time	t_{EM_RESET}	—	50	—	ms	Default
Emulation Reset Time Range	$t_{EM_RESET_RNG}$	50	—	175	ms	Note 5
Emulation Timeout Range	$t_{EM_TIMEOUT}$	0.8	—	12.8	s	Note 5
Stimulus Delay, SX_TD Range	t_{STIM_DEL}	0	—	100	ms	Note 5
Emulation Delay	t_{RES_EM}	—	—	0.5	s	Time from set impedance to impedance appears on D_P/D_M, Note 3.

Note 1: For split supply systems using the Attach Detection feature, V_S must not exceed V_{DD} + 150 mV.

2: This parameter is ensured by design and is not 100% tested.

3: This parameter is characterized, but not 100% production tested.

4: The current measurement full-scale range maximum value is 3.0A. However, the UCS81003 cannot report values above I_{LIM} (if $I_{BUS_R2MIN} \leq I_{LIM}$) or above I_{BUS_R2MIN} (if $I_{BUS_R2MIN} > I_{LIM}$ and $I_{LIM} \leq 1.68A$).

5: The Minimum and Maximum values represent the boundaries of a programmable range. Each value in the range is typical.

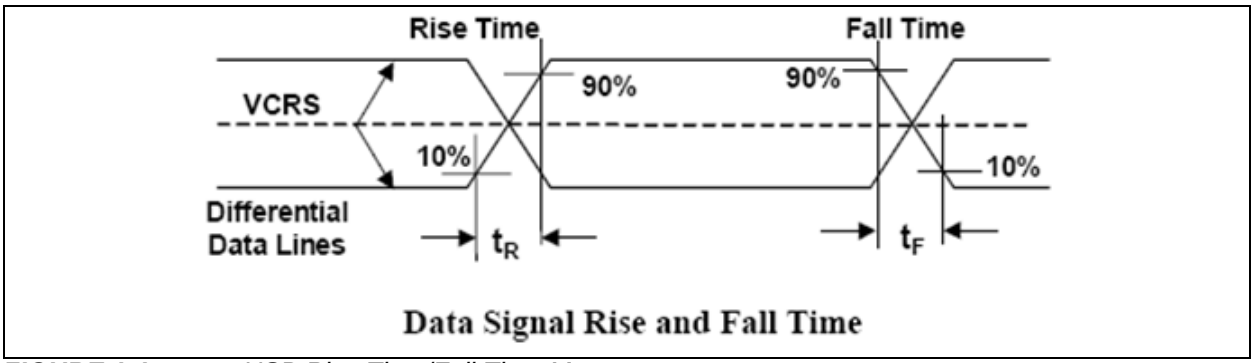

FIGURE 1-1: *USB Rise Time/Fall Time Measurement.*

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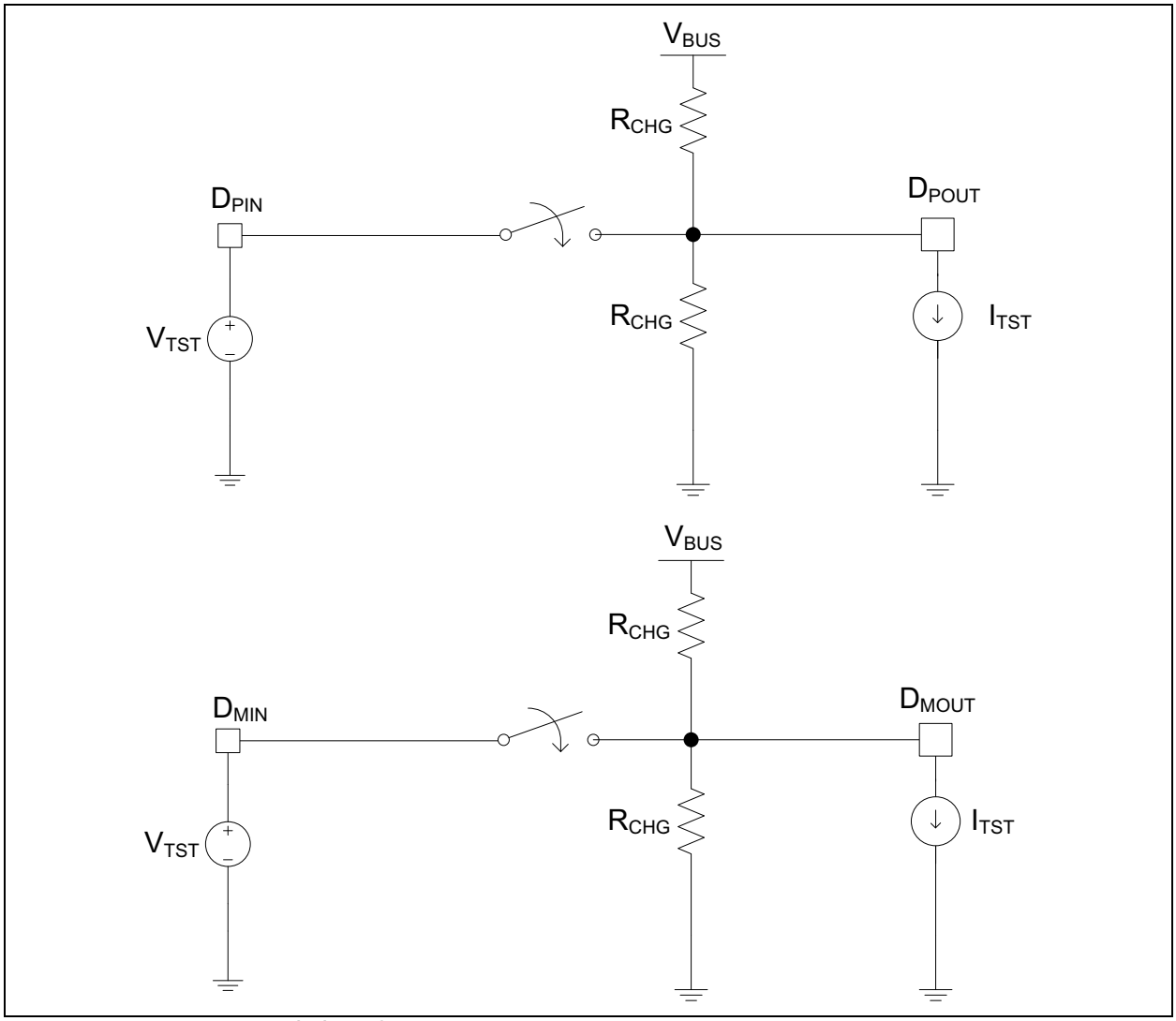

FIGURE 1-2: *Description of DC Terms.*

TABLE 1-3: TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Temperature Range	T_A	-40	—	+85	°C	
Storage Temperature Range	T_A	-55	—	+150	°C	
Thermal Package Resistances - see Table 1-1						

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, $V_{DD} = V_S = 5V$, $T_J = +27°C$.

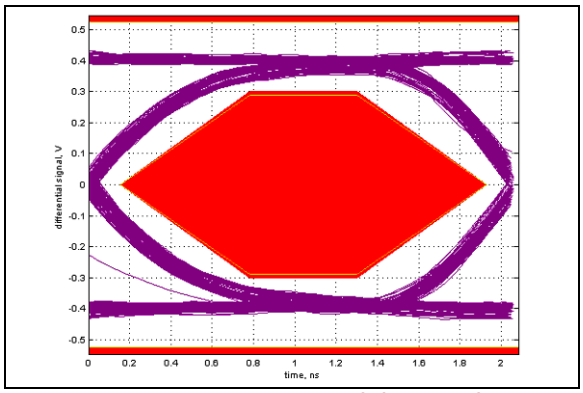

FIGURE 2-1: *USB-IF High-Speed Eye Diagram (Without Data Switch).*

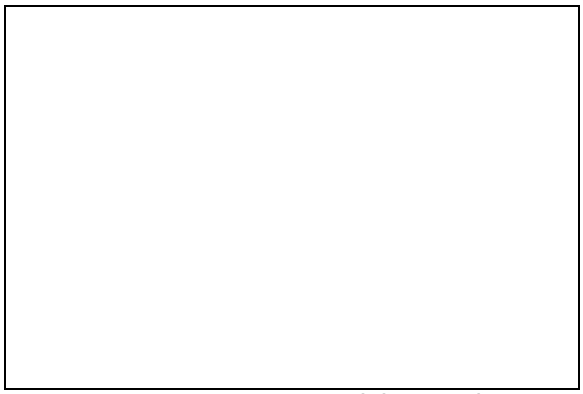

FIGURE 2-2: *USB-IF High-Speed Eye Diagram (With Data Switch).*

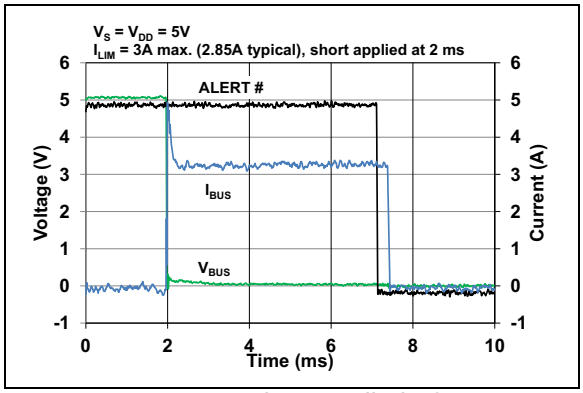

FIGURE 2-3: *Short Applied After Power-Up.*

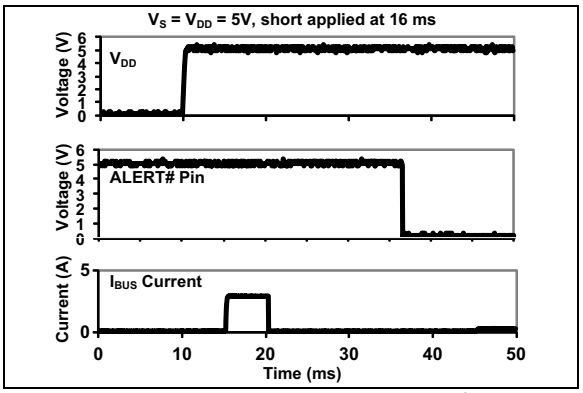

FIGURE 2-4: *Power-Up Into a Short.*

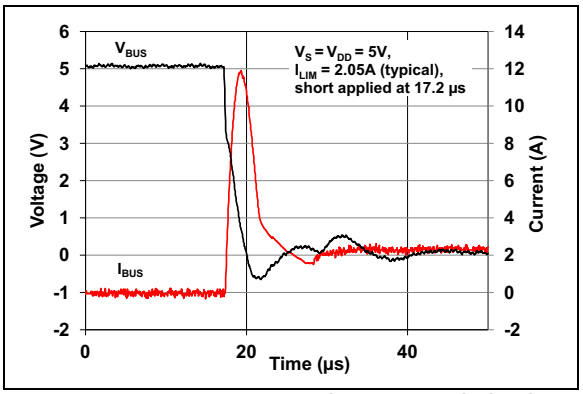

FIGURE 2-5: *Internal Power Switch Short Response.*

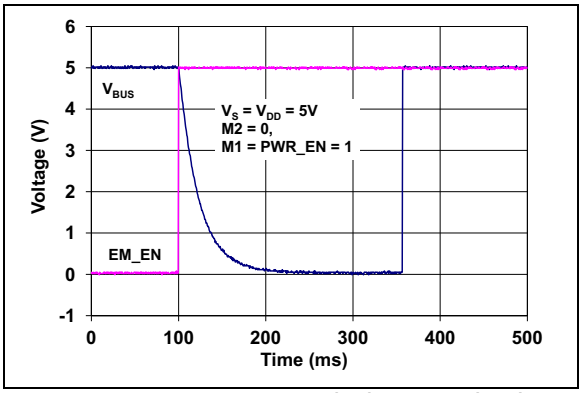

FIGURE 2-6: *V_{BUS} Discharge Behavior.*

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Note: Unless otherwise indicated, $V_{DD} = V_S = 5V$, $T_J = +27°C$.

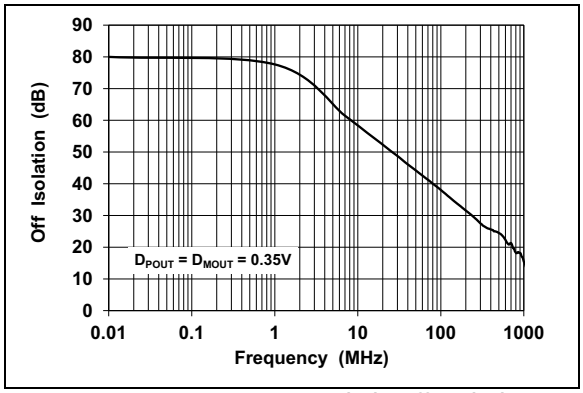

FIGURE 2-7: *Data Switch Off Isolation vs. Frequency.*

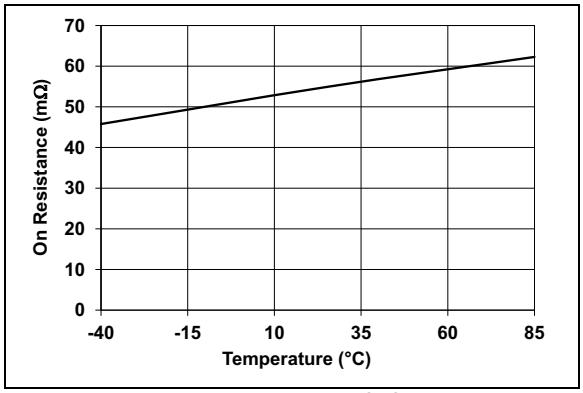

FIGURE 2-10: *Power Switch On Resistance vs. Temperature.*

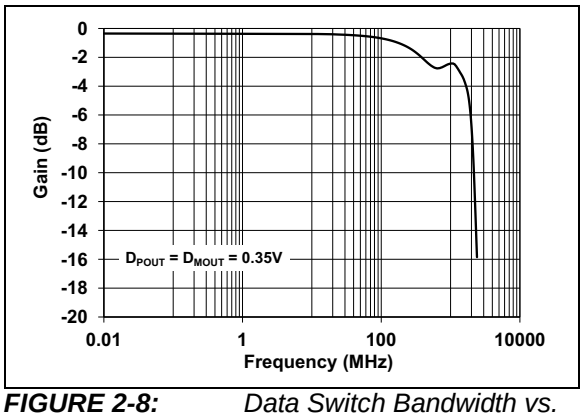

FIGURE 2-8: *Data Switch Bandwidth vs. Frequency.*

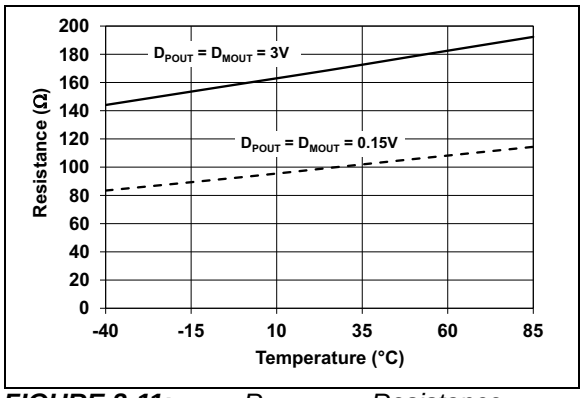

FIGURE 2-11: *R_{DCP_RES} Resistance vs.Temperature.*

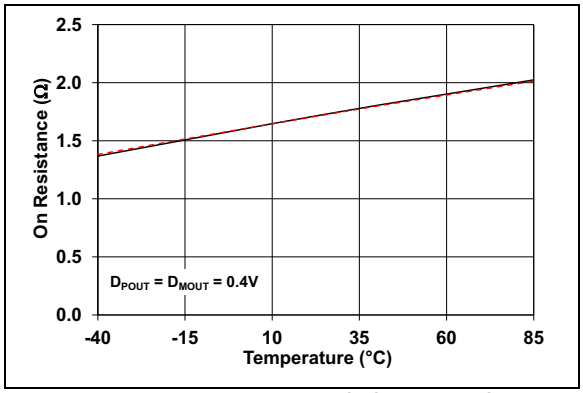

FIGURE 2-9: *Data Switch On Resistance vs. Temperature.*

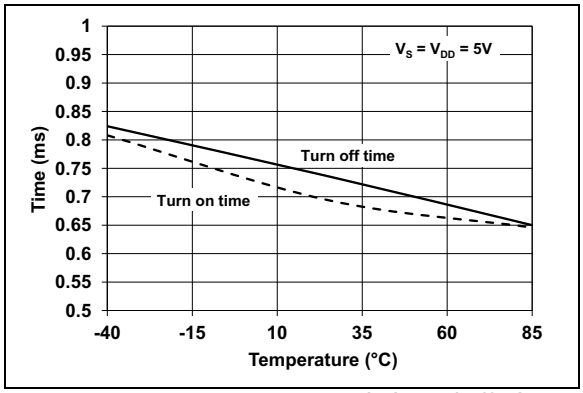

FIGURE 2-12: *Power Switch On/Off Time vs. Temperature.*

Note: Unless otherwise indicated, $V_{DD} = V_S = 5V$, $T_J = +27°C$.

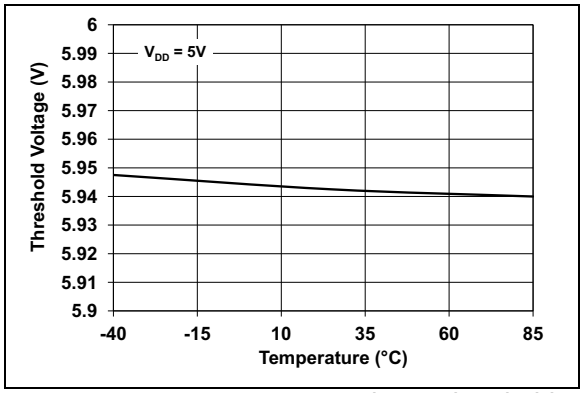

FIGURE 2-13: *V_S Overvoltage Threshold vs. Temperature.*

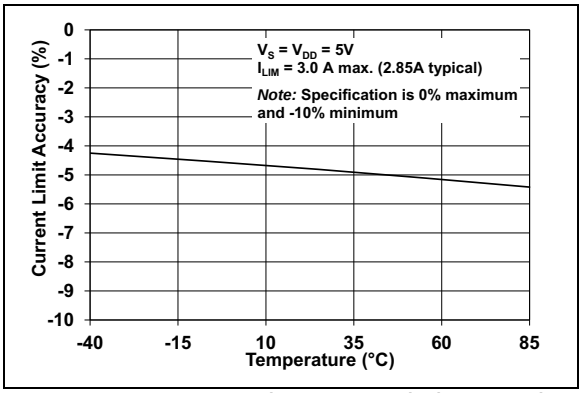

FIGURE 2-16: *Trip Current Limit Operation vs. Temperature.*

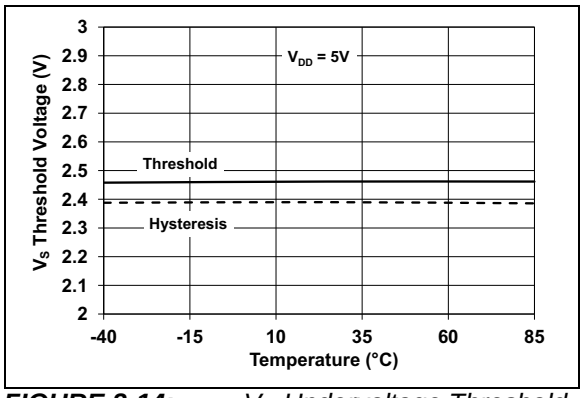

FIGURE 2-14: *V_S Undervoltage Threshold vs. Temperature.*

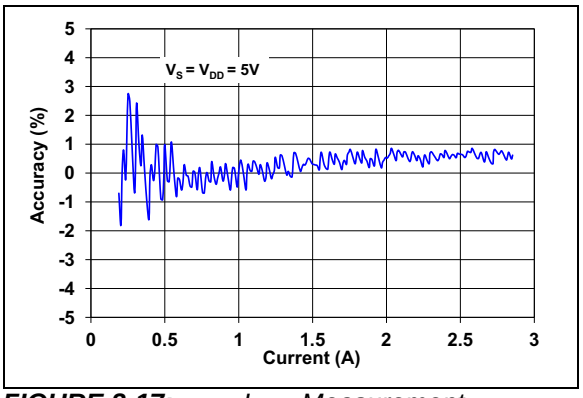

FIGURE 2-17: *I_{BUS} Measurement Accuracy.*

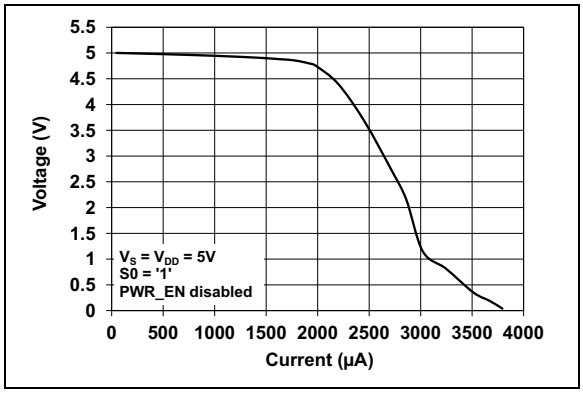

FIGURE 2-15: *Detect State V_{BUS} vs. I_{BUS}.*

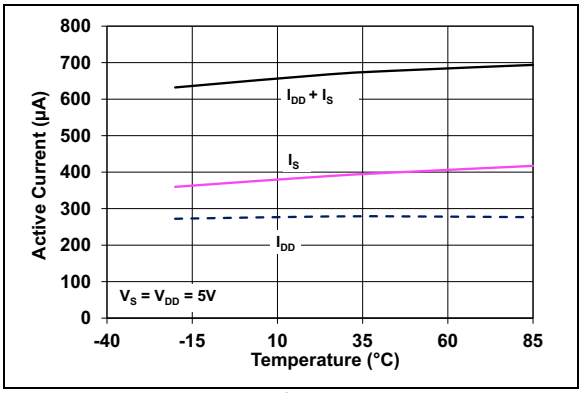

FIGURE 2-18: *Active State Current vs. Temperature.*

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3.0 PIN DESCRIPTION

The description of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

UCS81003 5x5 VQFN	Symbol	Function	Pin Type	Connection Type if Pin Not Used
1	NC	Not internally connected	n/a	Leave open
2	M1	Active mode selector input #1	DI	Connect to ground or V_{DD} (see Note 3)
3	M2	Active mode selector input #2	DI	Connect to ground or V_{DD} (see Note 3)
4	V_{BUS1}	Voltage output from Power Switch. These pins are internally connected and must be tied together.	Hi-Power Note 1	Leave open
5	V_{BUS2}			
6	V_{BUS3}			
7	COMM_SEL/I_{LIM}	COMM_SEL - Selects SMBus or Stand-alone mode of operation (see Table 11-1).	AIO	n/a
		I_{LIM} - Selects the hardware current limit at power-up.		
8	SEL	Selects polarity of PWR_EN control and SMBus address (see Table 11-2).	AIO	n/a
9	V_{S1}	Voltage input to Power Switch. These pins are internally connected and must be tied together.	Hi-Power	Connect to ground
10	V_{S2}			
11	V_{S3}			
12	V_{DD}	Main power supply input for chip functionality	Power	n/a
13	PWR_EN	Port power switch enable input. Polarity determined by SEL pin.	DI	Connect to ground or V_{DD} (see Note 3)
14	NC	Not internally connected	n/a	Leave open
15	NC	Not internally connected	n/a	Leave open

Note 1: Total leakage current from pins 4, 5 and 6 (V_{BUS}) to ground must be less than 100 µA for proper attach/removal detection operation.

2: It is recommended to use 2 MΩ pull-down resistors on the D_{POUT} and/or D_{MOUT} pin if a portable device stimulus is expected when using the Customer Charger Emulation profile with the high-speed data switch open. The 2 MΩ value is based on BC1.1 impedance characteristics for Dedicated Charging Ports.

3: To ensure operation, the PWR_EN pin must be enabled, as determined by the SEL pin decode, when it is not driven by an external device. Furthermore, one of the M1, M2 or EM_EN pins must be connected to V_{DD} if all three are not driven from an external device. If the PWR_EN pin is disabled or all of the M1, M2 and EM_EN pins are connected to ground, the UCS81003 will remain in the Sleep or Detect state unless activated via the SMBus.

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TABLE 3-1: PIN FUNCTION TABLE

UCS81003 5x5 VQFN	Symbol	Function	Pin Type	Connection Type if Pin Not Used
16	SMDATA/LATCH	**SMDATA** - SMBus data input/output (requires pull-up resistor)	DIOD	n/a
		LATCH - In Stand-Alone mode, Latch/Auto-recovery fault handling mechanism selection input (see **Section 7.5 "Fault Handling Mechanism"**)	DI	
17	SMCLK/S0	**SMCLK** - SMBus Clock Input (requires pull-up resistor)	DI	n/a
		S0 - In Stand-Alone mode, enables Attach/Removal Detection feature (see **Section 5.3.6 "S0 Input"**)		
18	ALERT#	Active low error event output flag (requires pull-up resistor)	OD	Connect to ground
19	D_{PIN}	USB data input (plus)	AIO	Connect to ground or ground through a resistor
20	D_{MIN}	USB data input (minus)	AIO	Connect to ground or ground through a resistor
21	NC	Not internally connected	n/a	Leave open
22	NC	Not internally connected	n/a	Leave open
23	D_{MOUT}	USB data output (minus)	AIO (see Note 2)	Connect to ground
24	D_{POUT}	USB data output (plus)	AIO (see Note 2)	Connect to ground
25	A_DET#	Active low device Attach Detection output flag (requires pull-up resistor)	OD	Connect to ground
26	EM_EN	Active mode selector input	DI	Connect to ground or V_{DD} (see Note 3)
27	GND	Ground	Power	n/a
28	NC	Not internally connected	n/a	Leave open
29	EP	Exposed Thermal Pad. Must be connected to the electrical ground.	EP	n/a

Note 1: Total leakage current from pins 4, 5 and 6 (V_{BUS}) to ground must be less than 100 µA for proper attach/removal detection operation.

2: It is recommended to use 2 MΩ pull-down resistors on the D_{POUT} and/or D_{MOUT} pin if a portable device stimulus is expected when using the Customer Charger Emulation profile with the high-speed data switch open. The 2 MΩ value is based on BC1.1 impedance characteristics for Dedicated Charging Ports.

3: To ensure operation, the PWR_EN pin must be enabled, as determined by the SEL pin decode, when it is not driven by an external device. Furthermore, one of the M1, M2 or EM_EN pins must be connected to V_{DD} if all three are not driven from an external device. If the PWR_EN pin is disabled or all of the M1, M2 and EM_EN pins are connected to ground, the UCS81003 will remain in the Sleep or Detect state unless activated via the SMBus.

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TABLE 3-2: PIN TYPES DESCRIPTION

Pin Type	Description
Power	This pin is used to supply power or ground to the device
Hi-Power	This pin is a high-current pin
AIO	Analog Input/Output - this pin is used as an I/O for analog signals.
DI	Digital Input - this pin is used as a digital input. This pin will be glitch-free.
DIOD	Open-Drain Digital Input/Output - this pin is bidirectional. It is open-drain and requires a pull-up resistor. This pin will be glitch-free.
OD	Open-Drain Digital Output - used as a digital output. It is open-drain and requires a pull-up resistor. This pin will be glitch-free.
EP	Exposed Thermal Pad

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4.0 TERMS AND ABBREVIATIONS

Note: The M1, M2, PWR_EN and EM_EN pins each have configuration bits (<pin name>_SET in **Section 10.4.3 "Switch Configuration Register"**) that may be used to perform the same function as the external pin state. These bits are accessed via the SMBus/I^2C and are OR'd with the respective pin. This OR'd combination of pin state and register bit is referenced as the <pin name> control.

TABLE 4-1: TERMS AND ABBREVIATIONS

Term/Abbreviation	Description
Active mode	Active power state operation mode: Data Pass-through, BC1.2 SDP, BC1.2 CDP, BC1.2 DCP or Dedicated Charger Emulation Cycle.
Attach Detection	An Attach Detection event occurs when the current drawn by a portable device is greater than I_{DET_QUAL} for longer than t_{DET_QUAL}.
Attachment	The physical insertion of a portable device into a USB port that UCS81003 is controlling.
CC	Constant Current
CDM	Charged Device Model. JEDEC® model for characterizing susceptibility of a device to damage from ESD.
CDP or USB-IF BC1.2 CDP	Charging Downstream Port. The combination of the UCS81003 CDP handshake and an active standard USB host comprises a CDP. This enables a BC1.2 compliant portable device to simultaneously draw current up to 1.5A while data communication is active. The USB high-speed data switch is closed in this mode.
Charge Enable	When a charger emulation profile has been accepted by a portable device and charging commences.
Charger Emulation Profile	Representation of a charger comprised of D_{POUT}, D_{MOUT} and V_{BUS} signaling, which make up a defined set of signatures or handshaking protocols.
Connection	USB-IF term which refers to establishing active USB communications between a USB host and a USB device.
Current Limiting Mode	Determines the action that is performed when the I_{BUS} current reaches the I_{LIM} threshold. Trip opens the port power switch. Constant Current (variable slope) allows V_{BUS} to be dropped by the portable device.
DCE	Dedicated Charger Emulation. Charger emulation in which the UCS81003 can deliver power only (by default). No active USB data communication is possible when charging in this mode (by default).
DCP or USB-IF BC1.2 DCP	Dedicated Charging Port. This functions as a dedicated charger for a BC1.2 portable device. This allows the portable device to draw currents up to 1.5A with Constant Current Limiting (and beyond 1.5A with Trip Current Limiting). No USB communications are possible (by default).
DC	Dedicated Charger. A charger which inherently does not have USB communications, such as an A/C wall adapter.
Disconnection	USB-IF term which refers to the loss of active USB communications between a USB host and a USB device.
Dynamic Thermal Management	The UCS81003 automatically adjusts port power switch limits and modes to lower internal power dissipation when the thermal regulation temperature value is approached.
Enumeration	A USB-specific term indicating that a host is detecting and identifying USB devices.
Handshake	Application of a charger emulation profile that requires a response. Two-way communication between the UCS81003 and the portable device.
HBM	Human Body Model
HSW	High-Speed switch
I_{BUS_R2MIN}	Current limiter mode boundary

TABLE 4-1: TERMS AND ABBREVIATIONS (CONTINUED)

Term/Abbreviation	Description
I_{LIM}	The I_{BUS} current threshold used in current limiting. In Trip mode, when I_{LIM} is reached, the port power switch is opened. In Constant Current mode, when the current exceeds I_{LIM}, operation continues at a reduced voltage and increased current; if V_{BUS} voltage drops below V_{BUS_MIN}, the port power switch is opened.
Legacy	USB devices that require non-BC1.2 signatures be applied on the D_{POUT} and D_{MOUT} pins to enable charging.
OCL	Overcurrent limit
POR	Power-on Reset
Portable Device	USB device attached to the USB port.
Power Thief	A USB device that does not follow the handshaking conventions of a BC1.2 device or Legacy devices and draws current immediately upon receiving power (i.e., a USB book light, portable fan, etc).
Removal Detection	A Removal Detection event occurs when the current load on the V_{BUS} pin drops to less than I_{REM_QUAL} for longer than t_{REM_QUAL}.
Removal	The physical removal of a portable device from a USB port that the UCS81003 is controlling.
Response	An action, usually in response to a stimulus, in charger emulation performed by the UCS81003 device via the USB data lines.
SDP or USB-IF SDP	Standard downstream port. The combination of the UCS81003 high-speed switch being closed with an upstream USB host present comprises a BC1.2 SDP. This enables a BC1.2 compliant portable device to simultaneously draw current up to 0.5A while data communication is active.
Signature	Application of a charger emulation profile without waiting for a response. One-way communication from the UCS81003 to the portable device.
Stand-Alone Mode	Indicates that the communications protocol is not active and all communications between the UCS81003 and a controller are done via the external pins only (M1, M2, EM_EN, PWR_EN, S0 and LATCH as inputs, and ALERT# and A_DET# as outputs).
Stimulus	An event in charger emulation detected by the UCS81003 device via the USB data lines.

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5.0 GENERAL DESCRIPTION

The UCS81003 provides a single USB port power switch for precise control of up to 3.0A continuous current with overcurrent limit (OCL), dynamic thermal management, latch or auto-recovery fault handling, selectable active-low or -high enable, under and overvoltage lockout, and back-voltage protection.

Split supply support for V_{BUS} and V_{DD} is an option for low power in system standby states.

In addition to power switching and current limiting, the UCS81003 provides automatic and configurable charger emulation profiles to charge a wide variety of portable devices, including USB-IF BC1.2 (CDP or DCP modes), YD/T-1591 (2009), 12W charging, most Apple and RIM portable devices and many others.

The UCS81003 also provides current monitoring to allow intelligent management of system power and charge rationing for controlled delivery of current regardless of the host power state. This is especially important for battery-operated applications that need to provide power without excessively draining the battery, or that require power allocation depending on application activities.

Figure 5-1 shows a UCS81003 full-featured system configuration in which the UCS81003 provides a port power switch and low-power Attach Detection with wake-up signaling (wake on USB). The current limit is established at power-up. It can be lowered if required after power-up via the SMBus/I^2C. This configuration also provides configurable USB data line-charger emulation, programmable current limiting (as determined by the accepted charger emulation profile), active current monitoring and port charge rationing.

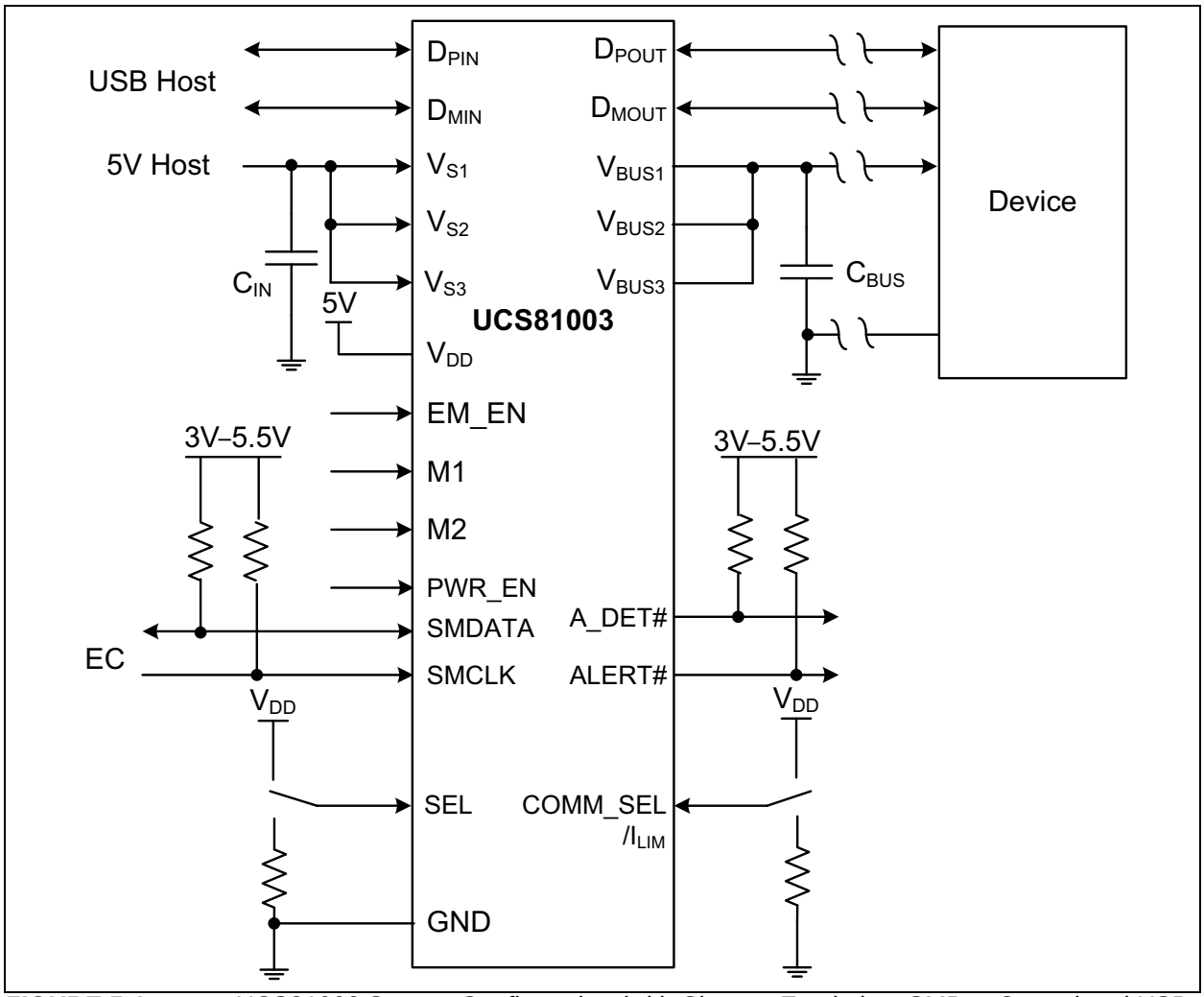

FIGURE 5-1: *UCS81003 System Configuration (with Charger Emulation, SMBus Control and USB Host).*

Figure 5-2 shows a system configuration in which the UCS81003 provides a USB data switch, port power switch, low-power Attach Detection and portable device Attach/Removal Detection signaling. This configuration does not include configurable data line charger emulation, programmable current limiting or current monitoring and rationing.

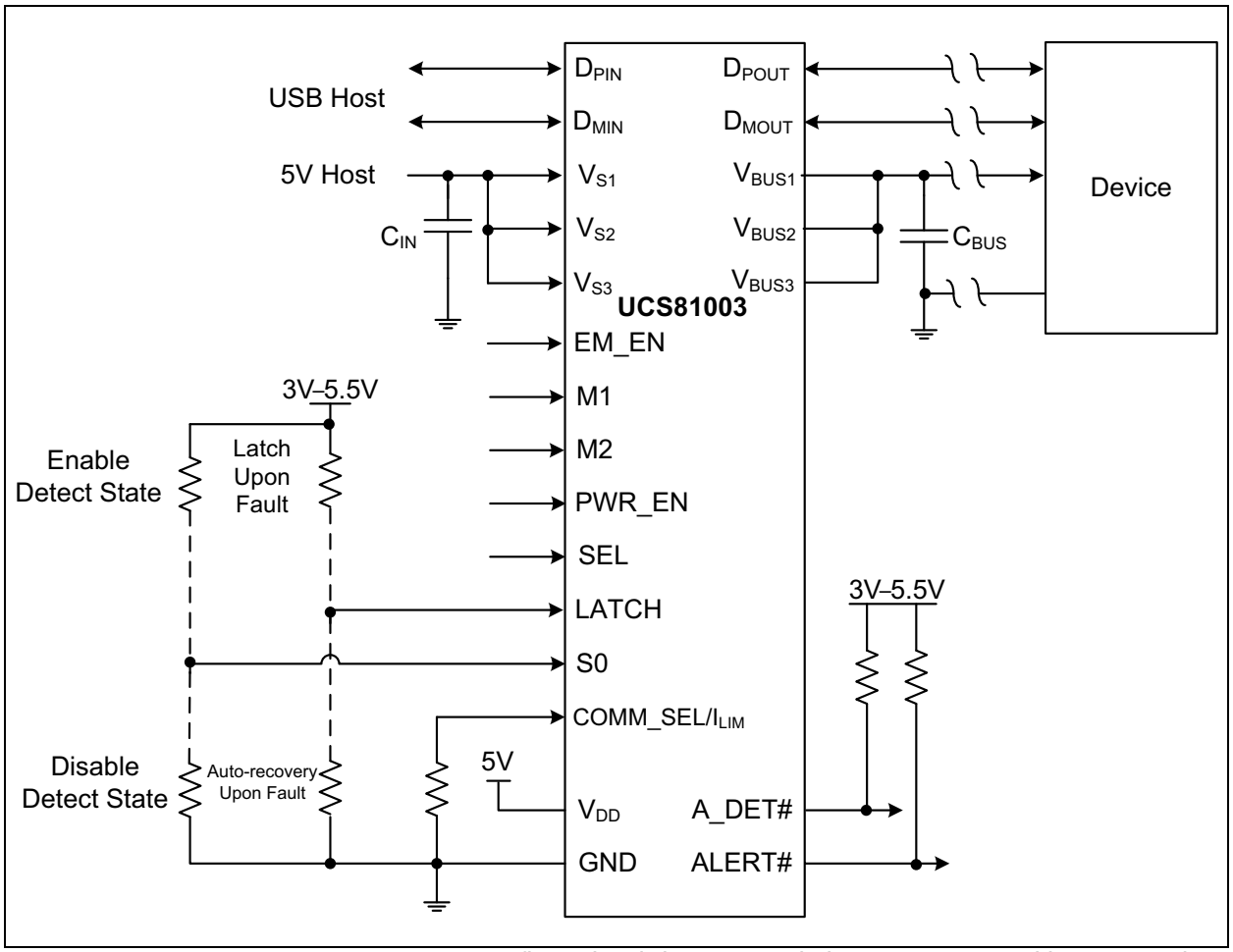

FIGURE 5-2: *UCS81003 System Configuration (Charger Emulation, No SMBus, with USB Host).*

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Figure 5-3 shows a system configuration in which the UCS81003 provides a port power switch, low-power Attach Detection and portable device attachment detected signaling. This configuration is useful for applications that already provide USB BC1.2 and/or legacy data line handshaking on the USB data lines, but still require port power switching and current limiting.

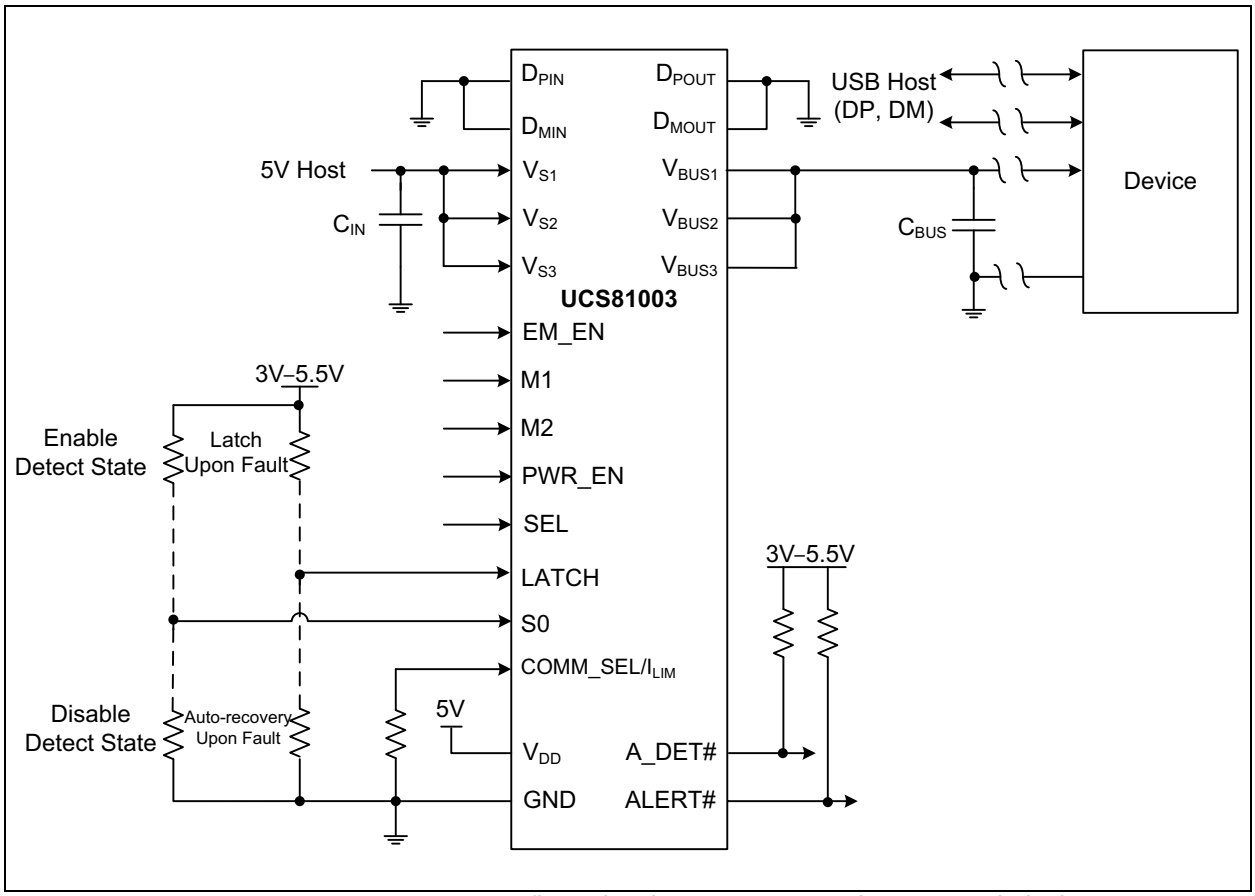

FIGURE 5-3: *UCS81003 System Configuration (No SMBus, No Charger Emulation).*

Figure 5-4 shows a system configuration in which the UCS81003 provides a port power switch, low-power Attach Detection, charger emulation (with no USB host) and portable device attachment detected signaling. This configuration is useful for wall adapter-type applications and cigarette-plug adapters.

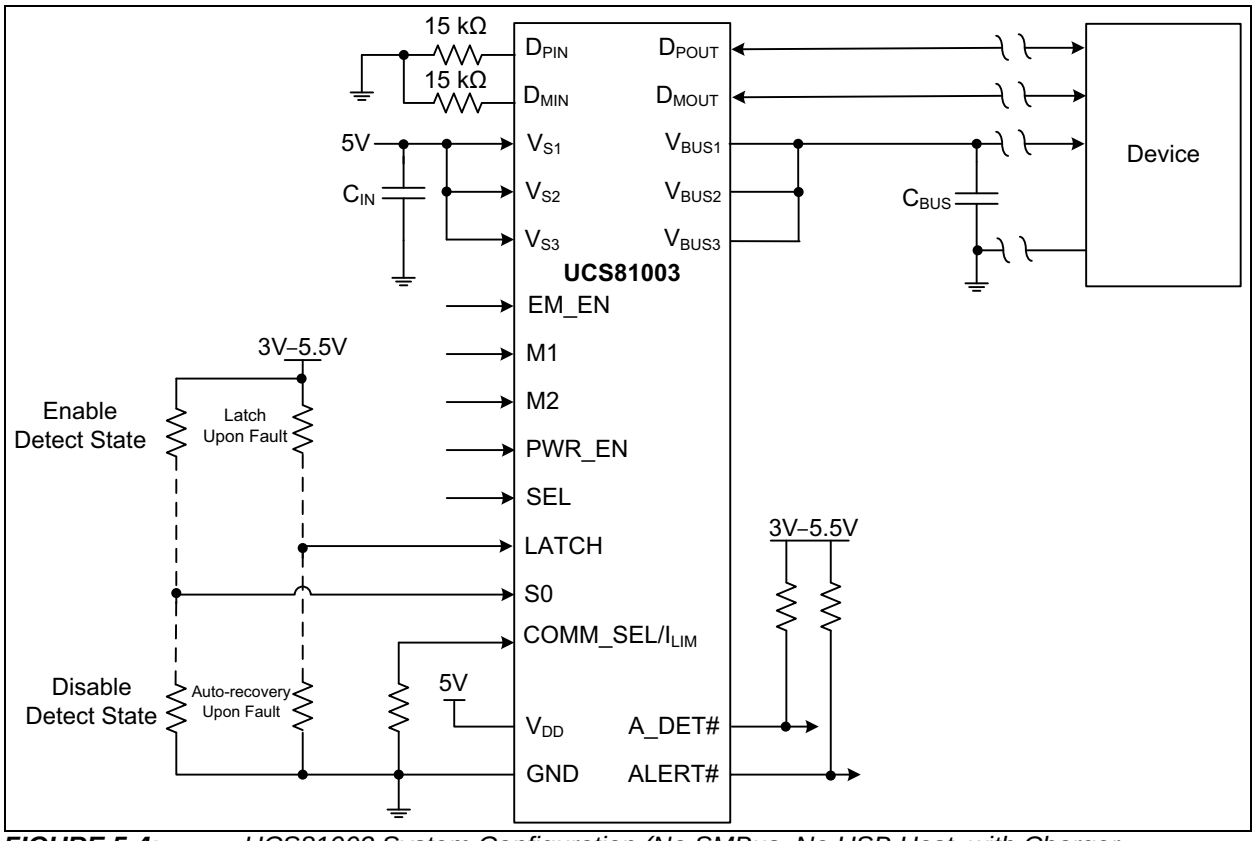

FIGURE 5-4: *UCS81003 System Configuration (No SMBus, No USB Host, with Charger Emulation).*

5.1 UCS81003 Power States

The UCS81003 has the following power states:

TABLE 5-1: POWER STATES DESCRIPTION

State	Description
Off	This power state is entered when the voltage at the V_{DD} pin voltage is < V_{DD_TH}. In this state, the device is considered “off”. The UCS81003 will not retain its digital states and register contents, nor respond to SMBus/I^2C communications. The port power switch, bypass switch and the high-speed data switches will be off. See **Section 5.1.1 “Off State Operation”**.
Sleep	This is the lowest power state available. While in this state, the UCS81003 will retain digital functionality, respond to changes in emulation controls and wake to respond to SMBus/I^2C communications. The high-speed switch and all other functionality will be disabled. See **Section 5.1.2 “Sleep State Operation”**.
Detect	This is a low-current power state. In this state, the device is actively looking for a portable device to be attached. The high-speed switch is disabled by default. While in this state, the UCS81003 will retain the configuration and charge rationing data, but it will not monitor the bus current. SMBus/I^2C communications will be fully functional. See **Section 5.1.3 “Detect State Operation”**.
Error	This power state is entered when a fault condition exists. See **Section 5.1.5 “Error State Operation”**.
Active	This power state provides full functionality. While in this state, operations include activation of the port power switch, USB data line handshaking/charger emulation and current limiting and charge rationing. See **Section 5.1.4 “Active State Operation”**.

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Table 5-2 shows the settings for the various power states, except Off and Error. If $V_{DD} < V_{DD_TH}$, the UCS81003 is in the Off state. To determine the mode of operation in the Active state, see Table 9-1.

Note: Using configurations not listed in Table 5-2 is not recommended and may produce undesirable results.

TABLE 5-2: POWER STATES CONTROL SETTINGS

Power State	V_S	PWR_EN	S0	M1, M2, EM_EN	Portable Device Attached	Behavior
Sleep	n/a	disabled	0	Not set to Data Pass-Through. (**Note 1**)	n/a	• All switches disabled. • V_{BUS} will be near ground potential. • The UCS81003 wakes to respond to SMBus communications.
	n/a	enabled	0	All = 0b	n/a	
Detect (see **Section 8.0 "Detect State"**	n/a	disabled	1	n/a	n/a	• High-Speed switch disabled (by default). • Port power switch disabled. • Host-Controlled transition to Active state (see **Section 5.1.3.2 "Host-Controlled Transition from Detect to Active"**).
	< V_{S_UVLO}	enabled	1	All ≠ 0b	n/a	
	> V_{S_UVLO}	enabled	1	All ≠ 0b	No	• High-Speed switch disabled (by default). • Automatic transition to Active state when conditions met (see **Section 5.1.3.1 "Automatic Transition from Detect to Active"**).
Active (see **Section 9.0 "Active State"**)	> V_{S_UVLO}	enabled	0	All ≠ 0b	n/a	• High-Speed switch enabled/disabled based on mode. • Port power switch is on at all times. • Attach and Removal Detection disabled. See **Note 2**.
	> V_{S_UVLO}	enabled	1	All ≠ 0b	Yes	• Port power switch is on. • Removal Detection enabled.

Note 1: In order to transition from Active State Data Pass-through mode into Sleep with these settings, change the M1, M2 and EM_EN pins before changing the PWR_EN pin. See **Section 9.4 "Data Pass-Through (No Charger Emulation)"**.

2: If S0 = '0' and a portable device is not attached in DCE Cycle mode, the UCS81003 will be cycling through charger emulation profiles (by default). There is no guarantee which charger emulation profile will be applied first when a portable device attaches.

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5.1.1 OFF STATE OPERATION

The device is in the Off state if V_{DD} is less than V_{DD_TH}. When the UCS81003 is in the Off state, it does nothing, and all circuitry is disabled. Digital register values are not stored and the device will not respond to SMBus commands.

5.1.2 SLEEP STATE OPERATION

When the UCS81003 is in the Sleep state, the device is in its lowest-power state. The high-speed switch, bypass switch and the port power switch are disabled. The Attach and Removal Detection feature is disabled. V_{BUS} will be near ground potential. The ALERT# pin is not asserted. If asserted prior to entering the Sleep state, the ALERT# pin will be released. The A_DET# pin is released. SMBus activity is limited to single byte read or write.

The first data byte read from the UCS81003 when in the Sleep state will wake the device; however, the data to be read will return all 0's and should be considered invalid. This is a "dummy" read byte meant to wake the UCS81003. Subsequent read or write bytes will be accepted normally. After the dummy read, the UCS81003 will be in a higher-power state (see Figure 5-6). The device will return to Sleep after the last communication, or if no further communication has occurred.

Figure 5-5 shows timing diagrams for waking the UCS81003 via external pins. Figure 5-6 shows the timing for waking the UCS81003 via SMBus.

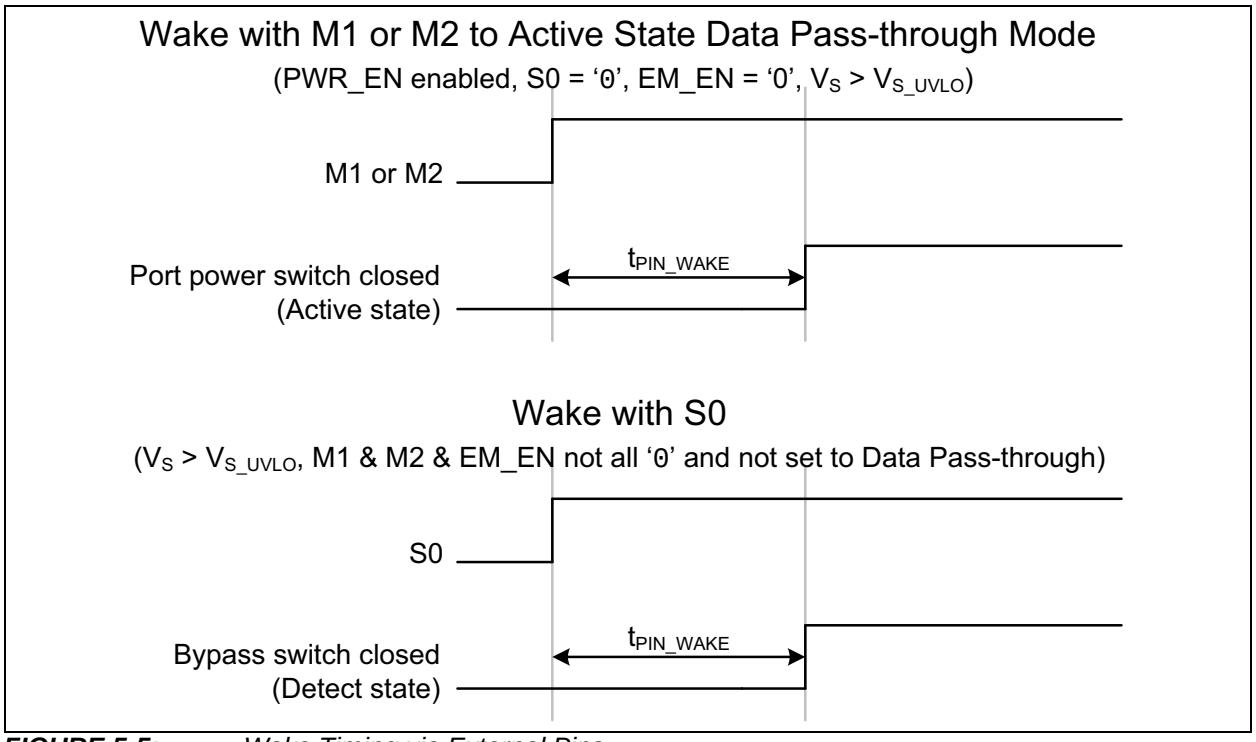

FIGURE 5-5: *Wake Timing via External Pins.*

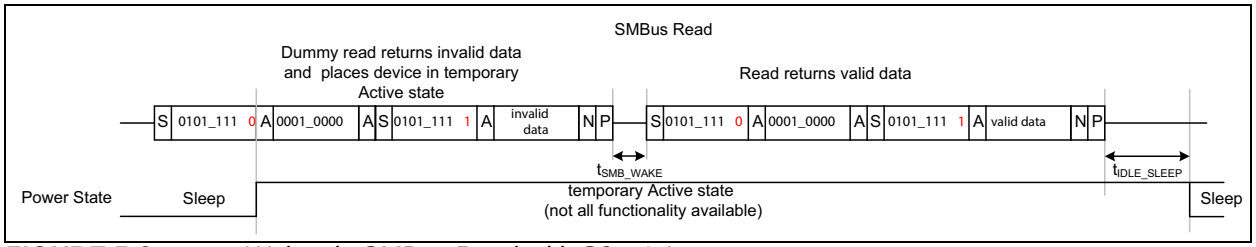

FIGURE 5-6: *Wake via SMBus Read with S0 = '0'.*

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5.1.3 DETECT STATE OPERATION

When the UCS81003 is in the Detect state, the port power switch will be disabled. The high-speed switch is also disabled by default. The V_{BUS} output will be connected to the V_{DD} voltage by a secondary bypass switch (see **Section 8.0 "Detect State"**).

There is one **non-recommended** configuration which places the UCS81003 in the Detect state, but V_{BUS} will not be discharged and a portable device attachment will not be detected. For the recommended configurations, see Table 5-2.

There are two methods for transitioning from the Detect state to the Active state: automatic and host-controlled.

5.1.3.1 Automatic Transition from Detect to Active

For the Detect state, set S0 to '1', enable PWR_EN, set the EM_EN, M1 and M2 controls to the desired Active mode (Table 9-1), and supply $V_S > V_{S_UVLO}$. When a portable device is attached and an Attach Detection event occurs, the UCS81003 will automatically transition to the Active state and operate according to the selected Active mode.

5.1.3.2 Host-Controlled Transition from Detect to Active

For the Detect state, set S0 to '1', set the EM_EN, M1 and M2 controls to the desired Active mode (Table 9-1), and configure one of the following:

- disable PWR_EN and supply V_S,

  OR

- enable PWR_EN and don't supply V_S. When a portable device is attached and an Attach Detection event occurs, the host must respond to transition to the Active state.

Depending on the control settings in the Detect state, this could entail:

- enabling PWR_EN

  OR

- supplying V_S above the threshold.

Note:	If S0 is '1', PWR_EN is enabled and V_S is not present, the A_DET# pin will cycle if the current draw exceeds the current capacity of the bypass switch.

5.1.3.3 State Change from Detect to Active

When conditions cause the UCS81003 to transition from the Detect state to the Active state, the following occurs:

1. The Attach Detection feature will be disabled; the Removal Detection feature remains enabled, unless S0 is changed to '0'.
2. The bypass switch will be turned off.
3. The discharge switch will be turned on briefly for $t_{DISCHARGE}$.
4. The port power switch will be turned on.

5.1.4 ACTIVE STATE OPERATION

Every time that the UCS81003 enters the Active state and the port power switch is closed, it will enter the mode as instructed by the host controller (see **Section 9.0 "Active State"**). The UCS81003 cannot be in the Active state (and therefore, the port power switch cannot be turned on) if any of the following conditions exist:

- $V_S < V_{S_UVLO}$
- PWR_EN is disabled
- M1, M2 and EM_EN are all set to '0'
- S0 is set to '1' and an Attach Detection event has not occurred

5.1.5 ERROR STATE OPERATION

The UCS81003 will enter the Error state from the Active state when any of the following events are detected:

- The maximum allowable internal die temperature (T_{TSD}) has been exceeded (see **Section 7.2.1.2 "Thermal Shutdown"**).
- An overcurrent condition has been detected (see **Section 7.1.1 "Current Limit Setting"**).
- An undervoltage condition on V_{BUS} has been detected (see **Section 5.2.5 "Undervoltage Lockout on VS"**).
- A back-drive condition has been detected (see **Section 5.2.3 "Back-voltage Detection"**).
- A discharge error has been detected (see **Section 7.3 "VBUS Discharge"**).
- An overvoltage condition on the V_S pins.

The UCS81003 will enter the Error state from the Detect state when a back-drive condition has been detected or when the maximum allowable internal die temperature has been exceeded.

The UCS81003 will enter the Error state from the Sleep state when a back-drive condition has been detected.

When the UCS81003 enters the Error state, the port power switch, V_{BUS} bypass switch and the high-speed switch are turned off, and the ALERT# pin is asserted (by default). They will remain off while in this power state. The UCS81003 will leave this state as determined by the fault handling selection (see **Section 7.5 "Fault Handling Mechanism"**).

When using the Latch fault handler and the user has re-activated the device by clearing the ERR bit (see **Section 10.3 "Status Registers"**), or toggling the PWR_EN control, the UCS81003 will check that all of the error conditions have been removed. If using Auto-Recovery fault handler, after the t_{CYCLE} time period, the UCS81003 will check that all of the error conditions have been removed.

If all of the error conditions have been removed, the UCS81003 will return to the Active state or Detect state, as applicable. Returning to the Active state will cause the UCS81003 to restart the selected mode (see **Section 9.2 "Active Mode Selection"**).

If the device is in the Error state and a Removal Detection event occurs, it will check the error conditions and then return to the power state defined by the PWR_EN, M1, M2, EM_EN and S0 controls.

5.2 Supply Voltages

5.2.1 V_{DD} SUPPLY VOLTAGE

The UCS81003 requires 4.5V to 5.5V present on the V_{DD} pin for core device functionality. Core device functionality consists of maintaining register states, wake-up upon SMBus/I^2C query and Attach Detection.

5.2.2 V_S SOURCE VOLTAGE

V_S can be a separate supply and can be greater than V_{DD} to accommodate high-current applications in which current path resistances result in unacceptable voltage drops that may prevent optimal charging of some portable devices.

5.2.3 BACK-VOLTAGE DETECTION

Whenever the following conditions are true, the port power switch will be disabled, the V_{BUS} bypass switch will be disabled, the high-speed data switch will be disabled, and a back-voltage event will be flagged. This will cause the UCS81003 to enter the Error power state (see **Section 5.1.5 "Error State Operation"**).

- The V_{BUS} voltage exceeds the V_S voltage by V_{BV_TH} and the port power switch is closed. The port power switch will be opened immediately. If the condition lasts for longer than t_{MASK}, then the UCS81003 will enter the Error state. Otherwise, the port power switch will be turned on as soon as the condition is removed.
- The V_{BUS} voltage exceeds the V_{DD} voltage by V_{BV_TH} and the V_{BUS} bypass switch is closed. The bypass switch will be opened immediately. If the condition lasts for longer than t_{MASK}, then the UCS81003 will enter the Error state. Otherwise, the bypass switch will be turned on as soon as the condition is removed.

5.2.4 BACK-DRIVE CURRENT PROTECTION

If a self-powered portable device is attached, it may drive the V_{BUS} port to its power supply voltage level; however, the UCS81003 is designed such that leakage current from the V_{BUS} pins to the V_{DD} or V_S pins shall not exceed I_{BD_1} (if the V_{DD} voltage is zero) or I_{BD_2} (if the V_{DD} voltage exceeds V_{DD_TH}).

5.2.5 UNDERVOLTAGE LOCKOUT ON V_S

The UCS81003 requires a minimum voltage (V_{S_UVLO}) be present on the V_S pin for Active power state.

5.2.6 OVERVOLTAGE DETECTION AND LOCKOUT ON V_S

The UCS81003 port power switch will be disabled if the voltage on the V_S pin exceeds a voltage (V_{S_OV}) for longer than the specified time (t_{MASK}). This will cause the device to enter the Error state.

5.3 Discrete Input Pins

Note:	If it is necessary to connect any of the control pins except the COMM_SEL/I_{LIM} or SEL pins via a resistor to V_{DD} or GND, the resistor value should not exceed 100 kΩ in order to meet the V_{IH} and V_{IL} specifications.

5.3.1 COMM_SEL/I_{LIM} INPUT

The COMM_SEL/I_{LIM} input determines the initial I_{LIM} settings and the communications mode, as shown in Table 11-1.

5.3.2 SEL INPUT

The SEL pin selects the polarity of the PWR_EN control. In addition, if the UCS81003 is not configured to operate in Stand-Alone mode, the SEL pin determines the SMBus address. See Table 11-2. The SEL pin state is latched upon device power-up and further changes will have no effect.

5.3.3 M1, M2 AND EM_EN INPUTS

The M1, M2 and EM_EN input controls determine the Active mode and affect the power state (see Table 5-2 and Table 9-1). When these controls are all set to '0' and PWR_EN is enabled, the UCS81003 Attach and Removal Detection feature is disabled. In SMBus mode, the M1, M2 and EM_EN pin states will be ignored by the UCS81003 if the PIN_IGN configuration bit is set (see **Section 10.4.3 "Switch Configuration Register"**); otherwise, the M1_SET, M2_SET and EM_EN_SET configuration bits (see **Section 10.4.3 "Switch Configuration Register"**) are checked along with the pins.

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5.3.4 PWR_EN INPUT

The PWR_EN control enables the port power switch to be turned on if conditions are met and affects the power state (see Table 5-2). The port power switch cannot be closed if PWR_EN is disabled. However, if PWR_EN is enabled, the port power switch is not necessarily closed (see **Section 5.1.4 "Active State Operation"**). Polarity is controlled by the SEL pin. In SMBus mode, the PWR_EN pin state will be ignored by the UCS81003 if the PIN_IGN configuration bit is set (see **Section 10.4.3 "Switch Configuration Register"**); otherwise, the PWR_ENS configuration bit (see **Section 10.4.3 "Switch Configuration Register"**) is checked along with the pin.

5.3.5 LATCH INPUT

The Latch input control determines the behavior of the fault handling mechanism (see **Section 7.5 "Fault Handling Mechanism"**).

When the UCS81003 is configured to operate in Stand-Alone mode (see **Section 11.3 "Stand-Alone Operating Mode"**), the LATCH control is available exclusively via the LATCH pin (see Table 11-10). When the UCS81003 is configured to operate in SMBus mode, the LATCH control is available exclusively via the LATCHS configuration bit (see **Section 10.4.3 "Switch Configuration Register"**).

5.3.6 S0 INPUT

The S0 control enables the Attach and Removal Detection feature and affects the power state (see Table 5-2). When S0 is set to '1', an Attach Detection event must occur before the port power switch can be turned on (this statement requires PWR_EN_BEH OTP bit is set to '1'). When S0 is set to '0', the Attach and Removal Detection feature is not enabled.

When the device is configured to operate in SMBus mode (see **Section 11.3 "Stand-Alone Operating Mode"**), the S0 control is available exclusively via the S0_SET configuration bit (see **Section 10.4.3 "Switch Configuration Register"**). Otherwise, the S0 control is available exclusively via the S0 pin since the SMBus protocol will be disabled.

5.4 Discrete Output Pins

5.4.1 ALERT# AND A_DET# OUTPUT PINS

The ALERT# pin is an active low open-drain interrupt to the host controller. The ALERT# pin is asserted (by default - see ALERT_MASK in **Section 10.4.1 "General Configuration Register"**) when an error occurs (see Register 10-3). The ALERT# pin can also be asserted when the LOW_CUR (portable device is pulling less current and may be finished charging) or TREG (thermal regulation temperature exceeded) bits are set and linked. As well, when charge rationing is enabled, the ALERT# pin is asserted by default when the current rationing threshold is reached (as determined by RATION_BEH<1:0> - see Table 7-1). The ALERT# pin is released when all error conditions that may assert the ALERT# pin (such as an error condition, charge rationing, and TREG and LOW_CHG if linked) have been removed or reset as necessary.

The A_DET# pin provides an active-low open-drain output indication that a valid Attach Detection event has occurred. It will remain asserted until the UCS81003 is placed into the Sleep state or a Removal Detection event occurs. For wake on USB, the A_DET# pin assertion can be utilized by the system. If the S0 control is '0' and the UCS81003 is in the Active state, the A_DET# pin will be asserted regardless if a portable device is attached or not. If S0 is '1', PWR_EN is enabled and V_S is not present, the A_DET# pin will cycle if the current draw exceeds the current capacity of the bypass switch.

5.4.2 INTERRUPT BLANKING

The ALERT# and A_DET# pins will not be asserted for a specified time (up to t_{BLANK}) after power-up. Additionally, an error condition (except for the thermal shutdown) must be present for longer than a specified time (t_{MASK}) before the ALERT# pin is asserted.

6.0 USB HIGH-SPEED DATA SWITCH

The UCS81003 contains a series USB 2.0-compliant high-speed switch between the D_{PIN} and D_{MIN} pins and between the D_{POUT} and D_{MOUT} pins. This switch is designed for high-speed, low-latency functionality to allow USB 2.0 full-speed and high-speed communications with minimal interference.

Nominally, the switch is closed in the Active state, allowing uninterrupted USB communications between the upstream host and the portable device. The switch is opened when:

- The UCS81003 is actively emulating using any of the charger emulation profiles except CDP (by default - see **Section 10.4.5 "High-Speed Switch Configuration Register"**)
- The UCS81003 is operating as a dedicated charger unless the HSW_DCE configuration bit is set (see **Section 10.4.5 "High-Speed Switch Configuration Register"**)
- The UCS81003 is in the Detect state (by default) or in the Sleep state

Note:	If the V_{DD} voltage is less than V_{DD_TH}, the high-speed data switch will be disabled and opened.

6.1 USB-IF High-Speed Compliance

The USB data switch will not significantly degrade the signal integrity through the device D_P/D_M pins with USB high-speed communications.

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7.0 USB PORT POWER SWITCH

To assure compliance to various charging specifications, the UCS81003 contains a USB port power switch that supports two current-limiting modes: Trip and Constant Current (variable slope). The current limit (I_{LIM}) is pin selectable (and may be updated via the register set). The switch also includes soft start circuitry and a separate short-circuit current limit.

The port power switch is on in the Active state (except when V_{BUS} is discharging).

7.1 Current Limiting

7.1.1 CURRENT LIMIT SETTING

The UCS81003 hardware set current limit (I_{LIM}), can be one of eight values (see Table 11-1). This resistor value is read once upon UCS81003 power-up. The current limit can be changed via the SMBus/I^2C after power-up; however, the programmed current limit cannot exceed the hardware set current limit.

At power-up, the communication mode (Stand-Alone or SMBus/I^2C) and hardware current limit (I_{LIM}) are determined via the pull-down resistor (or pull-up resistor, if connected to V_{DD}) on the COMM_SEL/I_{LIM} pin, as shown in Table 11-1.

7.1.2 SHORT CIRCUIT OUTPUT CURRENT LIMITING

Short circuit current limiting occurs when the output current is above the selectable current limit (I_{LIMx}). This event will be detected and the current will immediately be limited (within t_{SHORT_LIM} time). If the condition remains, the port power switch will flag an Error condition and enter the Error state (see **Section 5.1.5 "Error State Operation"**).

7.1.3 SOFT START

When the PWR_EN control changes states to enable the port power switch, or an Attach Detection event occurs in the Detect power state and the PWR_EN control is already enabled, the UCS81003 invokes a soft start routine for the duration of the V_{BUS} rise time (t_{R_BUS}). This soft start routine will limit current flow from V_S into V_{BUS} while it is active. This circuitry will prevent current spikes due to a step in the portable device current draw.

In the case when a portable device is attached while the PWR_EN pin is already enabled, if the bus current exceeds I_{LIM}, the UCS81003 current limiter will respond within a specified time (t_{SHORT_LIM}) and will operate normally at this point. The C_{BUS} capacitor will deliver the extra current, if any, as required by the load change.

7.1.4 CURRENT-LIMITING MODES

The UCS81003 current limiting has two modes: Trip and Constant Current (variable slope). Either mode functions at all times when the port power switch is closed. The current limiting mode used depends on the Active state mode (see **Section 9.9 "Current Limit Mode Associations"**). When operating in the Detect power state (see **Section 5.1.3 "Detect State Operation"**), the current capacity at V_{BUS} is limited to I_{BUS_BYP} as described in **Section 8.2 "VBUS Bypass Switch"**.

7.1.4.1 Trip Mode

When using Trip Current Limiting, the UCS81003 USB port power switch functions as a low-resistance switch and rapidly turns off if the current limit is exceeded. While operating using Trip Current Limiting, the V_{BUS} output voltage will be held relatively constant (equal to the V_S voltage minus the R_{ON} x I_{BUS} current) for all current values up to the I_{LIM}.

If the current drawn by a portable device exceeds I_{LIM}, the following occurs:

1. The port power switch will be turned off (Trip action).
2. The UCS81003 will enter the Error state and assert the ALERT# pin.
3. The fault handling circuitry will then determine subsequent actions.

Trip Current Limiting is used by default when the UCS81003 is in Data Pass-Through and Dedicated Charger Emulation Cycle (except when the BC1.2 DCP charger emulation profile is accepted), and when there's no handshake. This method is also used when charger emulation is active.

Note:	To avoid cycling in Trip mode, set I_{LIM} higher than the highest expected portable device current draw.

7.1.4.2 Constant Current Limiting (Variable Slope)

Constant Current Limiting is used when a portable device handshakes using the BC1.2 DCP charger emulation profile and the current drawn is greater than I_{LIM} (and I_{LIM} < 1.68A). It is also used in BC1.2 CDP mode and during the DCE Cycle when a charger emulation profile is being applied and the emulation timeout is active.

In CC mode, the port power switch allows the attached portable device to reduce V_{BUS} output voltage to less than the input V_S voltage while maintaining current delivery. The V/I slope depends on the user set I_{LIM} value. This slope is held constant for a given I_{LIM} value.

7.2 Thermal Management and Voltage Protection

7.2.1 THERMAL MANAGEMENT

The UCS81003 utilizes two-stage internal thermal management. The first is named Dynamic Thermal Management and the second is a Fixed Thermal Shutdown.

7.2.1.1 Dynamic Thermal Management

For the first stage (active in both current limiting modes), referred to as Dynamic Thermal Management, the UCS81003 automatically adjusts port power switch limits and modes to lower power dissipation when the thermal regulation temperature value is approached, as described below.

If the internal temperature exceeds the T_{REG} value, the port power switch is opened, the current limit (I_{LIM}) will be lowered by one step and a timer is started (t_{DC_TEMP}). When this timer expires, the port power switch is closed and the internal temperature will be checked again. If it remains above the T_{REG} threshold, the UCS81003 will repeat this cycle (open port power switch and reduce the I_{LIM} setting by one step) until I_{LIM} reaches its minimum value.

Note 1: If the temperature exceeds the T_{REG} threshold while operating in the DCE Cycle mode after a charger emulation profile has been accepted, the profile will be removed. The UCS81003 will not restart the DCE Cycle until one of the control inputs changes states to restart emulation.

2: The UCS81003 will not actively discharge V_{BUS} as a result of the temperature exceeding T_{REG}; however, any load current provided by a portable device or other load will cause V_{BUS} to be discharged when the port power switch is opened, possibly resulting in an attached portable device resetting.

If the UCS81003 is operating using Constant Current Limiting (variable slope) and the I_{LIM} setting has been reduced to its minimum set point and the temperature is still above T_{REG}, the UCS81003 will switch to operating using Trip Current Limiting. This will be done by reducing the I_{BUS_R2MIN} setting to 120 mA and restoring the I_{LIM} setting to the value immediately below the programmed setting (e.g., if the programmed I_{LIM} is 2.05A, the value will be set to 1.68A). If the temperature continues to remain above T_{REG}, the UCS81003 will continue this cycle (open the port power switch and reduce the I_{LIM} setting by one step).

If the UCS81003 internal temperature drops below $T_{REG} - T_{REG_HYST}$, the UCS81003 will take action based on the following:

1. If the Current Limit mode changed from CC mode to Trip mode, then a timer is started. When this timer expires, the UCS81003 will reset the port power switch operation to its original configuration, allowing it to operate using Constant Current Limiting (variable slope).
2. If the Current Limit mode did not change from CC mode to Trip mode, or was already operating in Trip mode, the UCS81003 will reset the port power switch operation to its original configuration.

If the UCS81003 is operating using Trip Current Limiting and the I_{LIM} setting has been reduced to its minimum set point and the temperature is above T_{REG}, the port power switch will be closed and the current limit will be held at its minimum setting until the temperature drops below $T_{REG} - T_{REG_HYST}$.

7.2.1.2 Thermal Shutdown

The second-stage thermal management consists of a hardware implemented thermal shutdown corresponding to the maximum allowable internal die temperature (T_{TSD}). If the internal temperature exceeds this value, the port power switch will immediately be turned off until the temperature is below $T_{TSD} - T_{TSD_HYST}$.

7.3 V_{BUS} Discharge

The UCS81003 will discharge V_{BUS} through an internal 100Ω resistor when at least one of the following conditions occurs:

- The PWR_EN control is disabled (triggered on the inactive edge of the PWR_EN control).
- A portable device Removal Detection event is flagged.
- The V_S voltage drops below a specified threshold (V_{S_UVLO}) that causes the port power switch to be disabled.
- When commanded into the Sleep power state via the EM_EN, M1 and M2 controls.
- Before each charger emulation profile is applied.
- Upon recovery from the Error state.
- When commanded via the SMBus (see **Section 10.4 "Configuration Registers"**) in the Active state.
- Any time that the port power switch is activated after the V_{BUS} bypass switch has been on (i.e., whenever V_{BUS} voltage transitions from being driven from V_{DD} to being driven from V_S, such as going from Detect to Active power state).
- Any time that the V_{BUS} bypass switch is activated after the port power switch has been on (i.e., going from Active to Detect power state).

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When the V_{BUS} discharge circuitry is activated, at the end of the $t_{DISCHARGE}$ time, the UCS81003 will confirm that V_{BUS} was discharged. If the V_{BUS} voltage is not below the V_{TEST} level, a discharge error will be flagged (by setting the DISCH_ERR status bit) and the UCS81003 will enter the Error state.

7.4 Battery Full

Delivery of bus current to a portable device can be rationed by the UCS81003. When this functionality is enabled, the host system must provide the UCS81003 with an accumulated charge maximum limit (in mAh). The charge rationing functionality works only in the Active power state. It continuously monitors the current delivered as well as the time elapsed since the mode was activated (or since the data was updated). This information is compiled to generate a charge-rationing number that is checked against the host limit.

Once the programmed current-rationing limit has been reached, the UCS81003 will take action as determined by the RATION_BEH bits, as described in Table 7-1. Note that this does not cause the device to enter the Error state.

Once the charge rationing circuitry has reached the programmed threshold, the UCS81003 will maintain the desired behavior until charge rationing is reset. Once charge rationing has been reset or disabled, the UCS81003 will recover as shown in Table 7-2.

TABLE 7-1: CHARGE RATIONING BEHAVIOR

RATION_BEH<1:0>		Behavior	Actions taken	Notes
1	0			
0	0	Report	ALERT# pin asserted.	
0	1	Report and Disconnect (default)	1. ALERT# pin asserted. 2. Charger emulation profile removed. 3. Port power switch disconnected.	The HSW will not be affected. All bus monitoring is still active. Changing the M1, M2, EM_EN, S0 and PWR_EN controls will cause the device to change power states as defined by the pin combinations; however, the port power switch will remain off until the rationing circuitry is reset. Furthermore, the bypass switch will not be turned on if enabled via the S0 control.
1	0	Disconnect and Go to Sleep	1. Port power switch disconnected. 2. Charger emulation profile removed. 3. Device will enter the Sleep state.	The HSW will be disabled. All VBUS and VS monitoring will be stopped. Changing the M1, M2, EM_EN, S0, and PWR_EN controls will have no effect on the power state until the rationing circuitry is reset.
1	1	Ignore	Take no further action.	

TABLE 7-2: CHARGE RATIONING RESET BEHAVIOR

Behavior	Reset Actions
Report	1. Reset the Total Accumulated Charge registers. 2. Clear the RATION status bit. 3. Release the ALERT# pin.
Report and Disconnect	1. Reset the Total Accumulated Charge registers. 2. Clear the RATION status bit. 3. Release the ALERT# pin. 4. Check the M1, M2, EM_EN, S0 and PWR_EN controls and enter the indicated power state if the controls changed (**Note 1**).

Note 1: Any time the charge rationing circuitry checks the pin conditions when changing rationing behavior or resetting charge rationing, if the external pin conditions have changed, then charger emulation will be restarted (provided emulation is enabled via the pin states). If the pin conditions have not changed, the UCS81003 returns to the previous power state as if the rationing threshold had not been reached (e.g., it will not discharge V_{BUS} or restart emulation).

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TABLE 7-2: CHARGE RATIONING RESET BEHAVIOR (CONTINUED)

Behavior	Reset Actions
Disconnect and Go to Sleep	1. Reset the Total Accumulated Charge registers. 2. Clear the RATION status bit. 3. Check the M1, M2, EM_EN, S0 and PWR_EN controls and enter the indicated power state if the controls changed (**Note 1**).
Ignore	1. Reset the Total Accumulated Charge registers. 2. Clear the RATION status bit.

Note 1: Any time the charge rationing circuitry checks the pin conditions when changing rationing behavior or resetting charge rationing, if the external pin conditions have changed, then charger emulation will be restarted (provided emulation is enabled via the pin states). If the pin conditions have not changed, the UCS81003 returns to the previous power state as if the rationing threshold had not been reached (e.g., it will not discharge V_{BUS} or restart emulation).

7.4.1 CHARGE RATIONING INTERACTIONS

When charge rationing is active, regardless of the specified behavior, the UCS81003 will function normally until the charge rationing threshold is reached. Note that charge rationing is only active when the UCS81003 is in the Active state, and it does not automatically reset when a Removal or Attach Detection event occurs. Charger emulation will start over if a Removal Detection event and Attach Detection event occur while charge rationing is active and the charge rationing threshold has not been reached. This allows charging of sequential portable devices while charge is being rationed, which means that the accumulated power given to several portable devices will still be held to the stated rationing limit.

Changing the charge rationing behavior will have no effect on the charge rationing data registers. If the behavior is changed prior to reaching the charge rationing threshold, this change will occur and be transparent to the user. When the charge rationing threshold is reached, the UCS81003 will take action, as shown in Table 7-1. If the behavior is changed after the charge rationing threshold has been reached, the UCS81003 will immediately adopt the newly programmed behavior, clearing the ALERT# pin and restoring switch operation respectively (see Table 7-3).

TABLE 7-3: EFFECTS OF CHANGING RATIONING BEHAVIOR AFTER THRESHOLD REACHED

Previous Behavior	New Behavior	Actions taken
Ignore	Report	Assert ALERT# pin.
	Report and Disconnect	1. Assert ALERT# pin. 2. Remove charger emulation profile. 3. Open port power switch. See the Report and Disconnect (default) in Table 7-1.
	Disconnect and Go to Sleep	1. Remove charger emulation profile. 2. Open port power switch. 3. Enter the Sleep state. See the Disconnect and Go to Sleep entry in Table 7-1.

Note 1: Any time the charge rationing circuitry checks the pin conditions when changing rationing behavior or resetting charge rationing, if the external pin conditions have changed, then charger emulation will be restarted (provided emulation is enabled via the pin states). If the pin conditions have not changed, the UCS81003 returns to the previous power state as if the rationing threshold had not been reached (e.g., it will not discharge V_{BUS} or restart emulation).

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TABLE 7-3: EFFECTS OF CHANGING RATIONING BEHAVIOR AFTER THRESHOLD REACHED

Previous Behavior	New Behavior	Actions taken
Report	Ignore	Release ALERT# pin.
	Report and Disconnect	Open port power switch. See the Report and Disconnect (default) entry in Table 7-1.
	Disconnect and Go to Sleep	1. Release the ALERT# pin. 2. Remove charger emulation profile. 3. Open the port power switch. 4. Enter the Sleep state. See the Disconnect and Go to Sleep entry in Table 7-1.
Report and Disconnect	Ignore	1. Release the ALERT# pin. 2. Check the M1, M2, EM_EN, S0 and PWR_EN controls and enter the indicated power state if the controls changed (see **Note 1**).
	Report	Check the M1, M2, EM_EN, S0, and PWR_EN controls and enter the indicated power state if the controls changed (see **Note 1**).
	Disconnect and Go to Sleep	1. Release the ALERT# pin. 2. Enter the Sleep state. See the Disconnect and Go to Sleep entry in Table 7-1.
Disconnect and Go to Sleep	Ignore	Check the M1, M2, EM_EN, S0, and PWR_EN controls and enter the indicated power state if the controls changed (see **Note 1**).
	Report	1. Assert the ALERT# pin. 2. Check the M1, M2, EM_EN, S0 and PWR_EN controls and enter the indicated power state if the controls changed (see **Note 1**).
	Report and Disconnect	1. Assert the ALERT# pin. 2. Check the M1, M2, EM_EN, S0 and PWR_EN controls to determine the power state, then enter that state except that the port power switch and bypass switch will not be closed (see **Note 1**).

Note 1: Any time the charge rationing circuitry checks the pin conditions when changing rationing behavior or resetting charge rationing, if the external pin conditions have changed, then charger emulation will be restarted (provided emulation is enabled via the pin states). If the pin conditions have not changed, the UCS81003 returns to the previous power state as if the rationing threshold had not been reached (e.g., it will not discharge V_{BUS} or restart emulation).

If the RTN_EN control is set to '0' prior to reaching the charge rationing threshold, rationing will be disabled and the Total Accumulated Charge registers will be cleared. If the RTN_EN control is set to '0' after the charge rationing threshold has been reached, the following will be done:

1. RATION status bit will be cleared.
2. The ALERT# pin will be released if asserted by the rationing circuitry and no other conditions are present.
3. The M1, M2, EM_EN, S0 and PWR_EN controls are checked to determine the power state. See Note 1 in Table 7-3.

Note: If the rationing behavior was set to "Report and Disconnect" when the charge rationing threshold was reached, and then the RTN_EN bit is cleared, the portable device may start charging sub-optimally because the charger emulation profile has been removed. Toggle the PWR_EN control to restart charger emulation.

Setting the RTN_RST control to '1' will automatically reset the Total Accumulated Charge registers to 00_00h. If this is done prior to reaching the charge rationing threshold, the data will continue to be accumulated restarting from 00_00h. If this is done after the charge rationing threshold is reached, the UCS81003 will take action, as shown in Table 7-2.

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7.5 Fault Handling Mechanism

The UCS81003 has two modes for handling faults:

- Latch (latch-upon-fault)
- Auto-Recovery (automatically attempt to restore the Active power state after a fault occurs).

If the SMBus is actively utilized, Auto-Recovery Fault Handling is the default error handler as determined by the LATCHS bit (see **Section 10.4.3 "Switch Configuration Register"**). Otherwise, the fault handling mechanism used depends on the state of the LATCH pin. Faults include overcurrent, overvoltage (on V_S), undervoltage (on V_{BUS}), back-voltage (V_{BUS} to V_S, or V_{BUS} to V_{DD}), discharge error and maximum allowable internal die temperature (T_{TSD}) exceeded (see **Section 5.1.5 "Error State Operation"**).

7.5.1 AUTO-RECOVERY FAULT HANDLING

When the LATCH control is low, Auto-Recovery Fault Handling is used. When an error condition is detected, the UCS81003 will immediately enter the Error state and assert the ALERT# pin (see **Section 5.1.5 "Error State Operation"**). Independently from the host controller, the UCS81003 will wait a preset time (t_{CYCLE}), check error conditions (t_{TST}) and restore Active operation if the error condition(s) no longer exist. If all other conditions that may cause the ALERT# pin to be asserted have been removed, the ALERT# pin will be released.

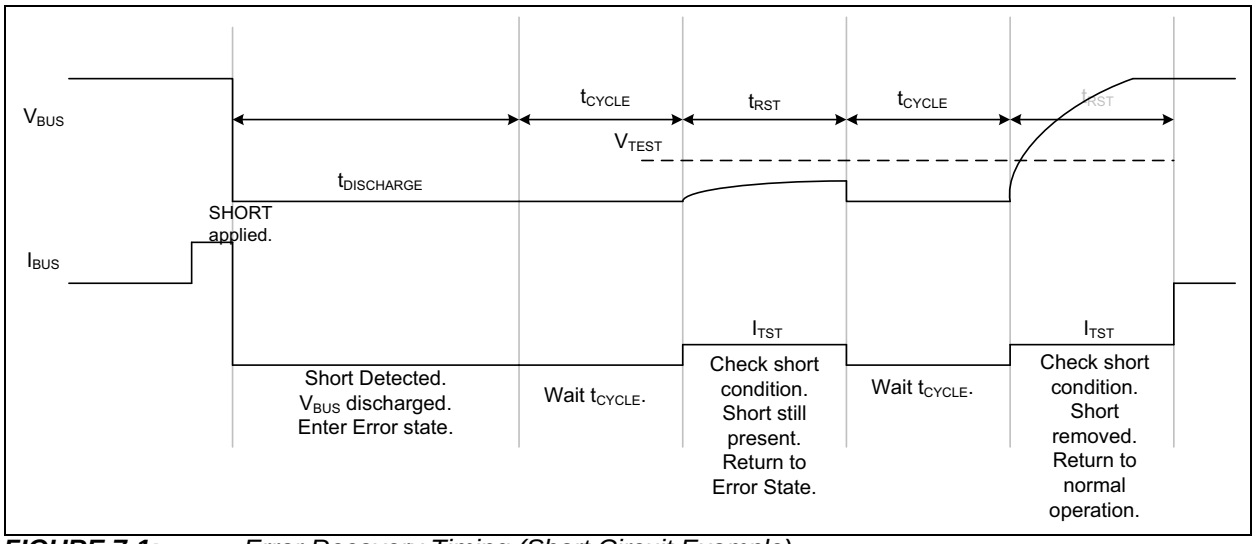

FIGURE 7-1: *Error Recovery Timing (Short Circuit Example).*

7.5.2 LATCHED FAULT HANDLING

When the LATCH control is high, Latch Fault Handling is used. When an error condition is detected, the UCS81003 will enter the Error power state and assert the ALERT# pin. Upon command from the host controller (by toggling the PWR_EN control from enabled to disabled or by clearing the ERR bit via SMBus), the UCS81003 will check error conditions once and restore Active operation if error conditions no longer exist. If an error condition still exists, the host controller is required to issue the command again to check error conditions.

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8.0 DETECT STATE

8.1 Device Attach/Removal Detection

The UCS81003 can detect the attachment and removal of a portable device on the USB port. Attach and Removal Detection does not perform any charger emulation or qualification of the device. The high-speed switch is “off” (by default) during the Detect power state.

8.2 V_{BUS} Bypass Switch

The UCS81003 contains circuitry to provide V_{BUS} current as shown in Figure 8-1. In the Detect state, V_{DD} is the voltage source; in the Active state, V_S is the voltage source. The bypass switch and the port power switch are never both on at the same time.

While the V_{BUS} bypass switch is active, the current available to a portable device will be limited to I_{BUS_BYP}, and the Attach Detection feature is active.

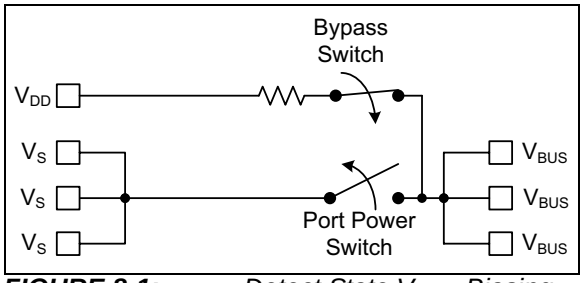

FIGURE 8-1: *Detect State V_{BUS} Biasing.*

8.3 Attach Detection

The primary Attach Detection feature is only active in the Detect power state. When active, this feature constantly monitors the current load on the V_{BUS} pin. If the current drawn by a portable device is greater than I_{DET_QUAL} for longer than t_{DET_QUAL}, an Attach Detection event occurs. This will cause the A_DET# pin to assert low and the ADET_PIN and ATT status bits to be set.

Until the port power switch is enabled, the current available to a portable device will be limited to that used to detect device attachment (I_{DET_QUAL}). Once an Attach Detection event occurs, the UCS81003 will wait for the PWR_EN control to be enabled (if not already). When PWR_EN is enabled and V_S is above the threshold, the UCS81003 will activate the USB port power switch and operate in the selected Active mode (see **Section 9.0 “Active State”**).

8.4 Removal Detection

The Removal Detection feature will be active in the Active and Detect power states if S0 = ‘1’. This feature monitors the current load on the V_{BUS} pin. If this load drops to less than $I_{REM_QUAL_DET}$ for longer than t_{REM_QUAL}, a Removal Detection event is flagged. When this event occurs, the following will be performed:

1. Disable the port power switch and the bypass switch.
2. De-assert the A_DET# pin and set the REM status register bit.
3. Enable an internal discharging device that will discharge the V_{BUS} line within $t_{DISCHARGE}$.
4. Once the V_{BUS} pin has been discharged, the device will return to the Detect state regardless of the PWR_EN control state.

9.0 ACTIVE STATE

9.1 Active State Overview

The UCS81003 has the following modes of operation in the Active state: Data Pass-Through, BC1.2 DCP, BC1.2 SDP, BC1.2 CDP and Dedicated Charger Emulation Cycle. The current limiting mode depends on the Active mode behavior (see Table 9-2).

9.2 Active Mode Selection

The Active mode selection is controlled by three controls: EM_EN, M1 and M2, as shown in Table 9-1.

TABLE 9-1: ACTIVE MODE SELECTION

M1	M2	EM_EN	Active mode
0	0	1	Dedicated Charger Emulation Cycle
0	1	0	Data Pass-Through
0	1	1	BC1.2 DCP
1	0	0	BC1.2 SDP - **Note 1**
1	0	1	Dedicated Charger Emulation Cycle
1	1	0	Data Pass-Through
1	1	1	BC1.2 CDP

Note 1: BC1.2 SDP behaves the same as the Data Pass-Through mode with the exception that it is preceded by a V_{BUS} discharge when the mode is entered per the BC1.2 specification.

9.3 BC1.2 Detection Renegotiation

The BC1.2 specification allows a charger to act as an SDP, CDP or DCP and to change between these roles. To force an attached portable device to repeat the charging detection procedure, V_{BUS} must be cycled. In compliance with this specification, the UCS81003 automatically cycles V_{BUS} when switching between the BC1.2 SDP, BC1.2 DCP and BC1.2 CDP modes.

9.4 Data Pass-Through (No Charger Emulation)

When commanded to Data Pass-Through mode, UCS81003 will close its USB high-speed data switch to allow USB communications between a portable device and host controller and will operate using Trip Current Limiting. No charger emulation profiles are applied in this mode. Data Pass-Through mode will persist until commanded otherwise by the M1, M2 and EM_EN controls.

Note 1: If it is desired that the Data Pass-Through mode operates as a traditional/standard port power switch, the S0 control should be set to '0' to allow the port power switch to be closed without requiring an Attach Detection event. When entering this mode, there is no automatic V_{BUS} discharge.

2: When the M1, M2 and EM_EN controls are set to '0', '1', '0' or to '1', '1', '0' respectively, Data Pass-Through mode will persist if the PWR_EN control is disabled; however, the UCS81003 will draw more current. To leave the Data Pass-Through mode, the PWR_EN control must be enabled before the M1, M2 and EM_EN controls are changed to the desired mode.

9.5 BC1.2 SDP (No Charger Emulation)

When commanded to BC1.2 SDP mode, UCS81003 will discharge V_{BUS}, close its USB high-speed data switch to allow USB communications between a portable device and host controller, and will operate using Trip Current Limiting. No charger emulation profiles are applied in this mode. BC1.2 SDP mode will persist until commanded otherwise by the M1, M2, EM_EN and PWR_EN controls.

Note: If it is desired that the BC1.2 SDP mode operates as a traditional/standard port power switch, the S0 control should be set to '0' to allow the port power switch to be closed without requiring an Attach Detection event.

9.6 BC1.2 CDP

When BC1.2 CDP is selected as the Active mode, UCS81003 will discharge V_{BUS}, close its USB high-speed data switch (by default), and apply the BC1.2 CDP charger emulation profile which performs handshaking per the specification. The combination of the UCS81003 CDP handshake along with a standard USB host comprises a charging downstream port. In BC1.2 CDP mode, there is no emulation timeout.

If the handshake is successful, the UCS81003 will operate using Constant Current Limiting (variable slope). If the handshake is not successful, the UCS81003 will leave the applied CDP profile in place, leave the high-speed switch closed, enable Constant Current Limiting, and persist in this condition until commanded otherwise by the M1, M2, EM_EN and PWR_EN controls.

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The UCS81003 will respond per the BC1.2 specification to the portable device initiated charger renegotiation requests.

Note 1:	BC1.2 compliance testing may require the S0 control to be set to '0' (Attach and Removal Detection feature disabled) while testing is in progress.
2:	When the UCS81003 is in BC1.2 CDP mode and the Attach and Removal Detection feature is enabled, if a power thief (such as a USB light or fan) attaches but does not assert D_P pin, a Removal event will not occur when the portable device is removed. However, if a standard USB device is subsequently attached, Removal Detection will again be fully functional. As well, if PWR_EN is cycled or M1, M2 and/or EM_EN change state, a Removal event will occur and Attach Detection will be reactivated.

9.6.1 BC1.2 CDP CHARGER EMULATION PROFILE

The BC1.2 CDP charger emulation profile acts in a reactionary manner based on stimulus from the portable device as described below and shown in Figure 2-1.

Note:	All CDP handshaking is performed with the high-speed switch closed.

1. V_{BUS} voltage is applied.
2. Primary Detection - When the portable device drives a voltage between 0.4V and 0.8V onto the D_{POUT} pin, the UCS81003 will drive 0.6V onto the D_{MOUT} pin within 20 ms.
3. When the portable device drives the D_{POUT} pin back to '0', the UCS81003 will then drive the D_{MOUT} pin back to '0' within 20 ms.
4. Optional Secondary Detection - If the portable device then drives a voltage of 0.6V (nominal) onto the D_{MOUT} pin, the UCS81003 will take no other action. This will cause the portable device to observe a '0' on the D_{POUT} pin and know that it is connected to a CDP.

9.7 BC1.2 DCP

When BC1.2 DCP is selected as the Active mode, UCS81003 will discharge V_{BUS} and apply the BC1.2 DCP charger emulation profile per the specification. In BC1.2 DCP mode, the emulation timeout and requirement for portable device current draw are automatically disabled. When the BC1.2 DCP charger emulation profile is applied within the Dedicated Charger Emulation Cycle (see **Section 9.11.3 "Legacy 3 Charger Emulation Profile"**), the timeout and current draw requirement are enabled.

If the portable device is charging after the DCP charger emulation profile is applied, the UCS81003 will leave in place the resistive short, leave the high-speed switch open and enable Constant Current Limiting (variable slope).

Note:	BC1.2 compliance testing may require the S0 control to be set to '0' (Attach and Removal Detection feature disabled) while testing is in progress.

9.7.1 BC1.2 DCP CHARGER EMULATION PROFILE

The BC1.2 DCP charger emulation profile is described as follows:

1. V_{BUS} voltage is applied. A resistor (R_{DCP_RES}) is connected between the D_{POUT} and D_{MOUT} pins.
2. Primary Detection - If the portable device drives 0.6V (nominal) onto the D_{POUT} pin, the UCS81003 will take no other action than to leave the resistor connected between D_{POUT} and D_{MOUT}. This will cause the portable device to see 0.6V (nominal) on the D_{MOUT} pin and know that it is connected to a DCP.
3. Optional Secondary Detection - If the portable device drives 0.6V (nominal) onto the D_{MOUT} pin, the UCS81003 will take no other action than to leave the resistor connected between D_{POUT} and D_{MOUT}. This will cause the portable device to see 0.6V (nominal) on the D_{POUT} pin and know that it is connected to a DCP.

9.8 Dedicated Charger

When commanded to Dedicated Charger Emulation cycle mode, the UCS81003 enables an attached portable device to enter its charging mode by applying specific charger emulation profiles in a predefined sequence. Using these profiles, the UCS81003 is capable of generating and recognizing several signal levels on the D_{POUT} and D_{MOUT} pins. The preloaded charger emulation profiles include ones compatible with YD/T-1591 (2009), 12W charging, Samsung and many RIM portable devices. Other levels, sequences and protocols are configurable via the SMBus/I^2C.

When a charger emulation profile is applied, a programmable timer for the emulation profile is started. When emulation timeout occurs, the UCS81003 checks the I_{BUS} current against a programmable threshold. If the current is above the threshold, the charger emulation profile is accepted and the associated current limiting mode is applied. No active USB data communication is possible when charging in this mode (by default - see **Section 10.4.5 "High-Speed Switch Configuration Register"**).

9.8.1 EMULATION RESET

Prior to applying any of the charger emulation profiles, the UCS81003 will perform an emulation reset. This means that the UCS81003 resets the V_{BUS} line by disconnecting the port power switch and connecting V_{BUS} to ground via an internal 100Ω resistor for $t_{DISCHARGE}$ time. The port power switch will be held open for a time equal to t_{EM_RESET} at which point the port power switch will be closed and the V_{BUS} voltage applied. The D_{POUT} and D_{MOUT} pins will be pulled low using internal 15 kΩ pull-down resistors.

Note:	To help prevent possible damage to a portable device, the D_{POUT} and D_{MOUT} pins have current limiting in place when the emulation profiles are applied.

9.8.2 EMULATION CYCLING

In Dedicated Charger Emulation Cycle mode, the charger emulation profiles (if enabled) will be applied in the following order:

1. Legacy 1
2. Legacy 2
3. Legacy 3
4. Legacy 4
5. Legacy 5
6. Legacy 6
7. Legacy 7
8. Custom (disabled by default). If the CS_FRST configuration bit is set, then the Custom charger emulation profile will be tested first and the order will proceed as given.

If S0 = '0' and a portable device is not attached in DCE Cycle mode, the UCS81003 will be cycling through charger emulation profiles (by default). There is no guarantee which charger emulation profile will be applied first when a portable device attaches.

The UCS81003 will apply a charger emulation profile until one of the following exit conditions occurs:

- Current greater than I_{BUS_CHG} is detected flowing out of V_{BUS} at the respective emulation timeout time. In this case, the profile is assumed to be accepted and no other profiles will be applied.
- The respective emulation timeout ($t_{EM_TIMEOUT}$) time is reached without current that exceeds the I_{BUS_CHG} limit flowing out of V_{BUS} (the emulation timeout is enabled by default, see **Section 10.4.2 "Emulation Configuration Register"** and Register 10-35). The profile is assumed to be rejected, and the UCS81003 will perform emulation reset and apply the next profile, if there is one.

Emulation timeouts can be programmed for each charger emulation profile (see **Section 10.11 "Preloaded Emulation Timeout Configuration Registers"** and Register 10-35).

9.8.3 DCE CYCLE RETRY

If none of the charger emulation profiles cause a charge current to be drawn, the UCS81003 will perform emulation reset and cycle through the profiles again (if the EM_RETRY bit is set (default - see **Section 10.4.2 "Emulation Configuration Register"**). The UCS81003 will continue to cycle through the profiles as long as charging current is not drawn and the PWR_EN control is enabled. If the Emulation Retry is not enabled, the UCS81003 will flag "No Handshake" and end the DCE Cycle using Trip Current Limiting.

9.9 Current Limit Mode Associations

The UCS81003 will close the port power switch and use the Current Limiting mode as shown in Table 9-2.

TABLE 9-2: CURRENT LIMIT MODE OPTIONS

Active Mode	Current Limit Mode (See Section 10.14 "Current Limiting Behavior Configuration Registers")
Data Pass-Through	Trip mode
BC1.2 SDP	Trip mode
BC1.2 CDP	CC mode if I_{LIM} < 1.68A, otherwise, Trip mode
BC1.2 DCP	CC mode if I_{LIM} < 1.68A, otherwise, Trip mode
DCE Cycle	
During DCE Cycle when a charger emulation profile is being applied and the emulation timeout is active	CC mode if I_{LIM} < 1.68A, otherwise, Trip mode

Note 1: As noted in the last three rows in Table 9-2, under those specific conditions with I_{LIM} < 1.68A, it is the relationship of I_{LIM} and I_{BUS_R2MIN} that determines the current limiting mode. In these cases, the value of I_{BUS_R2MIN} is determined by CS_R2_IMIN<2:0> bits 4-2 in the Custom Current Limiting Behavior Configuration register - 51h (Register 10-49).

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TABLE 9-2: CURRENT LIMIT MODE OPTIONS (CONTINUED)

Active Mode	Current Limit Mode (See Section 10.14 "Current Limiting Behavior Configuration Registers")
Legacy 3 charger emulation profile accepted or the emulation timeout is disabled	CC mode if I_{LIM} < 1.68A, otherwise, Trip mode
Legacy 1, Legacy 2 or Legacy 4 - Legacy 7 charger emulation profile accepted or the emulation timeout is disabled	Trip mode if I_{BUS_R2MIN} < I_{LIM} or I_{LIM} > 1.68A (normal operation), otherwise, CC mode (see Register 10-49)
Custom charger emulation profile accepted or the emulation timeout is disabled	Trip mode if I_{BUS_R2MIN} < I_{LIM} or I_{LIM} > 1.68A (normal operation), otherwise, CC mode (see Register 10-49)
No handshake (DCE Cycle with Emulation Retry not enabled)	Trip mode if IBUS_R2MIN < I_{LIM} or I_{LIM} > 1.68A (normal operation), otherwise, CC mode (see Register 10-49)

Note 1: As noted in the last three rows in Table 9-2, under those specific conditions with I_{LIM} < 1.68A, it is the relationship of I_{LIM} and I_{BUS_R2MIN} that determines the current limiting mode. In these cases, the value of I_{BUS_R2MIN} is determined by CS_R2_IMIN<2:0> bits 4-2 in the Custom Current Limiting Behavior Configuration register - 51h (Register 10-49).

9.10 No Handshake

In DCE Cycle mode with emulation retry disabled, a No Handshake condition is flagged (the NO_HS status bit stays set (see Register 10-5) when the end of the DCE Cycle is reached without a handshake and without drawing current.

All signatures/handshaking placed on the D_{POUT} and D_{MOUT} pins are removed. The UCS81003 will operate with the high-speed switch opened or closed as determined by the high-speed switch configuration, and will use Trip or Constant Current Limiting, as determined by the I_{BUS_R2MIN} setting (CS_R2_IMIN<2:0> bits 4-2 in the Custom Current Limiting Behavior Configuration register 51h).

The portable devices that can cause this are generally the ones that pull up D_{POUT} to some voltage and leave it there, or apply the wrong voltage.

9.11 Preloaded Charger Emulation Profiles

The following charger emulation profiles are resident to the UCS81003:

- Legacy 1 Charger Emulation Profile
- Legacy 2, 4, 5 and 7 Charger Emulation Profiles
- Legacy 3 Charger Emulation Profile
- Legacy 6 Charger Emulation Profile
- BC1.2 CDP Charger Emulation Profile
- BC1.2 DCP Charger Emulation Profile

9.11.1 LEGACY 1 CHARGER EMULATION PROFILE

Legacy 1 Charger Emulation Profile does the following:

1. The UCS81003 will apply 900 mV to both the D_{POUT} and the D_{MOUT} pins.
2. V_{BUS} voltage is applied.
3. If the portable device draws more than I_{BUS_CHG} current when the $t_{EM_TIMEOUT}$ timer expires, the UCS81003 will accept that the currently applied profile is the correct charger emulation profile for the attached portable device. Charging commences. The voltages applied to the D_{POUT} and D_{MOUT} pins will remain in place (unless EM_RESP is set to 0b). The UCS81003 will begin operating in Trip mode or CC mode as determined by the I_{BUS_R2MIN} setting (see **Section 10.14 "Current Limiting Behavior Configuration Registers"**).
4. If the portable device does not draw more than I_{BUS_CHG} current when $t_{EM_TIMEOUT}$ timer expires, the UCS81003 will stop the currently applied charger emulation profile. This will cause all voltages put onto the D_{POUT} and D_{MOUT} pins to be removed. Emulation reset occurs, and the UCS81003 will initiate the next charger emulation profile.

9.11.2 LEGACY 2, 4, 5 AND 7 CHARGER EMULATION PROFILES

Legacy 2, 4, 5 and 7 Charger Emulation Profiles follow the same pattern of operation, although the voltage that is applied on the D_{POUT} and D_{MOUT} pins will vary. They do the following:

1. The UCS81003 will apply a voltage on the D_{POUT} pin using either a current-limited voltage source or a voltage divider between V_{BUS} and ground with the center tap on the D_{POUT} pin.
2. The UCS81003 will apply a possibly different voltage on the D_{MOUT} pin, using either a current-limited voltage source or a voltage divider between V_{BUS} and ground, with the center tap on the D_{MOUT} pin.
3. V_{BUS} voltage is applied.

4. If the portable device draws more than I_{BUS_CHG} current when the $t_{EM_TIMEOUT}$ timer expires, the UCS81003 will accept that the currently applied profile is the correct charger emulation profile for the attached portable device. Charging commences. The voltages applied to the D_{POUT} and D_{MOUT} pins will remain in place (unless EM_RESP is set to 0b). The UCS81003 will begin operating in Trip mode or CC mode, as determined by the I_{BUS_R2MIN} setting (see **Section 10.14 "Current Limiting Behavior Configuration Registers"**).
5. If the portable device does not draw more than I_{BUS_CHG} current when $t_{EM_TIMEOUT}$ timer expires, the UCS81003 will stop the currently applied charger emulation profile. This will cause all voltages put onto the D_{POUT} and D_{MOUT} pins to be removed. Emulation reset occurs, and the UCS81003 will initiate the next charger emulation profile.

Additionally, the user may "build" a charger emulation profile by determining the voltage and resistance characteristics that are placed on each of the D_{POUT} and D_{MOUT} pins. See **Section 9.12 "Custom Charger Emulation Profile"**.

9.11.3 LEGACY 3 CHARGER EMULATION PROFILE

The Legacy 3 Charger Emulation Profile does the following:

1. The UCS81003 will connect a resistor (R_{DCP_RES}) between D_{POUT} and D_{MOUT}.
2. V_{BUS} is applied.
3. If the portable device draws more than I_{BUS_CHG} current when the $t_{EM_TIMEOUT}$ timer expires (enabled by default), the UCS81003 will accept that this is the correct charger emulation profile for the attached portable device. Charging commences. The resistive short between the D_{POUT} and D_{MOUT} pins will be left in place.
4. If the portable device does not draw more than I_{BUS_CHG} current when $t_{EM_TIMEOUT}$ timer expires, the UCS81003 will stop the Legacy 3 Charger Emulation. This will cause resistive short between the D_{POUT} and D_{MOUT} pins to be removed. Emulation reset occurs, and the UCS81003 will initiate the next charger emulation profile.

9.11.4 LEGACY 6 CHARGER EMULATION PROFILE

The Legacy 6 Charger Emulation Profile does the following:

1. The UCS81003 will apply a voltage on the D_{POUT} pin using a voltage divider between V_{BUS} and ground with the center tap on the D_{POUT} pin.
2. V_{BUS} voltage is applied.
3. If the portable device draws more than I_{BUS_CHG} current when the $t_{EM_TIMEOUT}$ timer expires, the UCS81003 will accept that Legacy 6 is the correct charger emulation profile for the attached portable device. Charging commences. The voltage applied to the D_{POUT} pin will remain in place (unless EM_RESP is set to 0b). The UCS81003 will begin operating in Trip mode or CC mode, as determined by the I_{BUS_R2MIN} setting (see **Section 10.14 "Current Limiting Behavior Configuration Registers"**).
4. If the portable device does not draw more than I_{BUS_CHG} current when $t_{EM_TIMEOUT}$ timer expires, the UCS81003 will stop the Legacy 6 Charger Emulation Profile. This will cause the voltage put onto the D_{POUT} pin to be removed. Emulation reset occurs, and the UCS81003 will initiate the next charger emulation profile.

9.12 Custom Charger Emulation Profile

The UCS81003 allows the user to create a Custom Charger emulation profile to handshake as any type of charger. This profile can be included in the DCE Cycle. In addition, it can be placed first or last in the profile sequence in the DCE Cycle. See Register 10-35.

The Custom charger emulation profile uses a number of registers to define stimuli and behaviors. The Custom Charger emulation profile uses three separate stimulus/response pairs that will be detected and applied in sequence, allowing flexibility to "build" any of the preloaded emulation profiles, or tailor the profile to match a specific charger application.

For details, see Application Note 24.14 – *"UCS1002 Fundamentals of Custom Charger Emulation"*.

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10.0 REGISTER DESCRIPTION

The registers shown in Table 10-1 are accessible through the SMBus or I^2C. While in the Sleep state, the UCS81003 will retain configuration and charge rationing data as indicated in the text. If a register does not indicate that data will be retained in the Sleep power state, this information will be lost when the UCS81003 enters the Sleep power state.

TABLE 10-1: REGISTER SET IN HEXADECIMAL ORDER

Register Address	Register Name	R/W	Function	Default Value	Page No.
00h	Current Measurement	R	Stores the current measurement	00h	47
01h	Total Accumulated Charge High Byte	R	Stores the total accumulated charge delivered high byte	00h	48
02h	Total Accumulated Charge Middle High Byte	R	Stores the total accumulated charge delivered middle high byte	00h	48
03h	Total Accumulated Charge Middle Low Byte	R	Stores the total accumulated charge delivered middle low byte	00h	48
04h	Total Accumulated Charge Low Byte	R	Stores the total accumulated charge delivered low byte	00h	48
0Fh	Other Status	R	Indicates emulation status as well as the ALERT# and A_DET# pin status	00h	49
10h	Interrupt Status	See Register 10-3	Indicates why ALERT# pin asserted	00h	50
11h	General Status	R/R-C	Indicates general status	00h	51
12h	Profile Status 1	R	Indicates which charger emulation profile was accepted	00h	52
13h	Profile Status 2	R		00h	53
14h	Pin Status	R	Indicates the pin states of the internal control pins	00h	54
15h	General Configuration	R/W	Controls basic functionality	01h	55
16h	Emulation Configuration	R/W	Controls emulation functionality	8Ch	56
17h	Switch Configuration	R/W	Controls advanced switch functions	04h	57
18h	Attach Detect Configuration	R/W	Controls Attach Detect functionality	46h	58
19h	Current Limit	R/W	Controls the maximum current limit	00h	60
1Ah	Charge Rationing Threshold High Byte	R/W	Controls the Current Threshold I_{THRESH} used by the charge rationing circuitry	FFh	60
1Bh	Charge Rationing Threshold Low Byte	R/W	Controls the Current Threshold I_{THRESH} used by the charge rationing circuitry	FFh	60
1Ch	Auto-recovery Configuration	R/W	Controls the Auto-Recovery functionality	2Ah	61
1Eh	I_{BUS_CHG} Configuration	R/W	Stores the limit for I_{BUS_CHG} used to determine if emulation is successful	0Fh	62
1Fh	t_{DET_CHARGE} Configuration	R/W	Stores bits that define the t_{DET_CHARGE} time	03h	63
20h	BCS Emulation Enable	R/W	Enables BCS charger emulation profiles	16h	63
21h	Legacy Emulation Enable	R/W	Enables Legacy charger emulation profiles	00h	64
22h	BCS Emulation Timeout Config	R/W	Controls timeout for each BCS charger emulation profile	10h	65

TABLE 10-1: REGISTER SET IN HEXADECIMAL ORDER (CONTINUED)

Register Address	Register Name	R/W	Function	Default Value	Page No.
23h	Legacy Emulation Timeout Config 1	R/W	Controls timeout for Legacy charger emulation profiles 1 – 4	6Ch	65
24h	Legacy Emulation Timeout Config 2	R/W	Controls timeout for Legacy charger emulation profiles 5 – 7	01h	66
25h	High-Speed Switch Configuration	R/W	Controls when the high-speed switch is enabled	14h	59
30h	Applied Charger Emulation	R	Indicates which charger emulation profile is being applied	00h	67
31h	Preloaded Emulation Stimulus 1 - Config 1	R	Indicates the stimulus and timing for Stimulus 1	00h	67
32h	Preloaded Emulation Stimulus 1 - Config 2	R	Indicates the response and magnitude for Stimulus 1	26h	68
33h	Preloaded Emulation Stimulus 1 - Config 3	R	Indicates the threshold and pull-up/pull-down settings for Stimulus 1	00h	69
34h	Preloaded Emulation Stimulus 1 - Config 4	R	Indicates the resistor ratio for Stimulus 1	02h	70
35h	Preloaded Emulation Stimulus 2 - Config 1	R	Indicates the stimulus and timing for Stimulus 2	00h	71
36h	Preloaded Emulation Stimulus 2 - Config 2	R	Indicates the response and magnitude for Stimulus 2	09h	72
37h	Preloaded Emulation Stimulus 2 - Config 3	R	Indicates the threshold and pull-up/pull-down settings for Stimulus 2	00h	73
38h	Preloaded Emulation Stimulus 2 - Config 4	R	Indicates the resistor ratio for Stimulus 2	04h	74
39h	Preloaded Emulation Stimulus 3 - Config 1	R	Indicates the stimulus and timing for Stimulus 3 (**CDP only**)	00h	75
3Ah	Preloaded Emulation Stimulus 3 - Config 2	R	Indicates the response and magnitude for Stimulus 3 (**CDP only**)	00h	76
3Bh	Preloaded Emulation Stimulus 3 - Config 3	R	Indicates the threshold and pull-up/pull-down settings for Stimulus 3 (**CDP only**)	00h	77
40h	Custom Emulation Config	R/W	Controls general configuration of the Custom charger emulation profile	01h	79
41h	Custom Stimulus/Response Pair 1 - Config 1	R/W	Sets the stimulus and timing for Stimulus 1	00h	80
42h	Custom Stimulus/Response Pair 1 - Config 2	R/W	Sets the response and magnitude for Stimulus 1	00h	81
43h	Custom Stimulus/Response Pair 1 - Config 3	R/W	Sets the threshold and pull-up/pull-down settings for Stimulus 1	00h	82
44h	Custom Stimulus/Response Pair 1 - Config 4	R/W	Sets the resistor ratio for Stimulus 1	00h	83
45h	Custom Stimulus/Response Pair 2 - Config 1	R/W	Sets the stimulus and timing for Stimulus 2	00h	84
46h	Custom Stimulus/Response Pair 2 - Config 2	R/W	Sets the response and magnitude for Stimulus 2	00h	85
47h	Custom Stimulus/Response Pair 2 - Config 3	R/W	Sets the threshold and pull-up/pull-down settings for Stimulus 2	00h	86
48h	Custom Stimulus/Response Pair 2 - Config 4	R/W	Sets the resistor ratio for Stimulus 2	00h	87

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TABLE 10-1: REGISTER SET IN HEXADECIMAL ORDER (CONTINUED)

Register Address	Register Name	R/W	Function	Default Value	Page No.
49h	Custom Emulation Stimulus 3 - Config 1	R/W	Sets the stimulus and timing for Stimulus 3	00h	88
4Ah	Custom Stimulus/Response Pair 3 - Config 2	R/W	Sets the response and magnitude for Stimulus 3	00h	89
4Bh	Custom Stimulus/Response Pair 3 - Config 3	R/W	Sets the threshold and pull-up/pull-down settings for Stimulus 3	00h	90
4Ch	Custom Stimulus/Response Pair 3 - Config 4	R/W	Sets the resistor ratio for Stimulus 3	00h	91
50h	Applied Current Limiting Behavior	R	Indicates the applied current limiting behavior	82h	92
51h	Custom Current Limiting Behavior Config	R/W	Controls the custom current limiting behavior	82h	93
FDh	Product ID	R	Stores a fixed value that identifies each product	4Eh	94
FEh	Manufacturer ID	R	Stores a fixed value that identifies Microchip	5Dh	94
FFh	Revision	R	Stores a fixed value that represents the revision number	82h	94

During power-on reset (POR), the default values are stored in the registers. A POR is initiated when power is first applied to the part and the voltage on the V_{DD} supply surpasses the V_{DD_TH} level, as specified in the electrical characteristics. Any reads to undefined registers will return 00h. Writes to undefined registers will not have an effect.

When a bit is “set”, this means that the user writes a logic ‘1’ to it. When a bit is “cleared”, this means that the user writes a logic ‘0’ to it.

10.1 Current Measurement Register (Address 00h)

Name	Bits	Address	Cof	Default
Current Measurement	8	00h	R	00h

The Current Measurement register stores the measured current value delivered to the portable device (I_{BUS}). This value is updated continuously while the device is in the Active power state. The bit weights are in mA and the range is from 0 mA to 2988.6A (the maximum value corresponds to 255 LSB, where 1 LSB = 11.72 mA).

This data will be cleared when the device enters the Sleep or Detect states. This data will also be cleared whenever the port power switch is turned off (including during emulation or any time that V_{BUS} is discharged).

10.2 Total Accumulated Charge Registers

Name	Bits	Address	Cof	Default
Total Accumulated Charge High Byte	8	01h	R	00h
Total Accumulated Charge Middle High	8	02h	R	00h
Total Accumulated Charge Middle Low Byte	8	03h	R	00h
Total Accumulated Charge Low Byte	8	04h	R	00h

The Total Accumulated Charge registers store the total accumulated charge delivered from the V_S source to a portable device. The bit weighting of the registers is given in mAh. The register value is reset to 00_00h only when the RTN_RST bit is set or if the RTN_EN bit is cleared. This value will be retained when the device transitions out of the Active state and resumes accumulation if the device returns to the Active state and charge rationing is still enabled.

These registers are updated every one (1) second while the UCS81003 is in the Active power state. Every time the value is updated, it is compared against the target value in the Charge Rationing Threshold registers (see **Section 10.6 “Charge Rationing Threshold Registers”**).

REGISTER 10-1: TOTAL ACCUMULATED CHARGE REGISTER (ADDRESSES 01H – 04H)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
ACC<25>	ACC<24>	ACC<23>	ACC<22>	ACC<21>	ACC<20>	ACC<19>	ACC<18>
bit 31							bit 24

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
ACC<17>	ACC<16>	ACC<15>	ACC<14>	ACC<13>	ACC<12>	ACC<11>	ACC<10>
bit 23							bit 16

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
ACC<9>	ACC<8>	ACC<7>	ACC<6>	ACC<5>	ACC<4>	ACC<3>	ACC<2>
bit 15							bit 8

R-0	R-0	R-x	R-x	R-x	R-x	R-x	R-x
ACC<1>	ACC<0>	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-6 **ACC<25:0>: Total Accumulated Charge**
1 LSB = 0.00325 mAh

bit 5-0 **Unimplemented**

10.3 Status Registers

Name	Bits	Address	Cof	Default
Other Status	8	0Fh	R	00h
Interrupt Status	8	10h	R/W	00h
General Status	8	11h	R/R-C	00h
Profile Status 1	8	12h	R	00h
Profile Status 2	8	13h	R	00h
Pin Status	8	14h	R	00h

The Status registers store bits that indicate error conditions as well as Attach Detection and Removal Detection. Unless otherwise noted, these bits will operate as described when the UCS81003 is operating in Stand-Alone mode.

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REGISTER 10-2: OTHER STATUS REGISTER (ADDRESS 0FH)

U-x	U-x	R-0	R-0	R-0	R-0	R-0	R-0
—	—	ALERT_PIN	ADET_PIN	CHG_ACT	EM_ACT	EM_STEP<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented**

bit 5 **ALERT_PIN:** Reflects the status of the ALERT# pin. This bit is set and cleared as the ALERT# pin changes states.

1 = ALERT# pin is asserted low
0 = ALERT# pin is released

bit 4 **ADET_PIN:** Reflects the status of the A_DET# pin. When set, indicates that the A_DET# pin is asserted low. This bit is set and cleared as the A_DET# pin changes states. (**Note 1**)

1 = A_DET# pin is asserted low
0 = A_DET# pin is released

bit 3 **CHG_ACT:** This bit is automatically set when IBUS > I_{BUS_CHG} and cleared when IBUS < I_{BUS_CHG}. (**Note 2**)

1 = IBUS > I_{BUS_CHG}
0 = IBUS < I_{BUS_CHG}

bit 2 **EM_ACT:** Indicates that the UCS81003 is in the Active state and emulating. The actual profile that is being applied is identified by PRE_EM_SEL<3:0> (see **Section 10.12.1 "Applied Charger Emulation Register"**). This bit is set and cleared automatically. (**Note 3**)

1 = Device is in Active state and emulating
0 = Device is not emulating

bit 1-0 **EM_STEP<1:0>:** Indicates which stimulus / response pair is currently being applied by the charger emulation profile as shown below. These bits are set and cleared automatically. Note that the Legacy charger emulation profiles and the BC1.2 DCP charger emulation profile do not use Stimulus / Response Pair #3.

00 = None Applied. Waiting for current.
01 = Stimulus/Response #1
10 = Stimulus/Response #2
00 = Stimulus/Response #3 if applicable

Note 1: If S0 is '1', PWR_EN is enabled, and V_S is not present, the ADET_PIN bit will cycle if the current draw exceeds the current capacity of the bypass switch.

2: The CHG_ACT bit does not indicate that a portable device has accepted one of the charger emulation profiles. This bit will cycle during the Dedicated Charger Emulation Cycle.

3: The EM_ACT bit does not indicate that a portable device has accepted one of the emulation profiles. This bit will cycle during the Dedicated Charger Emulation Cycle.

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REGISTER 10-3: INTERRUPT STATUS REGISTER (ADDRESS 10H)

R/W-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
ERR	DISCH_ERR	RESET	KEEP_OUT	TSD	OV_VOLT	BACK_V	OV_LIM
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **ERR:** Indicates that an error was detected and the device has entered the Error state. Writing this bit to a '0' will clear the Error state and allows the device to be returned to the Active state. When written to '0', all error conditions are checked. If all error conditions have been removed, the UCS81003 returns to the Active state. This bit is set automatically by the UCS81003 when the Error state is entered. Regardless of the fault handling mechanism used, if any other bit is set in the Interrupt Status register (10h), the device will not leave the Error state. (**Note 1** and **Note 2**)

This bit is cleared automatically by the UCS81003 if the Auto-Recovery fault handling functionality is active and no error conditions are detected. Likewise, this bit is cleared when the PWR_EN control is disabled.

1 = One or more errors have been detected, and the UCS81003 has entered the Error state.

0 = There are no errors detected.

bit 6 **DISCH_ERR:** Indicates that the UCS81003 was unable to discharge the V_{BUS} node. This bit will be cleared when read if the error condition has been removed or if the ERR bit is cleared. This bit will cause the ALERT# pin to be asserted and the device to enter the Error state.

1 = UCS81003 was unable to discharge the V_{BUS} node.

0 = No V_{BUS} discharge error.

bit 5 **RESET:** Indicates that the UCS81003 has just been reset and should be re-programmed. This bit will be set at power up. This bit is cleared when read or when the PWR_EN control is toggled. The ALERT# pin is not asserted when this bit is set. This data is retained in the Sleep state.

1 = UCS81003 has just been reset

0 = Reset did not occur.

bit 4 **KEEP_OUT:** Indicates that the V-I output on the V_{BUS} pins has dropped below V_{BUS_MIN}. This bit will be cleared when read if the error condition has been removed or if the ERR bit is cleared. This bit will cause the ALERT# pin to be asserted and the device to enter the Error state.

1 = $V_{BUS} < V_{BUS_MIN}$

0 = $V_{BUS} > V_{BUS_MIN}$

bit 3 **TSD:** Indicates that the internal temperature has exceeded T_{TSD} threshold and the device has entered the Error state. This bit will be cleared when read if the error condition has been removed or if the ERR bit is cleared. This bit will cause the ALERT# pin to be asserted and the device to enter the Error state.

1 = Internal temperature > T_{TSD}

0 = Internal temperature < T_{TSD}

bit 2 **OV_VOLT:** Indicates that the V_S voltage has exceeded the V_{S_OV} threshold and the device has entered the Error state. This bit will be cleared when read, if the error condition has been removed or if the ERR bit is cleared. This bit will cause the ALERT# pin to be asserted and the device to enter the Error state.

1 = $V_S > V_{S_OV}$

0 = $V_S < V_{S_OV}$

bit 1 **BACK_V:** Indicates that the V_{BUS} voltage has exceeded the V_S or V_{DD} voltages by more than 150 mV. This bit will be cleared when read if the error condition has been removed or if the ERR bit is cleared. This bit will cause the ALERT# pin to be asserted and the device to enter the Error state.

1 = $V_{BUS} > V_S$, or $V_{BUS} > V_{DD}$ by more than 150 mV

0 = V_{BUS} voltage has not exceeded the V_S and V_{DD} voltages by more than 150 mV

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REGISTER 10-3: INTERRUPT STATUS REGISTER (ADDRESS 10H) (CONTINUED)

bit 0 **OV_LIM:** Indicates that the I_{BUS} current has exceeded both the I_{LIM} threshold and the I_{BUS_R2MIN} threshold settings. This bit will be cleared when read if the error condition has been removed or if the ERR bit is cleared. This bit will cause the ALERT# pin to be asserted and the device to enter the Error state.

1 = $I_{BUS} > I_{LIM}$ and I_{BUS_R2MIN}
0 = I_{BUS} has not exceeded both I_{LIM} threshold and the I_{BUS_R2MIN} threshold settings

Note 1: If the Auto-Recovery fault handling is not used, the ERR bit must be written to a logic '0' to be cleared. It will also be cleared when the PWR_EN control is disabled.

2: Note that the ERR bit does not necessarily reflect the ALERT# pin status. The ALERT# pin may be cleared or asserted without the ERR bit changing states.

REGISTER 10-4: GENERAL STATUS REGISTER (ADDRESS 11H)

R-0	U-x	U-x	R-0	R-0	R-C	R-C	R-C
RATION	—	—	CC_MODE	TREG	LOW_CUR	REM	ATT
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
C = Clear on Read			

bit 7 **RATION:** Indicates that the UCS81003 has delivered the programmed amount of power to a portable device. If the RATION_BEH bits are set to interrupt the host, this bit will cause the ALERT# pin to be asserted. This bit is cleared when read. This bit is also cleared automatically when the RTN_RST bit is set or the RTN_EN bit is cleared (see **Section 10.4.1 "General Configuration Register"**).

1 = UCS81003 has delivered the programmed amount of power to a portable device
0 = UCS81003 has not delivered the programmed amount of power to a portable device

bit 6-5 **Unimplemented**

bit 4 **CC_MODE:** Indicates that the I_{BUS} current has exceeded I_{LIM}. Current is in Region 2 (I_{BUS_R2MIN}).

1 = $I_{BUS} > I_{LIM}$
0 = $I_{BUS} < I_{LIM}$

bit 3 **TREG:** Indicates that the internal temperature has exceeded T_{REG} and that the current limit has been reduced. This bit is cleared when read and will not cause the ALERT# pin to be asserted, unless the ALERT_LINK bit is set.

1 = Internal temperature > T_{REG}
0 = Internal temperature < T_{REG}

bit 2 **LOW_CUR:** Indicates that a portable device has reduced its charge current to below ~6.4 mA and may be finished charging. This bit is cleared when read and will not cause the ALERT# pin to be asserted, unless the ALERT_LINK bit is set.

1 = I_{BUS} < 6.4 mA
0 = I_{BUS} > 6.4 mA

bit 1 **REM:** Indicates that a Removal Detection event has occurred and there is no longer a portable device present. This bit is cleared when read and will not cause the ALERT# pin to be asserted. It will cause the A_DET# pin to be released.

1 = Removal Detected
0 = No Removal Detected

bit 0 **ATT:** Indicates that an Attach Detection event has occurred and there is a new portable device present. This bit is cleared when read and will not cause the ALERT# pin to be asserted. It will cause the A_DET# pin to be asserted.

1 = Attach Detected
0 = No Attach Detected

10.3.1 PROFILE STATUS 1 REGISTER

These bits are indicators only and will not cause the ALERT# pin or A_DET# pin to change states. The CUST, DCP, CDP and PT bits are cleared under the following circumstances:

- the PWR_EN control is disabled
- a new Active mode is selected
- a Removal Detection event occurs.

REGISTER 10-5: PROFILE STATUS 1 REGISTER (ADDRESS 12H)

R-0	U-x	U-x	R-0	R-0	R-0	R-0	R-0
NO_HS	—	—	VS_LOW	CUST	DCP	CDP	PT
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **NO_HS:** The NO_HS bit is only set during the Dedicated Charger Emulation Cycle (see **Section 9.10 "No Handshake"**). This bit is automatically cleared whenever a new charger emulation profile is applied. (**Note 1**)
1 = No handshake at the end of the DCE Cycle.
0 = A new charger emulation profile has been applied

bit 6-5 **Unimplemented**

bit 4 **VS_LOW:** Indicates that the V_S voltage is below the V_{S_UVLO} threshold and the port power switch is held off. This bit is cleared automatically when the V_S voltage is above the V_{S_UVLO} threshold.
1 = $V_S < V_{S_UVLO}$
0 = $V_S > V_{S_UVLO}$

bit 3 **CUST:** Indicates that the portable device successfully performed a handshake with the user-defined Custom Charger Emulation Profile during the DCE Cycle and is charging. Based on the Custom Charger Emulation Profile configuration, the high-speed switch will be either open or closed (see **Section 10.13 "Custom Emulation Configuration Registers"**). The port power switch current limiting mode is determined by the Custom current limiting behavior settings (see **Section 10.14.2 "Custom Current Limiting Behavior Configuration Register"**).
1 = Custom Profile handshake complete
0 = No Custom Profile handshake

bit 2 **DCP:** Indicates that the portable device accepted the BC1.2 DCP charger emulation profile and is charging. The high-speed switch will be controlled via the HSW_DCE bit (see **Section 10.4.5 "High-Speed Switch Configuration Register"**), and the port power switch will use Constant Current Limiting.
1 = DCP handshake complete
0 = No DCP handshake

bit 1 **CDP:** Indicates that the portable device successfully performed a handshake with the BC1.2 CDP charger emulation profile and is charging. The high-speed switch will be closed, and the port power switch will use Trip Current Limiting.
1 = CDP handshake complete
0 = No CDP handshake

bit 0 **PT:** Indicates that the UCS81003 is in the Data Pass-through or BC1.2 SDP Active mode. The high-speed switch will be closed, and the port power switch will use Trip Current Limiting. (**Note 2**)
1 = UCS81003 is in the Data Pass-through or BC1.2 SDP Active mode.
0 = UCS81003 is not in the Data Pass-through or BC1.2 SDP Active mode.

Note 1: The NO_HS bit does not indicate that a portable device is drawing current and it may be cleared to '0' (indicating a handshake) and a portable device not charge. This bit is set at the end of each charger emulation profile if a portable device does not handshake with it. This bit will not be set at the same time that any other Profile Status register bits are set.

2: When the UCS81003 is configured as a Data Pass-through and a Removal event and then an Attach event occur without changing the Active mode, the PT bit will not be set again even though the UCS81003 is still operating as a Data Pass-through as configured. Toggling the M1 control will re-enable the PT status bit.

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10.3.2 PROFILE STATUS 2 REGISTER

These bits indicate which profile was accepted. These bits are indicators only and will not cause the ALERT# pin or A_DET# pin to change states. These bits are cleared under the following circumstances:

- the PWR_EN control is disabled
- a new Active mode is selected
- a Removal Detection event occurs.

REGISTER 10-6: PROFILE STATUS 2 REGISTER (ADDRESS 13H)

U-x	R-0	R-0	R-0	R-0	R-0	R-0	R-0
—	LG7	LG6	LG5	LG4	LG3	LG2	LG1
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented**

bit 6 **LG7:** Indicates that the portable device successfully performed a handshake with the Legacy 7 charger emulation profile and is charging. The high-speed switch will be controlled via the HSW_DCE bit (see **Section 10.4.5 "High-Speed Switch Configuration Register"**). The port power switch current limiting mode is determined by the Custom current limiting behavior settings (see **Section 10.14.2 "Custom Current Limiting Behavior Configuration Register"**).

1 = Handshake successful with the Legacy 7 charger emulation profile and charging.
0 = Not charging with Legacy 7 charger emulation profile.

bit 5 **LG6:** Indicates that the portable device successfully performed a handshake with the Legacy 6 charger emulation profile and is charging. The high-speed switch will be controlled via the HSW_DCE bit (see **Section 10.4.5 "High-Speed Switch Configuration Register"**). The port power switch current limiting mode is determined by the Custom current limiting behavior settings (see **Section 10.14.2 "Custom Current Limiting Behavior Configuration Register"**).

1 = Handshake successful with the Legacy 6 charger emulation profile and charging.
0 = Not charging with Legacy 6 charger emulation profile.

bit 4 **LG5:** Indicates that the portable device successfully performed a handshake with the Legacy 5 charger emulation profile and is charging. The high-speed switch will be controlled via the HSW_DCE bit (see **Section 10.4.5 "High-Speed Switch Configuration Register"**). The port power switch current limiting mode is determined by the Custom current limiting behavior settings (see **Section 10.14.2 "Custom Current Limiting Behavior Configuration Register"**).

1 = Handshake successful with the Legacy 5 charger emulation profile and charging.
0 = Not charging with Legacy 5 charger emulation profile.

bit 3 **LG4:** Indicates that the portable device successfully performed a handshake with the Legacy 4 charger emulation profile and is charging. The high-speed switch will be controlled via the HSW_DCE bit (see **Section 10.4.5 "High-Speed Switch Configuration Register"**). The port power switch current limiting mode is determined by the Custom current limiting behavior settings (see **Section 10.14.2 "Custom Current Limiting Behavior Configuration Register"**).

1 = Handshake successful with the Legacy 4 charger emulation profile and charging.
0 = Not charging with Legacy 4 charger emulation profile.

bit 2 **LG3:** Indicates that the portable device successfully performed a handshake with the Legacy 3 charger emulation profile and is charging. The high-speed switch will be controlled via the HSW_DCE bit (see **Section 10.4.5 "High-Speed Switch Configuration Register"**). The port power switch current limiting mode is determined by the Custom current limiting behavior settings (see **Section 10.14.2 "Custom Current Limiting Behavior Configuration Register"**).

1 = Handshake successful with the Legacy 3 charger emulation profile and charging.
0 = Not charging with Legacy 3 charger emulation profile.

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REGISTER 10-6: PROFILE STATUS 2 REGISTER (ADDRESS 13H) (CONTINUED)

bit 1 **LG2:** Indicates that the portable device successfully performed a handshake with the Legacy 2 charger emulation profile and is charging. The high-speed switch will be controlled via the HSW_DCE bit (see **Section 10.4.5 "High-Speed Switch Configuration Register"**). The port power switch current limiting mode is determined by the Custom current limiting behavior settings (see **Section 10.14.2 "Custom Current Limiting Behavior Configuration Register"**).
1 = Handshake successful with the Legacy 2 charger emulation profile and charging.
0 = Not charging with Legacy 2 charger emulation profile.

bit 0 **LG1:** Indicates that the portable device successfully performed a handshake with the Legacy 1 charger emulation profile and is charging. The high-speed switch will be controlled via the HSW_DCE bit (see **Section 10.4.5 "High-Speed Switch Configuration Register"**). The port power switch current limiting mode is determined by the Custom current limiting behavior settings (see **Section 10.14.2 "Custom Current Limiting Behavior Configuration Register"**).
1 = Handshake successful with the Legacy 1 charger emulation profile and charging.
0 = Not charging with Legacy 1 charger emulation profile.

10.3.3 PIN STATUS REGISTER

The Pin Status register reflects the current pin state of the external control pins as well as identifying the power state. These bits are linked to the X_SET bits (see **Section 10.4.3 "Switch Configuration Register"**).

REGISTER 10-7: PIN STATUS REGISTER (ADDRESS 14H)

U-x	R-0	R-0	R-0	R-0	R-0	R-0	R-0
—	PWR_EN_PIN	M2_PIN	M1_PIN	EM_EN_PIN	SEL_PIN	PWR_STATE<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented**

bit 6 **PWR_EN_PIN:** Reflects the PWR_EN control state. This bit is set and cleared automatically as the PWR_EN pin/PWR_ENS bit state changes.
1 = PWR_EN is Logic 1
0 = PWR_EN is Logic 0

bit 5 **M2_PIN:** Reflects the M2 pin state. This bit is set and cleared automatically as the M2 pin/M2_SET state changes.
1 = M2 is Logic 1
0 = M2 is Logic 0

bit 4 **M1_PIN:** Reflects the M1 pin state. This bit is set and cleared automatically as the M1 pin/M1_SET state changes.
1 = M1 is Logic 1
0 = M1 is Logic 0

bit 3 **EM_EN_PIN:** Reflects the EM_EN pin state. This bit is set and cleared automatically as the EM_EN pin/EM_EN_SET state changes.
1 = EM_EN is Logic 1
0 = EM_EN Logic 0

bit 2 **SEL_PIN:** Reflects the polarity settings determined by the SEL pin decode. This bit is set or cleared automatically upon device power-up as the SEL pin is decoded.
1 = The PWR_EN control is active high
0 = The PWR_EN control is active low

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REGISTER 10-7: PIN STATUS REGISTER (ADDRESS 14H) (CONTINUED)

bit 1-0 **PWR_STATE<1:0>:** Indicates the current power state. These bits are set and cleared automatically as the power state changes. (**Note 1**)
- 00 = Sleep
- 01 = Detect
- 10 = Active
- 11 = Error

Note 1: Accessing the SMBus/I^{2}C causes the UCS81003 to leave the Sleep state. As a result, the PWR_STATE<1:0> bits will never read as 00b.

10.4 Configuration Registers

Name	Bits	Address	Cof	Default
General Configuration	8	15h	R/W	01h
Emulation Configuration	8	16h	R/W	8Ch
Switch Configuration	8	17h	R/W	04h
Attach Detect Configuration	8	18h	R/W	46h
High-Speed Switch Configuration	8	25h	R/W	14h

The Configuration registers control basic device functionality.

10.4.1 GENERAL CONFIGURATION REGISTER

The contents of this register are retained in Sleep.

REGISTER 10-8: GENERAL CONFIGURATION REGISTER (ADDRESS 15H)

R/W-0	U-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
ALERT_MASK	—	ALERT_LINK	DSCHG	RTN_EN	RTN_RST	RATION_BEH<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **ALERT_MASK:** Disables the ALERT# pin from asserting in the case of an error.
- 1 = The ALERT# pin will not be asserted in the event of an error condition.
- 0 = The ALERT# pin will be asserted if an error condition or indicator event is detected.

bit 6 **Unimplemented**

bit 5 **ALERT_LINK:** Links the ALERT# pin to be asserted when the LOW_CUR and/or TREG bits are set.
- 1 = The ALERT# pin will be asserted if the LOW_CUR or TREG indicator bit is set.
- 0 = The ALERT# pin will not be asserted if the LOW_CUR or TREG indicator bit is set.

bit 4 **DSCHG:** Forces the V_{BUS} to be reset and discharged when the UCS81003 is in the Active state. Writing this bit to a logic '1' will cause the port power switch to be opened and the discharge circuitry to activate to discharge V_{BUS}. The port power switch will remain open while this bit is '1'. This bit is not self-clearing.

bit 3 **RTN_EN:** Ration Enable – enables charge rationing functionality and power monitoring.
- 1 = Charge rationing is enabled (see **Section 7.4 "Battery Full"**).
- 0 = Charge rationing is disabled. The Total Accumulated Charge registers will be cleared to 00_00h and current data will no longer be accumulated. If the Total Accumulated Charge registers have already reached the Charge Rationing Threshold (see **Section 10.6 "Charge Rationing Threshold Registers"**), the applied response will be removed as if the charge rationing had been reset. This will also clear the RATION status bit (if set).

REGISTER 10-8: GENERAL CONFIGURATION REGISTER (ADDRESS 15H) (CONTINUED)

bit 2 **RTN_RST:** Ration Reset – resets the charge rationing functionality. When this bit is set to '1', the Total Accumulated Charge registers are reset to 00_00h. In addition, when this bit is set, the RATION status bit will be cleared and, if there are no other errors or active indicators, the ALERT# pin will be released.

1 = EM_EN is Logic 1
0 = EM_EN is Logic 0

bit 1-0 **RATION_BEH<1:0>:** Controls the behavior when the power rationing threshold is reached as shown in Table 7-1.

00 = Report
01 = Report and Disconnect
10 = Disconnect and Go to Sleep
11 = Ignore

10.4.2 EMULATION CONFIGURATION REGISTER

The contents of this register are retained in Sleep.

REGISTER 10-9: EMULATION CONFIGURATION REGISTER (ADDRESS 16H)

R/W-1	U-x	U-x	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0
DIS_TO	—	—	EM_TO_DIS	EM_RETRY	EM_RESP	EM_RESET_TIME<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **DIS_TO:** Disable Timeout: Disables the Timeout and Idle Reset functionality (see **Section 11.2.1.6 "SMBus Timeout and Idle Reset"**).

1 = The Timeout and Idle Reset functionality is disabled. This is used for I^2C compliance.
0 = The Timeout and Idle Reset functionality is enabled.

bit 6-5 **Unimplemented**

bit 4 **EM_TO_DIS:** Emulation Timeout Disable - Disables the emulation circuitry timeout for all charger emulation profiles in the DCE Cycle. There is a separate bit to enable/disable the emulation timeout for the Custom Charger Emulation profile (Register 10-35); however, if the EM_TO_DIS bit is set, the emulation timeout will also be disabled for the Custom charger emulation profile. (**Note 1**)

1 = Emulation timeout is disabled during the DCE Cycle. The applied charger emulation profile will not exit as a result of an emulation timeout event. The I_{BUS} current will be checked continuously and if it exceeds the I_{BUS_CHG} threshold for any reason, the charger emulation profile will be accepted.
0 = Emulation timeout is enabled during the DCE Cycle. An individual charger emulation profile will be applied and maintained for the duration of the $t_{EM_TIMEOUT}$ value. When this timer expires, the UCS81003 will determine whether the charger emulation profile was successful and take appropriate action.

bit 3 **EM_RETRY:** Configures whether the DCE Cycle will reset and restart if it reaches the final profile without the portable device drawing charging current and accepting one of the profiles. This bit is only used if the UCS81003 is configured to emulate a dedicated charger.

1 = Once the DCE Cycle is completed, it will perform emulation reset and restart from the first enabled charger emulation profile in the DCE Cycle.
0 = Once the DCE Cycle is completed, it will not restart. The D_{POUT} and D_{MOUT} will be left as High Z pins and the port power switch will be closed. The Current Limiting mode is determined by the Custom Current Limiting Behavior settings (see **Section 10.14.2 "Custom Current Limiting Behavior Configuration Register"**).

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REGISTER 10-9: EMULATION CONFIGURATION REGISTER (ADDRESS 16H) (CONTINUED)

bit 2 **EM_RESP:** Leave Emulation Response - Enables the Dedicated Charger Emulation Cycle mode to hold the D_{POUT} and D_{MOUT} stimulus response after the UCS81003 has finished emulation using the Legacy, BC1.2 DCP, or Custom charger emulation profiles (**Note 2**).

1 = If a portable device begins drawing charging current while the UCS81003 is applying the BC1.2 DCP, Custom or any of the Legacy charger emulation profiles during the DCE Cycle, the last response applied will be kept in place until a Removal Detection event occurs, the internal temperature exceeds the T_{REG} value, or emulation is restarted. In the case of the BC1.2 DCP or Legacy 3 charger emulation profiles, this will be the short (R_{DCP_RES}). In the case of the Legacy 1, Legacy 2 or Legacy 4 - 7 profiles, this will be the D_{POUT} and D_{MOUT} pin voltages. If a portable device does not draw charging current, the DCE Cycle will behave normally.

0 = The dedicated emulation circuitry will behave normally. It will remove the short condition when the $t_{EM_TIMEOUT}$ timer has expired, regardless if the portable device has drawn charging current or not.

bit 1-0 **EM_RESET_TIME<1:0>:** Determines the length of the t_{EM_RESET} time (see **Section 9.8.1 "Emulation Reset"**) as shown below. The value selected does not include discharge time; however, this value plus discharge result in the actual reset time.

00 = 50 ms
01 = 75 ms
10 = 125 ms
11 = 175 ms

Note 1: If the EM_TO_DIS bit is set and the Legacy 2, Legacy 4 or Custom charger emulation profiles were accepted during the DCE cycle, a removal is not detected. To avoid this issue, re-enable the emulation timeout after applying any test profiles and charging with the 'final' profile.

2: If the HSW_DCE bit is set, the high-speed switch will be closed regardless of the status of the EM_RESP bit. Leaving the emulation response applied will not allow normal USB traffic. Therefore, prior to setting the HSW_DCE bit, this bit should be cleared.

10.4.3 SWITCH CONFIGURATION REGISTER

The contents of this register are retained in Sleep.

REGISTER 10-10: SWITCH CONFIGURATION REGISTER (ADDRESS 17H)

R/W-0	U-x	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0
PIN_IGN	—	EM_EN_SET	M2_SET	M1_SET	S0_SET	PWR_ENS	LATCHS
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **PIN_IGN:** Ignores the M1, M2, PWR_EN and EM_EN pin states when determining the Active mode selection and power state.

1 = The Active mode selection and power state will be set by the individual control bits and not by the M1, M2, PWR_EN and EM_EN pin states. These pin states are ignored.

0 = The Active mode selection and power state will be set by the OR'd combination of the M1, M2, PWR_EN and EM_EN pin states and the corresponding bit states.

bit 6 **Unimplemented**

bit 5 **EM_EN_SET:** In conjunction with other controls, determines the Active mode that is selected (see **Section 9.2 "Active Mode Selection"**) and power state (see Table 5-2). This bit is OR'd with the EM_EN pin.

bit 4 **M2_SET:** In conjunction with other controls, determines the Active mode that is selected (see **Section 9.2 "Active Mode Selection"**) and power state (see Table 5-2). This bit is OR'd with the M2 pin.

bit 3 **M1_SET:** In conjunction with other controls, determines the Active mode that is selected (see **Section 9.2 "Active Mode Selection"**) and power state (see Table 5-2). This bit is OR'd with the M1 pin.

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REGISTER 10-10: SWITCH CONFIGURATION REGISTER (ADDRESS 17H) (CONTINUED)

bit 2 **S0_SET:** In SMBus mode, enables the Attach and Removal Detection feature and affects the power state (see **Section 9.2 "Active Mode Selection"**).
1 = Detection is enabled. Also see Table 5-2.
0 = Detection is not enabled. Also see Table 5-2.

bit 1 **PWR_ENS:** Controls whether the port power switch may be turned on or not and affects the power state (see **Section 5.3.4 "PWR_EN Input"**). This bit is OR'd with the PWR_EN pin and the polarity of both are controlled by SEL pin decode. Thus, if the polarity is set to active high, either the PWR_EN pin or this bit must be '1' to enable the port power switch.

bit 0 **LATCHS:** In SMBus mode, controls the fault handling routine that is used in the case that an error is detected (see **Section 5.3.5 "Latch Input"**).
1 = The UCS81003 will latch its error conditions. In order for the device to return to normal Active state, the ERR bit must be cleared by the user.
0 = The UCS81003 will automatically retry when an error condition is detected.

10.4.4 ATTACH DETECTION CONFIGURATION RESISTER

The contents of this register are retained in Sleep.

REGISTER 10-11: ATTACH DETECTION CONFIGURATION REGISTER (ADDRESS 18H)

R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-0
RESERVED				DISCHG_TIME_SEL<1:0>		ATT_TH<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **RESERVED:** Do not change.

bit 3-2 **DISCHG_TIME_SEL<1:0>:** Sets the $t_{DISCHARGE}$ time as follows:
00 = 100 ms
01 = 200 ms
10 = 300 ms
11 = 400 ms

bit 1-0 **ATT_TH<1:0>:** Determines the Attach Detection threshold (I_{DET_QUAL}) and Removal Detection thresholds ($I_{REM_QUAL_DET}$ and $I_{REM_QUAL_ACT}$) as shown below. (**Note 1**)
00 = 200 µA Attach, 100 µA Removal Threshold
01 = 400 µA Attach, 300 µA Removal Threshold
10 = 800 µA Attach, 700 µA Removal Threshold
11 = 1000 µA Attach, 900 µA Removal Threshold

Note 1: The removal threshold is different when operating in the Active power state versus when operating in the Detect power state.

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10.4.5 HIGH-SPEED SWITCH CONFIGURATION REGISTER

The contents of this register are retained in Sleep.

REGISTER 10-12: HIGH-SPEED SWITCH CONFIGURATION REGISTER (ADDRESS 25H)

U-x	U-x	U-x	R/W-1	R/W-0	R/W-1	R/W-0	R/W-0
—	—	—	RESERVED	HSW_CUST	HSW_CDP	HSW_DET	HSW_DCE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **Unimplemented**

bit 4 **RESERVED:** Do not change.

bit 3 **HSW_CUST:** Enables the USB high-speed data switch to be active during the Custom handshake. This control is checked at the beginning of charger emulation. Therefore, changing this control during emulation will have no immediate effect. Upon restarting charger emulation (as a result of the EM_RETRY bit being set, a Removal Detection event, or change of emulation controls), the high-speed switch will close.
- 1 = The USB high-speed data switch is enabled while the Custom charger emulation profile is applied. Also, if the Custom charger emulation profile is accepted during the Dedicated Charger Emulation Cycle, the high-speed switch will stay closed.
- 0 = The USB high-speed data switch is disabled while the Custom charger emulation profile is applied.

bit 2 **HSW_CDP:** Enables the USB high-speed data switch to be active during the CDP handshake. This control is checked at the beginning of charger emulation. Therefore, changing this control during emulation will have no immediate effect. Upon restarting charger emulation (as a result of a Removal Detection event or change of emulation controls), the high-speed switch will close.
- 1 = The USB high-speed data switch is enabled during the CDP handshake.
- 0 = The USB high-speed data switch is disabled during the CDP handshake.

bit 1 **HSW_DET:** Enables the USB high-speed data switch to be active during the Detect power state. If the S0 control is set to '0', this bit is ignored.
- 1 = The USB high-speed data switch will be closed during the Detect power state.
- 0 = The USB high-speed data switch is open during the Detect power state.

bit 0 **HSW_DCE:** Enables the USB high-speed data switch after the DCP charger emulation profile or one of the Legacy charger emulation profiles was accepted during the DCE Cycle and the portable device is charging. This bit is ignored if the UCS81003 is not in the Active state. This bit will not cause the high-speed switch to be closed during emulation when the DCP and Legacy profiles are applied, only after the DCP or a Legacy charger emulation profile has been accepted.
- 1 = The USB high-speed data switch will be closed.
- 0 = The USB high-speed data switch will be open.

10.5 Current Limit Register

Name	Bits	Address	Cof	Default
Current Limit	8	19h	R/W	00h

The Current Limit register controls the ILIM used by the port power switch. The default setting is based on the resistor on the COMM_SEL/I_{LIM} pin and this value cannot be changed to be higher than hardware set value.

The contents of this register are retained in Sleep.

REGISTER 10-13: CURRENT LIMIT REGISTER (ADDRESS 19H)

U-x	U-x	U-x	U-x	U-x	R/W-0	R/W-0	R/W-0
—	—	—	—	—	ILIM_SW<2:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-3 **Unimplemented**

bit 2-0 **ILIM_SW<2:0>:** Sets the I_{LIM} value as follows:

```
000 = 0.57A
001 = 1.00A
010 = 1.13A
011 = 1.35A
100 = 1.68A
101 = 2.05A
110 = 2.28A
111 = 2.85A (3.0A maximum)
```

Note 1: Unless otherwise indicated, the values specified above are the typical I_{LIM} in the Table 1-2.

10.6 Charge Rationing Threshold Registers

Name	Bits	Address	Cof	Default
Charge Rationing Threshold High Byte	8	1Ah	R/W	FFh
Charge Rationing Threshold Low Byte	8	1Bh	R/W	FFh

The Charge Rationing Threshold registers set the maximum allowed charge that will be delivered to a portable device. Every time the Total Accumulated Charge registers are updated, the value is checked against this limit. If the value meets or exceeds this limit, the RATION bit is set (see **Section 10.4.1 "General Configuration Register"**) and action taken according to the RATION_BEH<1:0> bits (see **Section 10.4.1 "General Configuration Register"**).

The units are in mAh, with a range from 0 to ~218429.

The contents of this register are retained in Sleep.

REGISTER 10-14: CHARGE RATIONING THRESHOLD (ADDRESS 1AH - 1BH)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
CHTHR<15>	CHTHR<14>	CHTHR<13>	CHTHR<12>	CHTHR<11>	CHTHR<10>	CHTHR<9>	CHTHR<8>
bit 15							bit 8
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
CHTHR<7>	CHTHR<6>	CHTHR<5>	CHTHR<4>	CHTHR<3>	CHTHR<2>	CHTHR<1>	CHTHR<0>
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **CHTHR<15:1>: Charge Rationing Threshold**
LSB = 3.333 mAh

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10.7 Auto-Recovery Configuration Register

Name	Bits	Address	Cof	Default
Auto-Recovery Configuration	8	1Ch	R/W	2Ah

The contents of this register are retained in Sleep.

The Auto-Recovery Configuration register sets the parameters used when the Auto-Recovery fault handling algorithm is invoked (see **Section 7.5.1 "Auto-Recovery Fault Handling"**).

Once the Auto-Recovery fault handling algorithm has checked the overtemperature and back-drive conditions, it will set the I_{LIM} value to I_{TEST} and then turn on the port power switch and start the t_{RST} timer. If, after the timer has expired, the V_{BUS} voltage is less than V_{TEST}, then it is assumed that a short-circuit condition is present and the Error state is reset.

REGISTER 10-15: AUTO-RECOVERY CONFIGURATION REGISTER (ADDRESS 1CH)

U-x	R/W-0	R/W-1	R/W-0	R/W-1	R/W-0	R/W-1	R/W-0
—	TCYCLE<2:0>			TRST_SW<1:0>		VTST_SW<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented**

bit 6-4 **TCYCLE<2:0>:** Defines the delay (t_{CYCLE}) after the Error state is entered before the Auto-recovery fault handling algorithm is started as shown below.

000 = 15 ms
001 = 20 ms
010 = 25 ms
011 = 30 ms
101 = 40 ms
110 = 45 ms
111 = 50 ms

bit 3-2 **TRST_SW<1:0>:** Sets the t_{RST} time as shown as shown below.

00 = 10 ms
01 = 15 ms
10 = 20 ms
11 = 25 ms

bit 1-0 **VTST_SW<1:0>:** Sets the V_{TEST} value as shown below.

00 = 250 mV
01 = 500 mV
10 = 750 mV
11 = 1000 mV

10.8 IBUS_CHG Configuration Register

Name	Bits	Address	Cof	Default
IBUS_CHG Configuration	8	1Eh	R/W	0Fh

The IBUS_CHG Configuration register sets the I_{BUS_CHG} current value. If current greater than I_{BUS_CHG} is detected flowing out of V_{BUS}, emulation is successful. The bit weights are in mA, and the range is from 11.72 mA to 175.8 mA.

The contents of this register are not retained in Sleep.

REGISTER 10-16: IBUS_CHG CONFIGURATION REGISTER (ADDRESS 1EH)

U-x	U-x	U-x	U-x	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	—	ICHG<3>	ICHG<2>	ICHG<1>	ICHG<0>
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **Unimplemented**

bit 3-0 **ICHG<3:0>**
1 LSB = 11.72 mA

10.9 TDET_CHARGE Configuration Register

Name	Bits	Address	Cof	Default
TDET_CHARGE Configuration	8	1Fh	R/W	03h

The TDET_CHARGE Configuration register controls the t_{DC_TEMP} and t_{DET_CHARGE} timing. The t_{DC_TEMP} timer is started whenever the temperature exceeds T_{REG}. This timer is meant to give the system time to cool at the lower I_{LIM} setting before changing I_{LIM} again. The t_{DET_CHARGE} timer is started whenever the V_{BUS} voltage is discharged and the bypass switch is re-activated. This timer is meant to be a delay to allow the V_{BUS} capacitor to charge before detecting an Attach Detection event.

If t_{DET_CHARGE} time is increased greater than 800 ms, larger bus capacitors can be accommodated; however, with a portable device present and PWR_EN disabled, a Removal Detection event and then another Attach Detection event will occur.

The contents of this register are retained in Sleep.

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REGISTER 10-17: TDET_CHARGE CONFIGURATION REGISTER (ADDRESS 1FH)

U-x	U-x	U-x	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1
—	—	—	DC_TEMP_SET<1:0>		DET_CHARGE_SET<2:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **Unimplemented**

bit 4-3 **DC_TEMP_SET<1:0>:** Determines the t_{DC_TEMP} time as shown below.
00 = 200 ms
01 = 400 ms
10 = 800 ms
11 = 1600 ms

bit 2-0 **DET_CHARGE_SET<2:0>:** Determines the t_{DET_CHARGE} time as shown below.
000 = 200 ms
001 = 400 ms
010 = 600 ms
011 = 800 ms
100 = 1000 ms
101 = 1200 ms
110 = 1400 ms
111 = 2000 ms

10.10 Preloaded Emulation Enable Registers

Name	Bits	Address	Cof	Default
BCS Emulation Enable	8	20h	R/W	16h
Legacy Emulation Enable	8	21h	R/W	00h

The Preloaded Emulation Enable registers enable the charger emulation profiles used by the emulation circuitry.

The contents of these registers are retained in Sleep.

REGISTER 10-18: BCS EMULATION ENABLE REGISTER (ADDRESS 20H)

U-x	U-x	U-x	R/W-1	U-x	R/W-1	R/W-1	R/W-0
—	—	—	DCP_EM_DIS	—	RESERVED		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **Unimplemented**

bit 4 **DCP_EM_DIS:** Disables the DCP charger emulation profile in the DCE Cycle. This bit is ignored if the M1, M2 and EM_EN control settings have selected DCP mode (see Table 9-1).
1 = The BC1.2 DCP charger emulation profile is not enabled during the DCE Cycle.
0 = The BC1.2 DCP charger emulation profile is enabled during the Dedicated Charger Emulation Cycle.

bit 3 **Unimplemented**

bit 2-0 **RESERVED:** Do not change.

REGISTER 10-19: LEGACY EMULATION ENABLE REGISTER (ADDRESS 21H)

U-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	L7EM_DIS	L6EM_DIS	L5EM_DIS	L4EM_DIS	L3EM_DIS	L2EM_DIS	L1EM_DIS
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented**

bit 6 **L7EM_DIS:** Disables the Legacy 7 charger emulation profile.
1 = The Legacy 7 charger emulation profile is not enabled.
0 = The Legacy 7 charger emulation profile is enabled.

bit 5 **L6EM_DIS:** Disables the Legacy 6 charger emulation profile.
1 = The Legacy 6 charger emulation profile is not enabled.
0 = The Legacy 6 charger emulation profile is enabled.

bit 4 **L5EM_DIS:** Disables the Legacy 5 charger emulation profile.
1 = The Legacy 5 charger emulation profile is not enabled.
0 = The Legacy 5 charger emulation profile is enabled.

bit 3 **L4EM_DIS:** Disables the Legacy 4 charger emulation profile.
1 = The Legacy 4 charger emulation profile is not enabled.
0 = The Legacy 4 charger emulation profile is enabled.

bit 2 **L3EM_DIS:** Disables the Legacy 3 charger emulation profile.
1 = The Legacy 3 charger emulation profile is not enabled.
0 = The Legacy 3 charger emulation profile is enabled.

bit 1 **L2EM_DIS:** Disables the Legacy 2 charger emulation profile.
1 = The Legacy 2 charger emulation profile is not enabled.
0 = The Legacy 2 charger emulation profile is enabled.

bit 0 **L1EM_DIS:** Disables the Legacy 1 charger emulation profile.
1 = The Legacy 1 charger emulation profile is not enabled.
0 = The Legacy 1 charger emulation profile is enabled.

10.11 Preloaded Emulation Timeout Configuration Registers

Name	Bits	Address	Cof	Default
BCS Emulation Timeout Config	8	22h	R/W	10h
Legacy Emulation Timeout Config 1	8	23h	R/W	6Ch
Legacy Emulation Timeout Config 2	8	24h	R/W	01h

The Preloaded Emulation Timeout Configuration registers control the $t_{EM_TIMEOUT}$ setting that is applied whenever the indicated preloaded charger emulation profile is applied during the DCE Cycle. These settings are not used if the EM_TO_DIS bit is set.

The contents of this registers are retained in Sleep.

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REGISTER 10-20: BCS EMULATION TIMEOUT CONFIG REGISTER (ADDRESS 22H)

U-x	U-x	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
—	—	DCP_EM_TO<1:0>		RESERVED			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented**

bit 5-4 **DCP_EM_TO<1:0>:** Defines the $t_{EM_TIMEOUT}$ setting, as shown below. Is applied when the BC1.2 DCP charger emulation profile is used during the DCE Cycle.

00 = 0.8s
01 = 1.6s
10 = 6.4s
00 = 12.8s

bit 3-0 **RESERVED:** Do not change.

REGISTER 10-21: LEGACY EMULATION TIMEOUT CONFIG 1 REGISTER (ADDRESS 23H)

R/W-0	R/W-1	R/W-1	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0
L1EM_TO<1:0>		L2EM_TO<1:0>		L3EM_TO<1:0>		L4EM_TO<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **L1EM_TO<1:0>:** Defines the $t_{EM_TIMEOUT}$ setting, as shown below. Is applied when the Legacy 1 charger emulation profile is used during the DCE Cycle.

00 = 0.8s
01 = 1.6s
10 = 6.4s
11 = 12.8s

bit 5-4 **L2EM_TO<1:0>:** Defines the $t_{EM_TIMEOUT}$ setting, as shown below. Is applied when the Legacy 2 charger emulation profile is used during the DCE Cycle.

00 = 0.8s
01 = 1.6s
10 = 6.4s
11 = 12.8s

bit 3-2 **L3EM_TO<1:0>:** Defines the $t_{EM_TIMEOUT}$ setting, as shown below. Is applied when the Legacy 3 charger emulation profile is used during the DCE Cycle.

00 = 0.8s
01 = 1.6s
10 = 6.4s
11 = 12.8s

bit 1-0 **L4EM_TO<1:0>:** Defines the $t_{EM_TIMEOUT}$ setting, as shown below. Is applied when the Legacy 4 charger emulation profile is used during the DCE Cycle.

00 = 0.8s
01 = 1.6s
10 = 6.4s
11 = 12.8s

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REGISTER 10-22: LEGACY EMULATION TIMEOUT CONFIG 2 REGISTER (ADDRESS 24H)

U-x	U-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
—	—	L5EM_TO<1:0>		L6EM_TO<1:0>		L7EM_TO<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented**

bit 5-4 **L5EM_TO<1:0>:** Defines the $t_{EM_TIMEOUT}$ setting, as shown below. Is applied when the Legacy 5 charger emulation profile is used during the DCE Cycle.
00 = 0.8s
01 = 1.6s
10 = 6.4s
11 = 12.8s

bit 3-2 **L6EM_TOV<1:0>:** Defines the $t_{EM_TIMEOUT}$ setting, as shown below. Is applied when the Legacy 6 charger emulation profile is used during the DCE Cycle.
00 = 0.8s
01 = 1.6s
10 = 6.4s
11 = 12.8s

bit 1-0 **L7EM_TO<1:0>:** Defines the $t_{EM_TIMEOUT}$ setting, as shown below. Is applied when the Legacy 7 charger emulation profile is used during the DCE Cycle.
00 = 0.8s
01 = 1.6s
10 = 6.4s
11 = 12.8s

10.12 Preloaded Emulation Configuration Registers

Name	Bits	Address	Cof	Default
Applied Charger Emulation	8	30h	R	00h
Preloaded Emulation Stimulus 1 - Config 1	8	31h	R	00h
Preloaded Emulation Stimulus 1 - Config 2	8	32h	R	26h
Preloaded Emulation Stimulus 1 - Config 3	8	33h	R	00h
Preloaded Emulation Stimulus 1 - Config 4	8	34h	R	02h
Preloaded Emulation Stimulus 2 - Config 1	8	35h	R	00h
Preloaded Emulation Stimulus 2 - Config 2	8	36h	R	09h
Preloaded Emulation Stimulus 2 - Config 3	8	37h	R	00h
Preloaded Emulation Stimulus 2 - Config 4	8	38h	R	04h
Preloaded Emulation Stimulus 3 - Config 1	8	39h	R	00h
Preloaded Emulation Stimulus 3 - Config 2	8	3Ah	R	00h
Preloaded Emulation Stimulus 3 - Config 3	8	3Bh	R	00h

The Preloaded Emulation Configuration registers store the settings loaded from internal memory as required for the preloaded charger emulation profile that is actively being applied. These registers are read only.

The Legacy charger emulation profiles, the BC1.2 SDP, and the BC1.2 DCP charger emulation profile do not use the Stimulus 3 Configuration registers (39h - 3Bh). Whenever these charger emulation profiles are applied, registers 39h - 3Bh will not be updated and their contents should be ignored.

Whenever a Legacy charger emulation profile is applied within the DCE Cycle, these controls will not be updated and should be ignored. These settings are only used by the BC1.2 CDP and BC1.2 DCP charger emulation profiles.

The contents of registers 31h, 35 and 39h are not retained in Sleep. They are updated as needed.

The contents of registers 32h, 33h, 34h, 36h, 37h, 38h, 3Ah, 3Bh, 40h are retained in Sleep.

10.12.1 APPLIED CHARGER EMULATION REGISTER

The contents of this register are not retained in Sleep. The contents are updated as the charger emulation profile being applied changes.

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REGISTER 10-23: APPLIED CHARGER EMULATION REGISTER (ADDRESS 30H)

U-x	U-x	U-x	U-x	R-0	R-0	R-0	R-0
—	—	—	—	PRE_EM_SEL<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **Unimplemented**

bit 3-0 **PRE_EM_SEL<3:0>:** Indicates which of the charger emulation profiles is being actively applied, as shown below.

0000 = Data Pass-through or BC1.2 SDP
0001 = BC1.2 CDP
0010 = BC1.2 DCP
0011 = Legacy 1
0100 = Legacy 2
0101 = Legacy 3
0110 = Legacy 4
0111 = Legacy 5
1000 = Legacy 6
1001 = Legacy 7
1010 = Custom Profile
All others = Not used

REGISTER 10-24: PRELOADED EMULATION STIMULUS 1 CONFIGURATION 1 REGISTER (ADDRESS 31H)

U-x	R-0	R-0	R-0	R-0	R-0	R-0	R-0
—	S1_TD_TYPE	S1_TD<2:0>			STIM1<2:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented**

bit 6 **S1_TD_TYPE:** Determines the behavior of the stimulus timer.

1 = The stimulus timer controls how long the response is applied after the stimulus is detected. The response is applied immediately and held for the duration of the timer then removed (if the stimulus has been removed).
0 = The stimulus timer is a delay from when the stimulus is detected until the response is performed.

bit 5-3 **S1_TD<2:0>:** Determines the stimulus 1 t_{STIM_DEL} value as shown below.

000 = 0 ms
001 = 1 ms
010 = 5 ms
011 = 10 ms
100 = 20 ms
101 = 40 ms
110 = 80 ms
111 =100 ms

REGISTER 10-24: PRELOADED EMULATION STIMULUS 1 CONFIGURATION 1 REGISTER (ADDRESS 31H) (CONTINUED)

bit 2-0 **STIM1<2:0>:** Determines the Stimulus 1 that is used as shown below. Note that the lower threshold for the window comparator option is fixed at 400 mV and only applies to the D_{POUT} pin. This setting cannot be used for the D_{MOUT} port.

000 = V_{BUS} voltage ready to be applied before port power switch is closed. Next stimulus will not wait for this to be removed.
001 = D_{POUT} voltage is higher than the threshold (S1_TH).
010 = Window comparator. D_{POUT} voltage is lower than the threshold (S1_TH) and D_{POUT} voltage higher than the fixed threshold.
011 = D_{MOUT} voltage is higher than the threshold (S1_TH).
100 = Do not use.
101 = Do not use.
110 = D_{POUT} voltage is higher than the threshold (S1_TH).
111 = V_{BUS} voltage is present after port power switch is closed. Next stimulus will not wait for this to be removed.

REGISTER 10-25: PRELOADED EMULATION STIMULUS 1 CONFIGURATION 2 REGISTER (ADDRESS 32H)

R-0	R-0	R-1	R-0	R-0	R-1	R-1	R-0
S1_R1MAG<3:0>				S1_R1<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **S1_R1MAG<3:0>:**Determines the magnitude of the response to the stimulus. The bit decode changes meaning based on which response was selected. Data written to any field that is identified as 'do not use' will not be accepted. The data will not be updated and the settings will remain set at the previous value.

- **For S1_R1 settings 0000 - 0011**, the response is a voltage applied on D_{POUT}/D_{MOUT} pins. The S1_R1MAG bits specify the voltage relative to ground:

0000 = Pull Down	0110 = 600 mV	1100 = 1800 mV
0001 = 400 mV	0111 = 700 mV	1101 = 2000 mV
0010 = 400 mV	1000 = 800 mV	1110 = 2200 mV
0011 = 400 mV	1001 = 900 mV	1111 = Do not use
0100 = 400 mV	1010 = 1400 mV	
0101 = 500 mV	1011 = 1600 mV	

- **For S1_R1 settings 0100, 0111, 1101 - 1111**, the response is a resistor connected on D_{POUT}/D_{MOUT} to GND or V_{BUS}. The S1_R1MAG bits specify the resistor value:

0000 = 1.8 kΩ	0110 = 40 kΩ	1100 = 100 kΩ
0001 = 10 kΩ	0111 = 43 kΩ	1101 = 120 kΩ
0010 = 15 kΩ	1000 = 50 kΩ	1110 = 150 kΩ
0011 = 20 kΩ	1001 = 60 kΩ	1111 = Do not use
0100 = 25 kΩ	1010 = 75 kΩ	
0101 = 30 kΩ	1011 = 80 kΩ	

- **For S1_R1 settings 0110, 1001, 1100**, the response is a voltage divider applied from V_{BUS} to GND with "center" at D_{POUT}/D_{MOUT}. The S1_R1MAG bits specify the minimum resistance of the voltage divider (Sum of R1 + R2):

0000 = 93 kΩ	0110 = 200 kΩ	1100 = 200 kΩ
0001 = 100 kΩ	0111 = 200 kΩ	1101 = 200 kΩ
0010 = 125 kΩ	1000 = 93 kΩ	1110 = 200 kΩ
0011 = 150 kΩ	1001 = 100 kΩ	1111 = Do not use
0100 = 200 kΩ	1010 = 125 kΩ	
0101 = 200 kΩ	1011 = 150 kΩ	

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REGISTER 10-25: PRELOADED EMULATION STIMULUS 1 CONFIGURATION 2 REGISTER (ADDRESS 32H) (CONTINUED)

bit 3-0 **S1_R1<3:0>:** Defines the stimulus response as shown below:.

- 0000 = Remove previous response on D_{POUT} and D_{MOUT}
- 0001 = Apply voltage on D_{POUT} (Note 1).
- 0010 = Apply voltage on D_{MOUT} (Note 2).
- 0011 = Apply voltage on D_{POUT} and D_{MOUT}.
- 0100 = Connect resistor from D_{POUT} to GND (Note 1).
- 0101 = Do not use.
- 0110 = Connect voltage divider from V_{BUS} to GND with “center” at D_{POUT} (Note 1).
- 0111 = Connect resistor form D_{MOUT} to GND (Note 2).
- 1000 = Do not use.
- 1001 = Connect voltage divider from V_{BUS} to GND with “center” at D_{MOUT} (Note 2).
- 1010 = Connect ≤ 200Ω resistor from D_{POUT} to D_{MOUT}.
- 1011 = Do not use.
- 1100 = Connect voltage divider from V_{BUS} to GND with ‘center’ at D_{POUT} and D_{MOUT}.
- 1101 = Connect resistor from D_{POUT} to GND and D_{MOUT} to GND.
- 1110 = If STIM1 = 000, the 15 kΩ pull down resistors applied to D_{POUT} and D_{MOUT} during emulation reset are not removed. If STIM1 = 111, the 15 kΩ pull down resistors applied to D_{POUT} and D_{MOUT} during emulation reset are removed. For all other STIM1 settings, whatever was applied is not changed.
- 1111 = Same as 1110 case above.

Note 1: If STIM1<2:0> = 000b and no other response was applied to the D_{POUT} pin, the 15 kΩ pull-down resistor applied to the D_{POUT} pin during emulation reset is not removed. Otherwise, the previous response is left on the D_{POUT} pin (if applicable) or the 15 kΩ pull-down resistor is removed.

2: If STIM1<2:0> = 000b and no other response was applied to the D_{MOUT} pin, the 15 kΩ pull-down resistor applied to the D_{MOUT} pin during emulation reset is not removed. Otherwise, the previous response is left on the D_{MOUT} pin (if applicable) or the 15 kΩ pull-down resistor is removed.

REGISTER 10-26: PRELOADED EMULATION STIMULUS 1 CONFIGURATION 3 REGISTER (ADDRESS 33H)(Note 1)

U-x	U-x	R-0	R-0	R-0	R-0	R-0	R-0
—	—	S1_PUPD<1:0>		S1_TH<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented**

bit 5-4 **S1_PUPD<1:0>:** Determines the magnitude of the pull-down current applied on the D_{POUT} and D_{MOUT} pins when the stimulus response is to apply a voltage and the voltage magnitude is set at pull-down (0000b). The bit decode is given below.

- 00 = 10 µA
- 01 = 50 µA
- 10 = 100 µA
- 11 = 150 µA

REGISTER 10-26: PRELOADED EMULATION STIMULUS 1 CONFIGURATION 3 REGISTER (ADDRESS 33H)(Note 1) (CONTINUED)

bit 3-0 **S1_TH<3:0>:** Defines the threshold value, as shown below for the specified stimulus. If the stimulus is V_{BUS} voltage is ready to be applied or applied (i.e., STIM1<2:0> = 000b or 111b), the threshold value is ignored.

0000 = 400 mV
0001 = 400 mV
0010 = 400 mV
0011 = 300 mV
0100 = 400 mV
0101 = 500 mV
0110 = 600 mV
0111 = 700 mV
1000 = 800 mV
1001 = 900 mV
1010 = 1400 mV
1011 = 1600 mV
1100 = 1800 mV
1101 = 2000 mV
1110 = 2200 mV
1111 = Do not use.

Note 1: The Legacy charger emulation profiles do not use these settings. Whenever a Legacy charger emulation profile is applied within the DCE Cycle, these controls will not be updated and should be ignored. These settings are only used by the BC1.2 CDP and DCP charger emulation profiles.

REGISTER 10-27: PRELOADED EMULATION STIMULUS 1 CONFIGURATION 4 REGISTER (ADDRESS 34H)(Note 1)

U-x	U-x	U-x	U-x	U-x	R-0	R-1	R-0
—	—	—	—	—	S1_RATIO<2:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-3 **Unimplemented**

bit 2-0 **S1_RATIO<2:0>:** Determines the voltage divider ratio, as shown below, when the stimulus response is set to connect a voltage divider (i.e., S1_R1<3:0> = 0110b, 1001b, or 1100b).

000 = 0.25
001 = 0.33
010 = 0.4
011 = 0.5
100 = 0.54
101 = 0.6
110 = 0.66
111 = Do not use.

Note 1: The BC1.2 DCP and CDP charger emulation profiles do not use this control. Whenever the BC1.2 CDP or DCP charger emulation profile is applied, these controls will not be updated and should be ignored. These settings are only used by the Legacy charger emulation profiles.

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REGISTER 10-28: PRELOADED EMULATION STIMULUS 2 CONFIGURATION 1 REGISTER (ADDRESS 35H)

U-x	R-0	R-0	R-0	R-0	R-0	R-0	R-0
—	S2_TD_TYPE	S2_TD<2:0>			STIM2<2:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented**

bit 6 **S2_TD_TYPE:** Determines the behavior of the stimulus timer.

1 = The stimulus timer controls how long the response is applied after the stimulus is detected. The response is applied immediately and held for the duration of the timer, then removed (if the stimulus has been removed).

0 = The stimulus timer is a delay from when the stimulus is detected until the response is performed.

bit 5-3 **S2_TD<2:0>:** Determines the Stimulus 2 t_{STIM_DEL} value as shown below:

000 = 0 ms
001 = 1 ms
010 = 5 ms
011 = 10 ms
100 = 20 ms
101 = 40 ms
110 = 80 ms
111 = 100 ms

bit 2-0 **STIM2<2:0>:** Determines the Stimulus 2 that is used as shown below. Note that the lower threshold for the window comparator option is fixed at 400 mV and only applies to the D_{POUT} pin. This setting cannot be used for the DM_{OUT} port.

000 = V_{BUS} voltage ready to be applied before port power switch is closed. Next stimulus will not wait for this to be removed.
001 = D_{POUT} voltage is greater than the threshold (S2_TH).
010 = Window comparator. D_{POUT} voltage is lower than the threshold (S2_TH) and D_{POUT} voltage greater than the fixed threshold.
011 = D_{MOUT} voltage is greater than the threshold (S2_TH).
100 = Do not use.
101 = Do not use.
110 = D_{POUT} voltage is greater than the threshold (S2_TH).
111 = Voltage is present after the port power switch is closed. Next stimulus will not wait for this to be removed.

REGISTER 10-29: PRELOADED EMULATION STIMULUS 2 CONFIGURATION 2 REGISTER (ADDRESS 36H)

R-0	R-0	R-0	R-0	R-1	R-0	R-0	R-1
S2_R2MAG<3:0>				S2_R2<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **S2_R2MAG<3:0>:** Determines the magnitude of the response to the stimulus. The bit decode changes meaning based on which response was selected. Data written to any field that is identified as "Do not use" will not be accepted. The data will not be updated and the settings will remain set at the previous value.

- **For S2_R2 settings 0000 - 0011**, the response is a voltage applied on D_{POUT}/D_{MOUT} pins. The S2_R2MAG bits specify the voltage relative to ground:

0000 = Pull Down	0110 = 600 mV	1100 = 1800 mV
0001 = 400 mV	0111 = 700 mV	1101 = 2000 mV
0010 = 400 mV	1000 = 800 mV	1110 = 2200 mV
0011 = 400 mV	1001 = 900 mV	1111 = Do not use
0100 = 400 mV	1010 = 1400 mV	
0101 = 500 mV	1011 = 1600 mV	

- **For S2_R2 settings 0100, 0111, 1101 - 1111**, the response is a resistor connected on D_{POUT}/D_{MOUT} to GND or V_{BUS}. The S2_R2MAG bits specify the resistor value:

0000 = 1.8 kΩ	0110 = 40 kΩ	1100 = 100 kΩ
0001 = 10 kΩ	0111 = 43 kΩ	1101 = 120 kΩ
0010 = 15 kΩ	1000 = 50 kΩ	1110 = 150 kΩ
0011 = 20 kΩ	1001 = 60 kΩ	1111 = Do not use
0100 = 25 kΩ	1010 = 75 kΩ	
0101 = 30 kΩ	1011 = 80 kΩ	

- **For S2_R2 settings 0110, 1001, 1100**, the response is a voltage divider applied from V_{BUS} to GND with "center" at D_{POUT}/D_{MOUT}. The S2_R2MAG bits specify the minimum resistance of the voltage divider (Sum of R1 + R2):

0000 = 93 kΩ	0110 = 200 kΩ	1100 = 200 kΩ
0001 = 100 kΩ	0111 = 200 kΩ	1101 = 200 kΩ
0010 = 125 kΩ	1000 = 93 kΩ	1110 = 200 kΩ
0011 = 150 kΩ	1001 = 100 kΩ	1111 = Do not use
0100 = 200 kΩ	1010 = 125 kΩ	
0101 = 200 kΩ	1011 = 150 kΩ	

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REGISTER 10-29: PRELOADED EMULATION STIMULUS 2 CONFIGURATION 2 REGISTER (ADDRESS 36H) (CONTINUED)

bit 3-0 **S2_R2<3:0>:** Defines the stimulus response as shown below:

0000 = Remove previous response on D_{POUT} and D_{MOUT}
0001 = Apply voltage on D_{POUT} (Note 1).
0010 = Apply voltage on D_{MOUT} (Note 2).
0011 = Apply voltage on D_{POUT} and D_{MOUT}.
0100 = Connect resistor from D_{POUT} to GND (Note 1).
0101 = Do not use.
0110 = Connect voltage divider from V_{BUS} to GND with "center" at D_{POUT} (Note 1).
0111 = Connect resistor form D_{MOUT} to GND (Note 2).
1000 = Do not use.
1001 = Connect voltage divider from V_{BUS} to GND with "center" at D_{MOUT} (Note 2).
1010 = Connect ≤ 200Ω resistor from D_{POUT} to D_{MOUT}.
1011 = Do not use.
1100 = Connect voltage divider from V_{BUS} to GND with 'center' at D_{POUT} and D_{MOUT}.
1101 = Connect resistor from D_{POUT} to GND and D_{MOUT} to GND.
1110 = If STIM2 = 000, the 15 kΩ pull down resistors applied to D_{POUT} and D_{MOUT} during emulation reset are not removed. If STIM2 = 111, the 15 kΩ pull down resistors applied to D_{POUT} and D_{MOUT} during emulation reset are removed. For all other STIM2 settings, whatever was applied is not changed.
1111 = Same as 1110 case above.

Note 1: If STIM2<2:0> = 000b and no other response was applied to the D_{POUT} pin, the 15 kΩ pull-down resistor applied to the D_{POUT} pin during emulation reset is not removed. Otherwise, the previous response is left on the D_{POUT} pin (if applicable) or the 15 kΩ pull-down resistor is removed.

2: If STIM2<2:0> = 000b and no other response was applied to the D_{MOUT} pin, the 15 kΩ pull-down resistor applied to the D_{MOUT} pin during emulation reset is not removed. Otherwise, the previous response is left on the D_{MOUT} pin (if applicable) or the 15 kΩ pull-down resistor is removed.

REGISTER 10-30: PRELOADED EMULATION STIMULUS 2 CONFIGURATION 3 REGISTER (ADDRESS 37H)(Note 1)

U-x	U-x	R-0	R-0	R-0	R-0	R-0	R-0
—	—	S2_PUPD<1:0>		S2_TH<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented**

bit 5-4 **S2_PUPD<1:0>:** Determines the magnitude of the pull-down current applied on the D_{POUT} and D_{MOUT} pins when the stimulus response is to apply a voltage and the voltage magnitude is set at pull-down (0000b). The bit decode is as follows:

00 = 10 µA
01 = 50 µA
10 = 100 µA
11 = 150 µA

REGISTER 10-30: PRELOADED EMULATION STIMULUS 2 CONFIGURATION 3 REGISTER (ADDRESS 37H)(Note 1) (CONTINUED)

bit 3-0 **S2_TH<3:0>:** Defines the threshold value, as shown below for the specified stimulus. If the stimulus V_{BUS} voltage is ready to be applied or applied (i.e., STIM2<2:0> = 000b or 111b), the threshold value is ignored.
0000 = 400 mV
0001 = 400 mV
0010 = 400 mV
0011 = 300 mV
0100 = 400 mV
0101 = 500 mV
0110 = 600 mV
0111 = 700 mV
1000 = 800 mV
1001 = 900 mV
1010 = 1400 mV
1011 = 1600 mV
1100 = 1800 mV
1101 = 2000 mV
1110 = 2200 mV
1111 = Do not use.

Note 1: The Legacy charger emulation profiles do not use these settings. Whenever a Legacy charger emulation profile is applied within the DCE Cycle, these controls will not be updated and should be ignored. These settings are only used by the BC1.2 CDP and DCP charger emulation profiles.

REGISTER 10-31: PRELOADED EMULATION STIMULUS 2 CONFIGURATION 4 REGISTER (ADDRESS 38H)(Note 1)

U-x	U-x	U-x	U-x	U-x	R-1	R-0	R-0
—	—	—	—	—	S2_RATIO<2:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-3 **Unimplemented**

bit 2-0 **S2_RATIO<2:0>:** Determines the voltage divider ratio, as shown below, when the stimulus response is set to connect a voltage divider (i.e., S2_R2<3:0> = 0110b, 1001b, or 1100b).
000 = 0.25
001 = 0.33
010 = 0.4
011 = 0.5
100 = 0.54
101 = 0.6
110 = 0.66
111 = Do not use.

Note 1: The BC1.2 DCP and CDP charger emulation profiles do not use this control. Whenever the BC1.2 CDP or DCP charger emulation profile is applied, these controls will not be updated and should be ignored. These settings are only used by the Legacy charger emulation profiles.

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REGISTER 10-32: PRELOADED EMULATION STIMULUS 3 CONFIGURATION 1 REGISTER (ADDRESS 39H)

U-x	R-0	R-0	R-0	R-0	R-0	R-0	R-0
—	S3_TD_TYPE	S3_TD<2:0>			STIM3<2:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented**

bit 6 **S3_TD_TYPE:** Determines the behavior of the stimulus timer.
- 1 = The stimulus timer controls how long the response is applied after the stimulus is detected. The response is applied immediately and held for the duration of the timer, then removed (if the stimulus has been removed).
- 0 = The stimulus timer is a delay from when the stimulus is detected until the response is performed.

bit 5-3 **S3_TD<2:0>:** Determines the Stimulus 3 t_{STIM_DEL} value as shown below:
- 000 = 0 ms
- 001 = 1 ms
- 010 = 5 ms
- 011 = 10 ms
- 100 = 20 ms
- 101 = 40 ms
- 110 = 80 ms
- 111 = 100 ms

bit 2-0 **STIM3<2:0>:** Determines the Stimulus 3 that is used as shown below. Note that the lower threshold for the window comparator option is fixed at 400 mV and only applies to the D_{POUT} pin. This setting cannot be used for the DM_{OUT} port.
- 000 = V_{BUS} voltage ready to be applied before port power switch is closed. Next stimulus will not wait for this to be removed.
- 001 = D_{POUT} voltage is greater than the threshold (S3_TH).
- 010 = Window comparator. D_{POUT} voltage is less than the threshold (S3_TH) and D_{POUT} voltage greater than the fixed threshold.
- 011 = D_{MOUT} voltage is greater than the threshold (S3_TH).
- 100 = Do not use.
- 101 = Do not use.
- 110 = D_{POUT} voltage is greater than the threshold (S3_TH).
- 111 = Voltage is present after the port power switch is closed. Next stimulus will not wait for this to be removed.

REGISTER 10-33: PRELOADED EMULATION STIMULUS 3 CONFIGURATION 2 REGISTER (ADDRESS 3AH)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
S3_R3MAG<3:0>				S3_R3<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **S3_R3MAG<3:0>:** Determines the magnitude of the response to the stimulus. The bit decode changes meaning based on which response was selected. Data written to any field that is identified as "Do not use" will not be accepted. The data will not be updated and the settings will remain set at the previous value.

- **For S3_R3 settings `0000` - `0011`**, the response is a voltage applied on D_{POUT}/D_{MOUT} pins. The S3_R3MAG bits specify the voltage relative to ground:

`0000` = Pull Down	`0110` = 600 mV	`1100` = 1800 mV
`0001` = 400 mV	`0111` = 700 mV	`1101` = 2000 mV
`0010` = 400 mV	`1000` = 800 mV	`1110` = 2200 mV
`0011` = 400 mV	`1001` = 900 mV	`1111` = Do not use
`0100` = 400 mV	`1010` = 1400 mV	
`0101` = 500 mV	`1011` = 1600 mV	

- **For S3_R3 settings `0100`, `0111`, `1101` - `1111`**, the response is a resistor connected on D_{POUT}/D_{MOUT} to GND or V_{BUS}. The S3_R3MAG bits specify the resistor value:

`0000` = 1.8 kΩ	`0110` = 40 kΩ	`1100` = 100 kΩ
`0001` = 10 kΩ	`0111` = 43 kΩ	`1101` = 120 kΩ
`0010` = 15 kΩ	`1000` = 50 kΩ	`1110` = 150 kΩ
`0011` = 20 kΩ	`1001` = 60 kΩ	`1111` = Do not use
`0100` = 25 kΩ	`1010` = 75 kΩ	
`0101` = 30 kΩ	`1011` = 80 kΩ	

- **For S3_R3 settings `0110`, `1001`, `1100`**, the response is a voltage divider applied from V_{BUS} to GND with "center" at D_{POUT}/D_{MOUT}. The S3_R3MAG bits specify the minimum resistance of the voltage divider (Sum of R1 + R2):

`0000` = 93 kΩ	`0110` = 200 kΩ	`1100` = 200 kΩ
`0001` = 100 kΩ	`0111` = 200 kΩ	`1101` = 200 kΩ
`0010` = 125 kΩ	`1000` = 93 kΩ	`1110` = 200 kΩ
`0011` = 150 kΩ	`1001` = 100 kΩ	`1111` = Do not use
`0100` = 200 kΩ	`1010` = 125 kΩ	
`0101` = 200 kΩ	`1011` = 150 kΩ	

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REGISTER 10-33: PRELOADED EMULATION STIMULUS 3 CONFIGURATION 2 REGISTER (ADDRESS 3AH) (CONTINUED)

bit 3-0 **S3_R3<3:0>:** Defines the stimulus response as shown below:

0000 = Remove previous response on D_{POUT} and D_{MOUT}
0001 = Apply voltage on D_{POUT} (Note 1).
0010 = Apply voltage on D_{MOUT} (Note 2).
0011 = Apply voltage on D_{POUT} and D_{MOUT}.
0100 = Connect resistor from D_{POUT} to GND (Note 1).
0101 = Do not use.
0110 = Connect voltage divider from V_{BUS} to GND with "center" at D_{POUT} (Note 1).
0111 = Connect resistor form D_{MOUT} to GND (Note 2).
1000 = Do not use.
1001 = Connect voltage divider from V_{BUS} to GND with "center" at D_{MOUT} (Note 2).
1010 = Connect ≤ 200Ω resistor from D_{POUT} to D_{MOUT}.
1011 = Do not use.
1100 = Connect voltage divider from V_{BUS} to GND with 'center' at D_{POUT} and D_{MOUT}.
1101 = Connect resistor from D_{POUT} to GND and D_{MOUT} to GND.
1110 = If STIM3 = 000, the 15 kΩ pull down resistors applied to D_{POUT} and D_{MOUT} during emulation reset are not removed. If STIM3 = 111, the 15 kΩ pull down resistors applied to D_{POUT} and D_{MOUT} during emulation reset are removed. For all other STIM3 settings, whatever was applied is not changed.
1111 = Same as 1110 case above.

Note 1: If STIM3<2:0> = 000b and no other response was applied to the D_{POUT} pin, the 15 kΩ pull-down resistor applied to the D_{POUT} pin during emulation reset is not removed. Otherwise, the previous response is left on the D_{POUT} pin (if applicable) or the 15 kΩ pull-down resistor is removed.

2: If STIM3<2:0> = 000b and no other response was applied to the D_{MOUT} pin, the 15 kΩ pull-down resistor applied to the D_{MOUT} pin during emulation reset is not removed. Otherwise, the previous response is left on the D_{MOUT} pin (if applicable) or the 15 kΩ pull-down resistor is removed.

REGISTER 10-34: PRELOADED EMULATION STIMULUS 3 CONFIGURATION 3 REGISTER (ADDRESS 3BH)(Note 1)

U-x	U-x	R-0	R-0	R-0	R-0	R-0	R-0
—	—	S3_PUPD<1:0>		S3_TH<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented**

bit 5-4 **S3_PUPD<1:0>:** Determines the magnitude of the pull-down current applied on the D_{POUT} and D_{MOUT} pins when the stimulus response is to apply a voltage and the voltage magnitude is set at pull-down (0000b). The bit decode is as follows:

00 = 10 µA
01 = 50 µA
10 = 100 µA
11 = 150 µA

REGISTER 10-34: PRELOADED EMULATION STIMULUS 3 CONFIGURATION 3 REGISTER (ADDRESS 3BH)(Note 1) (CONTINUED)

bit 3-0 **S3_TH<3:0>:** Defines the threshold value, as shown below for the specified stimulus. If the stimulus is V_{BUS} voltage is ready to be applied or applied (i.e., STIM3<2:0> = 000b or 111b), the threshold value is ignored.
0000 = 400 mV
0001 = 400 mV
0010 = 400 mV
0011 = 300 mV
0100 = 400 mV
0101 = 500 mV
0110 = 600 mV
0111 = 700 mV
1000 = 800 mV
1001 = 900 mV
1010 = 1400 mV
1011 = 1600 mV
1100 = 1800 mV
1101 = 2000 mV
1110 = 2200 mV
1111 = Do not use.

Note 1: The Legacy charger emulation profiles do not use these settings. Whenever a Legacy charger emulation profile is applied within the DCE Cycle, these controls will not be updated and should be ignored. These settings are only used by the BC1.2 CDP and DCP charger emulation profiles.

10.13 Custom Emulation Configuration Registers

Name	Bits	Address	Cof	Default
Custom Emulation Config	8	40h	R/W	01h
Custom Emulation Stimulus 1 - Config 1	8	41h	R/W	00h
Custom Emulation Stimulus 1 - Config 2	8	42h	R/W	00h
Custom Emulation Stimulus 1 - Config 3	8	43h	R/W	00h
Custom Emulation Stimulus 1 - Config 4	8	44h	R/W	00h
Custom Emulation Stimulus 2 - Config 1	8	45h	R/W	00h
Custom Emulation Stimulus 2 - Config 2	8	46h	R/W	00h
Custom Emulation Stimulus 2 - Config 3	8	47h	R/W	00h
Custom Emulation Stimulus 2 - Config 4	8	48h	R/W	00h
Custom Emulation Stimulus 3 - Config 1	8	49h	R/W	00h
Custom Emulation Stimulus 3 - Config 2	8	4Ah	R/W	00h
Custom Emulation Stimulus 3 - Config 3	8	4Bh	R/W	00h
Custom Emulation Stimulus 3 - Config 3	8	4Ch	R/W	00h

The Custom Emulation Configuration registers store the values used by the Custom Charger Emulation circuitry. The Custom Charger Emulation profile is set up as three stimuli and the respective responses.

The contents of registers 40h to 4Ch are retained in Sleep.

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REGISTER 10-35: CUSTOM EMULATION CONFIGURATION REGISTER (ADDRESS 40H)

U-x	U-x	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R/W-1
—	—	CS_TO_DIS	CS_EM_TO<1:0>		CS_FRST	RESERVED	CSEM_DIS
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented**

bit 5 **CS_TO_DIS:** Disables the Emulation Timeout timer when the Custom Charger Emulation profile is applied during the DCE Cycle. If the EM_TO_DIS is set, this bit will have no effect (**Note 1**).

1 = The Emulation Timeout timer is disabled when the Custom charger emulation profile is applied during the DCE Cycle. When the Custom charger emulation profile is being applied, the UCS81003 will be constantly monitoring the I_{BUS} current. When the I_{BUS} current is greater than I_{BUS_CHG}, regardless of the reason, then the Custom Charger Emulation profile will accepted. If the portable device does not draw more than I_{BUS_CHG} current, then the UCS81003 will continue waiting until this bit is cleared.

0 = The Emulation Timeout timer is enabled when the Custom charger emulation profile is applied during the DCE Cycle and the EM_TO_DIS bit is not set

bit 4-3 **CS_EM_TO<1:0>:** Determines the $t_{EM_TIMEOUT}$ value, as shown below. Is used when the Custom charger emulation profile is used during the DCE Cycle.

00 = 0.8s
01 = 1.6s
10 = 6.4s
11 = 12.8s

bit 2 **CS_FRST:** Disables the Custom charger emulation profile.

1 = The Custom charger emulation profile is the first of the profiles applied during the DCE Cycle.
0 = The Custom charger emulation profile is the last of the profiles applied during the DCE Cycle.

bit 1 **RESERVED:** Do not change. This bit will read '0' and should not be written to a logic '1'.

bit 0 **CSEM_DIS:** Determines whether the Custom charger emulation profile is placed first or last in the DCE Cycle.

1 = The Custom charger emulation profile is not enabled.
0 = The Custom charger emulation profile is enabled.

Note 1: If the CS_TO_DIS bit is set and the Custom charger emulation profile was accepted during the DCE cycle, a removal is not detected. To avoid this issue, re-enable the emulation timeout after applying any test profiles and charging with the 'final' profile.

REGISTER 10-36: CUSTOM EMULATION STIMULUS 1 CONFIGURATION 1 REGISTER (ADDRESS 41H)

U-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W--0	R/W--0	R/W--0
—	CS_S1TYPE	CS_S1_TD<2:0>			CS_STIM1<2:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented**

bit 6 **CS_S1TYPE:** Determines the behavior of the stimulus timer.
- 1 = The stimulus timer controls how long the response is applied after the stimulus is detected. The response is applied immediately and held for the duration of the timer then removed (if the stimulus has been removed).
- 0 = The stimulus timer is a delay from when the stimulus is detected until the response is performed.

bit 5-3 **CS_S1_TD<2:0>:** Determines the stimulus 1 t_{STIM_DEL} value as shown below.
- 000 = 0 ms
- 001 = 1 ms
- 010 = 5 ms
- 011 = 10 ms
- 100 = 20 ms
- 101 = 40 ms
- 110 = 80 ms
- 111 =100 ms

bit 2-0 **CS_STIM1<2:0>:** Determines the Stimulus 1 that is used as shown below. Note that the lower threshold for the window comparator option is fixed at 400 mV and only applies to the D_{POUT} pin. This setting cannot be used for the D_{MOUT} port.
- 000 = V_{BUS} voltage ready to be applied before port power switch is closed. Next stimulus will not wait for this to be removed.
- 001 = D_{POUT} voltage is greater than the threshold (CS_S1_TH).
- 010 = Window comparator. D_{POUT} voltage is lower than the threshold (CS_S1_TH) and D_{POUT} voltage greater than the fixed threshold.
- 011 = D_{MOUT} voltage is greater than the threshold (CS_S1_TH).
- 100 = Do not use.
- 101 = Do not use.
- 110 = D_{POUT} voltage is greater than the threshold (CS_S1_TH).
- 111 = V_{BUS} voltage is present after port power switch is closed. Next stimulus will not wait for this to be removed.

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REGISTER 10-37: CUSTOM EMULATION STIMULUS 1 CONFIGURATION 2 REGISTER (ADDRESS 42H)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CS_S1_R1MAG<3:0>				CS_S1_R1<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **CS_S1_R1MAG<3:0>:** Determines the magnitude of the response to the stimulus. The bit decode changes meaning based on which response was selected. Data written to any field that is identified as 'Do not use' will not be accepted. The data will not be updated and the settings will remain set at the previous value.

- **For CS_S1_R1 settings `0000 - 0011`**, the response is a voltage applied on D_{POUT}/D_{MOUT} pins. The CS_S1_R1MAG bits specify the voltage relative to ground:

`0000` = Pull Down	`0110` = 600 mV	`1100` = 1800 mV
`0001` = 400 mV	`0111` = 700 mV	`1101` = 2000 mV
`0010` = 400 mV	`1000` = 800 mV	`1110` = 2200 mV
`0011` = 400 mV	`1001` = 900 mV	`1111` = Do not use
`0100` = 400 mV	`1010` = 1400 mV	
`0101` = 500 mV	`1011` = 1600 mV	

- **For CS_S1_R1 settings `0100`, `0111`, `1101 - 1111`**, the response is a resistor connected on D_{POUT}/D_{MOUT} to GND or V_{BUS}. The CS_S1_R1MAG bits specify the resistor value:

`0000` = 1.8 kΩ	`0110` = 40 kΩ	`1100` = 100 kΩ
`0001` = 10 kΩ	`0111` = 43 kΩ	`1101` = 120 kΩ
`0010` = 15 kΩ	`1000` = 50 kΩ	`1110` = 150 kΩ
`0011` = 20 kΩ	`1001` = 60 kΩ	`1111` = Do not use
`0100` = 25 kΩ	`1010` = 75 kΩ	
`0101` = 30 kΩ	`1011` = 80 kΩ	

- **For CS_S1_R1 settings `0110`, `1001`, `1100`**, the response is a voltage divider applied from V_{BUS} to GND with "center" at D_{POUT}/D_{MOUT}. The CS_S1_R1MAG bits specify the minimum resistance of the voltage divider (Sum of R1 + R2):

`0000` = 93 kΩ	`0110` = 200 kΩ	`1100` = 200 kΩ
`0001` = 100 kΩ	`0111` = 200 kΩ	`1101` = 200 kΩ
`0010` = 125 kΩ	`1000` = 93 kΩ	`1110` = 200 kΩ
`0011` = 150 kΩ	`1001` = 100 kΩ	`1111` = Do not use
`0100` = 200 kΩ	`1010` = 125 kΩ	
`0101` = 200 kΩ	`1011` = 150 kΩ	

REGISTER 10-37: CUSTOM EMULATION STIMULUS 1 CONFIGURATION 2 REGISTER (ADDRESS 42H) (CONTINUED)

bit 3-0 **CS_S1_R1<3:0>:** Defines the stimulus response as shown below:

0000 = Remove previous response on D_{POUT} and D_{MOUT}.
0001 = Apply voltage on D_{POUT} (Note 1).
0010 = Apply voltage on D_{MOUT} (Note 2).
0011 = Apply voltage on D_{POUT} and D_{MOUT}.
0100 = Connect resistor from D_{POUT} to GND (Note 1).
0101 = Do not use.
0110 = Connect voltage divider from V_{BUS} to GND with "center" at D_{POUT} (Note 1).
0111 = Connect resistor form D_{MOUT} to GND (Note 2).
1000 = Do not use.
1001 = Connect voltage divider from V_{BUS} to GND with "center" at D_{MOUT} (Note 2).
1010 = Connect ≤ 200Ω resistor from D_{POUT} to D_{MOUT}.
1011 = Do not use.
1100 = Connect voltage divider from V_{BUS} to GND with 'center' at D_{POUT} and D_{MOUT}.
1101 = Connect resistor from D_{POUT} to GND and D_{MOUT} to GND.
1110 = If CS_STIM1 = 000, the 15 kΩ pull down resistors applied to D_{POUT} and D_{MOUT} during emulation reset are not removed. If CS_STIM1 = 111, the 15 kΩ pull down resistors applied to D_{POUT} and D_{MOUT} during emulation reset are removed. For all other CS_STIM1 settings, whatever was applied is not changed.
1111 = Same as 1110 case above.

Note 1: If CS_STIM1<2:0> = 000b and no other response was applied to the D_{POUT} pin, the 15 kΩ pull-down resistor applied to the D_{POUT} pin during emulation reset is not removed. Otherwise, the previous response is left on the D_{POUT} pin (if applicable) or the 15 kΩ pull-down resistor is removed.

2: If CS_STIM1<2:0> = 000b and no other response was applied to the D_{MOUT} pin, the 15 kΩ pull-down resistor applied to the D_{MOUT} pin during emulation reset is not removed. Otherwise, the previous response is left on the D_{MOUT} pin (if applicable) or the 15 kΩ pull-down resistor is removed.

REGISTER 10-38: CUSTOM EMULATION STIMULUS 1 CONFIGURATION 3 REGISTER (ADDRESS 43H)(Note 1)

U-x	U-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	CS_S1_PUPD<1:0>		CS_S1_TH<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented**

bit 5-4 **CS_S1_PUPD<1:0>:** Determines the magnitude of the pull-down current applied on the D_{POUT} and D_{MOUT} pins when the stimulus response is to apply a voltage and the voltage magnitude is set at pull-down (0000b). The bit decode is given below.

00 = 10 µA
01 = 50 µA
10 = 100 µA
11 = 150 µA

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REGISTER 10-38: CUSTOM EMULATION STIMULUS 1 CONFIGURATION 3 REGISTER (ADDRESS 43H)(Note 1) (CONTINUED)

bit 3-0 **CS_S1_TH<3:0>:** Defines the threshold value, as shown below for the specified stimulus. If the stimulus is V_{BUS} voltage is ready to be applied or applied (i.e., CS_STIM1<2:0> = 000b or 111b), the threshold value is ignored.

0000 = 400 mV
0001 = 400 mV
0010 = 400 mV
0011 = 300 mV
0100 = 400 mV
0101 = 500 mV
0110 = 600 mV
0111 = 700 mV
1000 = 800 mV
1001 = 900 mV
1010 = 1400 mV
1011 = 1600 mV
1100 = 1800 mV
1101 = 2000 mV
1110 = 2200 mV
1111 = Do not use.

Note 1: The Legacy charger emulation profiles do not use these settings. Whenever a Legacy charger emulation profile is applied within the DCE Cycle, these controls will not be updated and should be ignored. These settings are only used by the BC1.2 CDP and DCP charger emulation profiles.

REGISTER 10-39: CUSTOM EMULATION STIMULUS 1 CONFIGURATION 4 REGISTER (ADDRESS 44H)(Note 1)

U-x	U-x	U-x	U-x	U-x	R/W-0	R/W-0	R/W-0
—	—	—	—	—	CS_S1_RATIO<2:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-3 **Unimplemented**

bit 2-0 **CS_S1_RATIO<2:0>:** Determines the voltage divider ratio, as shown below, when the stimulus response is set to connect a voltage divider (i.e., CS_S1_R1<3:0> = 0110b, 1001b, or 1100b).

000 = 0.25
001 = 0.33
010 = 0.4
011 = 0.5
100 = 0.54
101 = 0.6
110 = 0.66
111 = Do not use.

Note 1: The BC1.2 DCP and CDP charger emulation profiles do not use this control. Whenever the BC1.2 CDP or DCP charger emulation profile is applied, these controls will not be updated and should be ignored. These settings are only used by the Legacy charger emulation profiles.

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REGISTER 10-40: CUSTOM EMULATION STIMULUS 2 CONFIGURATION 1 REGISTER (ADDRESS 45H)

U-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	CS_S2TYPE	CS_S2_TD<2:0>			CS_STIM2<2:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented**

bit 6 **CS_S2TYPE:** Determines the behavior of the stimulus timer.

1 = The stimulus timer controls how long the response is applied after the stimulus is detected. The response is applied immediately and held for the duration of the timer, then removed (if the stimulus has been removed).

0 = The stimulus timer is a delay from when the stimulus is detected until the response is performed.

bit 5-3 **CS_S2_TD<2:0>:** Determines the Stimulus 2 t_{STIM_DEL} value as shown below:

000 = 0 ms
001 = 1 ms
010 = 5 ms
011 = 10 ms
100 = 20 ms
101 = 40 ms
110 = 80 ms
111 = 100 ms

bit 2-0 **CS_STIM2<2:0>:** Determines the Stimulus 2 that is used as shown below. Note that the lower threshold for the window comparator option is fixed at 400 mV and only applies to the D_{POUT} pin. This setting cannot be used for the DM_{OUT} port.

000 = V_{BUS} voltage ready to be applied before port power switch is closed. Next stimulus will not wait for this to be removed.
001 = D_{POUT} voltage is greater than the threshold (CS_S2_TH).
010 = Window comparator. D_{POUT} voltage is less than the threshold (S1_TH) and D_{POUT} voltage greater than the fixed threshold.
011 = D_{MOUT} voltage is greater than the threshold (CS_S2_TH).
100 = Do not use.
101 = Do not use.
110 = D_{POUT} voltage is greater than the threshold (CS_S2_TH).
111 = Voltage is present after the port power switch is closed. Next stimulus will not wait for this to be removed.

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REGISTER 10-41: CUSTOM EMULATION STIMULUS 2 CONFIGURATION 2 REGISTER (ADDRESS 46H)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CS_S2_R2MAG<3:0>				CS_S2_R2<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **CS_S2_R2MAG<3:0>:** Determines the magnitude of the response to the stimulus. The bit decode changes meaning based on which response was selected. Data written to any field that is identified as "Do not use" will not be accepted. The data will not be updated and the settings will remain set at the previous value.

- **For CS_S2_R2 settings `0000` - `0011`**, the response is a voltage applied on D_{POUT}/D_{MOUT} pins. The CS_S2_R2MAG bits specify the voltage relative to ground:

`0000` = Pull Down	`0110` = 600 mV	`1100` = 1800 mV
`0001` = 400 mV	`0111` = 700 mV	`1101` = 2000 mV
`0010` = 400 mV	`1000` = 800 mV	`1110` = 2200 mV
`0011` = 400 mV	`1001` = 900 mV	`1111` = Do not use
`0100` = 400 mV	`1010` = 1400 mV	
`0101` = 500 mV	`1011` = 1600 mV	

- **For CS_S2_R2 settings `0100`, `0111`, `1101` - `1111`**, the response is a resistor connected on D_{POUT}/D_{MOUT} to GND or V_{BUS}. The CS_S2_R2MAG bits specify the resistor value:

`0000` = 1.8 kΩ	`0110` = 40 kΩ	`1100` = 100 kΩ
`0001` = 10 kΩ	`0111` = 43 kΩ	`1101` = 120 kΩ
`0010` = 15 kΩ	`1000` = 50 kΩ	`1110` = 150 kΩ
`0011` = 20 kΩ	`1001` = 60 kΩ	`1111` = Do not use
`0100` = 25 kΩ	`1010` = 75 kΩ	
`0101` = 30 kΩ	`1011` = 80 kΩ	

- **For CS_S2_R2 settings `0110`, `1001`, `1100`**, the response is a voltage divider applied from V_{BUS} to GND with "center" at D_{POUT}/D_{MOUT}. The CS_S2_R2MAG bits specify the minimum resistance of the voltage divider (Sum of R1 + R2):

`0000` = 93 kΩ	`0110` = 200 kΩ	`1100` = 200 kΩ
`0001` = 100 kΩ	`0111` = 200 kΩ	`1101` = 200 kΩ
`0010` = 125 kΩ	`1000` = 93 kΩ	`1110` = 200 kΩ
`0011` = 150 kΩ	`1001` = 100 kΩ	`1111` = Do not use
`0100` = 200 kΩ	`1010` = 125 kΩ	
`0101` = 200 kΩ	`1011` = 150 kΩ	

REGISTER 10-42: CUSTOM EMULATION STIMULUS 2 CONFIGURATION 3 REGISTER (ADDRESS 47H)(Note 1) (CONTINUED)

bit 3-0 **CS_S2_TH<3:0>:** Defines the threshold value, as shown below for the specified stimulus. If the stimulus is V_{BUS} voltage is ready to be applied or applied (i.e., CS_STIM2<2:0> = 000b or 111b), the threshold value is ignored.
0000 = 400 mV
0001 = 400 mV
0010 = 400 mV
0011 = 300 mV
0100 = 400 mV
0101 = 500 mV
0110 = 600 mV
0111 = 700 mV
1000 = 800 mV
1001 = 900 mV
1010 = 1400 mV
1011 = 1600 mV
1100 = 1800 mV
1101 = 2000 mV
1110 = 2200 mV
1111 = Do not use.

Note 1: The Legacy charger emulation profiles do not use these settings. Whenever a Legacy charger emulation profile is applied within the DCE Cycle, these controls will not be updated and should be ignored. These settings are only used by the BC1.2 CDP and DCP charger emulation profiles.

REGISTER 10-43: CUSTOM EMULATION STIMULUS 2 CONFIGURATION 4 REGISTER (ADDRESS 48H)(Note 1)

U-x	U-x	U-x	U-x	U-x	R/W-0	R/W-0	R/W-0
—	—	—	—	—	CS_S2_RATIO<2:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-3 **Unimplemented**

bit 2-0 **CS_S2_RATIO<2:0>:** Determines the voltage divider ratio, as shown below, when the stimulus response is set to connect a voltage divider (i.e., CS_S2_R2<3:0> = 0110b, 1001b, or 1100b).
000 = 0.25
001 = 0.33
010 = 0.4
011 = 0.5
100 = 0.54
101 = 0.6
110 = 0.66
111 = Do not use.

Note 1: The BC1.2 DCP and CDP charger emulation profiles do not use this control. Whenever the BC1.2 CDP or DCP charger emulation profile is applied, these controls will not be updated and should be ignored. These settings are only used by the Legacy charger emulation profiles.

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REGISTER 10-44: CUSTOM EMULATION STIMULUS 3 CONFIGURATION 1 REGISTER (ADDRESS 49H)

U-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	CS_S3TYPE	CS_S3_TD<2:0>			CS_STIM3<2:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented**

bit 6 **CS_S3TYPE:** Determines the behavior of the stimulus timer.

1 = The stimulus timer controls how long the response is applied after the stimulus is detected. The response is applied immediately and held for the duration of the timer, then removed (if the stimulus has been removed).

0 = The stimulus timer is a delay from when the stimulus is detected until the response is performed.

bit 5-3 **CS_S3_TD<2:0>:** Determines the Stimulus 3 t_{STIM_DEL} value as shown below:

000 = 0 ms
001 = 1 ms
010 = 5 ms
011 = 10 ms
100 = 20 ms
101 = 40 ms
110 = 80 ms
111 = 100 ms

bit 2-0 **CS_STIM3<2:0>:** Determines the Stimulus 3 that is used as shown below. Note that the lower threshold for the window comparator option is fixed at 400 mV and only applies to the D_{POUT} pin. This setting cannot be used for the DM_{OUT} port.

000 = V_{BUS} voltage ready to be applied before port power switch is closed. Next stimulus will not wait for this to be removed.
001 = D_{POUT} voltage is greater than the threshold (CS_S3_TH).
010 = Window comparator. D_{POUT} voltage is lower than the threshold (CS_S3_TH) and D_{POUT} voltage greater than the fixed threshold.
011 = D_{MOUT} voltage is greater than the threshold (CS_S3_TH).
100 = Do not use.
101 = Do not use.
110 = D_{POUT} voltage is greater than the threshold (CS_S3_TH).
111 = Voltage is present after the port power switch is closed. Next stimulus will not wait for this to be removed.

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REGISTER 10-45: CUSTOM EMULATION STIMULUS 3 CONFIGURATION 2 REGISTER (ADDRESS 4AH)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CS_S3_R3MAG<3:0>				CS_S3_R3<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **CS_S3_R3MAG<3:0>:** Determines the magnitude of the response to the stimulus. The bit decode changes meaning based on which response was selected. Data written to any field that is identified as "Do not use" will not be accepted. The data will not be updated and the settings will remain set at the previous value.

- **For CS_S3_R3 settings `0000` - `0011`**, the response is a voltage applied on D_{POUT}/D_{MOUT} pins. The CS_S3_R3MAG bits specify the voltage relative to ground:

`0000` = Pull Down	`0110` = 600 mV	`1100` = 1800 mV
`0001` = 400 mV	`0111` = 700 mV	`1101` = 2000 mV
`0010` = 400 mV	`1000` = 800 mV	`1110` = 2200 mV
`0011` = 400 mV	`1001` = 900 mV	`1111` = Do not use
`0100` = 400 mV	`1010` = 1400 mV	
`0101` = 500 mV	`1011` = 1600 mV	

- **For CS_S3_R3 settings `0100`, `0111`, `1101` - `1111`**, the response is a resistor connected on D_{POUT}/D_{MOUT} to GND or V_{BUS}. The CS_S3_R3MAG bits specify the resistor value:

`0000` = 1.8 kΩ	`0110` = 40 kΩ	`1100` = 100 kΩ
`0001` = 10 kΩ	`0111` = 43 kΩ	`1101` = 120 kΩ
`0010` = 15 kΩ	`1000` = 50 kΩ	`1110` = 150 kΩ
`0011` = 20 kΩ	`1001` = 60 kΩ	`1111` = Do not use
`0100` = 25 kΩ	`1010` = 75 kΩ	
`0101` = 30 kΩ	`1011` = 80 kΩ	

- **For CS_S3_R3 settings `0110`, `1001`, `1100`**, the response is a voltage divider applied from V_{BUS} to GND with "center" at D_{POUT}/D_{MOUT}. The CS_S3_R3MAG bits specify the minimum resistance of the voltage divider (Sum of R1 + R2):

`0000` = 93 kΩ	`0110` = 200 kΩ	`1100` = 200 kΩ
`0001` = 100 kΩ	`0111` = 200 kΩ	`1101` = 200 kΩ
`0010` = 125 kΩ	`1000` = 93 kΩ	`1110` = 200 kΩ
`0011` = 150 kΩ	`1001` = 100 kΩ	`1111` = Do not use
`0100` = 200 kΩ	`1010` = 125 kΩ	
`0101` = 200 kΩ	`1011` = 150 kΩ	

REGISTER 10-45: CUSTOM EMULATION STIMULUS 3 CONFIGURATION 2 REGISTER (ADDRESS 4AH) (CONTINUED)

bit 3-0 **CS_S3_R3<3:0>:** Defines the stimulus response as shown below:

0000 = Remove previous response on D_{POUT} and D_{MOUT}
0001 = Apply voltage on D_{POUT} (Note 1).
0010 = Apply voltage on D_{MOUT} (Note 2).
0011 = Apply voltage on D_{POUT} and D_{MOUT}.
0100 = Connect resistor from D_{POUT} to GND (Note 1).
0101 = Do not use.
0110 = Connect voltage divider from V_{BUS} to GND with "center" at D_{POUT} (Note 1).
0111 = Connect resistor form D_{MOUT} to GND (Note 2).
1000 = Do not use.
1001 = Connect voltage divider from V_{BUS} to GND with "center" at D_{MOUT} (Note 2).
1010 = Connect ≤ 200Ω resistor from D_{POUT} to D_{MOUT}.
1011 = Do not use.
1100 = Connect voltage divider from V_{BUS} to GND with 'center' at D_{POUT} and D_{MOUT}.
1101 = Connect resistor from D_{POUT} to GND and D_{MOUT} to GND.
1110 = If CS_STIM3 = 000, the 15 kΩ pull down resistors applied to D_{POUT} and D_{MOUT} during emulation reset are not removed. If CS_STIM3 = 111, the 15 kΩ pull down resistors applied to D_{POUT} and D_{MOUT} during emulation reset are removed. For all other CS_STIM3 settings, whatever was applied is not changed.
1111 = Same as 1110 case above.

Note 1: If CS_STIM3<2:0> = 000b and no other response was applied to the D_{POUT} pin, the 15 kΩ pull-down resistor applied to the D_{POUT} pin during emulation reset is not removed. Otherwise, the previous response is left on the D_{POUT} pin (if applicable) or the 15 kΩ pull-down resistor is removed.

2: If CS_STIM3<2:0> = 000b and no other response was applied to the D_{MOUT} pin, the 15 kΩ pull-down resistor applied to the D_{MOUT} pin during emulation reset is not removed. Otherwise, the previous response is left on the D_{MOUT} pin (if applicable) or the 15 kΩ pull-down resistor is removed.

REGISTER 10-46: CUSTOM EMULATION STIMULUS 3 CONFIGURATION 3 REGISTER (ADDRESS 4BH)(Note 1)

U-x	U-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	CS_S3_PUPD<1:0>		CS_S3_TH<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented**

bit 5-4 **CS_S3_PUPD<1:0>:** Determines the magnitude of the pull-down current applied on the D_{POUT} and D_{MOUT} pins when the stimulus response is to apply a voltage and the voltage magnitude is set at pull-down (0000b). The bit decode is as follows:

00 = 10 µA
01 = 50 µA
10 = 100 µA
11 = 150 µA

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REGISTER 10-46: CUSTOM EMULATION STIMULUS 3 CONFIGURATION 3 REGISTER (ADDRESS 4BH)(Note 1) (CONTINUED)

bit 3-0 **CS_S3_TH<3:0>:** Defines the threshold value, as shown below for the specified stimulus. If the stimulus is V_{BUS} voltage is ready to be applied or applied (i.e., CS_STIM3<2:0> = 000b or 111b), the threshold value is ignored.
0000 = 400 mV
0001 = 400 mV
0010 = 400 mV
0011 = 300 mV
0100 = 400 mV
0101 = 500 mV
0110 = 600 mV
0111 = 700 mV
1000 = 800 mV
1001 = 900 mV
1010 = 1400 mV
1011 = 1600 mV
1100 = 1800 mV
1101 = 2000 mV
1110 = 2200 mV
1111 = Do not use.

Note 1: The Legacy charger emulation profiles do not use these settings. Whenever a Legacy charger emulation profile is applied within the DCE Cycle, these controls will not be updated and should be ignored. These settings are only used by the BC1.2 CDP and DCP charger emulation profiles.

REGISTER 10-47: CUSTOM EMULATION STIMULUS 3 CONFIGURATION 4 REGISTER (ADDRESS 4CH)(Note 1)

U-x	U-x	U-x	U-x	U-x	R/W-0	R/W-0	R/W-0
—	—	—	—	—	CS_S3_RATIO<2:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-3 **Unimplemented**

bit 2-0 **CS_S3_RATIO<2:0>:** Determines the voltage divider ratio, as shown below, when the stimulus response is set to connect a voltage divider (i.e., CS_S3_R3<2:0> = 0110b, 1001b, or 1100b).
000 = 0.25
001 = 0.33
010 = 0.4
011 = 0.5
100 = 0.54
101 = 0.6
110 = 0.66
111 = Do not use

Note 1: The BC1.2 DCP and CDP charger emulation profiles do not use this control. Whenever the BC1.2 CDP or DCP charger emulation profile is applied, these controls will not be updated and should be ignored. These settings are only used by the Legacy charger emulation profiles.

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10.14 Current Limiting Behavior Configuration Registers

Name	Bits	Address	Cof	Default
Applied Current Limiting Behavior	8	50h	R	82h
Custom Current Limiting Behavior Config	8	51h	R/W	82h

10.14.1 APPLIED CURRENT LIMITING BEHAVIOR REGISTER

The Applied Current Limiting Behavior Register stores the values used by the applied current limiting mode (Trip or CC) when the custom settings are not used. The contents of this register are updated automatically when charger emulation is completed.

REGISTER 10-48: APPLIED CURRENT LIMITING BEHAVIOR REGISTER (ADDRESS 50H)

R-1	R-0	U-x	R-0	R-0	R-0	R-1	R-0
SEL_VBUS_MIN<1:0>		—	SEL_R2_IMIN<2:0>			RESERVED	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **SEL_VBUS_MIN<1:0>:** Define the V_{BUS_MIN} voltage as follows:
00 = 1.5V
01 = 1.75V
10 = 2.0V
11 = 2.25V

bit 5 **Unimplemented**

bit 4-2 **SEL_R2_IMIN<2:0>:** Define the I_{BUS_R2MIN} current as follows:
000 = 120 mA
001 = 570 mA
010 = 1000 mA
011 = 1350 mA
100 = 1680 mA
101 = 2050 mA

bit 1-0 **RESERVED:** Do not change.

Note 1: The values specified above are the typical ones..

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10.14.2 CUSTOM CURRENT LIMITING BEHAVIOR CONFIGURATION REGISTER

The Custom Current Limiting Behavior Configuration Register allows programming of current limit parameters. These controls are used when a portable device handshakes using the Legacy charger emulation profiles (except Legacy 3), the Custom charger emulation profile, or does not handshake as a dedicated charger (i.e., a power thief).

The contents of this register are retained in Sleep.

REGISTER 10-49: CUSTOM CURRENT LIMITING BEHAVIOR CONFIG REGISTER (ADDRESS 51H)

R/W-1	R/W-0	U-x	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0
CS_VBUS_MIN<1:0>		—	CS_R2_IMIN<2:0>			RESERVED	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 CS_VBUS_MIN<1:0>: Defines the Custom V_{BUS_MIN} voltage as shown below. Note that V_{BUS_MIN} is checked even when operating with Trip Current Limiting.
00 = 1.5V
01 = 1.75V
10 = 2.0V
11 = 2.25V

bit 5 Unimplemented

bit 4-2 CS_R2_IMIN<2:0>: Define the Custom I_{BUS_R2MIN} threshold as shown below. The default is 120 mA. This value is used under the following conditions: when a portable device handshakes using the Legacy charger emulation profiles (except Legacy 3) the Custom charger emulation profile or when it does not handshake in DCE Cycle (i.e., a power thief). Under these conditions, the current limiting mode is determined by the relative value of I_{BUS_R2MIN} and ILIM. When $I_{BUS_R2MIN} \leq I_{LIM}$ or $I_{LIM} > 1.68$ A, Trip Current Limiting used; otherwise, CC mode is used.
Define the I_{BUS_R2MIN} current as follows:
000 = 120 mA
001 = 570 mA
010 = 1000 mA
011 = 1350 mA
100 = 1680 mA
101 = 2050 mA

bit 1-0 RESERVED: Do not change.

Note 1: The values specified above are the typical ones..

10.15 Product ID Register

Name	Bits	Address	Cof	Default
Product ID	8	FDh	R	4Eh

The Product ID register stores a unique 8-bit value that identifies the UCS device family.

10.16 Manufacturer ID Register

Name	Bits	Address	Cof	Default
Manufacturer ID	8	FEh	R	5Dh

The Manufacturer ID register stores a unique 8-bit value that identifies Microchip Technology Inc.

10.17 Revision Register

Name	Bits	Address	Cof	Default
Revision	8	FFh	R	82h

The Revision register stores an 8-bit value that represents the part revision.

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11.0 COMMUNICATIONS

11.1 Operating Mode

The UCS81003 can operate in SMBus mode (see **Section 11.2 "SMBus Operating Mode"**) or Stand-Alone mode (see **Section 11.3 "Stand-Alone Operating Mode"**). The resistor on the COMM_SEL/I_{LIM} pin determines the operating mode and the hardware-set I_{LIM} setting, as shown in Table 11-1. Unless connected to GND or V_{DD}, the resistors in Table 11-1 are pull-down resistors.

Note: If it is necessary to connect the COMM_SEL/I_{LIM} pin to V_{DD} via a pull-up resistor, it is recommended that this resistor value not exceed 100 kΩ.

TABLE 11-1: UCS81003 COMMUNICATION MODE AND I_{LIM} SELECTION (Note 1)

SELECTION Resistor ±5%	I_{LIM} Setting	Communications Mode
GND	570 mA	SMBus - see **Section 11.2.1.2**
10 kΩ pull-down	1000 mA	SMBus - see **Section 11.2.1.2**
12 kΩ pull-down	1130 mA	SMBus - see **Section 11.2.1.2**
15 kΩ pull-down	1350 mA	SMBus - see **Section 11.2.1.2**
18 kΩ pull-down	1680 mA	SMBus - see **Section 11.2.1.2**
22 kΩ pull-down	2050 mA	SMBus - see **Section 11.2.1.2**
27 kΩ pull-down	2280 mA	SMBus - see **Section 11.2.1.2**
33 kΩ pull-down	2850 mA (3000 mA maximum)	SMBus - see **Section 11.2.1.2**
47 kΩ pull-down	570 mA	Stand-Alone mode
56 kΩ pull-down	1000 mA	Stand-Alone mode
68 kΩ pull-down	1130 mA	Stand-Alone mode
82 kΩ pull-down	1350 mA	Stand-Alone mode
100 kΩ pull-down	1680 mA	Stand-Alone mode
120 kΩ pull-down	2050 mA	Stand-Alone mode
150 kΩ pull-down	2280 mA	Stand-Alone mode
V_{DD} (If a pull-up resistor is used, its value must not exceed 100 kΩ.)	2850 mA (3000 mA maximum)	Stand-Alone mode

Note 1: Unless otherwise indicated, the values specified in this table are the typical I_{LIM} in Table 1-2.

11.2 SMBus Operating Mode

When the COMM_SEL/I_{LIM} pin is connected directly to ground or though a pull-down resistor with a value of 33 kΩ or below as listed in Table 11-1, the UCS81003 communicates via the SMBus or I^2C communications protocols.

Note 1: Upon power-up, the UCS81003 will not respond to any SMBus communications for 5.5 ms. After this time, full functionality is available.

2: When in the Sleep state, the first SMBus read command sent to the UCS81003 device address will wake it. Any data sent to the UCS81003 will be ignored and any data read from the UCS81003 should be considered invalid. The UCS81003 will be fully functional 3 ms after this first read command is sent. See **Section 5.1.2 "Sleep State Operation"**.

11.2.1 SYSTEM MANAGEMENT BUS

In SMBus mode, the UCS81003 communicates with a host controller. The SMBus is a two-wire serial communication protocol between a computer host and its peripheral devices. A detailed timing diagram is shown in Figure 11-1. Stretching of the SMCLK signal is supported; however, the UCS81003 will not stretch the clock signal.

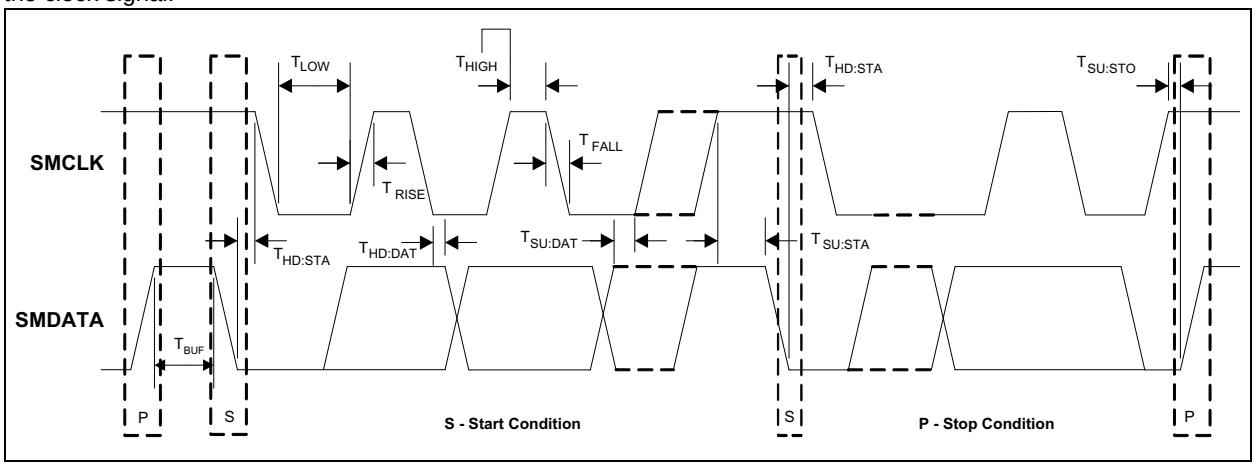

FIGURE 11-1: *SMBus Timing Diagram.*

11.2.1.1 SMBus Start Bit

The SMBus Start bit is defined as a transition of the SMBus data line from a logic '1' state to a logic '0' state while the SMBus clock line is in a logic '1' state.

11.2.1.2 SMBus Address and RD/$\overline{WR}$ Bit

The SMBus Address Byte consists of the 7-bit client address followed by the RD/$\overline{WR}$ indicator bit. If this RD/$\overline{WR}$ bit is a logic '0', the SMBus host is writing data to the client device. If this RD/$\overline{WR}$ bit is a logic '1', the SMBus host is reading data from the client device.

The SMBus address is determined based on the resistor connected on the SEL pin as shown in Table 11-2.

Note:	If it is necessary to connect the SEL pin to V_{DD} via a resistor, the pull-up resistor may be any value up to 100 kΩ.

TABLE 11-2: SEL PIN DECODE

Resistor (±5%)	PWR_EN Polarity	SMBus Address
GND	Active Low	1010_111(r/$\overline{w}$)
10 kΩ pull-down	Active Low	1010_110(r/$\overline{w}$)
12 kΩ pull-down	Active Low	1010_101(r/$\overline{w}$)
15 kΩ pull-down	Active Low	1010_100(r/$\overline{w}$)
18 kΩ pull-down	Active Low	0110_000(r/$\overline{w}$)
22 kΩ pull-down	Active Low	0110_001(r/$\overline{w}$)
27 kΩ pull-down	Active Low	0110_010(r/$\overline{w}$)
33 kΩ pull-down	Active Low	0110_011(r/$\overline{w}$)
47 kΩ pull-down	Active High	0110_011(r/$\overline{w}$)
56 kΩ pull-down	Active High	0110_010(r/$\overline{w}$)
68 kΩ pull-down	Active High	0110_001(r/$\overline{w}$)
82 kΩ pull-down	Active High	0110_000(r/$\overline{w}$)
100 kΩ pull-down	Active High	1010_100(r/$\overline{w}$)
120 kΩ pull-down	Active High	1010_101(r/$\overline{w}$)
150 kΩ pull-down	Active High	1010_110(r/$\overline{w}$)
V_{DD} (If a pull-up resistor is used, its value must not exceed 100 kΩ)	Active High	1010_111(r/$\overline{w}$)

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11.2.1.3 SMBus Data Bytes

All SMBus data bytes are sent most significant bit first and composed of eight bits of information.

11.2.1.4 SMBus ACK and NACK Bits

The SMBus client will acknowledge all data bytes that it receives. This is done by the client device pulling the SMBus data line low after the 8th bit of each byte that is transmitted. This applies to both the Write Byte and Block Write protocols.

By holding the SMBus data line high after the 8th data bit has been sent, the host will NACK (not acknowledge) the last data byte to be received from the client. For the Block Read protocol, the host will ACK each data byte that it receives except the last data byte.

11.2.1.5 SMBus Stop Bit

The SMBus Stop bit is defined as a transition of the SMBus data line from a logic '0' state to a logic '1' state while the SMBus clock line is in a logic '1' state. When the UCS81003 detects an SMBus Stop bit, and it has been communicating with the SMBus protocol, it will reset its client interface and prepare to receive further communications.

11.2.1.6 SMBus Timeout and Idle Reset

The UCS81003 includes an SMBus timeout feature. If the clock is held at logic '0' for $t_{TIMEOUT}$, the device can time-out and reset the SMBus interface. The SMBus interface can also reset if both the clock and data lines are held at a logic '1' for t_{IDLE_RESET}. Communication is restored with a Start condition. This functionality defaults to disabled and can be enabled by clearing the DIS_TO bit in the Emulation Configuration register (Register 10-9).

11.2.2 SMBUS AND I^{2}C COMPATIBILITY

The major differences between SMBus and I^{2}C devices are highlighted in this section. For more information, refer to the SMBus 2.0 and I^{2}C specifications.

- UCS81003 supports I^{2}C fast mode at 400 kHz. This covers the SMBus maximum time of 100 kHz.
- Minimum frequency for SMBus communications is 10 kHz.
- The SMBus client protocol will reset if the clock is held at a logic '0' for longer than 30 ms. This time-out functionality is disabled by default in the UCS81003 and can be enabled by clearing the DIS_TO bit. I^{2}C does not have a timeout.
- Except when operating in Sleep mode, the SMBus client protocol will reset if both the clock and data lines are held at a logic '1' for longer than 200 µs (idle condition). This function is disabled by default in the UCS81003 device and can be enabled by clearing the DIS_TO bit. I^{2}C does not have an idle condition.
- I^{2}C devices do not support the Alert Response Address functionality (which is optional for SMBus).
- I^{2}C devices support block read and write differently. I^{2}C protocol allows for unlimited number of bytes to be sent in either direction. The SMBus protocol requires that an additional data byte indicating number of bytes to read/write is transmitted. The UCS81003 supports I^{2}C formatting only.

11.2.3 SMBUS PROTOCOLS

The UCS81003 is SMBus 2.0-compatible and supports Write Byte, Read Byte, Send Byte, and Receive Byte as valid protocols as shown in the following sections.

All protocols in these sections use the convention in Table 11-3.

TABLE 11-3: PROTOCOL FORMAT

Data Sent to Device	Data Sent to the Host
Data sent	Data sent

11.2.3.1 SMBus Write Byte

The Write Byte is used to write one byte of data to a specific register as shown in Table 11-4.

TABLE 11-4: WRITE BYTE PROTOCOL

START	Client Address	WR	ACK	Register Address	ACK	Register Data	ACK	STOP
1 ->0	YYYY_YYY	0	0	XXh	0	XXh	0	0 -> 1

11.2.3.2 SMBus Read Byte

The Read Byte protocol is used to read one byte of data from the registers as shown in Table 11-5.

TABLE 11-5: READ BYTE PROTOCOL

START	Client Address	WR	ACK	Register Address	ACK	START	Client Address	RD	ACK	Register Data	NACK	STOP
1->0	YYYY_YYY	0	0	XXh	0	1 ->0	YYYY_YYY	1	0	XXh	1	0 -> 1

11.2.3.3 SMBus Send Byte

The Send Byte protocol is used to set the internal address register pointer to the correct address location. No data is transferred during the Send Byte protocol as shown in Table 11-6.

TABLE 11-6: SEND BYTE PROTOCOL

START	Client Address	WR	ACK	Register Address	ACK	STOP
1 -> 0	YYYY_YYY	0	0	XXh	0	0 -> 1

11.2.3.4 SMBus Receive Byte

The Receive Byte protocol is used to read data from a register when the internal register address pointer is known to be at the right location (e.g., set via Send Byte). This is used for consecutive reads of the same register as shown in Table 11-7.

TABLE 11-7: RECEIVE BYTE PROTOCOL

START	CLIENT ADDRESS	RD	ACK	Register Data	NACK	STOP
1 -> 0	YYYY_YYY	1	0	XXh	1	0 -> 1

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11.2.4 I²C PROTOCOLS

The UCS81003 supports I²C Block Read and Block Write. The protocols listed below use the convention in Table 11-3.

11.2.4.1 Block Write

The Block Write is used to write multiple data bytes to a group of contiguous registers as shown in Table 11-8.

Note:	When using the Block Write protocol, the internal address pointer will be automatically incremented after every data byte is received. It will wrap from FFh to 00h.

TABLE 11-8: BLOCK WRITE PROTOCOL

START	Client Address	WR	ACK	Register Address	ACK	Register Data	ACK
1 ->0	YYYY_YYY	0	0	XXh	0	XXh	0
Register Data	**ACK**	**Register Data**	**ACK**	**. . .**	**Register Data**	**ACK**	**STOP**
XXh	0	XXh	0	. . .	XXh	0	0 -> 1

11.2.4.2 Block Read

The Block Read is used to read multiple data bytes from a group of contiguous registers as shown in Table 11-9.

Note:	When using the Block Read protocol, the internal address pointer will be automatically incremented after every data byte is received. It will wrap from FFh to 00h.

TABLE 11-9: BLOCK READ PROTOCOL

START	Client Address	WR	ACK	Register Address	ACK	START	Client Address	RD	ACK	Register Data
1->0	YYYY_YYY	0	0	XXh	0	1 ->0	YYYY_YYY	1	0	XXh
ACK	**Register Data**	**ACK**	**Register Data**	**ACK**	**Register Data**	**ACK**	**. . .**	**Register Data**	**NACK**	**STOP**
0	XXh	0	XXh	0	XXh	0	. . .	XXh	1	0 -> 1

11.3 Stand-Alone Operating Mode

Stand-Alone mode allows the UCS81003 to operate without active SMBus/I^2C communications. Stand-Alone mode can be enabled by connecting a pull-down resistor greater or equal to 47 kΩ on the COMM_SEL/I_{LIM} pin as shown in Table 11-1.

When the device is configured to operate in Stand-Alone mode, the fault handling and Attach Detection controls are determined via the LATCH and S0 pins as shown in Table 11-10.

Note: If it is necessary to connect the S0 or LATCH pins to V_{DD} via a pull-up resistor, the pull-up resistor value should be 100 kΩ in order to guarantee V_{IH} specification. Similarly, if it is necessary to connect the S0 or LATCH pins to GND via a pull-down resistor, the pull-down resistor value should be 100 kΩ in order to guarantee V_{IL} specification.

TABLE 11-10: STAND-ALONE FAULT AND ATTACH DETECTION SELECTION

Latch Pin	S0 Pin	Command
Low	Low	No Attach Detection. Auto-Recovery upon error detection.
Low	High	Attach Detection in the Detect power state. Auto-Recovery upon error detection.
High	Low	No Attach Detection. Error states are Latched and require host to change PWR_EN control to recover from Error state.
High	High	Attach Detection in the Detect power state. Error states are Latched and require host to change PWR_EN control to recover from Error state.

In the Stand-Alone operating mode, communications from and to the UCS81003 are limited to the PWR_EN, EM_EN, M2, M1, ALERT# and A_DET# pins.

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12.0 PACKAGING INFORMATION

12.1 Package Marking Information

28-Lead VQFN (5x5x0.9 mm)

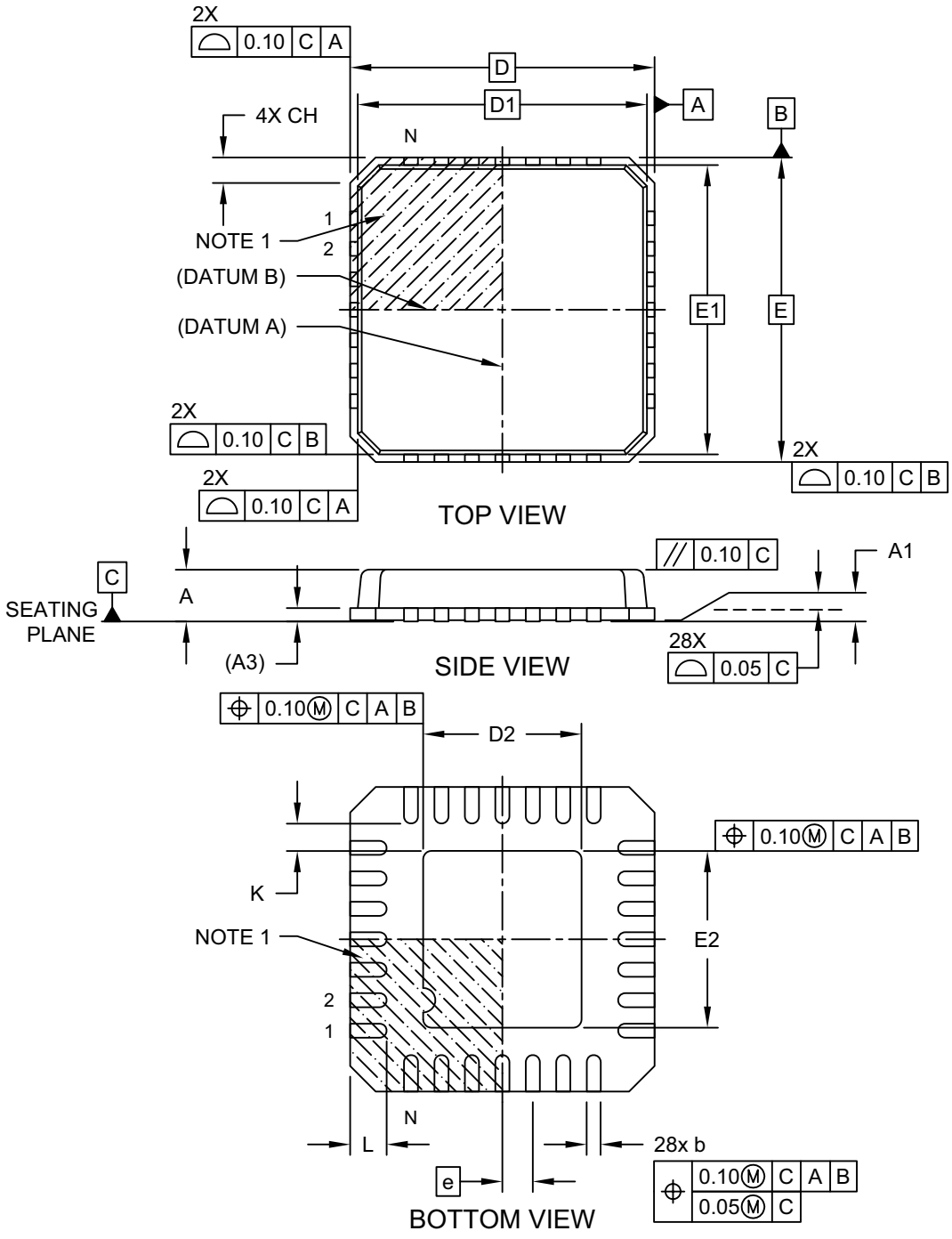
Example

Legend:	Y	Year code (last digit of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	<R>	Package
	<COO>	Country of origin
	e3	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

28-Lead Very Thin Plastic Quad Flat Pack, No Lead Package (PV) 5x5 mm Body [VQFN] With Rectangular Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



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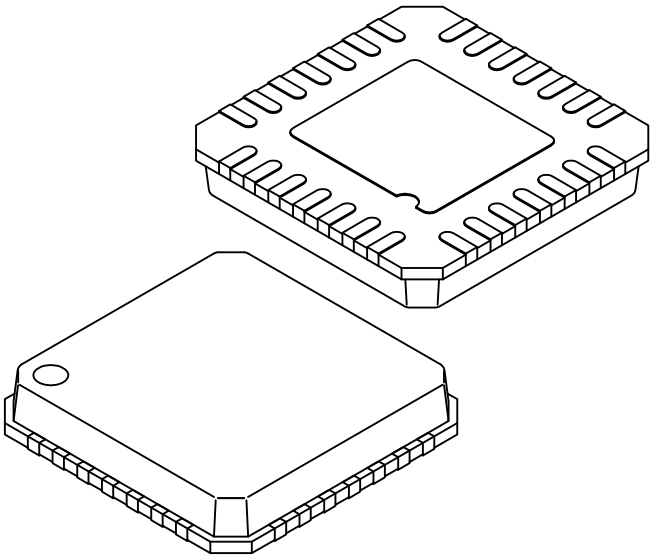

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		28	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.01	0.05
Terminal Thickness	(A3)		0.20 REF	
Overall Width	D		5.00 BSC	
Molded Cap Width	D1		4.75 BSC	
Exposed Pad Width	D2	2.50	2.60	2.70
Overall Length	E		5.00 BSC	
Molded Cap Length	E1		4.75 BSC	
Exposed Pad Length	E2	2.80	2.90	3.00
Corner Chamfer	CH	0.24	0.42	0.60
Terminal Width	b	0.18	0.23	0.30
Terminal Length	L	0.50	0.60	0.70
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is punch singulated
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

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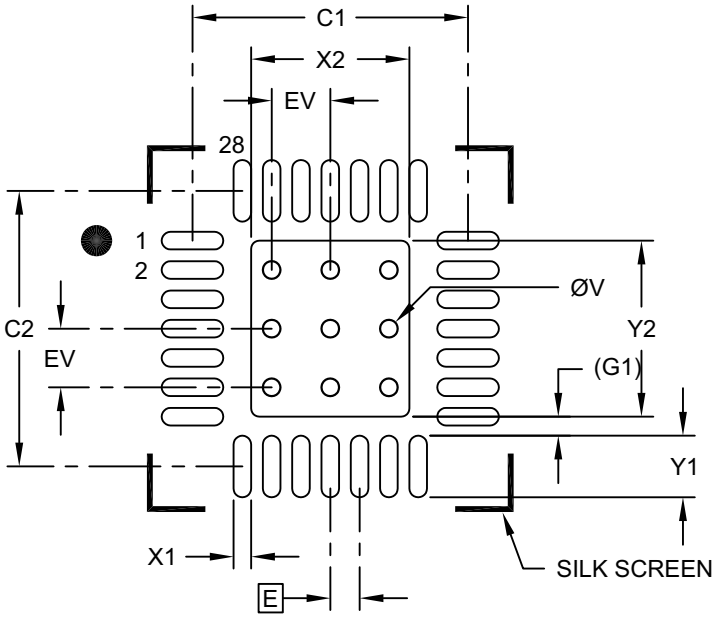
28-Lead Very Thin Plastic Quad Flat, No Lead Package (PV) - 5x5 mm Body [VQFN] With Rectangular Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			2.70
Optional Center Pad Length	Y2			3.00
Contact Pad Spacing	C1		4.70	
Contact Pad Spacing	C2		4.70	
Contact Pad Width (X28)	X1			0.30
Contact Pad Length (X28)	Y1			1.05
Contact Pad to Center Pad (X28)	(G1)		0.475 REF	
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2334A

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APPENDIX A: REVISION HISTORY

Revision A (September 2014)

- Original Release of this Document.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X](1)	-XXX
Device	Tape and Reel	Package

Device:	UCS81003AM:	Automotive USB Port Power Controller with Charger Emulation
Tape and Reel Option:	Blank =	Standard packaging (tube or tray)
	R =	Tape and Reel(1)
Package:	C1A =	Very Thin Plastic Quad Flat, No Lead Package – 5x5 mm Body with Rectangular Exposed Pad, 28-Lead (VQFN)

Examples:

a) UCS81003AM-C1A: 28-pin, 5x5 VQFN Lead-Free ROHS Compliant Package.

b) UCS81003AMR-C1A: Tape and Reel, 28-pin, 5x5 VQFN Lead-Free ROHS Compliant Package.

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip sales office for package availability for the Tape and Reel option.

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