

# NCP1855

## Product Preview

# 9 V / 2.5 A, 12 V / 2 A, Fully Integrated Li-Ion Switching Battery Charger with Power Path Management and USB On-The-Go Support

The NCP1855 is a fully programmable single cell Lithium-ion switching battery charger optimized for charging from a USB compliant input supply and AC adaptor power source. The device integrates a synchronous PWM controller, power MOSFETs, and the entire charge cycle monitoring including safety features under software supervision. An optional battery FET can be placed between the system and the battery in order to isolate and supply the system. The NCP1855 junction temperature is monitored during charge cycle and both current and voltage can be modified accordingly through I<sup>2</sup>C setting. The charger activity and status are reported through a dedicated pin to the system. The input pin is protected against overvoltages.

The NCP1855 also provides USB OTG support by boosting the battery voltage as well as providing overvoltage protected power supply for USB transceiver.

### Features

- 2.5 A Buck Converter with Integrated Pass Devices
- Input Current Limiting to Comply to USB Standard
- Automatic Charge Current for AC Adaptor Charging
- High Accuracy Voltage and Current Regulation
- Input Overvoltage Protection up to +28 V
- Factory Mode
- 1000 mA Boosted Supply for USB OTG Peripherals
- Reverse Leakage Protection Prevents Battery Discharge
- Protected USB Transceiver Supply Switch
- Dynamic Power Path with Optional Battery FET
- Silicon Temperature Supervision for Optimized Charge Cycle
- Safety Timers
- Flag Output for Charge Status and Interrupts
- I<sup>2</sup>C Control Bus up to 3.4 MHz
- Small Footprint 2.2 x 2.55 mm CSP Package
- These Devices are Pb-Free and are RoHS Compliant

### Typical Applications

- Smart Phone
- Handheld Devices
- Tablets
- PDAs

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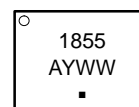
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25 BUMP  
FLIP-CHIP  
CASE 499BN

### MARKING DIAGRAM



1855 = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 25 of this data sheet.

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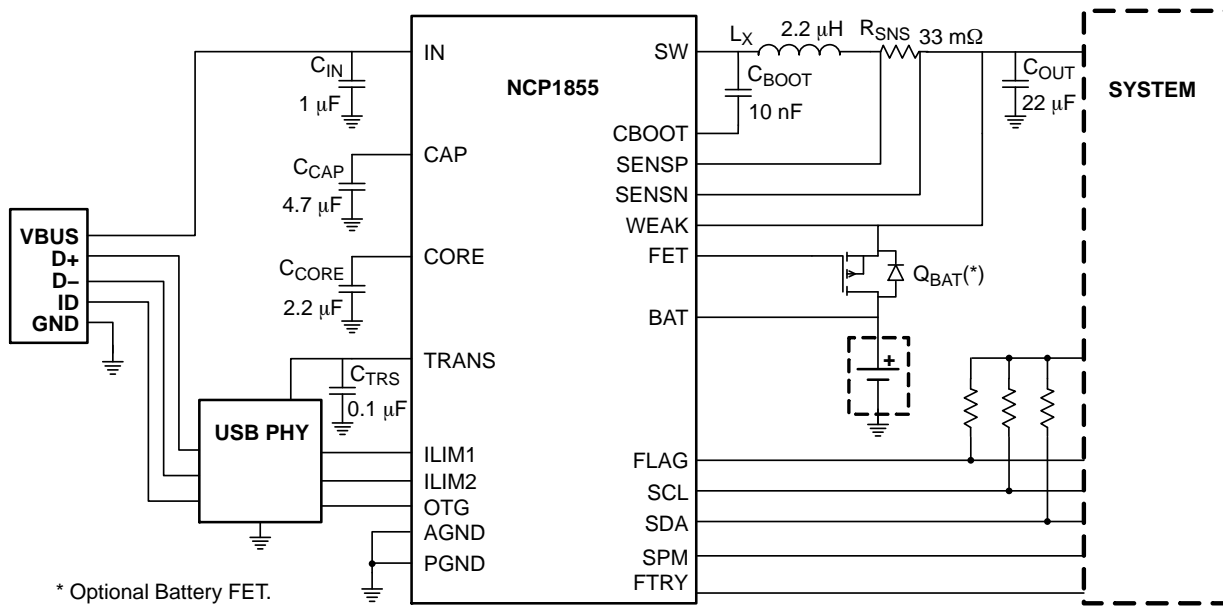
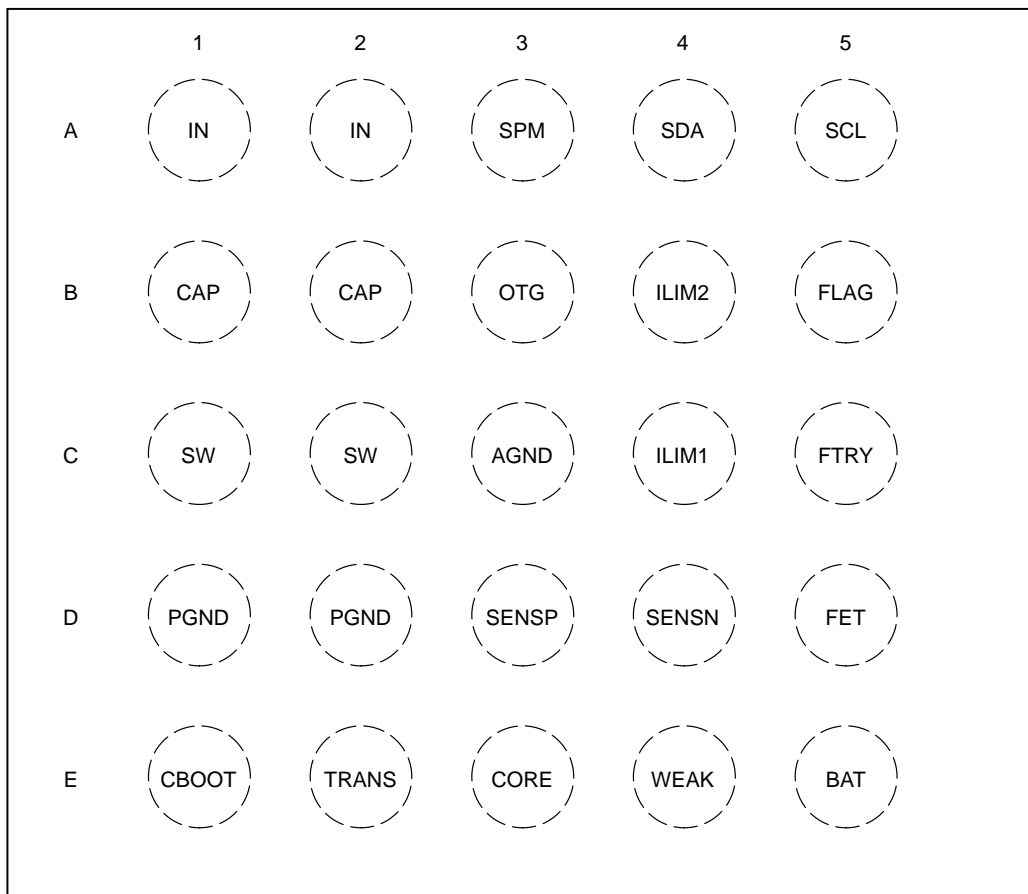


Figure 1. Typical Application Circuit

## PIN CONNECTIONS



(Top View)

Figure 2. Package Outline CSP

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**Table 1. PIN FUNCTION DESCRIPTION**

Pin	Name	Type	Description
A1	IN	POWER	Battery Charger Input. These two pins must be decoupled by at least 1 $\mu$ F capacitor and connected together.
A2	IN	POWER	
A3	SPM	DIGITAL INPUT	System Power Monitor input.
A4	SDA	DIGITAL BIDIRECTIONAL	I <sup>2</sup> C data line
A5	SCL	DIGITAL INPUT	I <sup>2</sup> C clock line
B1	CAP	POWER	CAP pin is the intermediate power supply input for all internal circuitry. Bypass with at least 4.7 $\mu$ F capacitor. Must be tied together.
B2	CAP	POWER	
B3	OTG	DIGITAL INPUT	Enables OTG boost mode. OTG = 0, the boost is powered OFF OTG = 1 turns boost converter ON
B4	ILIM2	DIGITAL INPUT	Automatic charge current / Input current limiter level selection (can be defeated by I <sup>2</sup> C).
B5	FLAG	OPEN DRAIN OUTPUT	Charging state active low. This is an open drain pin that can either drive a status LED or connect to interrupt pin of the system.
C1	SW	ANALOG OUTPUT	Connection from power MOSFET to the Inductor. These pins must be connected together.
C2	SW	ANALOG OUTPUT	
C3	AGND	ANALOG GROUND	Analog ground / reference. This pin should be connected to the ground plane and must be connected together.
C4	ILIM1	DIGITAL INPUT	Input current limiter level selection (can be defeated by I <sup>2</sup> C).
C5	FTRY	DIGITAL INPUT	Factory mode pin. Refer to section "Factory mode and no battery operation". Internally pulled up to CORE pin.
D1	PGND	POWER GND	Power ground. These pins should be connected to the ground plane and must be connected together.
D2	PGND	POWER GND	
D3	SENSP	ANALOG INPUT	Current sense input. This pin is the positive current sense input. It should be connected to the R <sub>SENSE</sub> resistor positive terminal.
D4	SENSN	ANALOG INPUT	Current sense input. This pin is the negative current sense input. It should be connected to the R <sub>SENSE</sub> resistor negative terminal. This pin is also voltage sense input of the voltage regulation loop when the FET is present and open.
D5	FET	ANALOG OUTPUT	Battery FET driver output. When not used, this pin must be directly tied to ground.
E1	CBOOT	ANALOG IN/OUT	Floating Bootstrap connection. A 10 nF capacitor must be connected between CBOOT and SW.
E2	TRANS	ANALOG OUTPUT	Output supply to USB transceiver. This pin can source a maximum of 50 mA to the external USB PHY or any other IC that needs +5 V USB. This pin is Overvoltage protected and will never be higher than 5.5 V. This pin should be bypassed by a 100 nF ceramic capacitor.
E3	CORE	ANALOG OUTPUT	5 V reference voltage of the IC. This pin should be bypassed by a 2.2 $\mu$ F capacitor. No load must be connected to this pin.
E4	WEAK	ANALOG OUTPUT	Weak battery charging current source input.
E5	BAT	ANALOG INPUT	Battery connection

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**Table 2. MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
IN (Note 1)	$V_{IN}$	-0.3 to +28	V
CAP (Note 1)	$V_{CAP}$	-0.3 to +28	V
Power balls: SW, CBOOT (Note 1)	$V_{PWR}$	-0.3 to +24	V
IN pin with respect to VCAP	$V_{IN\_CAP}$	-0.3 to +7.0	V
SW with respect to SW	$V_{SW\_CAP}$	-0.3 to +7.0	V
Sense/Control balls: SENSP, SENSN, VBAT, FET, TRANS, CORE, FLAG, INTB and WEAK. (Note 1)	$V_{CTRL}$	-0.3 to +7.0	V
Digital Input: SCL, SDA, SPM, OTG, ILIM, FTRY (Note 1)	$V_{DG}$ $I_{DG}$	-0.3 to +7.0 V	V
Input Voltage		20	mA
Input Current			
Storage Temperature Range	$T_{STG}$	-65 to +150	°C
Maximum Junction Temperature (Note 4)	$T_J$	-40 to +TSD	°C
Moisture Sensitivity (Note 5)	MSL	Level 1	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**Table 3. OPERATING CONDITIONS**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IN}$	Operational Power Supply		3.6		$V_{INOV}$	V
$V_{DG}$	Digital input voltage level		0		5.5	V
$T_A$	Ambient Temperature Range		-40	25	+85	°C
$I_{SINK}$	FLAG sink current				10	mA
$C_{IN}$	Decoupling input capacitor			1		μF
$C_{CAP}$	Decoupling Switcher capacitor			4.7		μF
$C_{CORE}$	Decoupling core supply capacitor			2.2		μF
$C_{OUT}$	Decoupling system capacitor			22		μF
$L_X$	Switcher Inductor			2.2		μH
$R_{SNS}$	Current sense resistor			33		mΩ
$R_{θJA}$	Thermal Resistance Junction to Air	(Notes 4 and 6)		70		°C/W
$T_J$	Junction Temperature Range		-40	25	+125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

1. With Respect to PGND. According to JEDEC standard JESD22-A108.
2. This device series contains ESD protection and passes the following tests:  
Human Body Model (HBM) ±2.0 kV per JEDEC standard: JESD22-A114 for all pins.  
Machine Model (MM) ±200 V per JEDEC standard: JESD22-A115 for all pins.
3. Latch up Current Maximum Rating: ±100 mA or per ±10 mA JEDEC standard: JESD78 class II.
4. A thermal shutdown protection avoids irreversible damage on the device due to power dissipation. See Electrical Characteristics.
5. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J-STD-020.
6. The  $R_{θJA}$  is dependent on the PCB heat dissipation. Board used to drive this data was a 2s2p JEDEC PCB standard.

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**Table 4. ELECTRICAL CHARACTERISTICS**

Min & Max Limits apply for  $T_A$  between  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  and  $T_J$  up to  $+125^{\circ}\text{C}$  for  $V_{IN}$  between 3.9 V to 7 V (Unless otherwise noted). Typical values are referenced to  $T_A = +25^{\circ}\text{C}$  and  $V_{IN} = 5\text{ V}$  (Unless otherwise noted).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
<b>INPUT VOLTAGE</b>							
$V_{INDET}$	Valid input detection threshold	$V_{IN}$ rising	3.8	3.85	3.9	V	
		$V_{IN}$ falling	3.55	3.6	3.65	V	
$V_{BUSUV}$	USB under voltage detection	$V_{IN}$ falling	4.3	4.4	4.5	V	
		Hysteresis	50	100	150	mV	
$V_{BUSOV}$	USB over voltage detection	$V_{IN}$ rising	5.55	5.65	5.75	V	
		Hysteresis	25	75	125	mV	
$V_{INOV}$	Valid input high threshold	$V_{IN}$ rising	15.5	15.75	16	V	
		Hysteresis	125	375	600	mV	
<b>INPUT CURRENT LIMITING</b>							
$I_{INLIM}$	Input current limit	$V_{IN} = 5\text{ V}$	Maximum Current range	100		2000	mA
			Default value	70	85	100	mA
			Accuracy from 500 mA to 2000 mA	-15		0	%
			I <sup>2</sup> C Programmable granularity (From 500 mA to 2000 mA)		100		mA
<b>INPUT SUPPLY CURRENT</b>							
$I_{Q\_SW}$	VBUS supply current	No load, Charger active state		15		mA	
$I_{OFF}$			Charger not active		500		$\mu\text{A}$
<b>CHARGER DETECTION</b>							
$V_{CHGDET}$	Charger detection threshold voltage	$V_{IN} - V_{SENSN}$ , $V_{IN}$ rising	50	110	180	mV	
		$V_{IN} - V_{SENSN}$ , $V_{IN}$ falling	20	30	50	mV	
<b>REVERSE BLOCKING CURRENT</b>							
$I_{LEAK}$	$V_{BAT}$ leakage current	Battery leakage, $V_{BAT} = 4.2\text{ V}$ , $V_{IN} = 0\text{ V}$ , $SDA = SCL = 0\text{ V}$		5		$\mu\text{A}$	
$R_{RBFET}$	Input RBFET On resistance (Q1)	Charger active state, Measured between IN and CAP, $V_{IN} = 5\text{ V}$	-	45	75	m $\Omega$	
<b>BATTERY AND SYSTEM VOLTAGE REGULATION</b>							
$V_{CHG}$	Output voltage range	Programmable by I <sup>2</sup> C	3.3		4.5	V	
		Default value		3.6		V	
	Voltage regulation accuracy	Constant voltage mode, $T_A = 25^{\circ}\text{C}$	-0.5		0.5	%	
			-1		1	%	
	I <sup>2</sup> C Programmable granularity			25		mV	
<b>BATTERY VOLTAGE THRESHOLD</b>							
$V_{SAFE}$	Safe charge threshold voltage	$V_{BAT}$ rising	2.1	2.15	2.2	V	
$V_{PRE}$	Conditioning charge threshold voltage	$V_{BAT}$ rising	2.75	2.8	2.85	V	
$V_{FET}$	End of weak charge threshold voltage	$V_{BAT}$ rising	Voltage range	3.1		3.6	V
			Default value		3.4		
			Accuracy	-2		2	%
			I <sup>2</sup> C Programmable granularity		100		mV
$V_{RECHG}$	Recharge threshold voltage	Relative to $V_{CHG}$ setting register		97		%	

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
<b>BATTERY VOLTAGE THRESHOLD</b>							
$V_{BUCKOV}$	Overvoltage threshold voltage	$V_{BAT}$ rising, relative to $V_{CHG}$ setting register, measured on SENSN or SENSP, $Q_{BAT}$ close or no $Q_{BAT}$		115		%	
		$Q_{BAT}$ open.		5		V	
<b>CHARGE CURRENT REGULATION</b>							
$I_{CHG}$	Charge current range	Programmable by I <sup>2</sup> C	450		2500	mA	
		Default value	950	1000	1050	mA	
	Charge current accuracy		-50		50	mA	
	I <sup>2</sup> C Programmable granularity			100		mA	
$I_{PRE}$	Pre-charge current	$V_{BAT} < V_{PRE}$	400	450	500	mA	
$I_{SAFE}$	Safe charge current	$V_{BAT} < V_{SAFE}$	30	40	50	mA	
$I_{WEAK}$	Weak battery charge current	BATFET present, $V_{SAFE} < V_{BAT} < V_{FET}$	$I_{WEAK}[1:0] = 01$	80	100	120	mA
			$I_{WEAK}[1:0] = 10$	180	200	220	
			$I_{WEAK}[1:0] = 11$	270	300	330	
<b>CHARGE TERMINATION</b>							
$I_{EOC}$	Charge current termination	$V_{BAT} \geq V_{RECHG}$	Current range	100		275	mA
			Default value		150		
			Accuracy, $I_{EOC} < 200\text{ mA}$	-25		25	
			I <sup>2</sup> C Programmable granularity		25		
<b>FLAG</b>							
$V_{FOL}$	FLAG output low voltage	$I_{FLAG} = 10\text{ mA}$			0.5	V	
$I_{FLEAK}$	Off-state leakage	$V_{FLAG} = 5\text{ V}$			1	$\mu\text{A}$	
$T_{FLGON}$	Interrupt request pulse duration	Single event	150	200	250	$\mu\text{s}$	
<b>DIGITAL INPUT (<math>V_{DG}</math>)</b>							
$V_{IH}$	High-level input voltage		1.2			V	
$V_{IL}$	Low-level input voltage				0.4	V	
$R_{DG}$	Pull up resistor (FRTY pin)			250		k $\Omega$	
	Pull down resistor (others pin)						
$I_{DLEAK}$	Input current	$V_{DG} = 0\text{ V}$	-0.5		0.5	$\mu\text{A}$	
<b>I<sup>2</sup>C</b>							
$V_{SYSUV}$	CAP pin supply voltage	I <sup>2</sup> C registers available	2.5			V	
$V_{I^2CINT}$	High level at SCL/SCA line		1.7		5	V	
$V_{I^2CIL}$	SCL, SDA low input voltage				0.4	V	
$V_{I^2CIH}$	SCL, SDA high input voltage		0.8* $V_{I^2CINT}$			V	
$V_{I^2COL}$	SCL, SDA low output voltage	$I_{SINK} = 3\text{ mA}$			0.3	V	
$F_{SCL}$	I <sup>2</sup> C clock frequency				3.4	MHz	

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>JUNCTION THERMAL MANAGEMENT</b>						
$T_{SD}$	Thermal shutdown	Rising	125	140	150	$^{\circ}\text{C}$
		Falling		115		$^{\circ}\text{C}$
$T_{H2}$	Hot temp threshold 2	Relative to $T_{SD}$		-7		$^{\circ}\text{C}$
$T_{H1}$	Hot temp threshold 1	Relative to $T_{SD}$		-11		$^{\circ}\text{C}$
$T_{WARN}$	Thermal warning	Relative to $T_{SD}$		-15		$^{\circ}\text{C}$
<b>BUCK CONVERTER</b>						
$F_{SWCHG}$	Switching Frequency		-	1.5	-	MHz
	Switching Frequency Accuracy		-10		+10	%
$T_{DTYC}$	Max Duty Cycle	Average		99.5		%
$I_{PKMAX}$	Maximum peak inductor current			3		A
$R_{ONLS}$	Low side Buck MOSFET $R_{DSON}$ (Q3)	Measured between PGND and SW, $V_{IN} = 5\text{ V}$	-	70	110	m $\Omega$
$R_{ONHS}$	High side Buck MOSFET $R_{DSON}$ (Q2)	Measured between CAP and SW, $V_{IN} = 5\text{ V}$	-	55	85	m $\Omega$
<b>PROTECTED TRANSCEIVER SUPPLY</b>						
$V_{TRANS}$	Voltage on TRANS pin	$V_{IN} \geq 5\text{ V}$		5	5.5	V
$I_{TRMAX}$	TRANS current capability		50			mA
$I_{TROCP}$	Short circuit protection				150	mA
<b>TIMING</b>						
$T_{WD}$	Watchdog timer			32		s
$T_{USB}$	USB timer			2048		s
$T_{CHG1}$	Charge timer	Safe-charge or pre-charge or weak-safe or weak-charge state.		3		h
$T_{CHG2}$		CC state		1		h
		CV state	TIMER_SEL = 0 (default)		2	
		TIMER_SEL = 1		1		h
$T_{WU}$	Wake-up timer			64		s
$T_{ST}$	Charger state timer, Minimum transition time from states to states	From Weak-Charge to Full-Charge State		32		s
		From wait-state to safe-charge and from weak-wait to weak-safe		127		ms
		All others state		16		ms
$T_{VRCHR}$	Deglitch time for end of charge voltage detection	$V_{BAT}$ rising		15		ms
		$V_{BAT}$ falling		127		ms
$T_{INDET}$	Deglitch time for input voltage detection	$V_{IN}$ rising		15		ms
$T_{DGS1}$	Deglitch time for signal crossing $I_{EOC}$ , $V_{PRE}$ , $V_{SAFE}$ , $V_{CHGDET}$ thresholds	Rising and falling edge		15		ms
$T_{DGS2}$	Deglitch time for signal crossing $V_{FET}$ , $V_{BUSUV}$ , $V_{BUSOV}$ thresholds	Rising and falling edge		1		ms

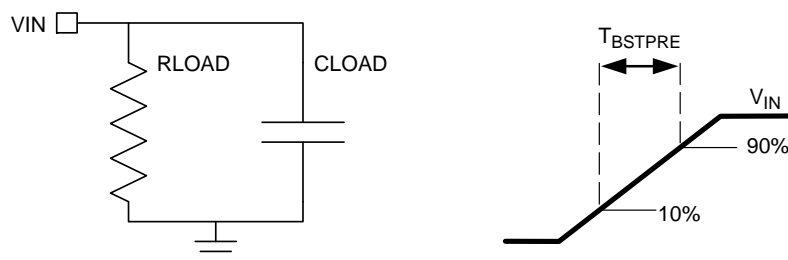
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Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
<b>BOOST CONVERTER AND OTG MODE</b>							
$V_{IBSTL}$	Boost minimum input operating range	Boost start-up	3.1	3.2	3.3	V	
		Boost running	2.9	3	3.1	V	
$V_{IBSTH}$	Boost maximum input operating range		4.4	4.5	4.6	V	
$V_{OBST}$	Boost Output Voltage	DC value measured on CAP pin, no load	5.00	5.1	5.15	V	
$V_{OBSTAC}$	Boost Output Voltage accuracy	Measured on CAP pin Including line and load regulation	-3		3	%	
$I_{BSTMX}$	Output current capability	Configured Mode	1000			mA	
		Un-configured Mode	150			mA	
$F_{SWBST}$	Switching Frequency		1.35	1.5	1.65	MHz	
$I_{BPKM}$	Maximum peak inductor current			2.5		A	
$V_{OBSTOL1}$	Boost overload	Voltage on CAP pin, falling	4.5	4.6	4.65	V	
$V_{OBSTOL2}$		Un-configured Mode, falling, Voltage on IN pin	4.3	4.4	4.5	V	
$T_{OBSTOL}$	Boost start-up time	From OTG enable to $V_{IN} > V_{OBSTOL}$			32	ms	
$I_{BSTPRE}$	Boost Pre-charge current	Un-configured Mode, Measured on IN pin RLOAD = 29 $\Omega$ , CLOAD = 10 $\mu\text{F}$			350	mA	
		Configured Mode, Measured on IN pin RLOAD = 5.1 $\Omega$ , CLOAD = 10 $\mu\text{F}$			1.1	A	
$T_{BSTPRE}$	Boost Rise time	Configured Mode, Measured on VIN, VIN rising (see Figure 3)	RLOAD = $\infty$ , CLOAD = 1 $\mu\text{F}$	0.3		4	ms
			RLOAD = 5.1 $\Omega$ , CLOAD = 10 $\mu\text{F}$				
$V_{OBSTOV}$	Overvoltage protection	$V_{IN}$ rising	5.55	5.65	5.75	V	
		Hysteresis	25	75	125	mV	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.



**Figure 3. Boost Test Schematic**



# NCP1855

## BLOCK DIAGRAM

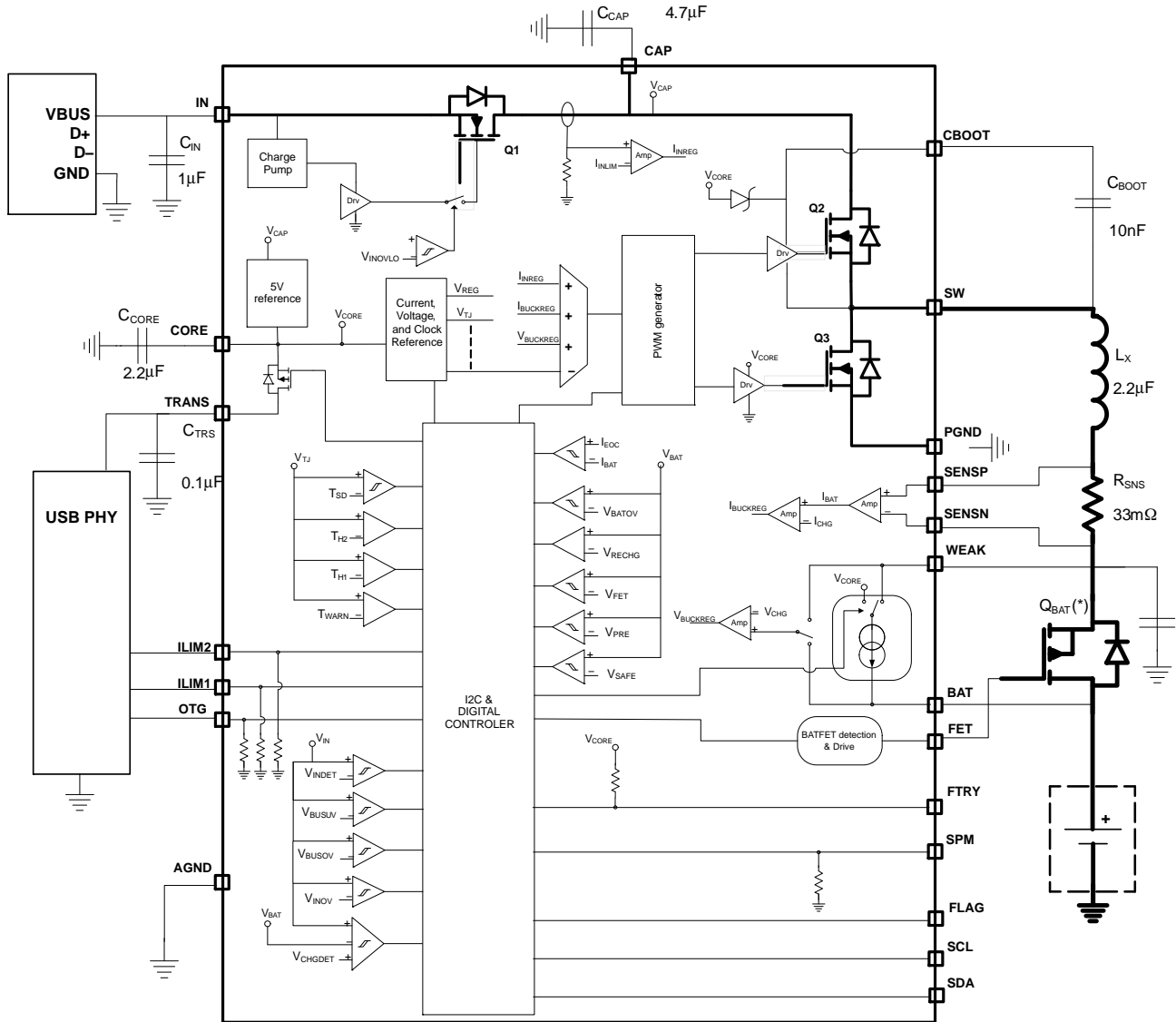
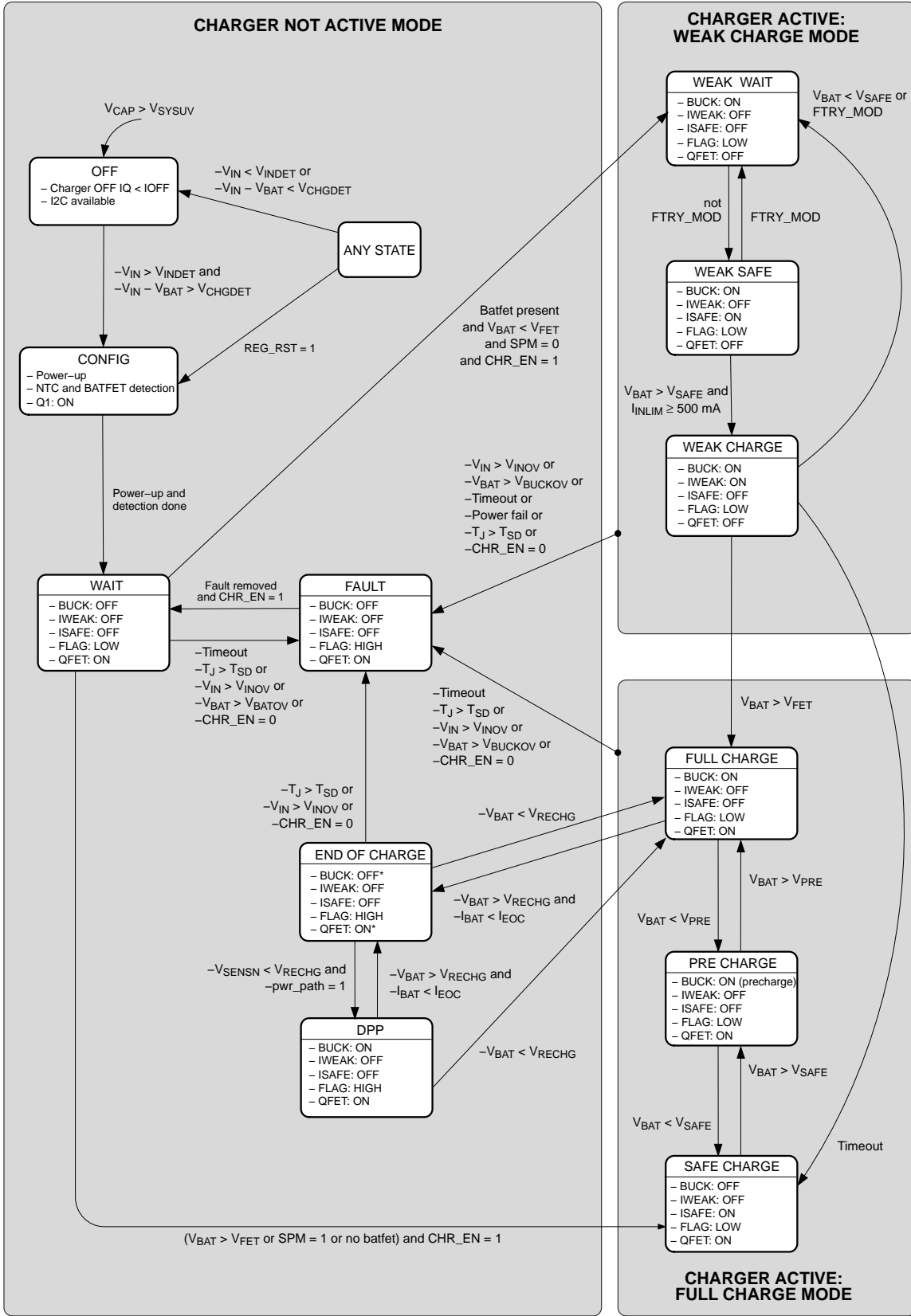


Figure 4. Block Diagram

CHARGING PROCESS



(\*) see Power Path Management section

Figure 5. Detailed Charging Process

CHARGE MODE OPERATION

Overview

The NCP1855 is a fully programmable single cell Lithium-ion switching battery charger optimized for charging from a USB compliant input supply. The device integrates a synchronous PWM controller; power MOSFETs, and monitoring the entire charge cycle including safety features under software supervision. An optional battery FET can be placed between the system and the battery in order to isolate and supply the system in case of weak battery. The NCP1855 junction temperature and battery temperature are monitored during charge cycle and current and voltage can be modified accordingly through I<sup>2</sup>C setting. The charger activity and status are reported through a dedicated pin to the system. The input pin is protected against overvoltages.

The NCP1855 is fully programmable through I<sup>2</sup>C interface (see Registers Map section for more details). All registers can be programmed by the system controller at any time during the charge process. The charge current (I<sub>CHG</sub>), charge voltage (V<sub>CHG</sub>), and input current (I<sub>INLIM</sub>) are controlled by a dynamic voltage and current scaling for disturbance reduction. Is typically 10 μs for each step.

NCP1855 also provides USB OTG support by boosting the battery voltage as well as an over voltage protected power supply for USB transceiver.

Charge Profile

In case of application without Q<sub>FET</sub>, the NCP1855 provides 4 main charging phases as described below. Unexpected behaviour or limitations that can modify the charge sequence are described further (see Charging Process section).

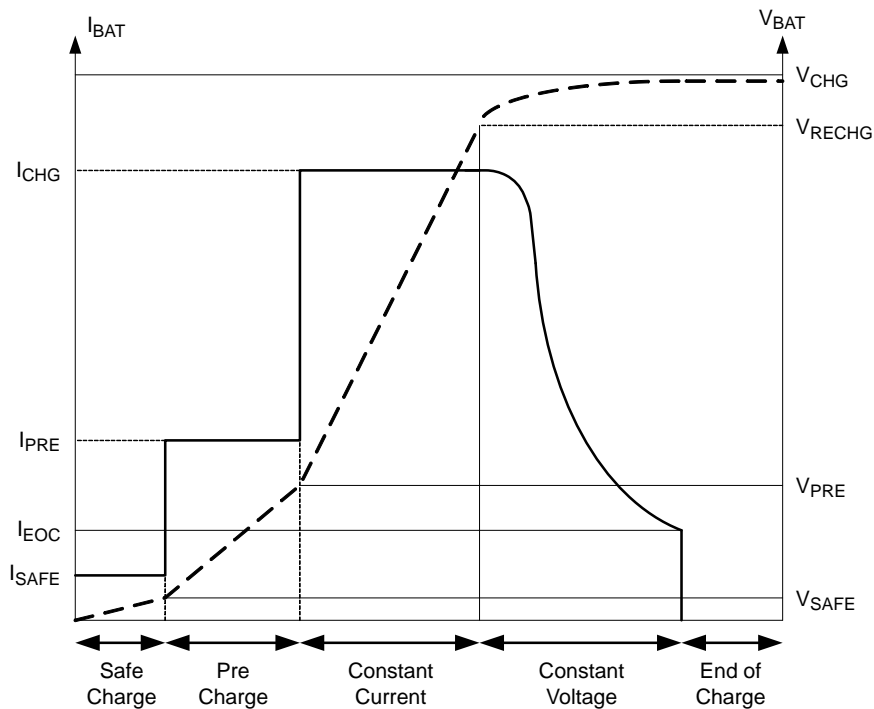


Figure 6. Typical Charging Profile of NCP1855

Safe Charge:

With a disconnected battery or completely empty battery, the charge process is in *safe charge* state, the charge current is set to I<sub>SAFE</sub> in order to charge up the system’s capacitors or the battery. When the battery voltage reaches V<sub>SAFE</sub> threshold, the battery enters in pre-conditioning.

Pre Conditioning (pre-charge):

In preconditioning (*pre charge* state), the DC-DC convertor is enabled and an I<sub>PRE</sub> current is delivered to the battery. This current is much lower than the full charge

current. The battery stays in preconditioning until the V<sub>BAT</sub> voltage is lower than V<sub>PRE</sub> threshold.

Constant Current (full charge):

In the constant current phase (*full charge* state), the DC-DC convertor is enabled and an I<sub>CHG</sub> current is delivered to the load. As battery voltage could be sufficient, the system may be awake and sink an amount of current. In this case the charger output load is composed of the battery and the system. Thus I<sub>CHG</sub> current delivered by the NCP1855 is shared between the battery and the system: I<sub>CHG</sub> = I<sub>SY</sub> + I<sub>BAT</sub>.

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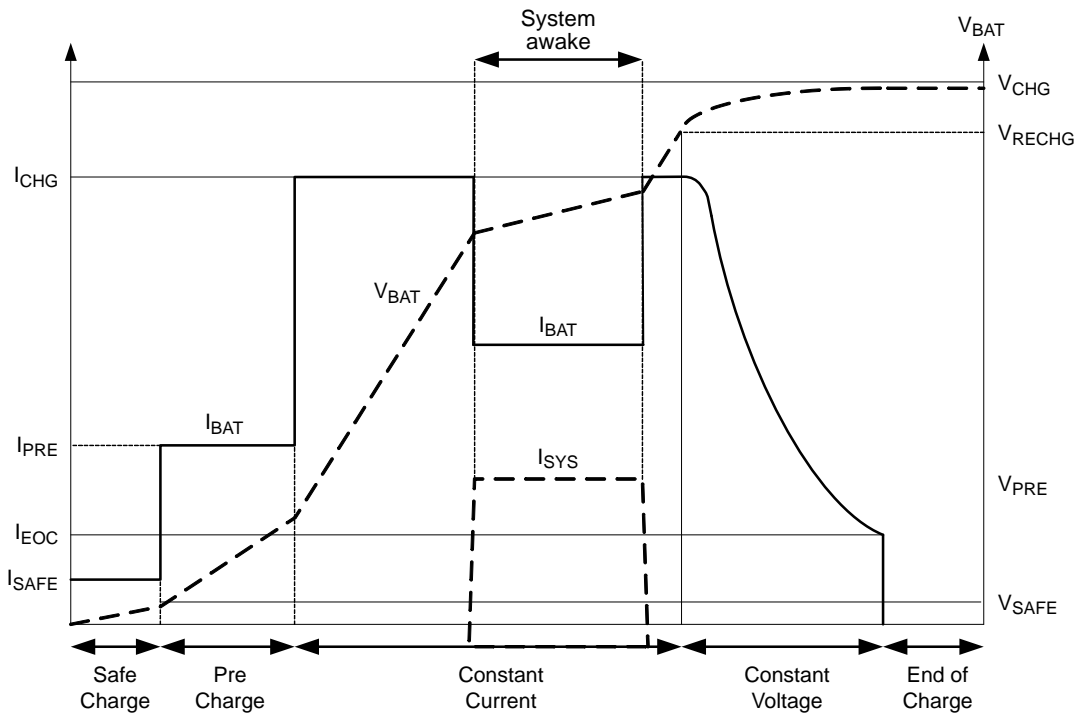


Figure 7. Typical Charging Profile of NCP1855 with System Awake

$I_{CHG}$  current is programmable using I2C interface (register `IBAT_SET` – bits `ICHG[3:0]` and `ICHG_HIGH`).

### Constant Voltage (full charge):

The constant voltage phase is also a part of the *full charge* state. When the battery voltage is close to its maximum ( $V_{CHG}$ ), the charge circuit will transition from a constant current to a constant voltage mode where the charge current will slowly decrease (taper off). The battery is now voltage controlled.  $V_{CHG}$  voltage is programmable using I2C interface (register `VBAT_SET`– bits `CTRL_VBAT[5:0]`).

### End of Charge:

The charge is completed (*end of charge* state) when the battery is above the  $V_{RECHG}$  threshold and the charge current below the  $I_{EOC}$  level. The battery is considered fully charged and the battery charge is halted. Charging is resumed in the constant current phase when the battery voltage drops below the  $V_{RECHG}$  threshold.  $I_{EOC}$  current is programmable using I2C interface (register `IBAT_SET`– bits `IEOC[2:0]`).

### Power Stage Control

NCP1855 provides a fully-integrated 1.5 MHz step-down DC-DC converter for high efficiency. For an optimized charge control, 3 feedback signals control the PWM duty cycle. These 3 loops are: maximum input current ( $I_{NLIM}$ ), maximum charge current ( $I_{CHG}$ ) and, maximum charge voltage ( $V_{CHG}$ ). The switcher is regulated by the first loop that reaches its corresponding threshold. Typically during charge current phase ( $V_{PRE} < V_{BAT} < V_{RECHG}$ ), the measured input current and output voltage are below the programmed limit and asking for more power. But in the same time, the measured output current is at the programmed limit and thus regulates the DC-DC converter.

In order to prevent battery discharge and overvoltage protection, Q1 (reverse voltage protection) and Q2 (high side N-MOSFET of the DC-DC converter) are mounted in a back-to-back common drain structure while Q3 is the low side N MOSFET of the DC-DC converter. Q2 gate driver circuitry required an external bootstrap capacitor connected between `CBOOT` pin and `SW` pin.

An internal current sense monitors and limits the maximum allowable current in the inductor to  $I_{PEAK}$  value.

### Charger Detection, Start-up Sequence and System Off

The start-up sequence begins upon an adaptor valid voltage plug in detection:  $V_{IN} > V_{INDET}$  and  $V_{IN} - V_{BAT} > V_{CHGDET}$  (*off* state).

Then, the internal circuitry is powered up and the presence of BATFET is reported (register `STATUS` – bit `BATFET`). When the power-up sequence is done, the charge cycle is automatically launched. At any time and any state, the user can hold the charge process and transit to *fault* state by setting `CHG_EN` to '0' (register `CTRL1`) in the I<sup>2</sup>C register. The I2C registers are accessible without valid voltage on  $V_{IN}$  if  $V_{CAP} > V_{SYSUV}$  (i.e. if  $V_{BAT}$  is higher than  $V_{SYSUV}$  + voltage drop across Q2 body diode).

At any time, the user can reset all register stacks (register `CTRL1` – bit `REG_RST`).

### Weak Battery Support

An optional battery FET ( $Q_{BAT}$ ) can be placed between the application and the battery. In this way, the battery can be isolated from the application and so-called weak battery operation is supported.

Typically, when the battery is fully discharged, also referred to as weak battery, its voltage is not sufficient to supply the application. When applying a charger, the battery first has to be pre-charged to a certain level before operation. During this time; the application is supplied by the DC-DC converter while integrated current sources will pre-charge the battery to the sufficient level before reconnecting.

The pin FET can drive a PMOS switch ( $Q_{BAT}$ ) connected between BAT and WEAK pin. It is controlled by the charger state machine (*Charging process* section). The basic behaviour of the FET pin is that it is always low. Thus the PMOS is conducting, except when the battery is too much discharged at the time a charger is inserted under the condition where the application is not powered on. The FET pin is always low for BAT above the  $V_{FET}$  threshold. Some exceptions exist which are described in the Charging process and *Power Path Management* section. The  $V_{FET}$  threshold is programmable (register MISC\_SET – bit CTRL\_VFET).

Batfet detection

The presence of a PMOS ( $Q_{BAT}$ ) at the FET pin is verified by the charging process during its *config* state. To distinguish the two types of applications, in case of no battery FET the pin FET is to be tied to ground. In the *config* state an attempt will be made to raise the FET pin voltage slightly up to a detection threshold. If this is successful it is considered that a battery FET is present. The batfet detection is completed for the whole charge cycle and will be done again upon unplug condition ( $V_{BAT} < V_{INDET}$  or  $V_{IN} - V_{BAT} < V_{CHGDET}$ ) or register reset (register CTRL1 – bit REG\_RST).

Weak wait

Weak wait state is entered from wait state (see Charging process section) in case of BATFET present, battery voltage lower than  $V_{FET}$  and host system in shutdown mode (SPM = 0). The DCDC converter from VIN to SW is enabled and set to  $V_{CHG}$  while the battery FET  $Q_{BAT}$  is opened. The system is now powered by the DC-DC. The internal current source to the battery is disabled.

Weak safe

The voltage at  $V_{BAT}$  is below the  $V_{SAFE}$  threshold. In *weak safe* state, the battery is charged with a linear current source at a current of  $I_{SAFE}$ . The DC-DC converter is enabled and set to  $V_{CHG}$  while the battery FET  $Q_{BAT}$  is opened. In case the ILIM pin is not made high or the input current limit defeated by I<sup>2</sup>C before timer expiration, the state is left for the *safe charge* state after a certain amount of time (see *Wake up Timer* section). Otherwise, the state machine will transition to the *weak charge* state once the battery is above  $V_{SAFE}$ .

Weak charge

The voltage at  $V_{BAT}$  is above the  $V_{SAFE}$  threshold. The DC-DC converter is enabled and set to  $V_{CHG}$ . The battery is initially charged at a charge current of  $I_{WEAK}$  supplied by a linear current source from WEAK pin (i.e. DC-DC converter) to BAT pin.  $I_{WEAK}$  value is programmable (register MISC\_SET bits IWEAK). The weak charge timer (see *Wake up Timer* section) is no longer running. When the battery is above the  $V_{FET}$  threshold (programmable), the state machine transitions to the *full charge* state thus BATFET  $Q_{BAT}$  is closed.

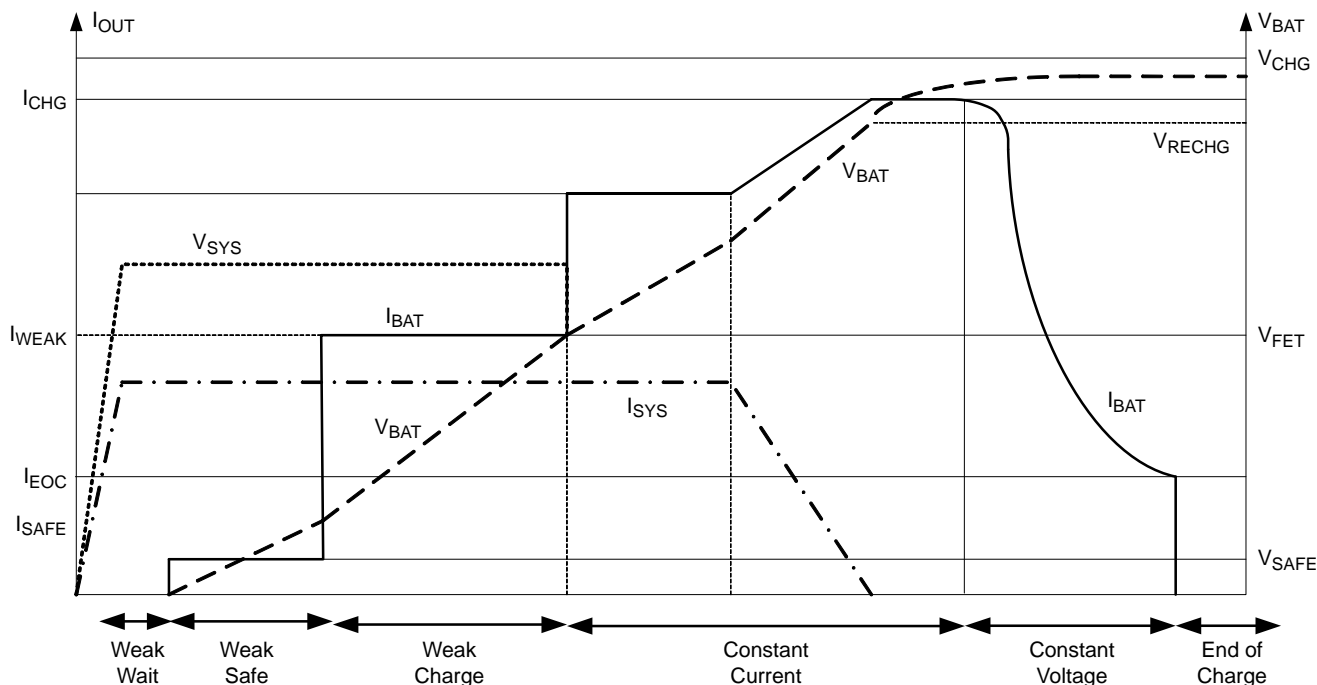


Figure 8. Weak Charge Profile

### Weak Charge Exit

In some application cases, the system may not be able to start in *weak charge states* due to current capability limitation or/and configuration of the system. If so, in order to avoid unexpected “drop and retry” sequence of the buck output, the charge state machine allows only 3 system power-up sequences based on SPM pin level: If SPM pin level is toggled 3 times during *weak charge states*, the system goes directly to *safe charge state* and a *full charge mode* sequence is initiated (“Power fail” condition in Charging process section).

### Power Path Management

Power path management can be supported when a battery FET (Q<sub>BAT</sub>) is placed between the application and the battery. When the battery is fully charged (end of charge state), power path management disconnects the battery from the system by opening Q<sub>BAT</sub>, while the DC-DC remains active. This will keep the battery in a fully charged state with the system being supplied from the DC-DC. If a load transient appears exceeding the DC-DC output current and thus causing V<sub>SENSEN</sub> to fall below V<sub>RECHG</sub>, the FET Q<sub>BAT</sub> is instantaneously closed to reconnect the battery in order to provide enough current to the application. The FET Q<sub>BAT</sub> remains closed until the end of charge state conditions are reached again. The power path management function is enabled through the I<sup>2</sup>C interface (register CTRL2 bit PWR\_PATH=1).

### Safety Timer Description

The safety timer ensures proper and safe operation during charge process. The set and reset condition of the different safety timer (Watchdog timer, Charge timer, Wakeup timer and USB timer) are detailed below. When a timer expires (condition “timeout” in Charging process section), the charge process is halted.

#### Watchdog Timer

Watchdog timer ensures software remains alive once it has programmed the IC. The watchdog timer is no longer running since I<sup>2</sup>C interface is not available. Upon an I<sup>2</sup>C write, automatically a watchdog timer T<sub>WD</sub> is started. The watchdog timer is running during *charger active states* and *fault state*. Another I<sup>2</sup>C write will reset the watchdog timer. When the watchdog times out, the state machine reverts to *fault state* and reported through I<sup>2</sup>C interface (register CHINT2- bit WDTO). Also used to time out the *fault state*. This timer can be disabled (Register CTRL2 bit WDTO\_DIS).

#### Charge Timer

A charge timer T<sub>CHG</sub> is running that will make that the overall charge to the battery will not exceed a certain amount of energy. The charge timer is running during *charger active states* and halted during *charger not active states* (see *Charging process* section). The timer can also be cleared any time through I<sup>2</sup>C (register CTRL1 – bit TCHG\_RST). The state machine transitions to *fault state* when the timer expires. This timer can be disabled (Register CTRL2 bit CHGTO\_DIS).

#### USB Timer

A USB charge timer T<sub>USB</sub> is running in the *charger active states* while halted in the *charger non active states*. The timer keeps running as long as the lowest input current limit remains selected either by ILIM pin or I<sup>2</sup>C (register I\_SET – bit IINLIM and IINLIM\_EN and register IINLIM\_SET bits IINLIM\_TA). This will avoid exceeding the maximum allowed USB charge time for un-configured connections. When expiring, the state machine will transition to *fault state*. The timer is cleared in the *off state* or by I<sup>2</sup>C command (register CTRL1 – bit TCHG\_RST).

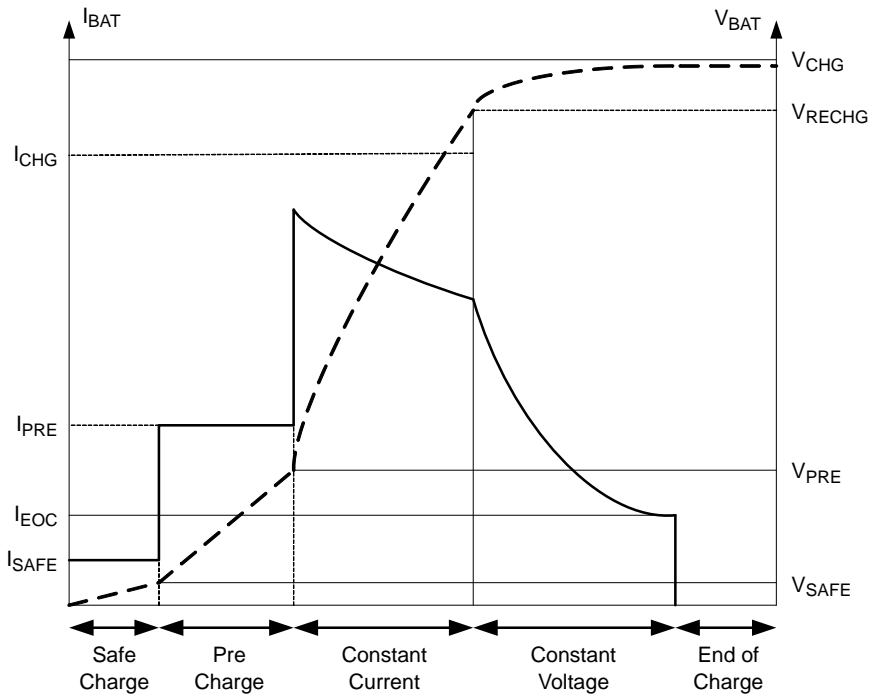
#### Wake up Timer

Before entering *weak charge state*, NCP1855 verifies if the input current available is enough to supply both the application and the charge of the battery. A wake-up timer T<sub>WU</sub> verifies if ILIM pin is raised fast enough or application powered up (by monitoring register I\_SET – bit IINLIM and IINLIM\_EN and register IINLIM\_SET bits IINLIM\_TA) after a USB attachment. The wake up timer is running in *weak wait state* and *weak safe state* and clears when the input current limit is higher than 100 mA.

### Input Current Limitation

In order to be USB specification compliant, the input current at V<sub>IN</sub> is monitored and could be limited to the I<sub>INLIM</sub> threshold. The input current limit threshold is selectable through the ILIMx pin. When low, the one unit USB current is selected (I<sub>IN</sub> ≤ 100 mA), where when made high 5 units are selected (I<sub>IN</sub> ≤ 500 mA). In addition, this current limit can be programmed through I<sup>2</sup>C (register MISC\_SET bits IINLIM and register IINLIM\_SET bits IINLIM\_TA) therefore defeating the state of the ILIMx pin. In case of non-limited input source, current limit can be disabled (register CTRL2 bit IINLIM\_EN). The current limit is valid within operating input voltage range (V<sub>INDET</sub> < V<sub>IN</sub> < V<sub>INOV</sub>).

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**Figure 9. Typical Charging Profile of NCP1855 with Input Current Limit**

### Input Voltage Based Automatic Charge Current

If the input power source capability is unknown, automatic charge current will automatically increase the charge current step by step until the  $V_{IN}$  drops to  $V_{BUSUV}$ . Upon  $V_{BUSUV}$  being triggered, the charge current  $I_{CHG}$  is immediately reduced by 1 step and stays constant until  $V_{IN}$  drops again to  $V_{BUSUV}$ . The  $I_{CHG}$  current is clamped to the I<sup>2</sup>C register value (register IBAT\_SET, bits ICHG). This unique feature is enabled when the pins ILIM1 = 0 and ILIM2 = 1 or through I<sup>2</sup>C register (register CTRL2 bit AICL\_EN).

ILIM1	ILIM2	Input Current Limit
0	0	100 mA
0	1	Automatic Charge Current
1	0	500 mA
1	1	900 mA

### Junction Temperature Management

During the charge process, NCP1855 monitors the temperature of the chip. If this temperature increases to  $T_{WARN}$ , an interrupt request (described in section Charge status reporting) is generated and bit TWARN\_SNS is set to '1' (register TEMP\_SENSE). Knowing this, the user is free to halt the charge (register CTRL – bit CHG\_EN) or reduce the charge current (register I\_SET – bits ICHG). When chip temperature reaches  $T_{SD}$  value, the charge process is automatically halted.

Between  $T_{WARN}$  and  $T_{SD}$  threshold, a junction temperature management option is available by setting 1 to TJ\_WARN\_OPT bit (register CONTROL). In this case, if the die temperature hits  $T_{M1}$  threshold, an interrupt is generated again but NCP1855 will also reduce the charge current  $I_{CHG}$  by two steps or 200 mA. This should in most cases stabilize the die temperature because the power dissipation will be reduced by approximately 50 mW. If the die temperature increases further to hit  $T_{M2}$ , an interrupt is generated and the charge current is reduced to its lowest level or 400 mA. The initial charge current will be re-established when the die temperature falls below the  $T_{WARN}$  again.

If bit TJ\_WARN\_OPT = 0 (register CTRL1), the charge current is not automatically reduced, no current changes actions are taken by the chip until  $T_{SD}$ .

### Regulated Power Supply (Trans pin)

NCP1855 has embedded a linear voltage regulator ( $V_{TRANS}$ ) able to supply up to  $I_{TRMAX}$  to external loads. This output can be used to power USB transceiver. Trans pin is enabled if  $V_{IN} > V_{BUSUV}$  and can be disabled through I<sup>2</sup>C (bit TRANS\_EN\_REG register CTRL2).

## Charge Status Reporting

### FLAG pin

FLAG pin is used to report charge status to the system processor and for interruption request.

During *charger active* states and *wait* state, the pin FLAG is low in order to indicate that the charge of the battery is in progress. When charge is completed or disabled or a fault occurs, the FLAG pin is high as the charge is halted.

### STATUS and CONTROL Registers

The status register contains the current charge state, BATFET connection as well as fault and status interrupt (bits FAULTINT and STATINT in register STATUS). The charge state (bits STATE in register STATUS) is updated on the fly and corresponds to the charging state described in Charging process section. An interruption (see description below) is generated upon a state change. In the *config* state, hardware detection is performed on BAFTET pins. From *wait* state, their statuses are available (bit BATFET in register STATUS). STATINT bit is set to 1 if an interruption appears on STAT\_INT register (see description below). FAULTINT bit is set to 1 if an interruption appears on registers CH1\_INT, CH1\_INT or BST\_INT. Thanks to this register, the system controller knows the chip status with only one I<sup>2</sup>C read operation. If a fault appears or a status change (STATINT bits and FAULTINT), the controller can read corresponding registers for more details.

### Interruption

Upon a state or status change, the system controller is informed by sensing FLAG pin. A T<sub>FLAGON</sub> pulse is generated on this pin in order to signalize an event. The level of this pulse depends on the state of the charger (see *Charging process* section):

- When charger is in *charger active* states and *wait* state the FLAG is low and consequently the pulse level on FLAG pin is high.
- In the other states, the pulse level is low as the FLAG stable level is high.

Charge state transition even and all bits of register STAT\_INT, CH1\_INT, CH2\_INT, BST\_INT generate an interrupt request on FLAG pin and can be masked with the corresponding mask bits in registers STAT\_MSK, CH1\_MSK, CH2\_MSK and BST\_MSK. All interrupt signals can be masked with the global interrupt mask bit (bit INT\_MASK register CTRL1). All these bits are read to clear. The register map (see REGISTERS MAP section) indicated the active transition of each bits (column “TYPE” in REGISTERS MAP section).

If more than 1 interrupt appears, only 1 pulse is generated while interrupt registers (STAT\_INT, CH1\_INT, CH2\_INT, BST\_INT) will not fully clear.

### Sense and Status Registers

At any time the system processor can know the status of all the comparators inside the chip by reading VIN\_SNS, VBAT\_SNS, and TEMP\_SNS registers (read only). These bits give to the system controller the real time values of all the corresponding comparators outputs (see BLOCK DIAGRAM).

### **Battery Removal**

During normal charge operation the battery may bounce or be removed. The state transition of the state machine only occurs upon deglitched signals which allow bridging any battery bounce. True battery removal will last longer than the debounce times. The NCP1855 handles battery removal if a BATFET is present and power path option is enable (register CTRL2 bit PWR\_PATH=1)

If the battery removal appears during the charge cycle, the NCP1855 will behave normally and charge up very quickly the equivalent capacitor seen on VSENSN and/or VBAT (from tens to hundreds of milliseconds). The state machine will automatically end up in *end of charge / dpp* state while the DCDC is still enabled and the system still supplied.

### **Factory Mode and No Battery Operation**

During factory testing no battery is present in the application and a supply could be applied through the bottom connector to power the application. The state machine will support this mode of operation if a BATFET is present and if the application processor can configure NCP1855 within 32 seconds. In factory mode condition, the NCP1855 is locked in weak wait state (DCDC enable and no weak charge). The factory mode is enabled through the FTRY pin or through I<sup>2</sup>C (Register CTRL1 Bit FCTRY\_MOD\_REG) according to the following logic table.

FTRY Pin	FCTRY_MOD_REG	FTRY_MODE (Factory mode)
0	0	Enable
0	1	Disable
1	0	Disable
1	1	Enable

Remark: The charge current loop (ICHG) and input current loop are disabled in factory mode so full power is available for the system.

Through I<sup>2</sup>C the device is entirely programmable so the controller can configure appropriate current and voltage threshold to handle factory testing.



## BOOST MODE OPERATION

The DC–DC Converter can also be operated in a Boost mode where the application voltage is stepped up to the input  $V_{IN}$  for USB OTG supply. The converter operates in a 1.5 MHz fixed frequency PWM mode or in pulse skipping mode under low load condition. In this mode, where CAP is the regulated output voltage, Q3 is the main switch and Q2 is the synchronous rectifier switch. While the boost converter is running, the Q1 MOSFET is conducting.

### Boost Start–up Sequence

The boost mode is enabled through the OTG pin or I<sup>2</sup>C (register CTRL1 – bit OTG\_EN). Upon a turn on request, the converter regulates CAP pin to  $V_{OBS}$  by smoothly boost up (DVS) the battery voltage while Q1 MOSFET is maintained open. The rest of the startup sequence depends on the accessory configuration:

- **Un–Configured USB port (USB\_CFG = 0)**

According to USB Spec, the maximum load that can be placed at the downstream end of a cable is 10  $\mu$ F in parallel with 29  $\Omega$ . In that case, the  $I_{BSTPRE}$  current source will precharge the IN pin to the operating voltage.

- **Configured USB port (USB\_CFG = 1)**

A configured USB OTG port should be able to provide 5 units (650 mA DC). End user can program the NCP1855 to provide the maximum current during start up in case of specific USB dual role application (register CTRL1 – bit USB\_CFG). A soft start circuitry of Q1 MOSFET will control the inrush current

### Boost Running

When running, user can change from Un–configured to configured mode on the fly and vice versa thanks to USB\_CFG bit.

### Boost Over–Voltage Protection

The NCP1855 contains integrated over–voltage protection on the  $V_{IN}$  line. During boost operation ( $V_{IN}$  supplied), if an over–voltage condition is detected ( $V_{IN} > V_{OBSOV}$ ), the controller turns off the PWM converter and a fault is indicated to the system controller (bit VBUSOV register BST\_INT).

### Boost Over–Current Protection

The NCP1855 contains over current protection to prevent the device and battery damage when  $V_{IN}$  is overloaded. When the CAP voltage drops down to  $V_{OBSOL1}$ , NCP1855 determine an over–current condition is met, so Q1 MOSFET and PWM converter are turned off. A fault is indicated to the system controller (bit  $V_{OBSOL1}$  register BST\_INT).

### Boost Over–Load Indication (Un–configured mode)

In un–configured mode, the load on IN can exceed  $I_{BSTPRE}$ . In that case, the system indicated to the user (bit  $V_{OBSOL2}$  register BST\_INT) that a more than 1 unit load is connected to the NCP1855.

This indicator can also be used to detect a device attached upon a hot plug on VIN.

### Battery Out of Range Protection

During boost mode, when the battery voltage is lower than the battery under voltage threshold ( $V_{BAT} < V_{IBSTL}$ ), or higher than the overvoltage threshold ( $V_{BAT} > V_{IBSTH}$ ), the IC turns off the PWM converter. A fault is indicated to the system controller (bit VBAT\_NOK register BST\_INT)

A toggle on OTG pin or OTG\_EN bit (register CTRL1) is needed to start again a boost operation.

### Boost Status Reporting

#### STATUS and CTRL Registers

The status register contains the boost status. Bits STATE in register STATUS gives the boost state to the system controller. Bits FAULTINT and STATINT in register STATUS are also available in boost mode. If a fault appears or a status changes (STATINT bits and FAULTINT) the processor can read corresponding registers for more details.

#### Interruption

In boost mode, valid interrupt registers are STAT\_INT and BST\_INT while CH1\_INT and CH2\_INT are tied to their reset value. Upon a state or status changes, the system controller is informed by sensing FLAG pin. Like in charge mode,  $T_{FLAGON}$  pulse is generated on this pin in order to signalize the event. The pulse level is low as the FLAG level is high in boost mode. Charge state transition even and all signals of register BST\_INT can generate an interrupt request on FLAG pin and can be masked with the corresponding mask bits in register BST\_MSK. All these bits are read to clear. The register map (see Registers Map section) indicates the active transition of each bits (column “TYPE” in see Registers Map section). If more than 1 interrupt appears, only 1 pulse is generated while interrupt registers (listed just above) will not fully clear.

#### Sense and Status Registers

At any time the system controller can know the status of all the comparator inside the chip by reading VIN\_SNS and TEMP\_SNS registers (read only). These bits give to the controller the real time values of all the corresponding comparators outputs (see Block Diagram).

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**Table 5. REGISTERS MAP**

Bit	Type	Reset	Name	RST Value	Function
<b>STATUS REGISTER – Memory location : 00</b>					
7-4	R	No_Reset	STATE[3:0]	0000	Charge mode: -0000 : OFF -0001 : WAIT + STBY -0010 : SAFE CHARGE -0011 : PRE CHARGE -0100 : FULL CHARGE -0101 : VOLTAGE CHARGE -0110 : CHARGE DONE -0111 : DPP -1000 : WEAK WAIT -1001 : WEAK SAFE -1010 : WEAK CHARGE -1011 : FAULT Boost mode: -1100 : OTG SET UP -1101 : OTG UNCONFIGURED -1110 : OTG CONFIGURED -1111 : OTG FAULT
3	R	No_Reset	BATFET	0	Indicate if a battfet is connected: 0 : No BATFET is connected 1 : BATFET is connected.
2	R	No_Reset	RESERVED	0	
1	R	No_Reset	STATINT	0	Status interrupt: 0 : No status interrupt 1 : Interruption flagged on STAT_INT register
0	R	No_Reset	FAULTINT	0	Fault interrupt: 0 : No status interrupt 1 : interruption flagged on CHRIN1, CHRIN2 or BST_INT register
<b>CTRL1 REGISTER – Memory location : 01</b>					
7	RW	OFF STATE, POR, REG_RST	REG_RST	0	Reset: 0 : No reset 1 : Reset all registers
6	RW	OFF STATE, POR, REG_RST	CHG_EN	1	Charge control: 0 : Halt charging (go to fault state) or OTG operation 1 : Charge enabled / Charge resume
5	RW	OFF STATE, POR, REG_RST, CHGMODE	OTG_EN	0	On the go enable: 0 : no OTG operation 1 : OTG operation (set by I2C or OTG pin)
4	RW	OFF STATE, POR, REG_RST, OTGMODE	FCTRY_MOD_REG	1	Factory mode (See Section Factory mode and No battery operation)
3	RW	OFF STATE, POR, REG_RST	TJ_WARN_OPT	0	Enable charge current vs Junction temperature 0 : No current change versus junction temperature 1 : Charge current is reduced when TJ is too high.
2	R	OFF STATE, POR, REG_RST	USB_CFG	1	0 : OCP between CAP and IN after boost start up done 1 : R <sub>RBFET</sub> between CAP and IN after boost start up done
1	RW	OFF STATE, POR, REG_RST, TRM_RST	TCHG_RST	0	Charge timer reset: 0 : no reset 1 : Reset and resume charge timer(tchg timer) (self clearing)
0	RW	OFF STATE, POR, REG_RST	INT_MASK	1	global interrupt mask 0 : All Interrupts can be active. 1 : All interrupts are not active

# NCP1855

**Table 5. REGISTERS MAP**

Bit	Type	Reset	Name	RST Value	Function
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**CTRL2 REGISTER – Memory location : 02**

7	RW	OFF STATE, POR, REG_RST, OTGMODE	WDTO_DIS	0	Disable watchdog timer 0: Watchdog timer enable 1: Watchdog timer disable
6	RW	OFF STATE, POR, REG_RST, OTGMODE	CHGTO_DIS	0	Disable charge timer 0: Charge timer enable 1: Charge timer disable
5	RW	OFF STATE, POR, REG_RST, OTGMODE	PWR_PATH	0	Power Path Management: 0: Power Path disable 1: Power Path enable
4	RW	OFF STATE, POR, REG_RST	TRANS_EN_REG	1	Trans pin operation enable: 0 : Trans pin is still off 1 : Trans pin is supply
3	R				Reserved
2	RW	OFF STATE, POR, REG_RST, OTGMODE	IINSET_PIN_EN	1	Enable input current set pin: 0: Input current limit and AICL control by I <sup>2</sup> C 1: Input current limit and AICL control by pins ILIMx
1	RW	OFF STATE, POR, REG_RST, OTGMODE	IINLIM_EN	1	Enable input current limit: 0: No input current limit 1: Input current limit is IINLIM[3:0]
0	RW	OFF STATE, POR, REG_RST, OTGMODE	AICL_EN	0	Enable automatic charge current: 0: No AICL 1: AICL

**STAT\_INT REGISTER – Memory location : 03**

7-6	R	No_Reset	RESERVED		
5	RCDual	OFF STATE, POR, REG_RST	TWARN	0	0 : Silicon temperature is below TWARN threshold 1 : Silicon temperature is above TWARN threshold
4	RCDual	OFF STATE, POR, REG_RST	TM1	0	0 : Silicon temperature is below T1 threshold 1 : Silicon temperature is above T1 threshold
3	RCDual	OFF STATE, POR, REG_RST	TM2	0	0 : Silicon temperature is below T2 threshold 1 : Silicon temperature is above T2 threshold
2	RCDual	OFF STATE, POR, REG_RST	TSD	0	0 : Silicon temperature is below TSD threshold 1 : Silicon temperature is above TSD threshold
1	R	No_Reset	RESERVED	0	
0	RCDual	OFF STATE, REG_RST, POR, OTGMODE	VBUSOK	0	0: charger not in USB range 1: charger in USB charging range VBUSUV < VIN < VBUSOV

**CH1\_INT REGISTER – Memory location : 04**

7-5	R	No_Reset	RESERVED	0	
4	RCDual	OFF STATE, REG_RST, POR, OTGMODE	VINLO	0	VIN changer detection interrupt: 1: VIN – VBAT > VCHGDET and VIN < VINDET
3	RCDual	OFF STATE, REG_RST, POR, OTGMODE	VINHI	0	VIN over voltage lock out interrupt: 1: VIN > VINOV
2	R	No_Reset	RESERVED	0	
1	RCDual	OFF STATE, REG_RST, POR, OTGMODE	BUCKOVP	0	VBAT over voltage interrupt: 1: VBAT > VOVP
0	R	No_Reset	CHINT2	0	charger related interrupt (CH2_INT register)

# NCP1855

**Table 5. REGISTERS MAP**

Bit	Type	Reset	Name	RST Value	Function
<b>CH2_INT REGISTER – Memory location : 05</b>					
7	R	No_Reset	RESERVED	0	
6	R	No_Reset	RESERVED	0	
5	R	No_Reset	RESERVED	0	
4	R	No_Reset	RESERVED	0	
3	RCSingle	OFF STATE, POR, REG_RST, TRM_RST, OTGMODE	WDTO	0	watchdog timeout expires interrupt: 1: 32s timer expired.
2	RCSingle	OFF STATE, POR, REG_RST, TRM_RST, OTGMODE	USBTO	0	usb timeout expires interrupt: 1: 2048s timer expired
1	RCSingle	OFF STATE, POR, REG_RST, TRM_RST, OTGMODE	CHGTO	0	charge timeout expires interrupt: 1: 3600s timer expired
0	R	No_Reset	CHINT1	0	charger related interrupt (CH1_INT register)
<b>BST_INT REGISTER – Memory location : 06</b>					
7–4	R	No_Reset	RESERVED	0000	
3	RCDual	OFF STATE, BOOST START UP STATE, POR, REG_RST, CHGMODE	VOBSTOL2	0	vbus overload interrupt: 1: Vbus voltage < V <sub>OBSTOL2</sub>
2	RCSingle	OFF STATE, POR, REG_RST, CHGMODE	VOBSTOL1	0	vbus overload interrupt: 1: VCAP voltage < V <sub>OBSTOL1</sub>
1	RCDual	OFF STATE, POR, REG_RST, CHGMODE	VBUSOV	0	vbus overvoltage interrupt: 1: Vbus voltage < V <sub>BUSOV</sub>
0	RCDual	OFF STATE, POR, REG_RST, CHGMODE	VBAT_NOK	0	vbat out of range interrupt: 1: V <sub>IBSTH</sub> < Vbat voltage < V <sub>IBSTL</sub>
<b>VIN_SNS REGISTER – Memory location : 07</b>					
7	R	No_Reset	VINOVLO_SNS	0	VIN over voltage lock out comparator 1: VIN > V <sub>INOV</sub>
6	R	No_Reset	RESERVED	0	
5	R	No_Reset	VBUSOV_SNS	0	VIN not is USB range comparator 1: VIN > V <sub>BUSOV</sub>
4	R	No_Reset	VBUSUV_SNS	0	VIN not is USB range comparator 1: VIN < V <sub>BUSUV</sub>
3	R	No_Reset	VINDET_SNS	0	VIN voltage detection comparator 1: VIN > V <sub>INDET</sub>
2	R	No_Reset	VCHGDET_SNS	0	VIN changer detection comparator 1: VIN – V <sub>BAT</sub> > V <sub>CHGDET</sub>
1	R	No_Reset	VOBSTOL2_SNS	0	VIN OTG under voltage comparator 1: Vbus voltage < V <sub>OBSTOL2</sub>
0	R	No_Reset	RESERVED	0	

# NCP1855

**Table 5. REGISTERS MAP**

Bit	Type	Reset	Name	RST Value	Function
<b>VBAT_SNS REGISTER – Memory location : 08</b>					
7	R	No_Reset	RESERVED	0	
6	R	No_Reset	VBAT_OV_SNS	0	VBAT over voltage comparator 1: VBAT > VOVP
5	R	No_Reset	VRECHG_OK_SNS	0	VBAT recharge comparator 1: VBAT > VRECHG
4	R	No_Reset	VFET_OK_SNS	0	VBAT weak charge comparator 1: VBAT > VFET
3	R	No_Reset	VPRE_OK_SNS	0	VBAT precharge comparator 1: VBAT > VPRE
2	R	No_Reset	VSAFE_OK_SNS	0	VBAT safe comparator 1: VBAT > VSAFE
1	R	No_Reset	IEOC_OK_SNS	0	End of charge current comparator 1: ICHARGE > IEOC
0	R	No_Reset	RESERVED	0	
<b>TEMP_SNS REGISTER – Memory location : 09</b>					
7	R	No_Reset	RESERVED	0	
6	R	No_Reset	RESERVED	0	
5	R	No_Reset	RESERVED	0	
4	R	No_Reset	RESERVED	0	
3	R	No_Reset	TSD_SNS	0	Chip thermal shut down comparator 1: Chip Temp > TSD
2	R	No_Reset	TM2_SNS	0	Chip thermal shut down comparator 1: Chip Temp > tm2
1	R	No_Reset	TM1_SNS	0	Chip thermal shut down comparator 1: Chip Temp > tm1
0	R	No_Reset	TWARN	0	Chip thermal shut down comparator 1: Chip Temp > twarn
<b>STAT_MSK REGISTER – Memory location : 0A</b>					
7	R	No_Reset	RESERVED	0	
6	R	No_Reset	RESERVED	0	
5	RW	OFF STATE, POR, REG_RST	TWARN_MASK	0	TWARN interruption mask bit.
4	RW	OFF STATE, POR, REG_RST	TM1_MASK	0	TM1 interruption mask bit.
3	RW	OFF STATE, POR, REG_RST	TM2_MASK	0	TM2 interruption mask bit.
2	RW	OFF STATE, POR, REG_RST	TSD_MASK	0	TSD interruption mask bit.
1	R	No_Reset	RESERVED	0	
0	RW	OFF STATE, POR, REG_RST, OTGMODE	VBUSOK_MASK	0	VBUSOK interruption mask bit.

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**Table 5. REGISTERS MAP**

Bit	Type	Reset	Name	RST Value	Function
<b>CH1_MSK REGISTER – Memory location : 0B</b>					
7–5	R	No_Reset	RESERVED	0	
4	RW	OFF STATE, POR, REG_RST, OTGMODE	VINLO_MASK	0	VINLO interruption mask bit.
3	RW	OFF STATE, POR, REG_RST, OTGMODE	VINHI_MASK	0	VINHI interruption mask bit.
2	R	No_Reset	RESERVED	0	
1	RW	OFF STATE, POR, REG_RST, OTGMODE	BUCKOVP_MASK	0	BUCKOVP interruption mask bit.
0	RW	OFF STATE, POR, REG_RST, OTGMODE	STATECHG_MASK	0	State transition interruption mask bit.
<b>CH2_MSK REGISTER – Memory location : 0C</b>					
7–4	R	No_Reset	RESERVED	0000	
3	RW	OFF STATE, POR, REG_RST, OTGMODE	WDTO_MASK	1	WDTO interruption mask bit.
2	RW	OFF STATE, POR, REG_RST, OTGMODE	USBTO_MASK	1	USBTO interruption mask bit.
1	RW	OFF STATE, POR, REG_RST, OTGMODE	CHGTO_MASK	1	CHGTO interruption mask bit.
0	R	No_Reset	RESERVED	0	
<b>BST_MSK REGISTER – Memory location : 0D</b>					
7–5	R	No_Reset	RESERVED	0	
4	RW	OFF STATE, POR, REG_RST, OTGMODE	VOBSTOL2_MASK	1	
3	RW	OFF STATE, POR, REG_RST, OTGMODE	VOBSTOL1_MASK	1	
2	RW	OFF STATE, POR, REG_RST, OTGMODE	VBUSOV_MASK	1	
1	RW	OFF STATE, POR, REG_RST, OTGMODE	VBAT_NOK_MASK	1	
0	RW	OFF STATE, POR, REG_RST, OTGMODE	STATEOTG_MASK	1	STATEOTG interruption mask bit.
<b>VBAT_SET REGISTER – Memory location : 0E</b>					
7–6	R	No_Reset	RESERVED	00	
5–0	RW	OFF STATE, POR, REG_RST, OTGMODE	CTRL_VBAT [5:0]	001100	000000: 3.3 V 001100: 3.6 V 110000: 4.5 V Step: 0.025 V
<b>IBAT_SET REGISTER – Memory location : 0F</b>					
7	RW	OFF STATE, POR, REG_RST, OTGMODE	ICHG_HIGH	0	Output current MSB: 0, ICHG[] = ICHG 1, ICHG[] = 1.6A + ICHG
6–4	RW	OFF STATE, POR, REG_RST, OTGMODE	IEOC[2:0]	010	000: 100 mA 010: 150 mA 111: 275 mA Step: 25 mA
3–0	RW	OFF STATE, POR, REG_RST, OTGMODE	ICHG[3:0]	0110	Output range current programmable range: 0000: 450 mA 1111: 1.9 A Step: 100 mA

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**Table 5. REGISTERS MAP**

Bit	Type	Reset	Name	RST Value	Function
<b>MISC_SET REGISTER – Memory location : 10</b>					
7	R				Reserved
6–5	RW	OFF STATE, POR, REG_RST, OTGMODE	IWEAK[1:0]	01	Charge current during weak battery states: 00: Disable 01: 100 mA 10: 200 mA 11: 300 mA
4–2	RW	OFF STATE, POR, REG_RST, OTGMODE	CTRL_VFET[2:0]	011	Battery to system re-connection threshold: 000: 3.1 V 001: 3.2 V 010: 3.3 V 011: 3.4 V 100: 3.5 V 101: 3.6 V
1–0	RW	OFF STATE, POR, REG_RST, OTGMODE	IINLIM[2:0]	00	Input current limit range: 00: 100 mA 01: 500 mA 10: 900 mA 11: 1500 mA
<b>IINLIM_SET REGISTER – Memory location : 11</b>					
7–4	RW	OFF STATE, POR, REG_RST, OTGMODE	IINLIM_TA[3:0]	0000	Input current limit range: 0000: IINLIM 0001: 600 mA 1111: 2000 mA Step: 100 mA

# NCP1855

## Application Information

### Bill of Material

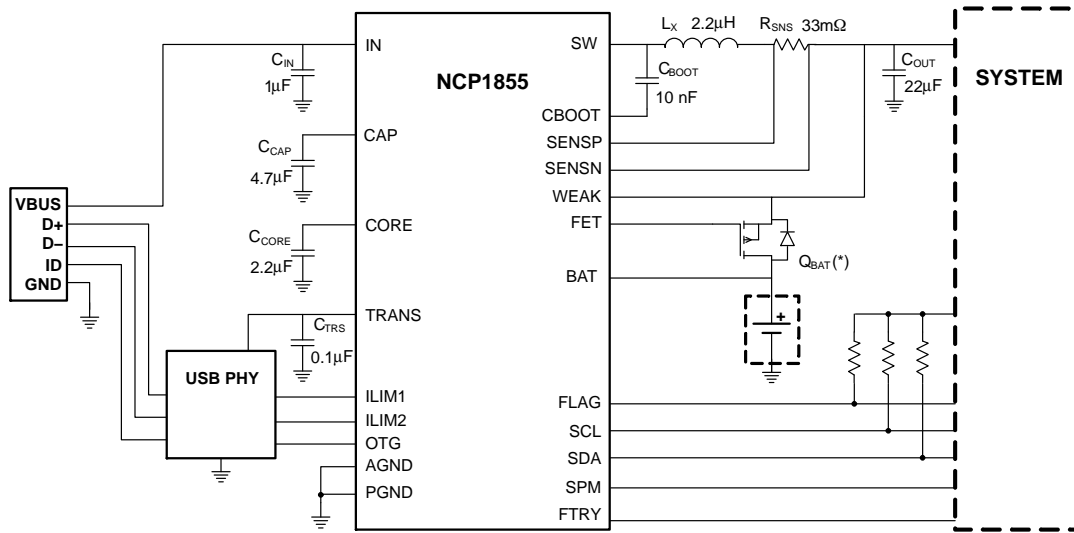


Figure 10. Typical Application Example

Item	Part Description	Ref	Value	PCB Footprint	Manufacturer	Manufacturer Reference
1	Ceramic Capacitor 25 V X5R	C <sub>IN</sub>	1 µF	0603	MURATA	GRM188R61E105K
2	Ceramic Capacitor 25 V X5R	C <sub>CAP</sub>	4.7 µF	0805	MURATA	GRM21BR61E475KA12L
3	Ceramic Capacitor 6.3 V X5R	C <sub>CORE</sub>	2.2 µF	0402	MURATA	GRM155R60J225M
4	Ceramic Capacitor 6.3 V X5R	C <sub>TRS</sub>	0.1 µF	0402	MURATA	GRM155R60J104K
5	Ceramic Capacitor 10 V X5R	C <sub>BOOT</sub>	10 nF	0402	MURATA	GRM155R60J103K
6	Ceramic Capacitor 6.3 V X5R	C <sub>OUT</sub>	22 µF	0603	MURATA	GRM31CR60J226K
7	SMD Inductor	L <sub>X</sub>	2.2 µH	3012	TDK	SPM3012T-2R2M
8	SMD Resistor 0.25 W, 1%	R <sub>SNS</sub>	33 mΩ	0805	YAGEO	RL0805FR-7W0R033L
9	Power channel P-MOSFET	Q <sub>BAT</sub>	18 mΩ	UDFN 2*2mm	ONSEMI	NTLUS3A18PZ

### PCB Layout Consideration

Particular attention must be paid with C<sub>CORE</sub> capacitor as it's decoupling the supply of internal circuitry including gate driver. This capacitor must be placed between CORE pin and PGND pin with a minimum track length.

The high speed operation of the NCP1855 demands careful attention to board layout and component placement. To prevent electromagnetic interference (EMI) problems, attention should be paid specially with components L<sub>X</sub>, C<sub>CAP</sub>, and C<sub>OUT</sub> as they constitute a high frequency current loop area. The power input capacitor C<sub>CAP</sub>, connected from CAP to PGND, should be placed as close as possible to the NCP1851. The output inductor L<sub>X</sub> and the output capacitor C<sub>OUT</sub> connected between R<sub>SNS</sub> and PGND should be placed close to the IC. C<sub>IN</sub> capacitor should also be placed as close as possible to IN and PGND pin as well.

The high current charge path through IN, CAP, SW, inductor L<sub>1</sub>, Resistor R<sub>1</sub>, optional BAFET, and battery pack must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces. An I<sub>WEAK</sub> current can flow through WEAK and BAT traces which defines the appropriate track width.

It's suggested to keep as complete ground plane under NCP1854 as possible. PGND and AGND pin connection must be connected to the ground plane.

Care should be taken to avoid noise interference between PGND and AGND. Finally it is always good practice to keep the sensitive tracks such as feedbacks connections (SENSEP, SENSNS, BAT) away from switching signal connections by laying the tracks on the other side or inner layer of PCB.



# NCP1855

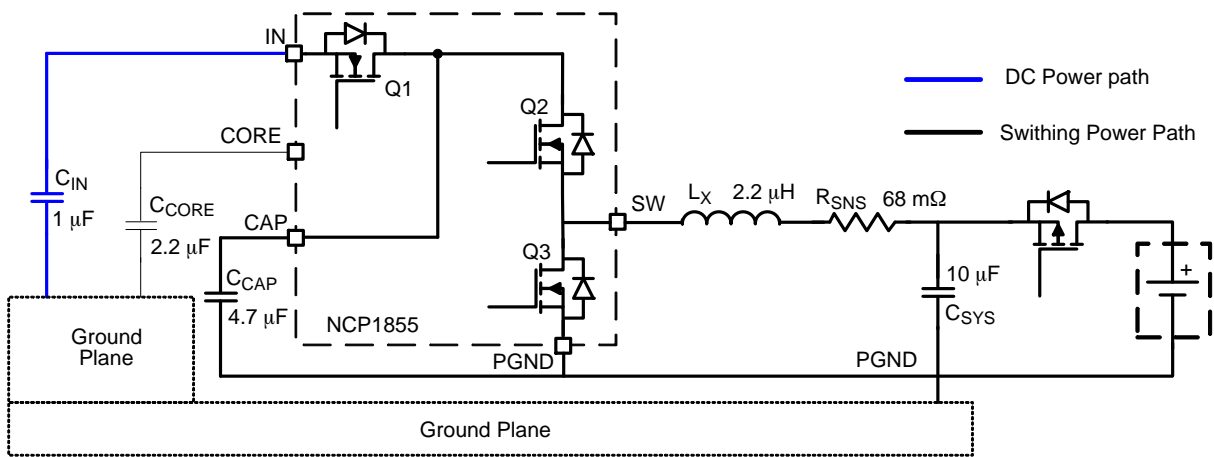


Figure 11. Power Path

It's suggested to use multiple layers (usually 2) under the power balls of the IC to reduce thermal heating to due to contact resistance between CSP and PCB.

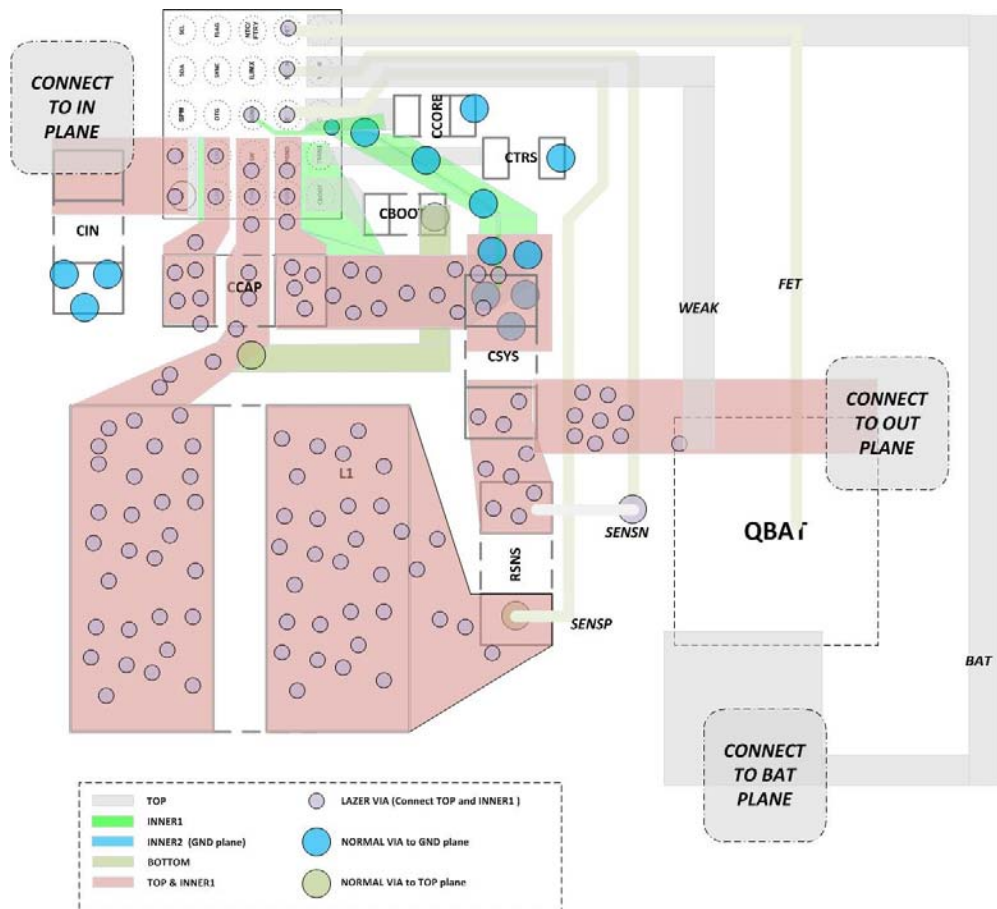


Figure 12. Layout Example

## ORDERING INFORMATION

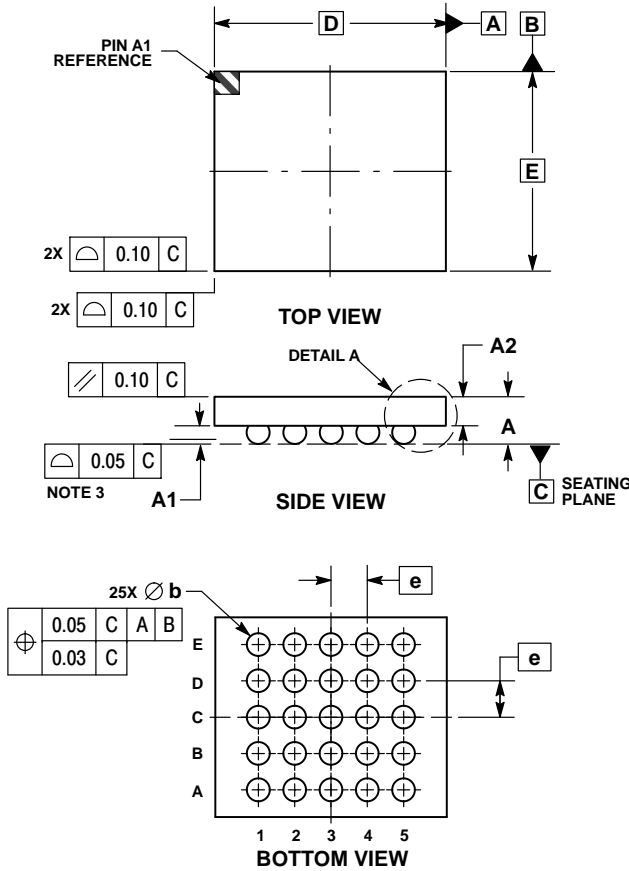
Device Order Number	I <sup>2</sup> C address	Marking	Shipping <sup>†</sup>
NCP1855FCCT1G	6C	1855	3000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NCP1855

## PACKAGE DIMENSIONS

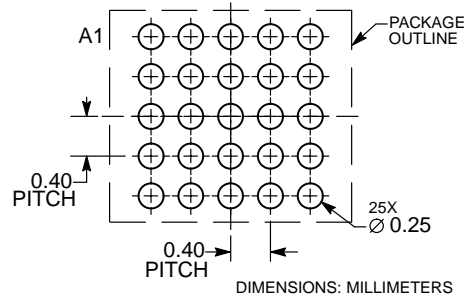
25 Pin Flip-Chip, 2.55x2.20  
CASE 499BN  
ISSUE A



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETERS.
  3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

MILLIMETERS		
DIM	MIN	MAX
A	---	0.60
A1	0.17	0.23
A2	0.36 REF	
A3	0.04 REF	
b	0.24	0.29
D	2.55 BSC	
E	2.20 BSC	
e	0.40 BSC	

### RECOMMENDED SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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