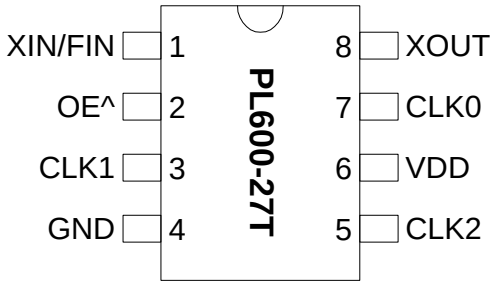
PL600-27T

Low Power 3 Output XO

FEATURES

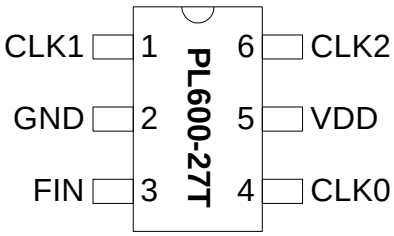
- 3 LVCMOS outputs with OE tri-state control
- Low current consumption:
  - <4.5mA @ 27MHz, 3.3V
- 10 to 52MHz fundamental crystal input
- 1 to 100MHz reference clock input
- Accepts both LVCMOS and sine wave inputs
- Low phase noise (-130 dBc @ 10kHz offset)
- Low jitter (RMS): 2.5ps period jitter
- 12mA drive capability at TTL output
- 1.8V to 3.3V operation
- Available in GREEN/RoHS 8-pin SOP and 6-pin SOT23 packages

PIN ASSIGNMENT



SOP-8L

^: Denotes internal Pull-up

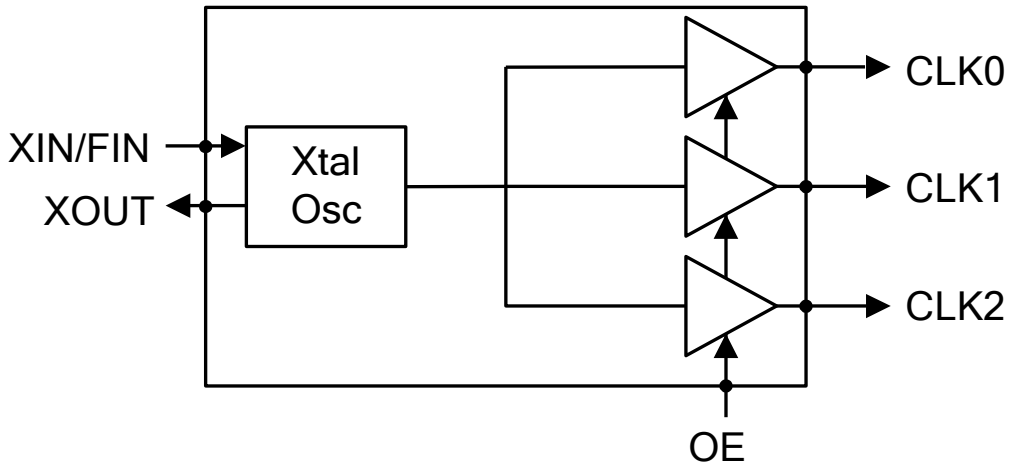


SOT23-6L

DESCRIPTION

The PL600-27T is a low cost XO IC, designed to replace multiple XO solutions saving the cost and board space of clock distribution buffers. In addition, it provides among the lowest current on the market for the 10MHz to 52MHz range. The PL600-27T accepts crystal and clock inputs from 10 to 52MHz (fundamental resonant mode crystal) and provides low phase noise (<-130dBc at 10kHz offset at 30MHz), and very low jitter (2.5 ps RMS period jitter) outputs.

BLOCK DIAGRAM



PIN DESCRIPTION

Name	Package Pin Number		Type	Description
	SOP-8L	SOT23-6L		
XIN/FIN	1	3 (FIN Only)	I	Crystal input (10MHz to 52MHz) or Ref Clock input (1MHz to 100MHz)
OE	2	-	I	Output Enable input. This pin has internal pull-up resistor. All outputs will be tri-stated when low.
CLK1	3	1	O	Output clock.
GND	4	2	P	Ground.
CLK2	5	6	O	Output clock.
VDD	6	5	P	Power supply.
CLK0	7	4	O	Output clock.
XOUT	8	-	I	Crystal output.

ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		4.6	V
Input Voltage, dc	V_I	-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	-0.5	V_{DD}+0.5	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature*	T_A	-40	85	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C
ESD Protection, Human Body Model			2	kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the dev ice at these or any other conditions above the operational limits noted in this specification is not implied. *Operating temperature is guaranteed by design. Parts are tested to commercial grade only.

2. AC Electrical Specifications

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Crystal Frequency		10		52	MHz
Input (FIN) Frequency	LVCMOS or Sine Wave input	1		100	MHz
Input (FIN) Signal Amplitude	Internally AC coupled (High Frequency)	0.5		V_{DD}	Vpp
Input (FIN) Signal Amplitude	Internally AC coupled (Low Frequency) 3.3V ≤50MHz, 2.5V ≤40MHz, 1.8V ≤15MHz	0.1		V_{DD}	Vpp
Settling Time	At power-up (V_{DD} ≤ 1.62V)			10	ms
Output Clock Rise/Fall Time	0.8V ~ 2.0V with 10 pF load		1.15		ns
	0.3V ~ 3.0V with 15 pF load		2.4		
VDD sensitivity	Frequency vs. V_{DD} +/- 10%	0.8		0.8	ppm
Output Clock Duty Cycle	Measured @ 50% V_{DD}	45	50	55	%
Short Circuit Current			±50		mA

3. Jitter and Phase Noise Specifications

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
RMS Period Jitter (1 sigma – 1000 samples)	With capacitive decoupling between V_{DD} and GND.		2.1	2.5	ps
Phase Noise relative to carrier	30MHz @100Hz offset		-80		dBc/Hz
Phase Noise relative to carrier	30MHz @1kHz offset		-110		dBc/Hz
Phase Noise relative to carrier	30MHz @10kHz offset		-130		dBc/Hz
Phase Noise relative to carrier	30MHz @100kHz offset		-138		dBc/Hz
Phase Noise relative to carrier	30MHz @1MHz offset		-145		dBc/Hz

4. DC Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current, Dynamic, with Loaded Outputs (at VDD = 3.3V)	I_{DD}	At 10MHz, Cload=15pF		2.0	2.5	mA
		At 27MHz, Cload=15pF		4.0	4.5	
		At 48MHz, Cload=15pF		7.0	7.5	
Supply Current in Tri-State	I_{DD}	Output disabled			520	µA
Operating Voltage	V_{DD}		1.62		3.63	V
Output High Voltage	V_{OH}	I_{OH} = -12mA (3.3V)	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 12mA (3.3V)			0.4	V
Output High Voltage	V_{OHC}	I_{OH} = -4mA	V_{DD} – 0.4			V
Output Drive Current		At TTL level (3.3V)	12			mA

5. Crystal Specifications

PARAMETERS	SYMBOL	MIN.	TYP.	MAX.	UNITS
Crystal Resonator Frequency	F_{XIN}	10		52	MHz
Crystal Loading Rating	$C_{L\ (xtal)}$		8.5		pF
Maximum Sustainable Drive Level				200	µW
Operating Drive Level			50		µW
C0 (for frequencies below 30MHz)				5	pF
C0 (for frequencies above 30MHz)				4	pF
ESR	R_S			30	Ω

LAYOUT RECOMMENDATIONS

The following guidelines are to assist you with a performance optimized PCB design:

Signal Integrity and Termination Considerations

- Keep traces short!

- Trace = Inductor. With a capacitive load this equals ringing!

- Long trace = Transmission Line. Without proper termination this will cause reflections (looks like ringing).

- Design long traces (> 1 inch) as "striplines" or "microstrips" with defined impedance.

- Match trace at one side to avoid reflections bouncing back and forth.

Decoupling and Power Supply Considerations

- Place decoupling capacitors as close as possible to the VDD pin(s) to limit noise from the power supply

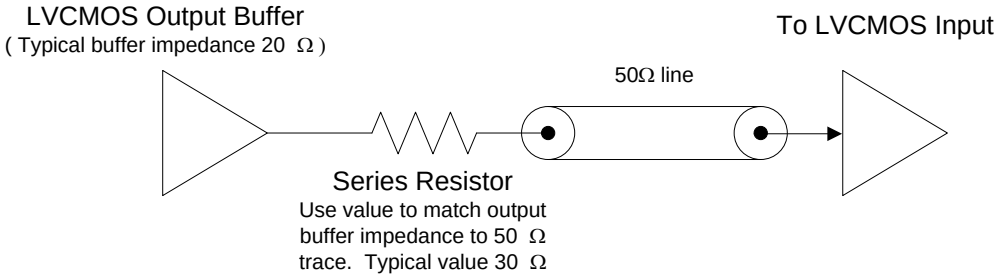
- Multiple VDD pins should be decoupled separately for best performance.

- Addition of a ferrite bead in series with VDD can help prevent noise from other board sources

- Value of decoupling capacitor is frequency dependant. Typical values to use are 0.1μF for designs using frequencies < 50MHz and 0.01μF for designs using frequencies > 50MHz.

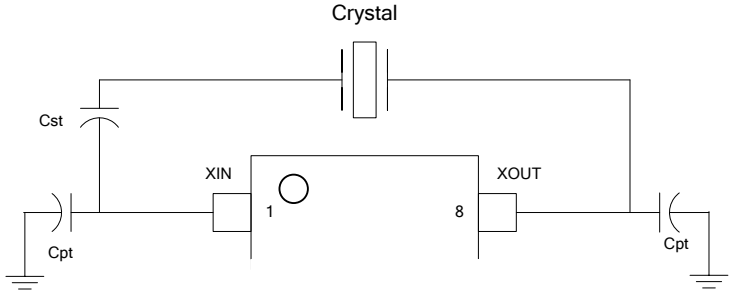
Typical LVCMOS termination

Place Series Resistor as close as possible to LVCMOS output



Crystal Tuning Circuit

Series and parallel capacitors used to fine tune the crystal load to the circuit load.



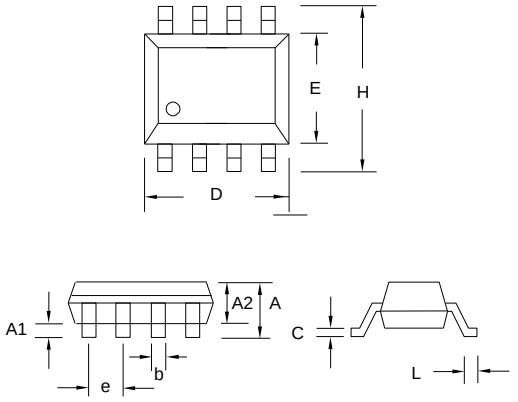
CST – Series Capacitor, used to lower circuit load to match crystal load. Raises frequency offset. This can be eliminated by using a crystal with a Cload of equal or greater value than the oscillator.

CPT – Parallel Capacitors, Used to raise the circuit load to match the crystal load. Lowers frequency offset.

PACKAGE DRAWINGS (GREEN PACKAGE COMPLIANT)

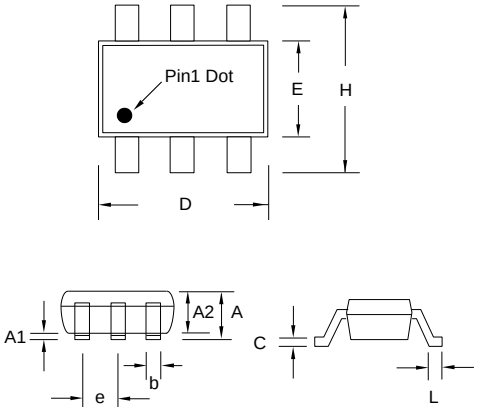
SOP-8L

Symbol	Dimension in MM	
	Min.	Max.
A	1.35	1.75
A1	0.10	0.25
A2	1.25	1.50
B	0.33	0.53
C	0.19	0.27
D	4.80	5.00
E	3.80	4.00
H	5.80	6.20
L	0.40	0.89
e	1.27 BSC	



SOT23-6L

Symbol	Dimension in MM	
	Min.	Max.
A	1.05	1.35
A1	0.05	0.15
A2	1.00	1.20
b	0.30	0.50
c	0.08	0.20
D	2.80	3.00
E	1.50	1.70
H	2.60	3.00
L	0.35	0.55
e	0.95 BSC	



ORDERING INFORMATION (GREEN PACKAGE COMPLIANT)

For part ordering, please contact our Sales Department:
2180 Fortune Drive, San Jose, CA 95131, USA
Tel: (408) 944-0800 Fax: (408) 474-1000

PART NUMBER
The order number for this device is a combination of the following:
Part number, Package type and Operating temperature range

PL600-27T X X X

Part Number

Shipping Option
Blank=Tube
R=Tape & Reel

Package Type
S=SOP-8L
T=SOT23-6L

Temperature Range
C=Commercial (0°C to 70°C)
I=Industrial (-40°C to 85°C)

Part / Order Number	Marking	Package Option
PL600-27TSC	P600-27T SC LLLLL	8-Pin SOP (Tube)
PL600-27TSC-R		8-Pin SOP (Tape and Reel)
PL600-27TSI	P600-27T SI LLLLL	8-Pin SOP (Tube)
PL600-27TSI-R		8-Pin SOP (Tape and Reel)
PL600-27TTC-R	A27T LLL	6-Pin SOT23 (Tape and Reel)
PL600-27TTI-R	A27T LLLI	6-Pin SOT23 (Tape and Reel)

† **Marking Notes :**
LLL and LLLLL represent the production lot number