Ordering number : ENA2010

SANYO Semiconductors
DATA SHEET

An ON Semiconductor Company

LC08101CT — Bi-CMOS IC Shaft Slide Actuator Driver IC

Overview

The LC08101CT is a Shaft Slide Actuator Driver IC.

Features

The shaft slide actuator can be driven simply by I^2C communication.
Constant current control is exercised for the output of the supply to suppress the fluctuation in the coil current due to the temperature fluctuations.

- The drive conditions can be set externally using serial input through the I^2C interface.
  The kick-pulse width and brake-pulse width are set using the clock count.
- ENIN input that controls the startup/stop of the IC.
- The time for which the actuator is driven is determined with the drive frequency setting based on I^2C communication.
- Provides a busy signal output during periods when the actuator is being driven by OUT pin output so that applications can be aware of the actuator operating/stopped state.
- Built-in oscillator circuit (1 MHz typical). Capable of switching to an external clock.
- Separate drive waveforms can be set in steps, i.e., when the actuator is activated, stopped and subjected to braking.
- Built-in thermal protection function, reduced voltage detection/protection circuits, and register power-on reset function

Specifications

Absolute Maximum Ratings at Ta = 25°C, SGND = PGND = 0V

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC} max		-0.5 to 4.0	V
Output current	I_O max		300	mA
Input signal voltage	V_{IN} max	SCL/SDA/CLK/WP	-0.5 to V_{CC}+0.5	V
Allowable power dissipation	Pd max	*Mounted on a specified board.	650	mW
Operating temperature	Topr		-30 to +85	°C
Storage temperature	Tstg		-55 to +150	°C

*: When mounted on the specified printed circuit board (50mm ×50mm ×1.6mm), glass epoxy board

Caution 1) Absolute maximum ratings represent the value which cannot be exceeded for any length of time.

Caution 2) Even when the device is used within the range of absolute maximum ratings, as a result of continuous usage under high temperature, high current, high voltage, or drastic temperature change, the reliability of the IC may be degraded. Please contact us for the further details.

Allowable Operating Conditions at Ta = 25°C, SGND = PGND = 0V

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC}		2.2 to 3.6	V
Input signal voltage	V_{IN}		-0.3 to V_{CC}	V
Corresponding CLK input frequency	Fclk		to 60	MHz
Maximum operating frequency	Ct max		Set STP count × 512	Times

Electrical Characteristics at Ta = 25°C, V_{CC} = 2.8V, SGND = PGND = 0V, unless otherwise specified.

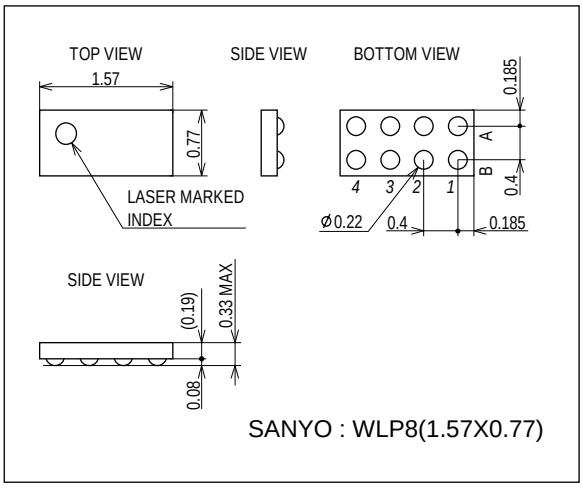
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Standby mode current drain	$I_{CC}0$	CLK/SCL/SDA=0V, When ENIN=0			1.0	μA
Operating mode current drain for driber area	$I_{CC}1$	Internal oscillator movement SCL/SDA=0, When ENIN=1		0.65	1.0	mA
High-level input voltage	V_{IH}	2.2V ≤ V_{CC} ≤ 3.3V SCL, SDA	1.4		V_{CC}+0.3	V
Low-level input voltage	V_{IL}	2.2V ≤ V_{CC} ≤ 3.3V SCL, SDA	-0.3		0.3	V
CLK pin high-level input voltage	$V_{IH}2$	CLK	0.45×V_{CC}		V_{CC}+0.3	V
CLK pin low-level input voltage	$V_{IL}2$	CLK	-0.3		0.2×V_{CC}	V
Internal oscillator dispatch frequency	Fclk	It is calculated by an output wave pattern	0.80	0.95	1.20	MHz
Output constant current	$I_{O}C1$	I_{OUT} register D3 to D0 = 1010	95	105	115	mA
	$I_{O}C2$	I_{OUT} register D3 to D0 = 0000	190	210	230	mA
Reduced voltage protection detection voltage	Vres	V_{CC} voltage	1.8	2.0	2.2	V
Output block upper-side on resistance	RonP	I include a current current sense resistor		1.35	1.545	Ω
Output block lower-side on resistance	RonN			0.4	0.55	Ω
Turn on time	TPLH	With no load *1		0.1	0.25	μS
Turn off time	TPHL	With no load *1		0.03	0.1	μS

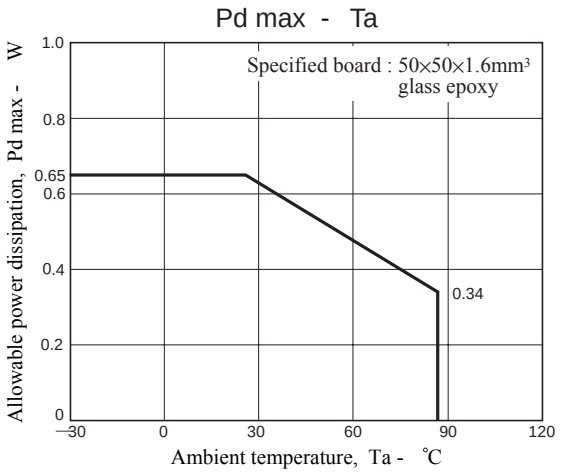
*1 : Rising time from 10 to 90% and falling time from 90 to 10% are specified with regard to the OUT pin voltage.

Package Dimensions

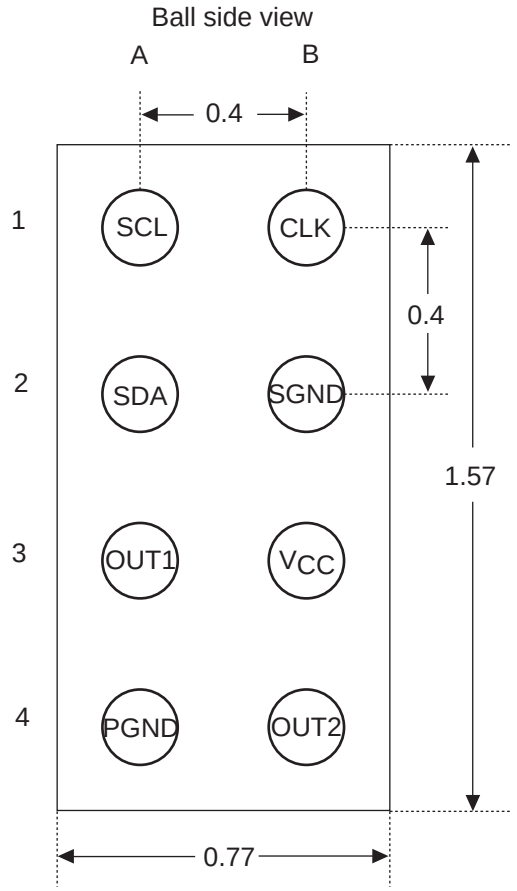
unit : mm (typ)

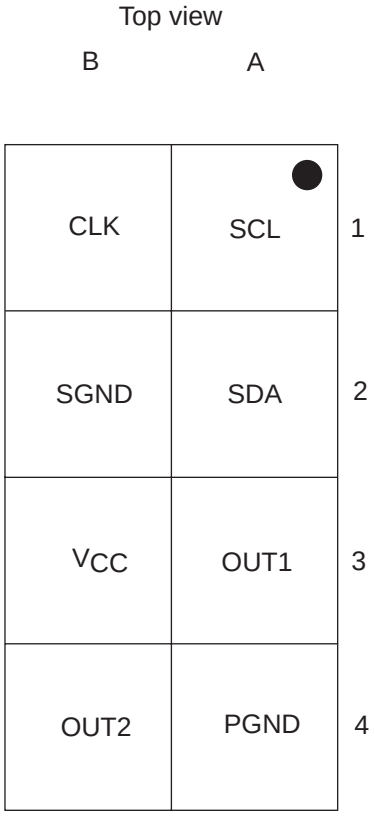
3423





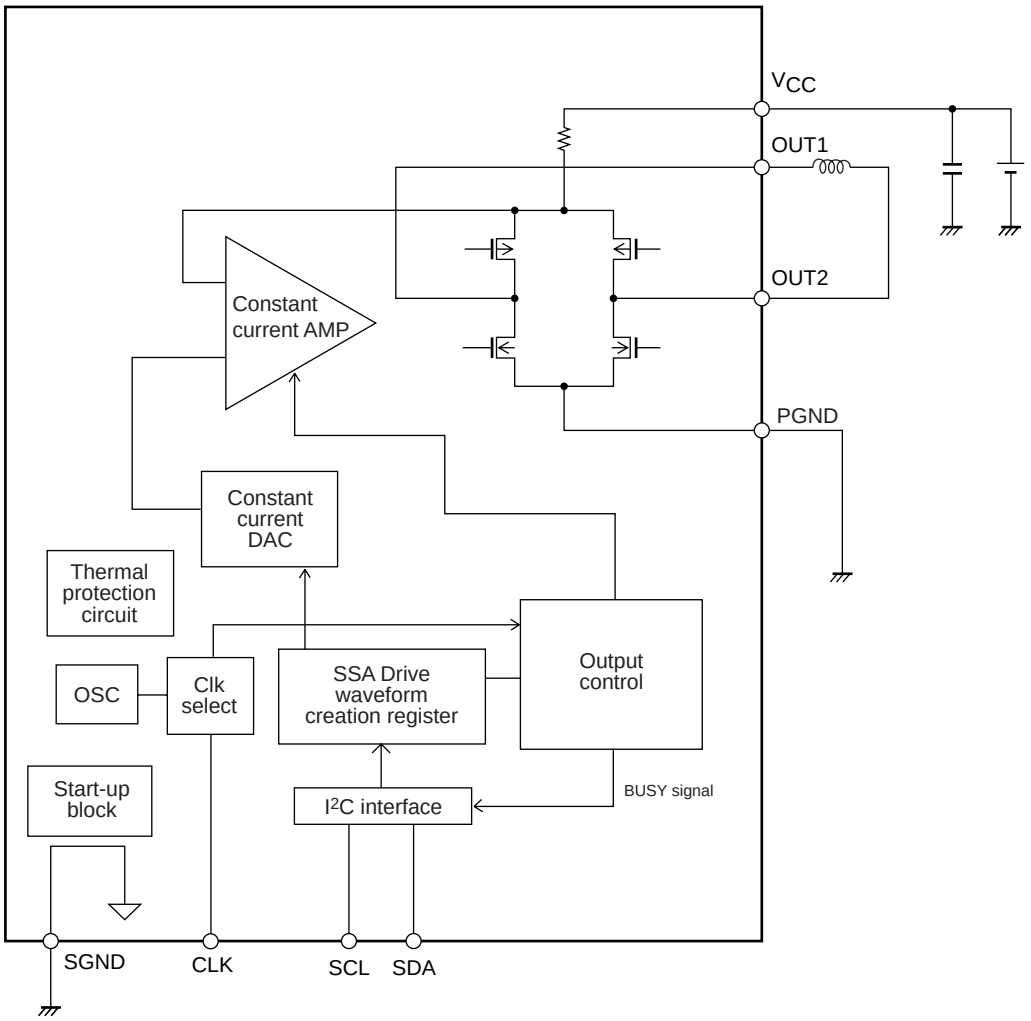
Pin Assignment





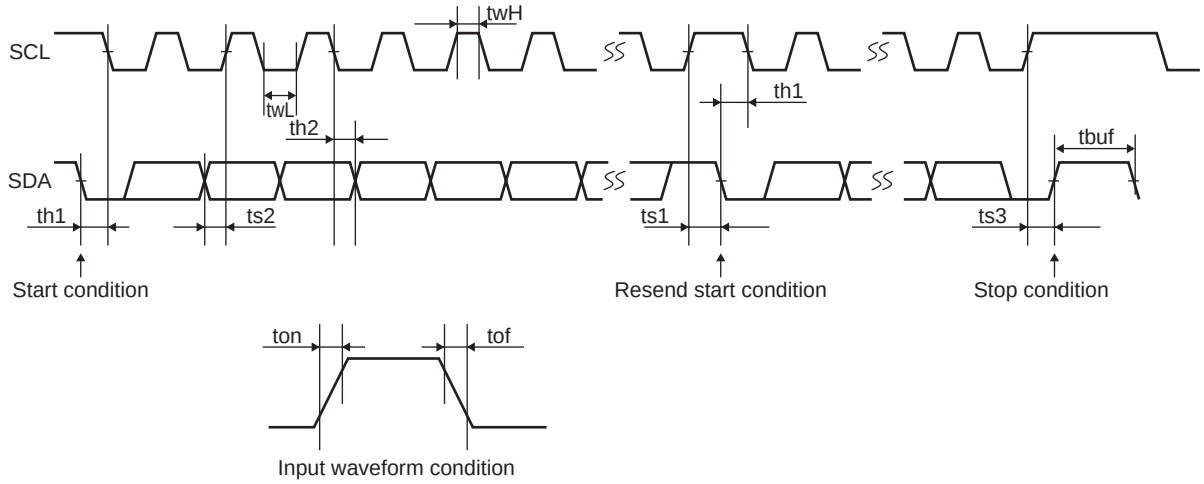
A1:CLK	B1:CLK
A2:SDA	B2:SGND
A3:OUT1	B3:V_{CC}
A4:PGND	B4:OUT2

Block Diagram



Serial Bus Communication Specifications

I²C serial transfer timing conditions



Standard mode

Parameter	symbol	Conditions	min	typ	max	unit
SCL clock frequency	fscl	SCL clock frequency	0	-	100	kHz
Data setup time	ts1	Setup time of SCL with respect to the falling edge of SDA	4.7	-	-	µs
	ts2	Setup time of SDA with respect to the rising edge of SCL	250	-	-	ns
	ts3	Setup time of SCL with respect to the rising edge of SDA	4.0	-	-	µs
Data hold time	th1	Hold time of SCL with respect to the rising edge of SDA	4.0	-	-	µs
	th2	Hold time of SDA with respect to the falling edge of SCL	0.06	-	-	µs
Pulse width	twL	SCL low period pulse width	4.7	-	-	µs
	twH	SCL high period pulse width	4.0	-	-	µs
Input waveform conditions	ton	SCL/SDA (input) rising time	-	-	1000	ns
	tof	SCL/ SDA (input) falling time	-	-	300	ns
Bus free time	tbuf	Interval between stop condition and start condition	4.7	-	-	µs

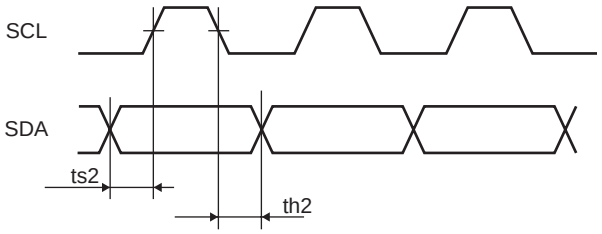
High Speed mode

Parameter	symbol	Conditions	min	typ	max	unit
SCL clock frequency	fscl	SCL clock frequency	0	-	400	kHz
Data setup time	ts1	Setup time of SCL with respect to the falling edge of SDA	0.6	-	-	µs
	ts2	Setup time of SDA with respect to the rising edge of SCL	100	-	-	ns
	ts3	Setup time of SCL with respect to the rising edge of SDA	0.6	-	-	µs
Data hold time	th1	Hold time of SCL with respect to the rising edge of SDA	0.6	-	-	µs
	th2	Hold time of SDA with respect to the falling edge of SCL	0.06	-	-	µs
Pulse width	twL	SCL low period pulse width	1.3	-	-	µs
	twH	SCL high period pulse width	0.6	-	-	µs
Input waveform conditions	ton	SCL/SDA (input) rising time	-	-	300	ns
	tof	SCL/ SDA (input) falling time	-	-	300	ns
Bus free time	tbuf	Interval between stop condition and start condition	1.3	-	-	µs

I²C bus transfer method

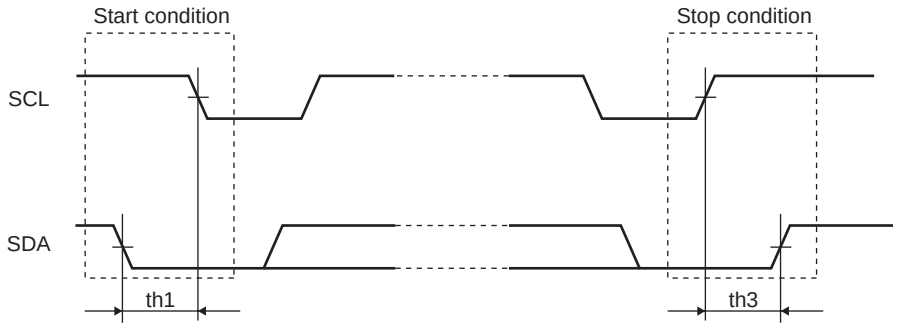
Start and stop conditions

The I²C bus requires that the state of SDA be preserved while SCL is high as shown in the timing diagram below during a data transfer operation.



When data is not being transferred, both SCL and SDA are in the high state. The start condition is generated and access is started when SDA is changed from high to low while SCL and SDA are high.

Conversely, the stop condition is generated and access is ended when SDA is changed from low to high while SCL is high.



Data transfer and acknowledgement response

After the start condition is generated, data is transferred one byte (8 bits) at a time. Any number of data bytes can be transferred consecutively.

An ACK signal is sent to the sending side from the receiving side every time 8 bits of data are transferred. The transmission of an ACK signal is performed by setting the receiving side SDA to low after SDA at the sending side is released immediately after the clock pulse of SCL bit 8 in the data transferred has fallen low.

After the receiving side has sent the ACK signal, if the next byte transfer operation is to receive only the byte, the receiving side releases SDA on the falling edge of the 9th clock of SCL.

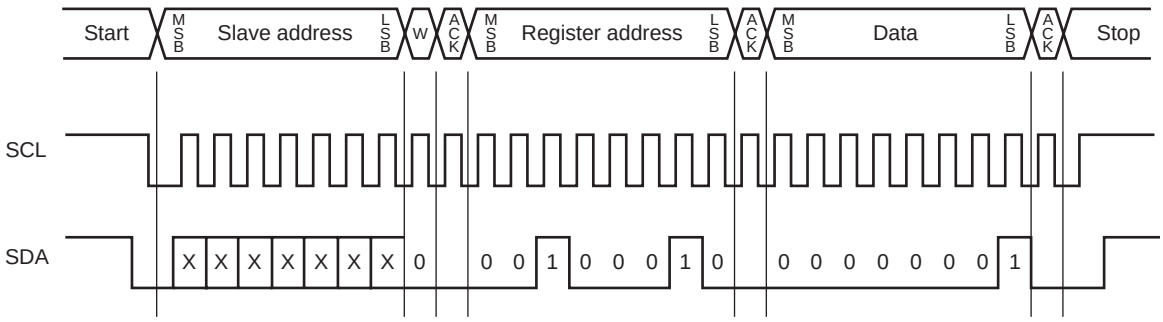
There are no CE signals in the I²C bus ; instead, a 7-bit slave address is assigned to each device, and the first byte of the transfer data is allocated to the 7-bit slave address and to the command (R/W) which specifies the direction of subsequent data transfer.

The READ function of the LC08101CT Driver area provides only the functionality to test the BUSY state.

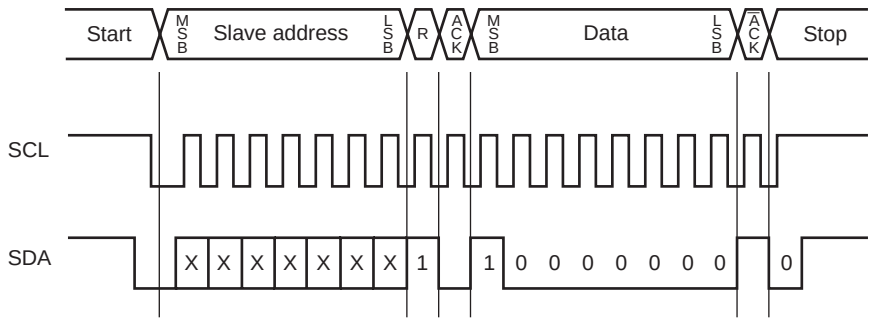
7-bit address data is transferred sequentially starting at the MSB and the second and subsequent bytes are written if the state of the 8th bit is low and read if the state is high.

In the LC08101CT Driver area, the slave address is stipulated to be “1110010.”

WRITE mode timing



READ mode timing



Data transfer write format

The slave address and Write command must be allocated to the first byte and the register address in the serial map must be designated in the second byte.

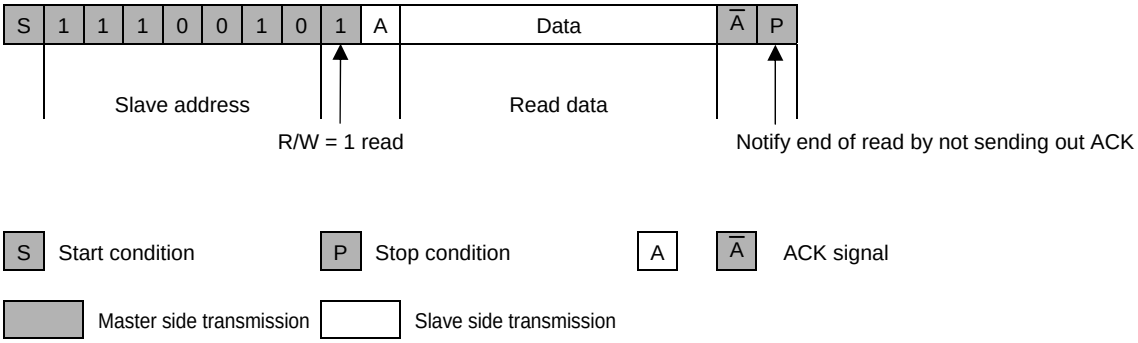
For the third byte, data transfer is carried out to the address designated by the register address which is written in the second byte. Subsequently, if data continues, the register address value is automatically incremented for the fourth and subsequent bytes.

Thus, continuous data transfer starting at the designated address is made possible.

After the register address reaches 1Fh, the transfer address for the next byte is set to 00h.

Data write example

Data read example



Driver area

Serial Map

	Register Address								Data							
	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	0	0	0	0	0	0	M/I	DRVPULSE[6:0]						
0									0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	1	×	×	ENIN	CKSEL[1:0]		INCLK[1:0]		BRON
1									0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	0	RST[7:0]							
2									0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	1	GTAS[7:0]							
3									0	0	0	0	0	0	0	0
	0	0	0	0	0	1	0	0	STP[7:0]							
4									0	0	0	0	0	0	0	0
	0	0	0	0	0	1	0	1	TEST[1:0]		SW1	SW2	IOUT[3:0]			
5									0	0	0	0	0	0	0	0
	0	0	0	0	0	1	1	0	TBRAKE[7:0]							
6									0	0	0	0	0	0	0	0
	0	0	0	0	0	1	1	1	×	×	NRPULSE1[5:0]					
7									0	0	0	0	0	0	0	0
	0	0	0	0	1	0	0	0	×	×	NRP-A[5:0]					
8									0	0	0	0	0	0	0	0
	0	0	0	0	1	0	0	1	×	×	NRP-B[5:0]					
9									0	0	0	0	0	0	0	0
	0	0	0	0	1	0	1	0	×	×	NRP-C[5:0]					
10									0	0	0	0	0	0	0	0
	0	0	0	0	1	0	1	1	×	×	NRP-D[5:0]					
11									0	0	0	0	0	0	0	0
	0	0	0	0	1	1	0	0	×	×	NRPULSE2[5:0]					
12									0	0	0	0	0	0	0	0
	0	0	0	0	1	1	0	1	×	×	NRP-E[5:0]					
13									0	0	0	0	0	0	0	0
	0	0	0	0	1	1	1	0	×	×	NRP-F[5:0]					
14									0	0	0	0	0	0	0	0
	0	0	0	0	1	1	1	1	×	×	NRP-G[5:0]					
15									0	0	0	0	0	0	0	0
	0	0	0	1	0	0	0	0	×	×	NRP-H[5:0]					
16									0	0	0	0	0	0	0	0
	0	0	0	1	0	0	0	1	×	×	NRPULSE3[5:0]					
17									0	0	0	0	0	0	0	0
	0	0	0	1	0	0	1	0	×	×	NRP-I[5:0]					
18									0	0	0	0	0	0	0	0
	0	0	0	1	0	0	1	1	×	×	NRP-J[5:0]					
19									0	0	0	0	0	0	0	0
	0	0	0	1	0	1	0	0	×	×	NRP-K[5:0]					
20									0	0	0	0	0	0	0	0
	0	0	0	1	0	1	0	1	×	×	NRP-L[5:0]					
21									0	0	0	0	0	0	0	0
	0	0	0	1	0	1	1	0	×	×	NRPULSE4[5:0]					
22									0	0	0	0	0	0	0	0
	Register Address								Data							

Upper : Register name Lower : Default value

Continued on next page.

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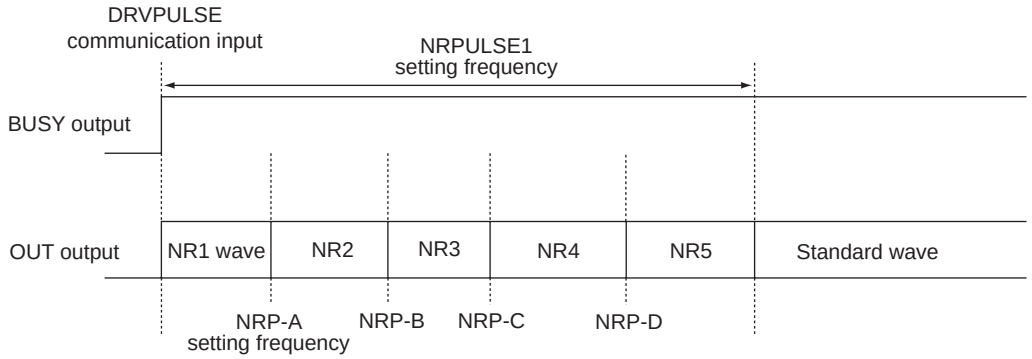
	Register Address								Data							
	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	0	1	0	1	1	1	×	×	NRP-M[5:0]					
23									0	0	0	0	0	0	0	0
	0	0	0	1	1	0	0	0	×	×	NRP-N[5:0]					
24									0	0	0	0	0	0	0	0
	0	0	0	1	1	0	0	1	×	×	NRP-O[5:0]					
25									0	0	0	0	0	0	0	0
	0	0	0	1	1	0	1	0	×	×	NRP-P[5:0]					
26									0	0	0	0	0	0	0	0
	0	0	0	1	1	0	1	1	NR1GTAS[7:0]							
27									0	0	0	0	0	0	0	0
	0	0	0	1	1	1	0	0	NR2GTAS[7:0]							
28									0	0	0	0	0	0	0	0
	0	0	0	1	1	1	0	1	NR3GTAS[7:0]							
29									0	0	0	0	0	0	0	0
	0	0	0	1	1	1	1	0	NR4GTAS[7:0]							
30									0	0	0	0	0	0	0	0
	0	0	0	1	1	1	1	1	NR5GTAS[7:0]							
31									0	0	0	0	0	0	0	0
	READ mode only register								BUSY	×	×	×	×	×	×	×
32									0	0	0	0	0	0	0	0
	Register Address								Data							

Upper : Register name Lower : Default value

NR pulse output

Rise-time operation

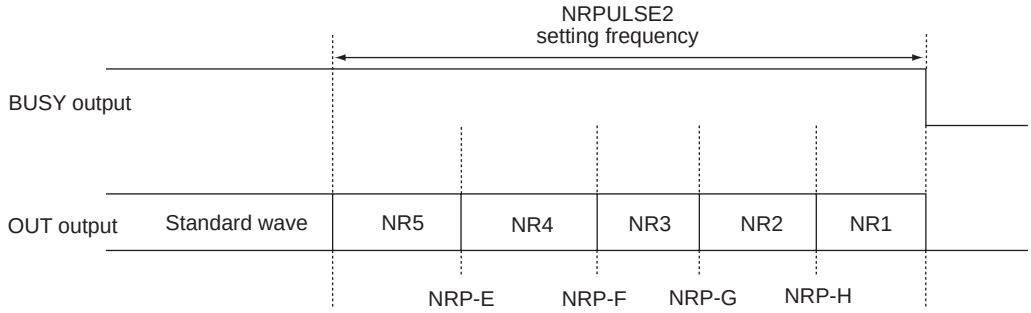


If, as an example, the NRPULSE1 setting is set to 15, the NRP-A setting is set to 3, the NRP-B setting is set to 6, the NRP-C setting is set to 9 and the NRP-D setting is set to 12, then after the NR1 waveform is output for three periods, the NR2 waveform for three periods, the NR3 waveform for three periods, the NR4 waveform for three periods and the NR5 waveform for three periods, the standard waveform is output for a period equivalent to the STP x DRVPULSE period.

When the NRPULSE setting is set to 0, the same output as the normal DRVPULSE input without the NR pulses is performed.

When the same value has been set for NRP-A and NRP-B, the NR2 waveform is not output, and the NR3 waveform is output after the NR1 waveform.

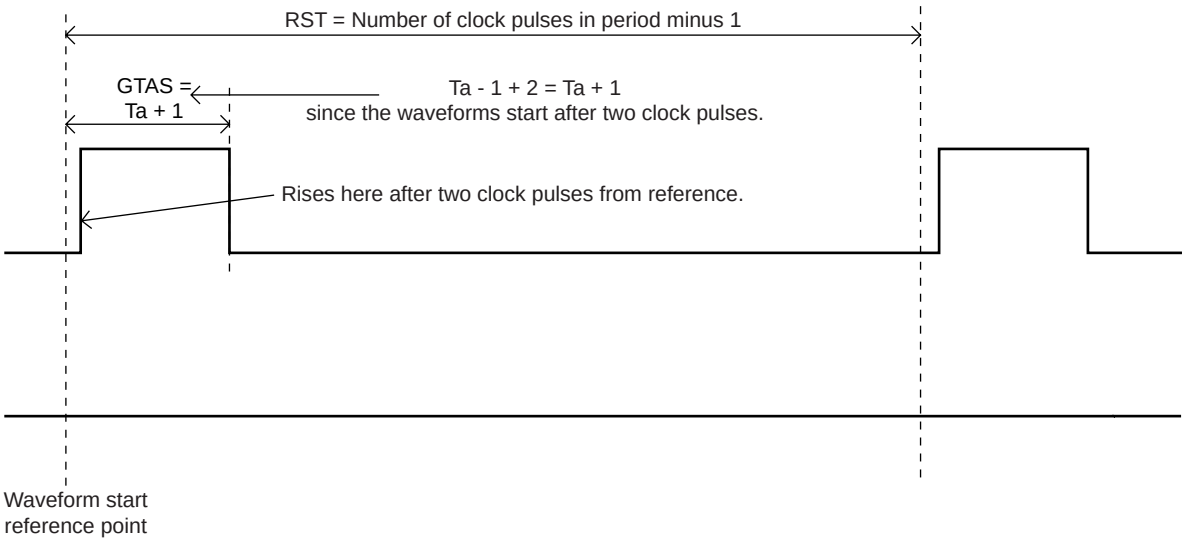
Fall-time operation



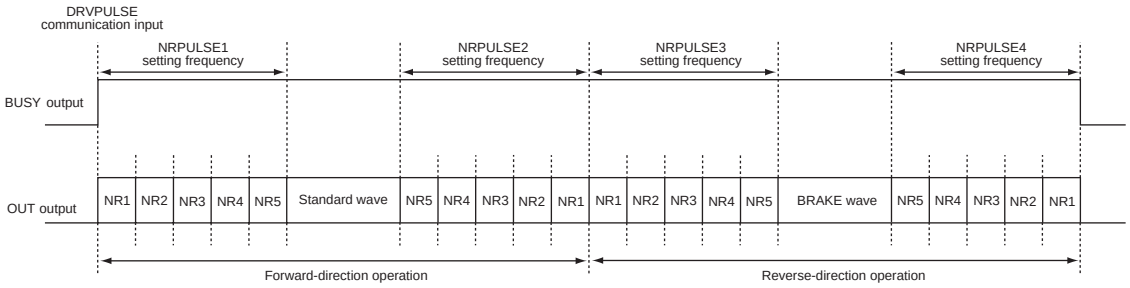
During the fall-time operation, the waveforms are output in sequence from the NR5 waveform to the NR1 waveform. The method used to set the switching timing is the same as for the rise-time operation.

NR drive waveform settings

The settings are the same as for the normal drive waveform. The same parameter as for the normal waveform is used for RST, and for GTAS the drive waveform is generated using the setting values for the NR waveforms.



NR pulse output when the brake is set



When the brake output has been set, a pulse equivalent to the TBRAKE frequency is output as the brake pulse in the reverse direction after the standard waveform has been output. If the NR settings are to be established, NR pulses can be set separately for the rise and fall of the standard waveform and the rise and fall of the brake waveform. When the brake setting is not to be established (when the BRON register is set to 0), the pulse is not output in the reverse direction so it is not output even when values have been set for NRPULSE3 and NRPULSE4.

Serial Mode Settings

0	0	0	0	0	0	0	0	0	D7	D6	D5	D4	D3	D2	D1	D0

D0 to D6: DRVPULSE [6 : 0]

Operation count setting register. Specify a number from 0 to 127.

The number of cyclic operations determined by <DRVPLUSE setting> × <STP setting> are performed.

Additional data can be input and data is added up to the equivalent of total of 512 pulses.

However, if the ENIN register is set to 0, the DRVPULSE input is not accepted because the DRVPULSE counter is in the reset state.

Since the output operation is carried out at the time the DRVPULSE input is recognized, the generation of the OUT signal is started at the time an ACK signal is generated after the execution of the instruction at address 00H according to the value of the waveform setup register established at that time.

D7	M/I
0	∞
1	macro

Operation direction switching

*Default Infinity distance direction

Macro direction

Operation direction switching register

The operation count setting register is reset when the register is switched. To stop the operation of the unit, switch the M/I register and set DRVPULSE to 0 for input.

1	0	0	0	0	0	0	0	1	0	0	D5	D4	D3	D2	D1	D0

D0: The register who selects whether you output brakes pulse after the movement end by the DRVPULSE input automatically.

D0	BRON
0	No brake
1	On brake

Initialization to be performed/not to be performed setting

*Default

D1, D2: The register who sets frequency of the oscillatory frequency when you operate an internal oscillator circuit.

D2	D1	INCLK
0	0	Oscillator stop
0	1	1.02MHz
1	0	1MHz
1	1	0.98MHz

Number of initialization sequence swing back

*Default

D3, D4: Register (when I use an internal oscillation invalidity) who sets the ratio to do a share lap when I count it in a clock pulse input into CLK pin or the IC inside as basic time.

D4	D3	CKSEL
0	0	1/4
0	1	1/2
1	0	1
1	1	1

Input clock division ratio switching

*Default 1/4

1/2

1 (no frequency division)

1 (no frequency division)

D5 : ENIN ENIN register is a register setting start, the stop of the IC.

Only as for the state of ENIN=1, the output of the IC operates. It becomes a wait mode at the time of ENIN=0.

2	0	0	0	0	0	0	1	0	D7	D6	D5	D4	D3	D2	D1	D0

RST7 to RST0 : Specifies the number of clocks per period (0 to 255). Default = 0

3	0	0	0	0	0	0	1	1	D7	D6	D5	D4	D3	D2	D1	D0

GTAS7 to GTAS0 : Sets the GATE_A pulse set value (0 to 255). Default = 0

4

0	0	0	0	0	1	0	0	D7	D6	D5	D4	D3	D2	D1	D0

STP7 to STP0 : Output pulse step number for the DRIVE input (1 to 256). Default = 1

+1 is the quantity that I did, and the set range is treated in data level.

When I input at 8 bits (0 to 255), it is treated in STP setting period of 1 to 256.

5

0	0	0	0	0	1	0	1	D7	D6	D5	0	D3	D2	D1	D0

D0 to D3: IOUT3 to IOUT0 Output constant current level setting (0 to 15). Default = 210mA typical

D3	D2	D1	D0	IOUT3 to IOUT0	Output current setting(typical)
0	0	0	0	0	210mA
0	0	0	1	1	199mA
0	0	1	0	2	189mA
0	0	1	1	3	178mA
0	1	0	0	4	168mA
0	1	0	1	5	157mA
0	1	1	0	6	147mA
0	1	1	1	7	136mA
1	0	0	0	8	126mA
1	0	0	1	9	115mA
1	0	1	0	10	105mA
1	0	1	1	11	94mA
1	1	0	0	12	84mA
1	1	0	1	13	73mA
1	1	1	0	14	63mA
1	1	1	1	15	52mA

D4, D5: SW1, SW2

It is a current value adjustment bit of the constant current output. Please usually use it in 00 setting at the time of use.

D6, D7: TEST1, TEST0

I use it with the test mode of the driver IC. Please usually use it in 00 setting at the time of use.

6

0	0	0	0	0	1	1	0	D7	D6	D5	D4	D3	D2	D1	D0

D0 to D7 : TBRAKE0 to TBRAKE7 Brakes pulse frequency setting (1 to 256). Default = 1

The setting value range is handled as the data value plus 1.

If, when the BRON register is set to 1, a drive command based on DRVPULSE is input, the brake pulse is output in the reverse direction after the normal operation has ended. The reverse-direction operation for the number of periods set by TBRAKE (the same drive waveform as when M/I is switched) is performed.

7

0	0	0	0	0	1	1	1	0	0	D5	D4	D3	D2	D1	D0

NRPUL15 to NRPUL10 (0 to 63). Default = 0

The total output frequency is set for the drive waveforms from NR1 to NR5 during the rise when a multiple number of drive waveforms are output continuously during actuator operation.

If 0 has been set, the NR drive waveforms are not output for the rise, and the normal operation is performed.

8

0	0	0	0	1	0	0	0	0	0	D5	D4	D3	D2	D1	D0

NRP-A5 to NRP-A0 (0 to 63). Default = 0

This register sets the timing of the first switching for the rise-time NR drive waveforms. The number of periods for which the NR1 waveform is to be output is set.

9

0	0	0	0	1	0	0	1	0	0	D5	D4	D3	D2	D1	D0

NRP-B5 to NRP-B0 (0 to 63). Default = 0

This register sets the timing of the second switching for the rise-time NR drive waveforms. It outputs the

NR2 waveform for the number of periods that is the difference between NRP-A and NRP-B.

10	0	0	0	0	1	0	1	0	0	0	D5	D4	D3	D2	D1	D0

NRP-C5 to NRP-C0 (0 to 63). Default = 0

This register sets the timing of the third switching for the rise-time NR drive waveforms. It outputs the NR3 waveform for the number of periods that is the difference between NRP-B and NRP-C.

11	0	0	0	0	1	0	1	1	0	0	D5	D4	D3	D2	D1	D0

NRP-D5 to NRP-D0 (0 to 63). Default = 0

This register sets the timing of the fourth switching for the rise-time NR drive waveforms.
The NR4 waveform is output for the number of periods that is the difference between NRP-C and NRP-D , and the NR5 waveform is output for the number of periods that is the difference between NRP-D and NRPUL1.

When setting the rise-time NR drive waveforms, set values which, in principle, satisfy the following relationship:

NRP-A ≤ NRP-B ≤ NRP-C ≤ NRP-D

(If this relationship is not satisfied, unintended drive waveforms may be output, but the IC will not be broken or damaged as a result.)

12	0	0	0	0	1	1	0	0	0	0	D5	D4	D3	D2	D1	D0

NRPUL25 to NRPUL20 (0 to 63). Default = 0

The total output frequency is set for the drive waveforms from NR1 to NR5 during the fall when a multiple number of drive waveforms are output continuously during actuator operation.
If 0 has been set, the NR drive waveforms are not output for the rise, and the stops.

13	0	0	0	0	1	1	0	1	0	0	D5	D4	D3	D2	D1	D0

NRP-E5 to NRP-E0 (0 to 63). Default = 0

This register sets the timing of the first switching for the fall-time NR drive waveforms. The number of periods for which the NR5 waveform is to be output is set.

14	0	0	0	0	1	1	1	0	0	0	D5	D4	D3	D2	D1	D0

NRP-F5 to NRP-F0 (0 to 63). Default = 0

This register sets the timing of the second switching for the fall-time NR drive waveforms. It outputs the NR4 waveform for the number of periods that is the difference between NRP-E and NRP-F.

15	0	0	0	0	1	1	1	1	0	0	D5	D4	D3	D2	D1	D0

NRP-G5 to NRP-G0 (0 to 63). Default = 0

This register sets the timing of the third switching for the fall-time NR drive waveforms. It outputs the NR3 waveform for the number of periods that is the difference between NRP-F and NRP-G.

16	0	0	0	1	0	0	0	0	0	0	D5	D4	D3	D2	D1	D0

NRP-H5 to NRP-H0 (0 to 63). Default = 0

This register sets the timing of the fourth switching for the fall-time NR drive waveforms.
The NR2 waveform is output for the number of periods that is the difference between NRP-G and NRP-H , and the NR1 waveform is output for the number of periods that is the difference between NRP-H and NRPUL2.

When setting the fall-time NR drive waveforms, set values which, in principle, satisfy the following relationship:

NRP-E ≤ NRP-F ≤ NRP-G ≤ NRP-H

(If this relationship is not satisfied, unintended drive waveforms may be output, but the IC will not be broken or damaged as a result.)

17

0	0	0	1	0	0	0	1	0	0	D5	D4	D3	D2	D1	D0

NRPUL35 to NRPUL30 (0 to 63). Default = 0

The total output frequency is set for the drive waveforms from NR1 to NR5 during the rise when a multiple number of drive waveforms are output continuously during actuator operation.

If 0 has been set, the NR drive waveforms are not output for the rise, and the start Brake output.

18

0	0	0	1	0	0	1	0	0	0	D5	D4	D3	D2	D1	D0

NRP-I5 to NRP-I0 (0 to 63). Default = 0

This register sets the timing of the first switching for the rise-time NR drive waveforms. The number of periods for which the NR1 waveform is to be output is set.

19

0	0	0	1	0	0	1	1	0	0	D5	D4	D3	D2	D1	D0

NRP-J5 to NRP-J0 (0 to 63). Default = 0

This register sets the timing of the second switching for the rise-time NR drive waveforms. It outputs the NR2 waveform for the number of periods that is the difference between NRP-I and NRP-J.

20

0	0	0	1	0	1	0	0	0	0	D5	D4	D3	D2	D1	D0

NRP-K5 to NRP-K0 (0 to 63). Default = 0

This register sets the timing of the third switching for the rise-time NR drive waveforms. It outputs the NR3 waveform for the number of periods that is the difference between NRP-J and NRP-K.

21

0	0	0	1	0	1	0	1	0	0	D5	D4	D3	D2	D1	D0

NRP-L5 to NRP-L0 (0 to 63). Default = 0

This register sets the timing of the fourth switching for the rise-time NR drive waveforms.

The NR4 waveform is output for the number of periods that is the difference between NRP-K and NRP-L , and the NR5 waveform is output for the number of periods that is the difference between NRP-L and NRPUL3.

When setting the rise-time NR drive waveforms, set values which, in principle, satisfy the following relationship:

NRP-I ≤ NRP-J ≤ NRP-K ≤ NRP-L

(If this relationship is not satisfied, unintended drive waveforms may be output, but the IC will not be broken or damaged as a result.)

22

0	0	0	1	0	1	1	0	0	0	D5	D4	D3	D2	D1	D0

NRPUL45 to NRPUL40 (0 to 63). Default = 0

The total output frequency is set for the drive waveforms from NR1 to NR5 during the fall when a multiple number of drive waveforms are output continuously during actuator operation.

If 0 has been set, the NR drive waveforms are not output for the rise, and the stops.

23

0	0	0	1	0	1	1	1	0	0	D5	D4	D3	D2	D1	D0

NRP-M5 to NRP-M0 (0 to 63). Default = 0

This register sets the timing of the first switching for the fall-time NR drive waveforms. The number of periods for which the NR5 waveform is to be output is set.

24

0	0	0	1	1	0	0	0	0	0	D5	D4	D3	D2	D1	D0

NRP-N5 to NRP-N0 (0 to 63). Default = 0

This register sets the timing of the second switching for the fall-time NR drive waveforms. It outputs the NR4 waveform for the number of periods that is the difference between NRP-M and NRP-N.

25	0	0	0	1	1	0	0	1	0	0	D5	D4	D3	D2	D1	D0

NRP-O5 to NRP-O0 (0 to 63). Default = 0

This register sets the timing of the third switching for the fall-time NR drive waveforms. It outputs the NR3 waveform for the number of periods that is the difference between NRP-N and NRP-O.

26	0	0	0	1	1	0	1	0	0	0	D5	D4	D3	D2	D1	D0

NRP-P5 to NRP-P0 (0 to 63). Default = 0

This register sets the timing of the fourth switching for the fall-time NR drive waveforms.
The NR2 waveform is output for the number of periods that is the difference between NRP-O and NRP-P , and the NR1 waveform is output for the number of periods that is the difference between NRP-P and NRPUL4.

When setting the fall-time NR drive waveforms, set values which, in principle, satisfy the following relationship:

NRP-M ≤ NRP-N ≤ NRP-O ≤ NRP-P

(If this relationship is not satisfied, unintended drive waveforms may be output, but the IC will not be broken or damaged as a result.)

27	0	0	0	1	1	0	1	1	D7	D6	D5	D4	D3	D2	D1	D0

NR1GTAS7 to NR1GTAS0 (0 to 255). Default = 0

GATE_A pulse set value for NR1 waveform

28	0	0	0	1	1	1	0	0	D7	D6	D5	D4	D3	D2	D1	D0

NR2GTAS7 to NR2GTAS0 (0 to 255). Default = 0

GATE_A pulse set value for NR2 waveform

29	0	0	0	1	1	1	0	1	D7	D6	D5	D4	D3	D2	D1	D0

NR3GTAS7 to NR3GTAS0 (0 to 255). Default = 0

GATE_A pulse set value for NR3 waveform

30	0	0	0	1	1	1	1	0	D7	D6	D5	D4	D3	D2	D1	D0

NR4GTAS7 to NR4GTAS0 (0 to 255). Default = 0

GATE_A pulse set value for NR4 waveform

31	0	0	0	1	1	1	1	1	D7	D6	D5	D4	D3	D2	D1	D0

NR5GTAS7 to NR5GTAS0 (0 to 255). Default = 0

GATE_A pulse set value for NR5 waveform

32	No register address								D7	0	0	0	0	0	0	0

This is a read-only register line.

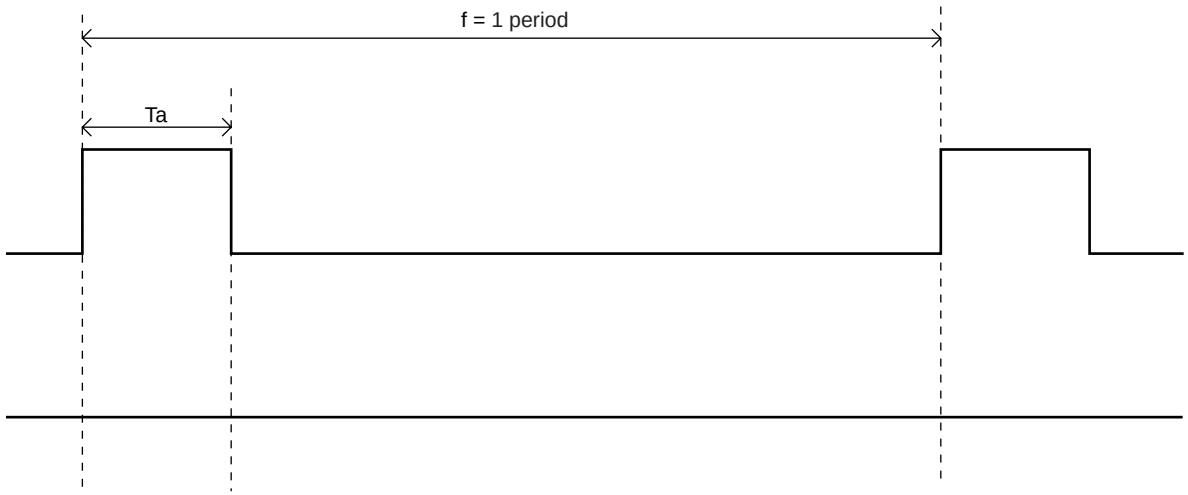
D7: BUSY register

"1" is output during output operations; "0" is output when the output has stopped.

Functional Description

1 period :

One period of OUT waveform operation is equivalent to one output operation.



CLK input :

The pin for the external CLK input that provides the reference time for generating drive waveforms.
The frequency division ratio for I²C communication can be selected from 1/4, 1/2, and 1/1. Drive waveforms are generated by counting this frequency-divided clk pulses as the basic count unit. The LC08101CT supports frequency from 10MHz to 60MHz depending on the frequency division ratio and counter settings.

Register setup sequence **:**

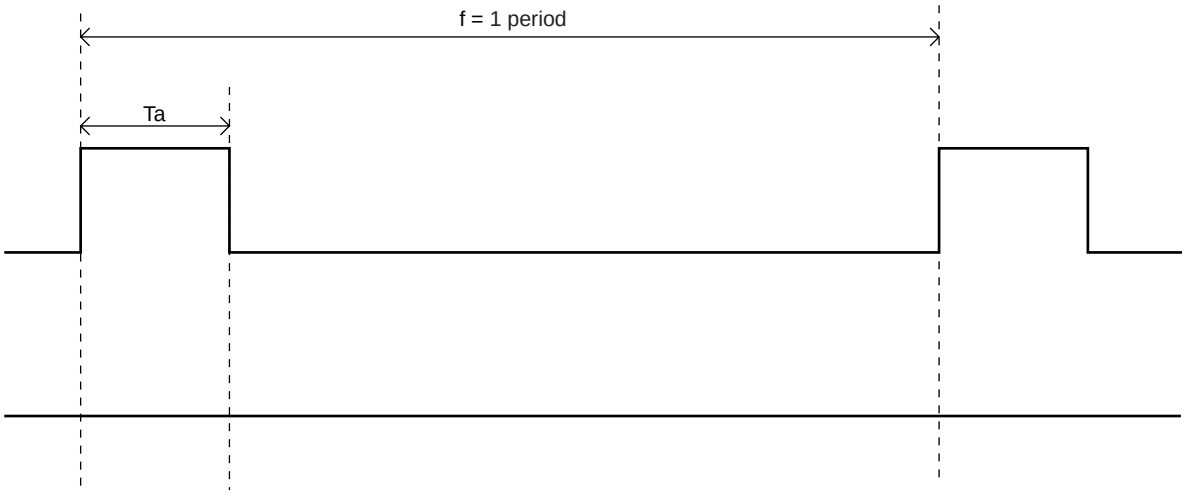
(1) Apply V_{CC}.
(2) Set register addresses 0x01 to 0x1F (set the waveform and drive conditions).
(3) Set the ENIN register to 1 (invoke initialization procedures if initialization is enabled or start up the IC).
(4) Set up M/I and DRVPULSE to start the AF operation (actuator operation instruction).

I^2C communication during output operation **:**

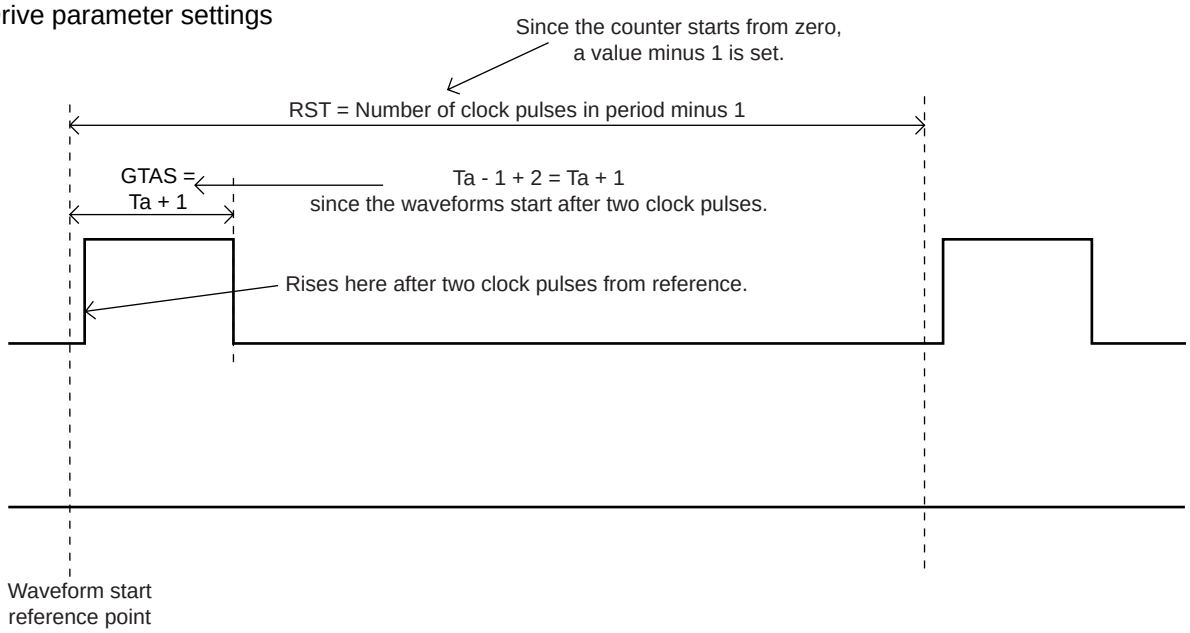
I^2C communication with all the registers is possible even when the IC is in operation (OUT processing or BUSY is held high).
However, if the drive waveform settings have been changed while the actuator is operating, for example, there is a possibility that unintended waveforms are output.

Actuator drive waveform settings :

Configuration of piezoelectric actuator drive waveform



Drive parameter settings



The drive waveforms are set using four parameters: RST, GTAS, GTBR and GTBS.

RST : Parameter determines the period, and sets the reference clock pulse count minus 1.

GTAS : Parameter determines the time taken for the gate signal A to the falling edge from the reference point. Since the signal raises after two clock pulses from the reference, the Ta reference clock cycle count plus 1 is set.

[Example of settings] When setting reference clock to 10MHz, period to 13μs, Ta to 2.0μs

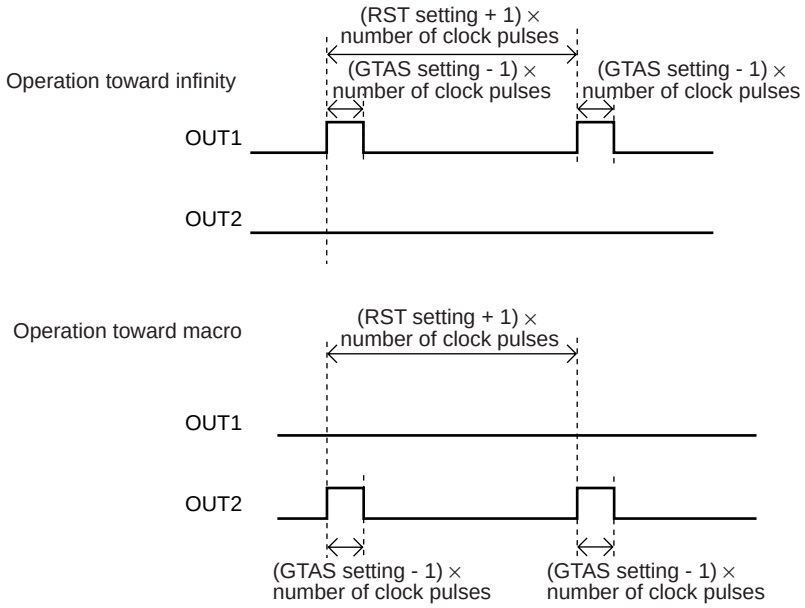
Since the reference clock time is 0.1μs :

The period is 130 clks. → Specify 129 (RST value of 130 -1).

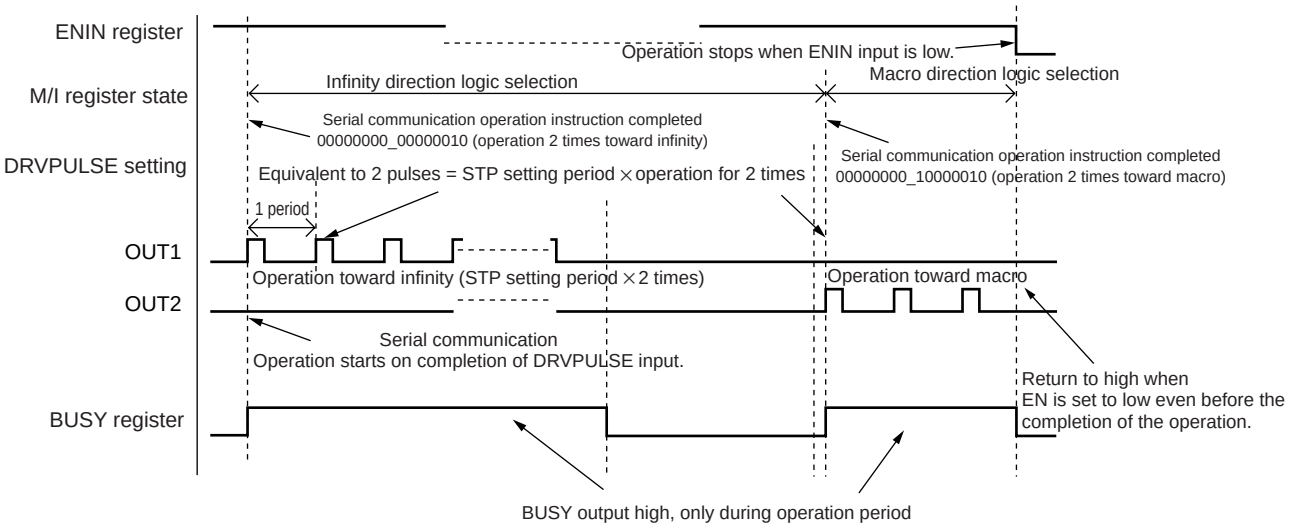
Ta is 20 clks. → Specify 21 (GTAS value of 20 + 1).

Timing charts

Enlarged view of the sequence of output signals



DRVPULSE input sequence



OUTPUT-Tr on/off truth table