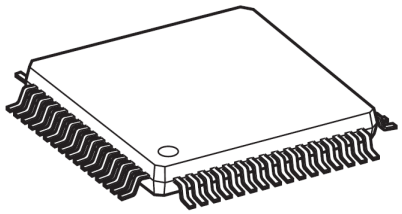
TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC90104AFG

Multi System Video Decoder

The TC90104AFG is a single chip IC that converts analog video signals to digital video signals (ITU-R BT. 601 / ITU-R BT. 656 YCbCr 16, 8bit digital signal).

Additionally, the TC90104AFG has a 3-channel A/D converter as an analog input interface, and has 3-line Y/C separation and multi-system color decoder functionality.



LQFP64-P-1010-0.50E

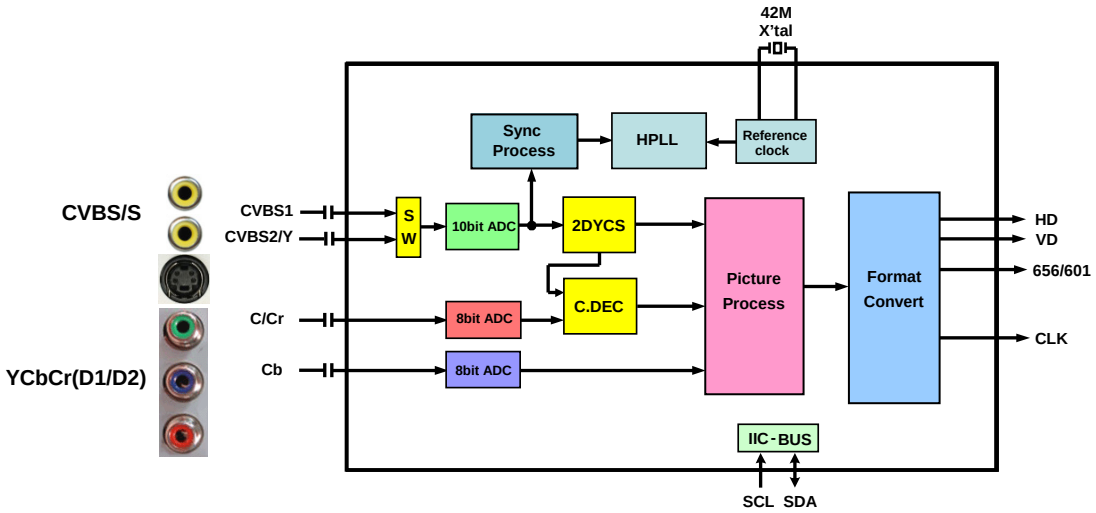
Weight: 0.4 g (typ.)

1. Features

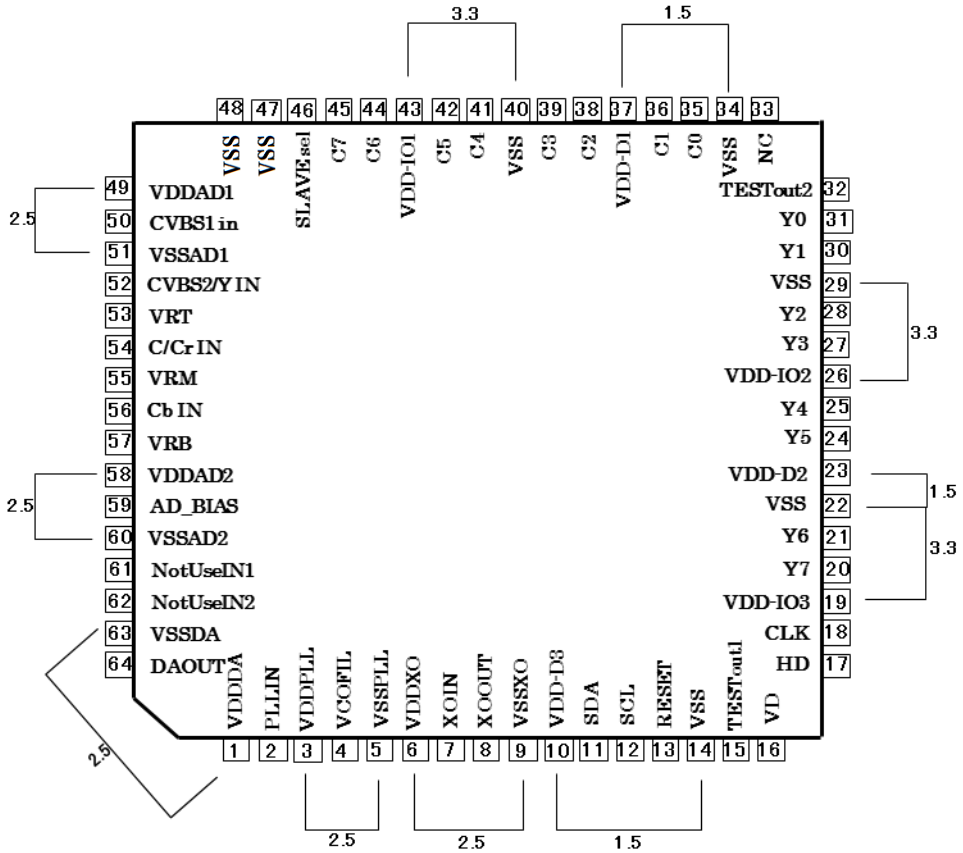
- Input: CVBS, Y/C (S-Video), Y/Cb/Cr (D1, D2)
- Multi-color decoder
- Synchronous playback/ Standard identification
- Y/C separation: 3-line YCS (NTSC/PAL)
  BPF processing. (SECAM)
- Picture process Y: V-Enhance, LTI, sharpness, noise cancel, contrast, brightness
  C: TOF, ACC, color gain, CTI, noise cancel
- Output: ITU-R BT.601(D1) / ITU-R BT.656(D1) / 16bit(D2) / 8bit serial(D2) .
- I^2C-bus control
- Package: LQFP 64 pin (0.50 mm pitch)
- Power supply: 3.3 V, 2.5 V, 1.5 V

2. Block Diagram

To explain the function, there are omitted part for function block and application circuit.



3. Pin Layout



4. Pin Descriptions

Pin No.	Pin Name	Pin Function	Pin type	Standard withstand voltage [V]	Processing at unused time
1	VDDDA	2.5 V power supply for DAC	VDD	2.5	-
2	PLLIN	Input of PLL circuit for clock	IN	2.5	-
3	VDDPLL	2.5 V power supply for PLL circuit	VDD	2.5	-
4	VCOFIL	VCO control bias for PLL circuit	Bias	2.5	-
5	VSSPLL	GND for PLL circuit	VSS	0	-
6	VDDXO	2.5V Power supply for X'tal circuit	VDD	2.5	-
7	XOIN	Input for X'tal circuit	IN	2.5	-
8	XOOUT	Output for X'tal circuit	OUT	2.5	-
9	VSSXO	GND for X'tal circuit	GND	0	-
10	VDD-D3	1.5 V power supply for Logic circuit	VDD	1.5	-
11	SDA	Serial data input/output <I^2C-BUS>	I / O	5	-
12	SCL	Serial clock input <I^2C-BUS>	IN	5	-
13	RESET	System reset	IN	3.3	-
14	VSS	Digital GND	GND	0	-
15	TESTout1	TEST output terminal 1	OUT	3.3	Open
16	VD	VD output	OUT	3.3	Open
17	HD	HD output	OUT	3.3	Open
18	CLK	Clock signal output	OUT	3.3	-
19	VDD-IO3	3.3 V power supply for I/O circuit	VDD	3.3	-
20	Y7	Y7 signal output (MSB) *1	OUT	3.3	-
21	Y6	Y6 signal output *1	OUT	3.3	-
22	VSS	Digital GND	GND	0	-
23	VDD-D2	1.5V power supply for logic circuit	VDD	1.5	-
24	Y5	Y5 signal output *1	OUT	3.3	-
25	Y4	Y4 signal output *1	OUT	3.3	-
26	VDD-IO2	3.3V power supply for I/O circuit	VDD	3.3	-
27	Y3	Y3 signal output *1	OUT	3.3	-
28	Y2	Y2 signal output *1	OUT	3.3	-
29	VSS	Digital GND	GND	0	-
30	Y1	Y1 signal output	OUT	3.3	-
31	Y0	Y0 signal output	OUT	3.3	-
32	TESTout2	TEST output terminal 2	OUT	3.3	Open

*1: It is available for SAV/EAV implantation when input signal is CVBS or YCbCr(D1) and output is ITU-R BT.656 format. It needs to use HD/VD output mode because it is not available for SAV/EAV implantation when output is D2 signal (54MHz 8bit).

Pin No.	Pin Name	Pin Function	Pin type	Standard withstand voltage [V]	Processing at unused time
33	NC	Non-connection	OUT	3.3	-
34	VSS	Digital GND	GND	0	-
35	C0	C0 signal output (LSB) *2	OUT	3.3	-
36	C1	C1 signal output *2	OUT	3.3	-
37	VDD-D1	1.5 V power supply for logic circuit	VDD	1.5	-
38	C2	C2 signal output *2	OUT	3.3	-
39	C3	C3 signal output *2	OUT	3.3	-
40	VSS	Digital GND	GND	0	-
41	C4	C4 signal output *2	OUT	3.3	-
42	C5	C5 signal output *2	OUT	3.3	-
43	VDD-IO1	3.3 V power supply for I/O circuit	VDD	3.3	-
44	C6	C6 signal output *2	OUT	3.3	-
45	C7	C7 signal output *2	OUT	3.3	-
46	SLAVE sel	I^2C-BUS slave-address selector	IN	3.3	-
47	VSS	Digital GND	GND	0	-
48	VSS	Digital GND	GND	0	-
49	VDDAD1	2.5 V power supply for ADC circuit	VDD	2.5	-
50	CVBS1 in	Composite video signal input	IN	2.5	GND via 0.1μF
51	VSSAD1	GND for ADC circuit	GND	0	-
52	CVBS2/Y IN	Composite video / Y signal input	IN	2.5	GND via 0.1μF
53	VRT	Reference top voltage for ADC	Bias	2.5	-
54	C/Cr IN	C / Cr video signal input	IN	2.5	GND via 0.1μF
55	VRM	Reference middle voltage for ADC	Bias	2.5	-
56	Cb IN	Cb video signal input	IN	2.5	GND via 0.1μF
57	VRB	Reference bottom voltage for ADC	Bias	2.5	-
58	VDDAD2	2.5 V power supply for ADC circuit	VDD	2.5	-
59	AD_BIAS	Reference voltage for ADC	Bias	2.5	-
60	VSSAD2	GND for ADC circuit	GND	0	-
61	NotUseIN1	To GND via 10kΩ resistor	IN	3.3	GND via 10kΩ resistor
62	NotUseIN2	To GND via 10kΩ resistor	IN	3.3	GND via 10kΩ resistor
63	VSSDA	GND for DAC circuit for clock	GND	0	-
64	DAOUT	Output of DAC circuit for clock	OUT	2.5	-

*2 When 8bit output mode, output of C7 to C0 terminal are fixed to Low. Therefore these must be open.

5. Function

5.1 Overview

- Analog input interface for Composite video signal, Y/C signal (S signal), Component signal (D1/D2)
- Multi system 3 line comb filter (2DYCS)
- Multi system color decoder and sync generation processing
- Color system detection (selectable auto detection or manual setting)
- Picture quality processing function
- Digital output interface for ITU-R BT. 601/656

5.2 Input signal

5.2.1 Input signal list

Input signal format			Frequency			Effective pixels		Total pixels	
			fH [kHz]	fV [Hz]	fs [MHz]	Horizontal	Vertical	Horizontal	Vertical
CVBS	NTSC		15.75/15.734	60/59.94	27	720	240	858	262.5
	PAL/SECAM		15.625	50	27	720	288	864	312.5
Y/C	NTSC		15.75/15.734	60/59.94	27	720	240	858	262.5
	PAL		15.625	50	27	720	288	864	312.5
YCbCr	D1	480i	15.75/15.734	60	27	720	240	858	262.5
		576i	15.625	50	27	720	288	864	312.5
	D2	480p	31.5/31.469	60	27	720	480	858	525
		576p	31.25	50	27	720	576	864	625

5.2.2 Input signal

The TC90104AFG is equipped with 3-ch ADC for Composite video signal, Y/C signal and YCbCr signal input.

The input-dynamic-range for ADC is designed in AVDD x 0.4 [V] with the normal input dynamic range being 1 Vp-p (AVDD = 2.5 V). Be sure to use 0.7 Vp-p (1 Vp-p x 0.7) with 140IRE input when using NTSC as the recommended reference input amplitude.

5.2.3 Table of Input – Output signal

Input signal				Processing		Output signal					
Input format			f H [kHz]	Sampling clock [MHz]	Internal Format	Output clock [MHz]	RGB	601 656	HD	VD	ENB
CVBS	NTSC		15.75/15.734	27	4:2:2	13.5 / 27	-	○	○	○	-
	PAL		15.625	27	4:2:2	13.5 / 27	-	○	○	○	-
Y/C	NTSC		15.75/15.734	27	4:2:2	13.5 / 27	-	○	○	○	-
	PAL		15.625	27	4:2:2	13.5 / 27	-	○	○	○	-
YCbCr	D1	480i	15.75/15.734	27	4:2:2	13.5 / 27	-	○	○	○	-
		576i	15.625	27	4:2:2	13.5 / 27	-	○	○	○	-
	D2	480p	31.5/31.469	27	4:2:2	27	-	○	○	○	-
		576p	31.25	27	4:2:2	27	-	○	○	○	-

5.2.4 Typical input level of analog input signal

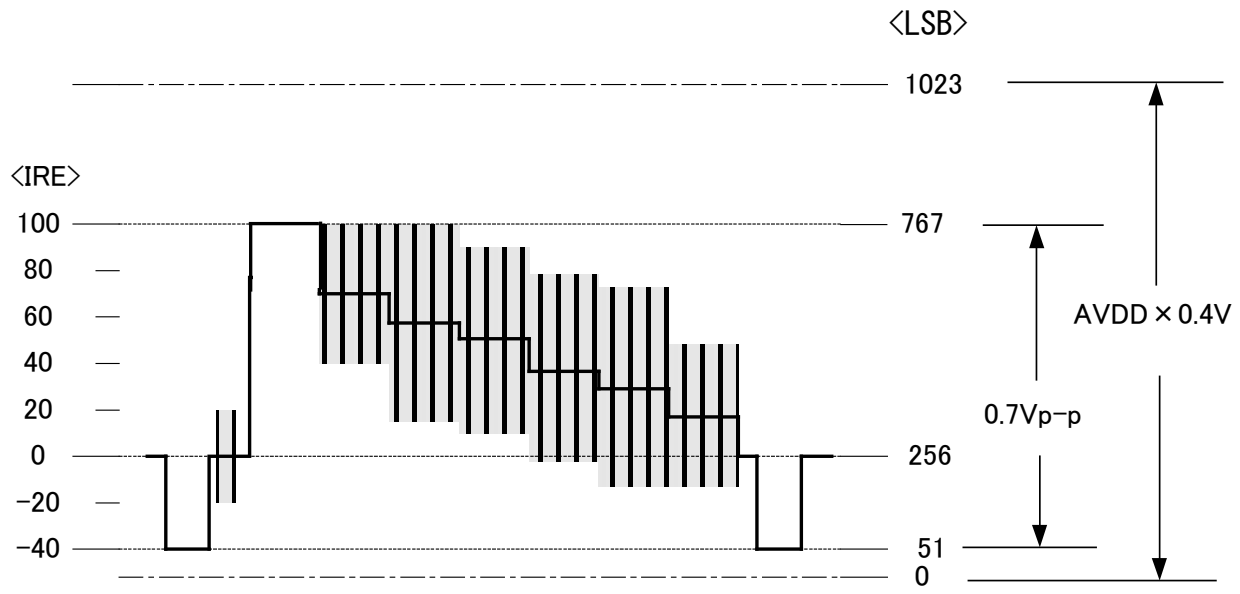


Fig.1 Reference input level to CVBS1(Composite Video) and CVBS2/Y/G(S-Video Y, Componet Y) when 100% White (i.e., composite video input)

CVBS, Y, Component-Y signal need to input 0.7 Vpp when 140IRE, and also C signal (S-signal) need to input 0.2 Vpp when 40IRE. (VDD = 2.5 V, 140IRE = 0.7 Vpp at NTSC)
When use Component-CbCr , CbCr-level is 0.7 Vpp for 100%.
An above waveform is color bar signal of 75%

Input terminal	Input level = Vp-p *1	Output : LSB *2	Notes
CVBS	0.7 Vp-p (500 mVp-p)	16-235 (for 8bit)	Output at 656/601 format
Y	0.7 Vp-p (500 mVp-p)	16-235 (for 8bit)	Output at 656/601 format
C	0.2 Vp-p (Burst signal)	31-225 (for 8bit)	Output at 656/601 format
Cb	0.7 Vp-p	31-225 (for 8bit)	Output at 656/601 format
Cr	0.7 Vp-p	31-225 (for 8bit)	Output at 656/601 format

*1 About input level,
It has indicate the case of NTSC.
CVBS and Y input level will be 140IRE at the White of 100%.
Please adjust to 0.7 V this 100%.
Values in the ( ) is the level of from the pedestal to white 100%.

Input level of C(= chroma signal) has indicate the burst level at the time of NTSC.
Input level of CbCr has indicate the level of color-100% at the time of NTSC.

*2 About output level,
It has indicate the case of NTSC.
CVBS and Y output level is white100% output level at the time of NTSC.
Values in the ( ) is the output level of from the pedestal to white 100%.

Output level of C(chroma signal) indicate the CbCr level at the time of color-100%.
Output level of CbCr indicate the level of color-100% at the time of NTSC.

Notes: The above output level is influenced by the picture quality adjustment of contrast, gain, ACC and others.
It does not indicate the maximum level.

Fig.2 Reference input level to C/Cr/R (S-Video C)

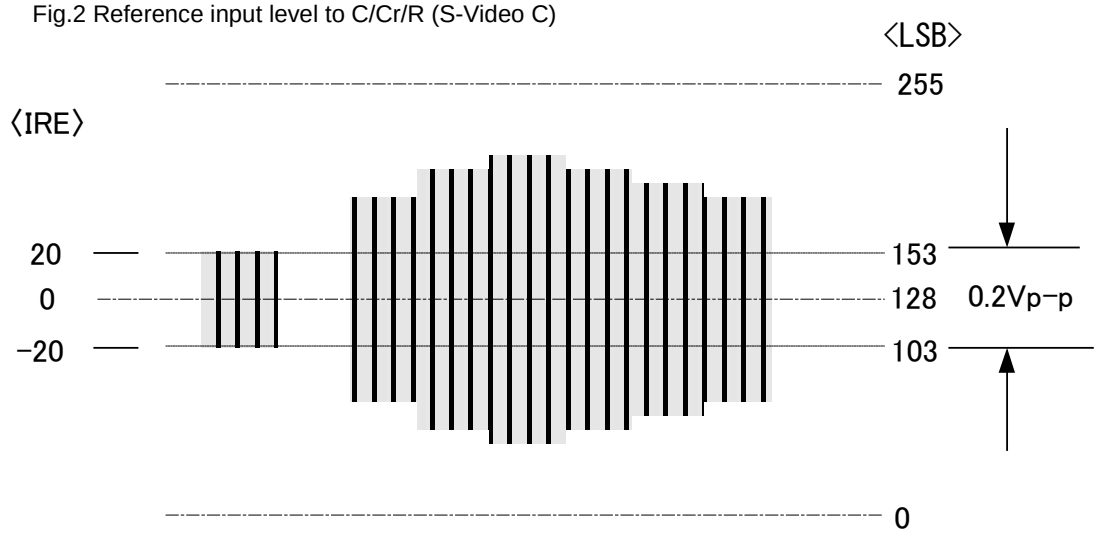
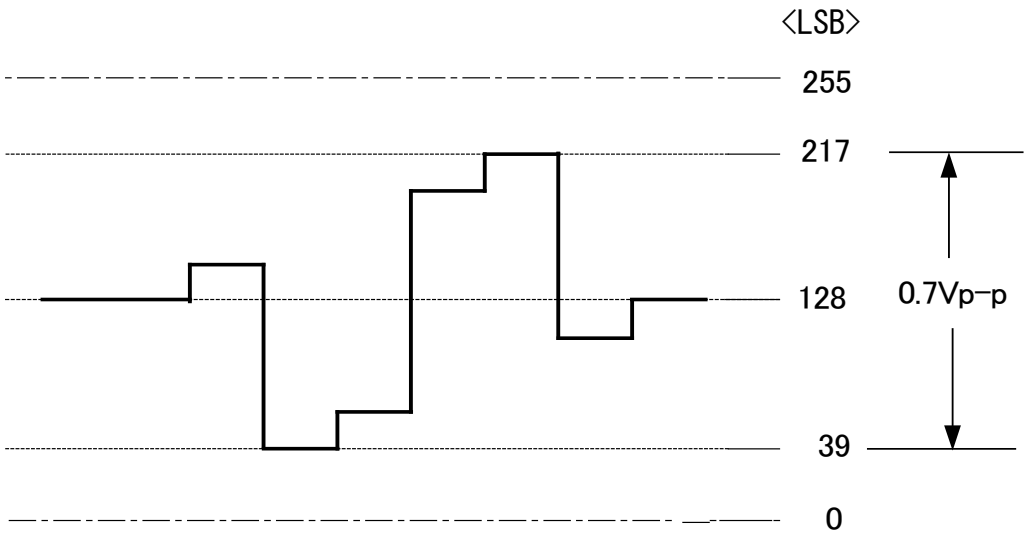


Fig.3 Typical input level to C/Cr./R (Component Cr) and Cb/B (Component Cb)



5.2.5 Output format

The output format (ITU-R BT.656/601) is below.

Output signal	Bit	Data rate	Description
Y [0-7]	8	13.5 MHz/27 MHz (ITU-R BT.601/656)	Y / YCbCr (ITU-R BT.601/656)
C [0-7]	8	6.75 MHz	Cb / Cr (CLK: 13.5 MHz)
CLK	1	13.5 MHz/27 MHz	864fH/1728fH: 625 line system 858fH/1716fH: 525 line system Polarity: negative (Initial setting)
HD	1	f H	Recovered horizontal sync signal
VD	1	f V	Recovered vertical sync signal

HD / VD pulse width in “Sync-through” mode

	525i system	625i system
HD pulse width	4.74 μs (128 cycle @ 27 MHz clock)	
VD pulse width	3.0 H	2.5 H or 3.0 H

*Notes

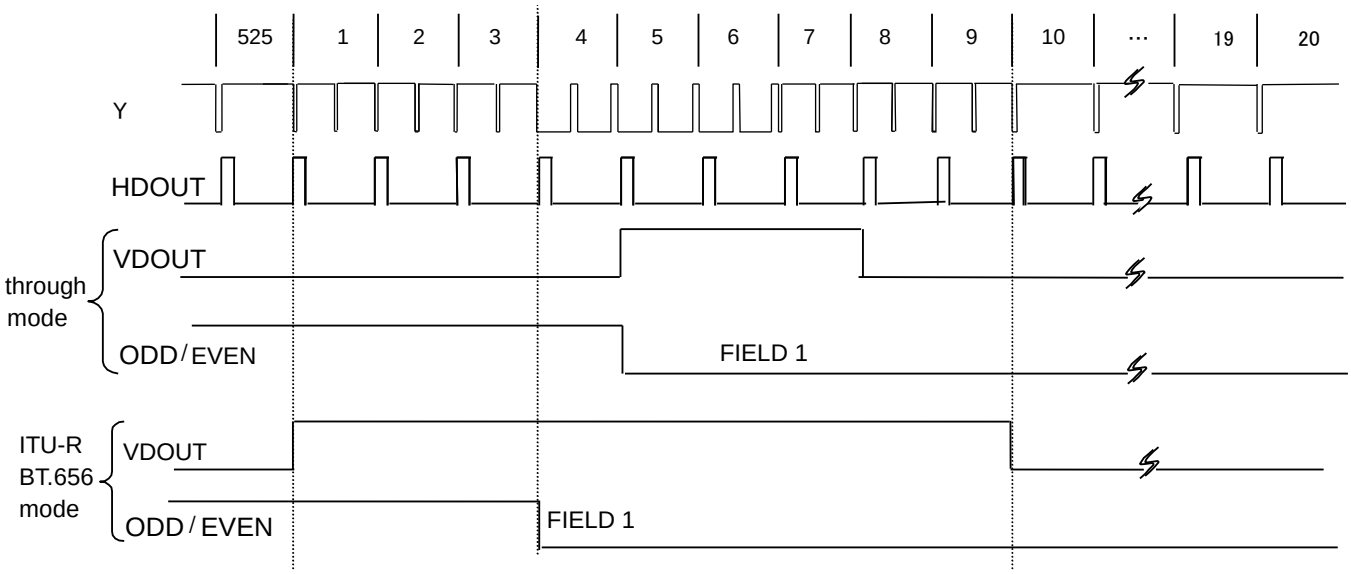
The HD pulse width used in ITU-R BT.656-compliant mode is the same as the zone defined from EAV to SAV.

If a non-standard signal is input during ITU-R BT.656-compliant mode, then the values may not necessarily be the values shown in the above chart.

The VD pulse is synchronized using the HD standard. As a result, if the H cycle jitters, then the VD width will also jitter. Also, in Through mode, the phase with the HD will be off 0.5 H in ODD/EVEN.

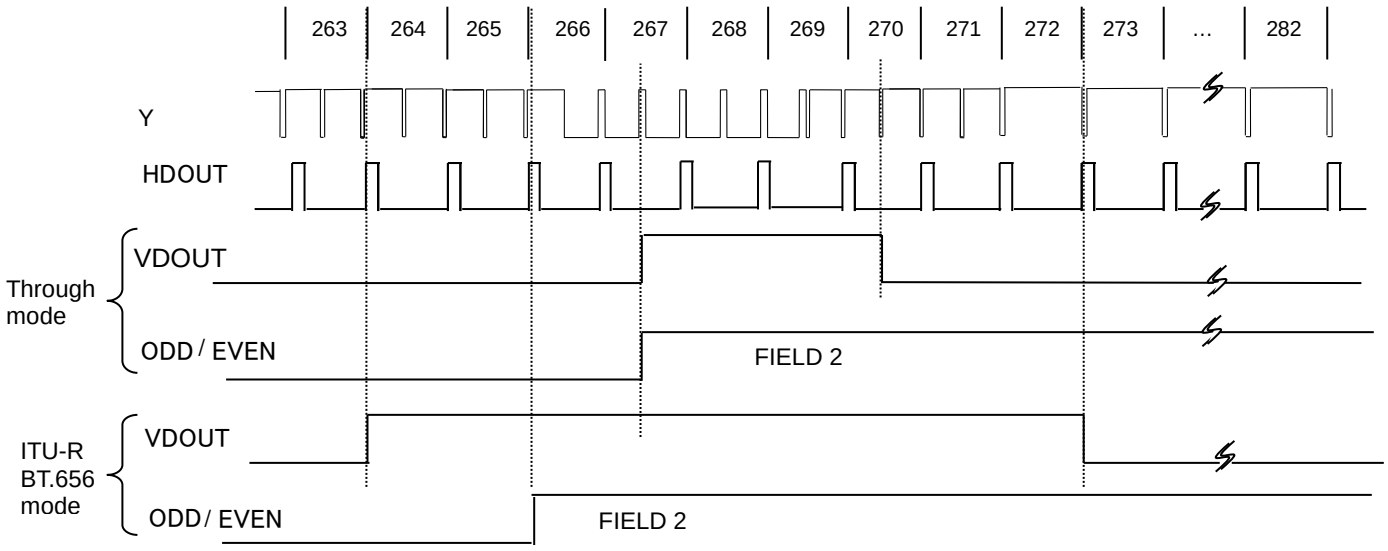
5.2.5.1. 525i/60Hz Input mode

(1st field **:** ODD)



Change of Through mode and ITU-R BT.656 mode
ITU-R BT.656**:** Field1; Line 4 EAV
Field Blanking ; Start → Line 1 EAV, Finish → Line 10 EAV

(2nd field :EVEN)

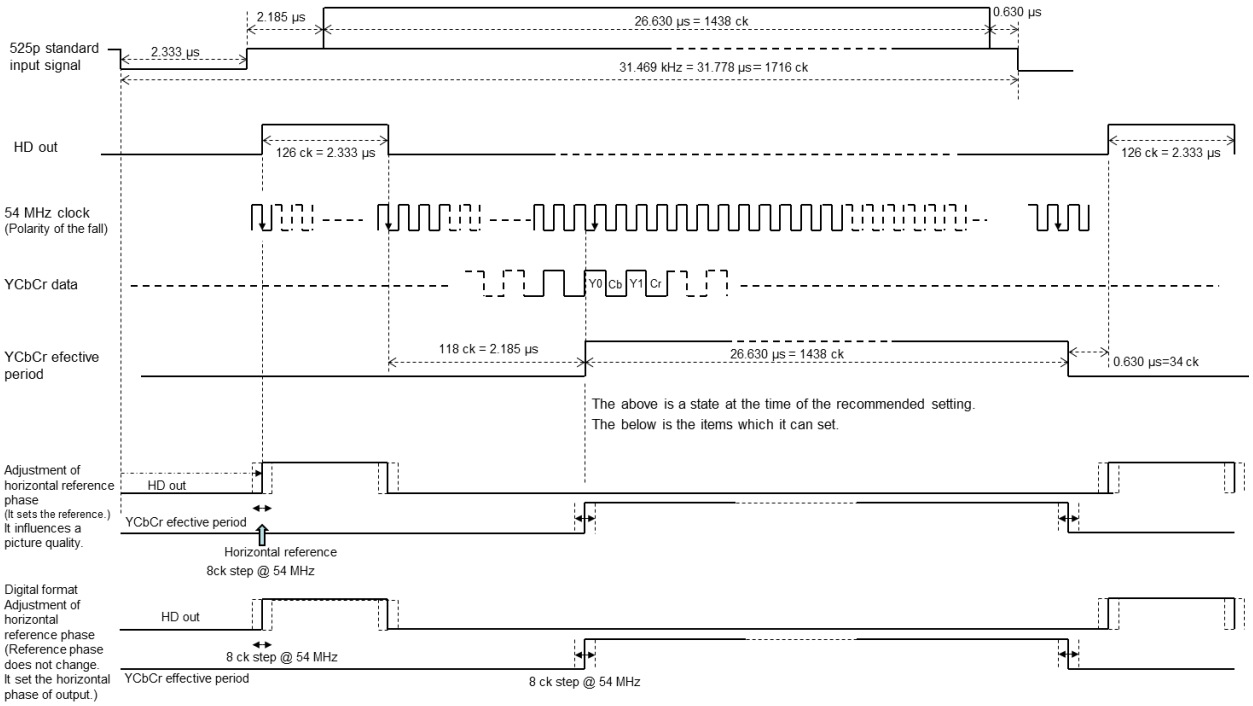


Change of Through mode and ITU-R BT.656 mode
ITU-R BT.656**:** Field 2; Line 266 EAV
Field Blanking ; Start → Line 264 EAV, Finish → Line 273 EAV

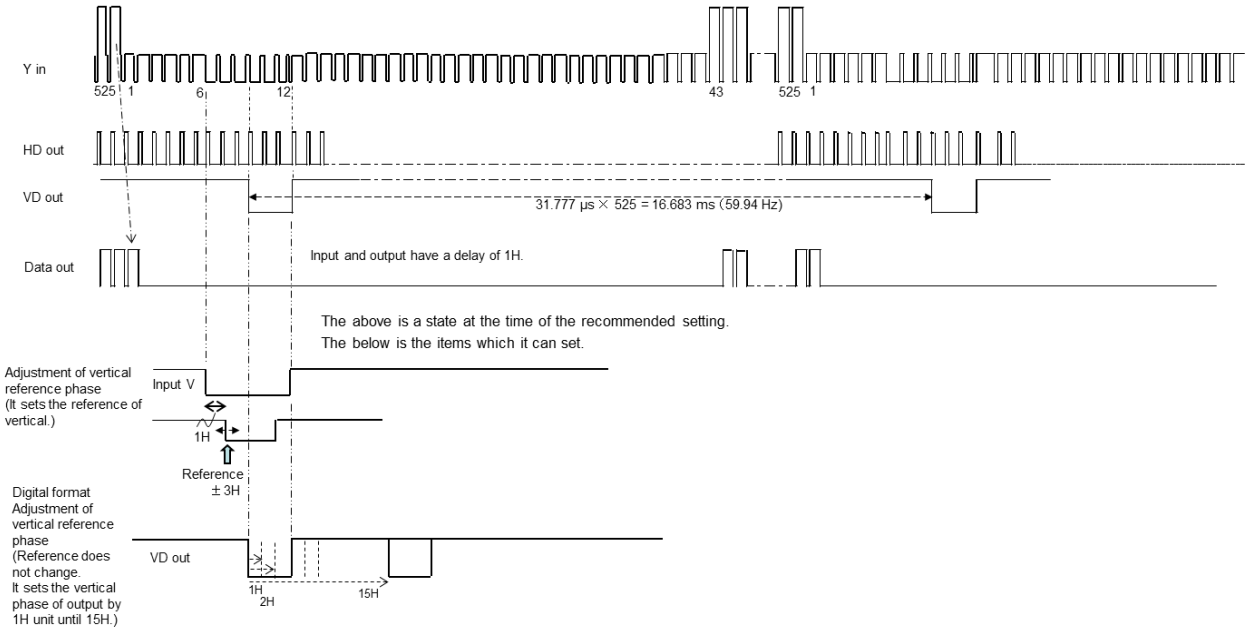
5.2.5.2. HD and VD timing when 480p/60Hz input

525p/59.94(fH = 31.469 kHz)@54 MHz_8bit output

H out (H:31.469kHz=1716ck_Effective horizontal period:26.630µs=1438ck)



V out （Vertical:525 line_Efective vertical :480 line）



6. Absolute Maximum rating

The maximum ratings are rated values which must not be exceeded during operation, even for an instant. Exceeding the maximum rating may result in destruction, degradation or other damage to the IC and other components. When designing applications for this IC, be sure that none of the maximum rating values will ever be exceeded.

Characteristics	Symbol	Rating	Unit
Power voltage1 (1.5 V system)	VDD1	-0.3 to VSS + 2.0	V
Power voltage2 (2.5 V system)	VDD2	-0.3 to VSS + 3.5	V
Power voltage3 (3.3 V system)	VDD3	-0.3 to VSS + 3.9	V
Input voltage (1.5 V system)	VIN1	-0.3 to VDD1 + 0.3	V
Input voltage (2.5 V system)	VIN2	-0.3 to VDD2 + 0.3	V
Input voltage (3.3 V system)	VIN3	-0.3 to VDD3 + 0.3	V
Input voltage (3.3 V system, 5 V withstand voltage)	VIN4 (Notes1)	-0.3 to VSS + 5.5	V
Potential difference between power pins (between 1.5 V system power pins)	ΔVDG1 (Notes2)	0.3	V
Potential difference between power pins (between 2.5 V system power pins)	ΔVDG2 (Notes2)	0.3	V
Potential difference between power pins (between 3.3 V system power pins)	ΔVDG3 (Notes2)	0.3	V
Power dissipation	PD (Notes3)	2190	mW
Storage temperature	Tstg	-40 to 125	°C

Note1**:** The withstand voltage for pins (SDA, SCL) is 5 V.

Note2**:** For each of 1.5 V and 2.5 V and 3.3 V, system power supply terminal is made into the same voltage. The maximum potential difference should not exceed rating for all power supply terminals then. In addition, potential difference between all V_{SS} terminal must be under 0.01 V in this status.

Note3**:** If you intended to use a temperature higher than Ta = 25°C, reduce by 21.9 mW per one degree (°C) increase.

7. Operating ranges

The TC90104AFG is not guaranteed to function correctly if it is used outside its specified power voltage rage (1.5 V system power**:** 1.40 V to 1.60 V, 2.5 V system power**:** 2.3 V to 2.7 V, 3.3 V system power**:** 3.0 V to 3.6V). Please use within the specified operating conditions.

If you temporarily leave and then return to the specified operating conditions, this IC's conditions will change, and so it is necessary to reset the IC's power to continue using it correctly within the specified operating conditions.

Characteristics	Corresponding terminal	Symbol	Min	Typ.	Max	Unit
Power voltage of digital block	10, 23, 37	VDD-D	1.4	1.5	1.6	V
Power voltage of I/O block	19, 26, 43	VDD-IO	3.0	3.3	3.6	V
Power voltage of XO block	6	VDDXO	2.3	2.5	2.7	V
Power voltage of PLL block	3	VDDPLL	2.3	2.5	2.7	V
Power voltage of analog block	1, 49, 58	VDDDA, VDDAD	2.3	2.5	2.7	V
Operating templature		Topr	-40	—	85	°C

8. Electrical characteristic

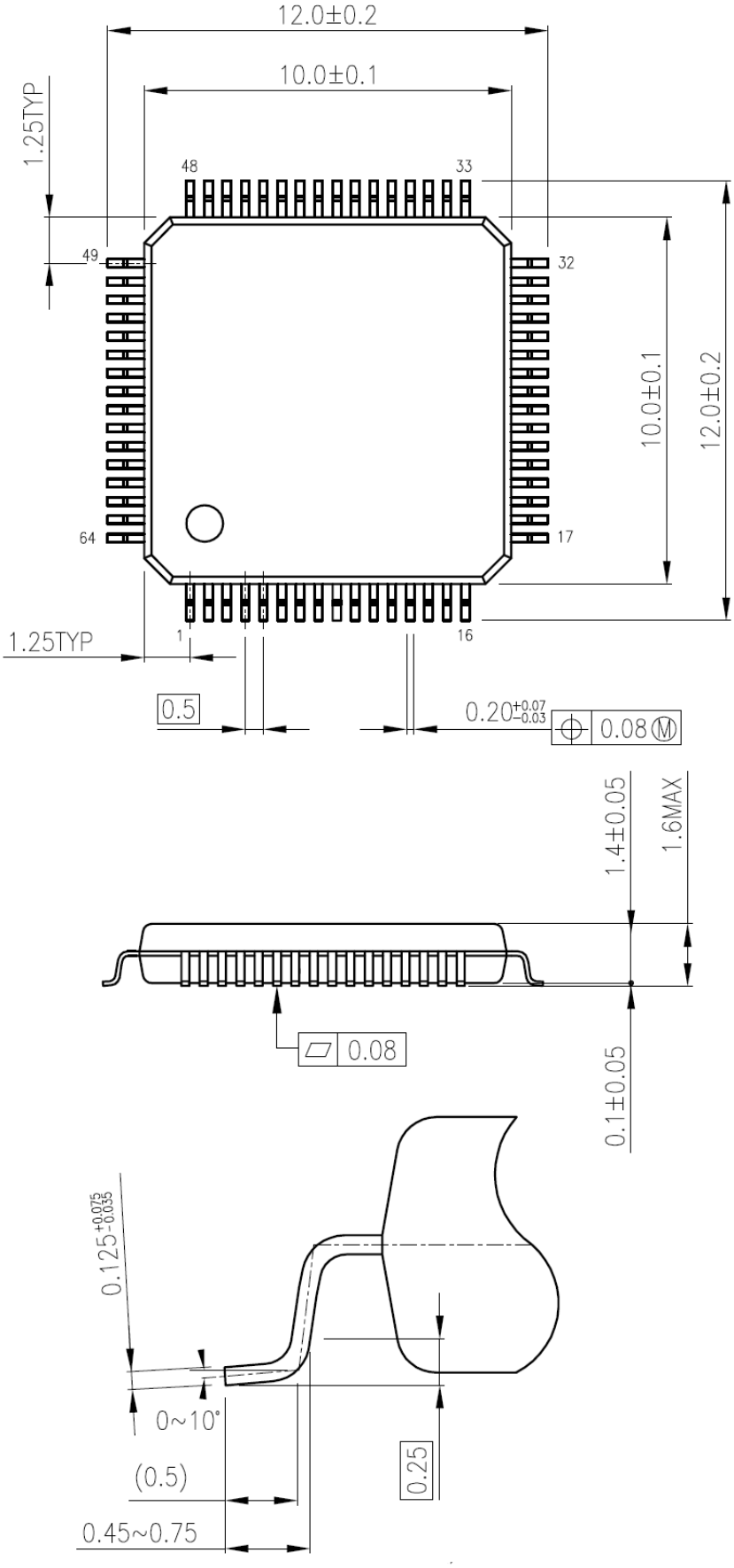
8.1 DC characteristic

(Ta = 25°C, 1.5 V system = 1.50 ± 0.1 V, 2.5 V system = 2.50 ± 0.2 V, 3.3 V system = 3.30 ± 0.3 V)

Characteristic	Terminal NO.	Symbol	Min	Typ.	Max	Unit	Note
Power supply current	10, 23, 37	IDD1 (1.5 V system)	–	46	70	mA	Depend on load at 3.3 V system.
	1, 3, 6, 49, 58	IDD2 (2.5 V system)	–	82	125	mA	
	19, 26, 43	IDD3 (3.3 V system)	–	10	–	mA	
Input voltage	13, 46, 47, 48, 61, 62	VIH	VDD3x0.8	–	VDD3	V	I/O input terminal of 3.3 V system
	11, 12						I/O input terminal of 5.0 V tlerant system
	13, 46, 47, 48, 61, 62	VIL	VSS	–	VDD3x0.2	V	I/O input terminal of 3.3 V system
	11,12						I/O input terminal of 5.0 V tlerant system
Input current	13, 46, 47, 48, 61, 62	IIH	-10	–	10	μA	I/O input terminal of 3.3 V system
	11, 12						I/O input terminal of 5.0 V tlerant system
	13, 46, 47, 48, 61, 62	IIL	-10	–	10	μA	I/O input terminal of 3.3 V system
	11, 12						I/O input terminal of 5.0 V tlerant system
Output voltage	15, 16, 17, 18, 20, 21, 24, 25, 27, 28, 30, 31, 32, 33, 35, 36, 38, 39, 41, 42, 44, 45	V_{OH}	VDD3-0.6	–	VDD3	V	I/O output terminal of 3.3 V system when load current: -4 mA
		V_{OL}	VSS	–	0.4	V	I/O output terminal of 3.3 V system when load current: +4 mA

9. Package

LOFP64-P-1010-0.50E **Unit: mm**



Weight: 0.4 g (Typ.)

10. Revision History

Date	Revision	Contents
2015/10/16	1.00	First edition

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