

## 74FR16245 16-Bit Transceiver with 3-STATE Outputs

### General Description

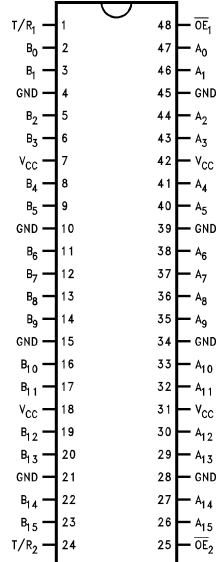
The 74FR16245 contains sixteen non-inverting bidirectional buffers with 3-STATE outputs and is intended for bus-oriented applications. Current sinking capability is 64 mA on both the A and B Ports. The device is byte controlled. Each byte has separate control inputs which can be shorted together for full 16-bit operation. The transmit/receive ( $T/\bar{R}_n$ ) inputs determine the direction of data flow through the transceiver. The output enable ( $\overline{OE}_n$ ) inputs disable both A and B Ports by placing them in a high impedance state.

### Features

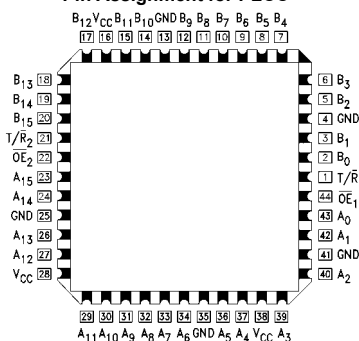
- Non-inverting buffers
- Bidirectional data paths
- A and B output sink capability of 64 mA, source capability of 15 mA
- Separate control pins for each byte
- Guaranteed pin-to-pin skew
- Low 3-STATE  $I_{IL}$
- 16-Bit version of the 74F245 or 74F645

### Connection Diagrams

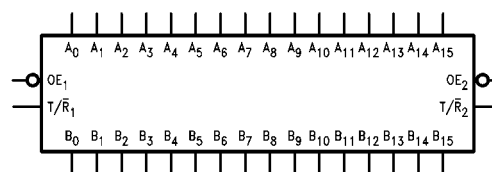
Pin Assignment for SSOP



Pin Assignment for PLCC



### Logic Symbol



**\* For complete Rochester ordering guide, please refer to page 2 \***

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# 74FR16245

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## Rochester Ordering Guide

Rochester Part Number	OCM Part Number	Package	Temperature
74FR16245QC	74FR16245QC	LDCC-44	0° to +70°C
74FR16245QCX	74FR16245QCX	LDCC-44	0° to +70°C
74FR16245SSC	74FR16245SSC	SSOP-48	0° to +70°C
74FR16245SSCX	74FR16245SSCX	SSOP-48	0° to +70°C

## Pin Descriptions

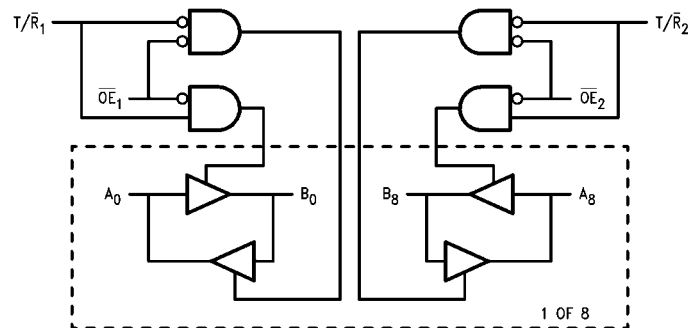
Pin Names	Description
$\overline{\text{OE}}_n$	Output Enable Input
$\text{T}/\overline{\text{R}}_n$	Transmit/Receive Input
$\text{A}_0\text{--}\text{A}_{15}$	A Bus Inputs/3-STATE Outputs
$\text{B}_0\text{--}\text{B}_{15}$	B Bus Inputs/3-STATE Outputs

## Truth Table

Inputs				Output Operating Mode	
Byte1 (0:7)		Byte2 (8:15)			
$\overline{OE}_1$	$T/R_1$	$\overline{OE}_2$	$T/R_2$	Byte1 (0:7)	Byte2 (8:15)
L	L	H	X	Bus B Data to A	High Z State
L	H	H	X	Bus A Data to B	High Z State
H	X	L	L	High Z State	Bus B Data to A
H	X	L	H	High Z State	Bus A Data to B
L	L	L	L	Bus B Data to A	Bus B Data to A
L	H	L	H	Bus A Data to B	Bus A Data to B
H	X	H	X	High Z State	High Z State

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial

## Logic Diagram



## Absolute Maximum Ratings<sup>(Note 1)</sup>

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output	
in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	−0.5V to V <sub>CC</sub>
3-STATE Output	−0.5V to +5.5V
Current Applied to Output	
in LOW State (Max)	Twice the Rated I <sub>OL</sub> (mA)
ESD Last Passing Voltage (Min)	4000V

## Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	V <sub>CC</sub>	Conditions
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			−1.2	V	Min	I <sub>IN</sub> = −18 mA
V <sub>OH</sub>	Output HIGH Voltage	2.4 2.0	2.8 2.44		V	Min	I <sub>OH</sub> = −3 mA I <sub>OH</sub> = −15 mA (A <sub>n</sub> , B <sub>n</sub> )
V <sub>OL</sub>	Output LOW Voltage		0.45	0.55	V	Min	I <sub>OL</sub> = 64 mA (A <sub>n</sub> , B <sub>n</sub> )
I <sub>IH</sub>	Input HIGH Current			5.0	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Break-Down Test			7.0	μA	Max	V <sub>IN</sub> = 7.0V (OE <sub>n</sub> , T/ $\overline{R}_n$ )
I <sub>BVIT</sub>	Input HIGH Current Breakdown Test (I/O)			0.1	mA	Max	V <sub>IN</sub> = 5.5V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>IL</sub>	Input LOW Current			−150 −100	μA	Max	V <sub>IN</sub> = 0.5V (T/ $\overline{R}_n$ , A <sub>n</sub> , B <sub>n</sub> ) V <sub>IN</sub> = 0.5V (OE <sub>n</sub> )
I <sub>OS</sub>	Output Short-Circuit Current	−100		−225	mA	Max	V <sub>OUT</sub> = 0V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>IH</sub> + I <sub>OZH</sub>	Output Leakage Current		0	25	μA	Max	V <sub>OUT</sub> = 2.7V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>IL</sub> + I <sub>OZL</sub>	Output Leakage Current		−20	−150	μA	Max	V <sub>OUT</sub> = 0.5V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>CEX</sub>	Output HIGH Leakage Current			50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub> (A <sub>n</sub> , B <sub>n</sub> )
V <sub>ID</sub>	Input Leakage Test	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Circuit Leakage Current			3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>ZZ</sub>	Bus Drainage Test			100	μA	0.0	V <sub>OUT</sub> = 5.25V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>CCH</sub>	Power Supply Current		70	105	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current		127	165	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current		71	105	mA	Max	V <sub>O</sub> = HIGH Z
C <sub>IN</sub>	Input Capacitance		8.0		pF	5.0	OE, T/ $\overline{R}$
			17.0		pF	5.0	A <sub>n</sub> , B <sub>n</sub>

## AC Electrical Characteristics

Symbol	Parameter	T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF		Unit
		Min	Typ	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay	1.3	2.7	4.3	1.3	4.3	ns
t <sub>PHL</sub>	A <sub>n</sub> to B <sub>n</sub> or B <sub>n</sub> to A <sub>n</sub>	1.3	2.2	4.3	1.3	4.3	
t <sub>PZH</sub>	Output Enable Time	3.9	6.9	13.9	3.9	13.9	ns
t <sub>PZL</sub>		3.9	9.7	13.9	3.9	13.9	
t <sub>PHZ</sub>	Output Disable Time	1.8	3.9	6.3	1.8	6.3	ns
t <sub>PLZ</sub>		1.8	4.4	6.3	1.8	6.3	

## Extended AC Characteristics

Symbol	Parameter	T <sub>A</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF 16 Outputs Switching (Note 4)		T <sub>A</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 250 pF (Note 5)		Unit
		Min	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay	1.3	5.8	3.2	8.2	ns
t <sub>PHL</sub>	A <sub>n</sub> to B <sub>n</sub> or B <sub>n</sub> to A <sub>n</sub>	1.3	5.8	3.2	8.2	
t <sub>PZH</sub>	Output Enable Time	3.9	14.6			ns
t <sub>PZL</sub>		3.9	14.6			
t <sub>PHZ</sub>	Output Disable Time	1.8	6.3			ns
t <sub>PLZ</sub>		1.8	6.3			
t <sub>OSHL</sub> (Note 3)	Pin-to-Pin Skew for HL Transitions		1.2			ns
t <sub>OSLH</sub> (Note 3)	Pin-to-Pin Skew for LH Transitions		2.2			ns
t <sub>OST</sub> (Note 3)	Pin-to-Pin Skew for HL/LH Transitions		2.5			ns

**Note 3:** Skew is defined as the absolute value of the difference between the actual propagation delays for any two outputs of the same device. The specification applies to any outputs switching HIGH-to-LOW (t<sub>OSHL</sub>) LOW-to-HIGH (t<sub>OSLH</sub>), or HIGH-to-LOW and/or LOW-to-HIGH (t<sub>OST</sub>). Specifications guaranteed with all outputs switching in phase.

**Note 4:** This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase, i.e., all LOW-to-HIGH, HIGH-to-LOW, 3-STATE-to-HIGH, etc.

**Note 5:** These specifications guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

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