MN103SL07 Series

32-bit Single-chip Microcontroller

■ Overview

The MN103S is a 32-bit microcontroller combining ease of use intended for programs development in the C language with a simple, high-performance architecture made possible through pursuit of cost performance.
This LSI series is well suited for in-vehicle electrical compressor control, in-vehicle body control, air conditioner, electrical power control and other applications.

Built around a compact 32-bit CPU with a basic instruction word length of 1 byte, this LSI includes internal memory for instructions and data, DMA controller, a clock generator, bus controller, interrupt controller, watchdog timer, standard peripheral circuitry such as timers and serial interfaces, PWM circuit best suited to controlling 3-phase motors, arithmetic unit for speed-up of inverter control and A/D converters for motor position control. The MN103S Series' high-speed CPU coupled with abundance of peripheral features provides an easy means of developing low-cost, high-performance and multifunctional system on LSI for motor and power control applications requiring fast response - a feature previously unavailable with conventional microcontrollers.

■ Product Summary

This datasheet describes the following model.

Model	ROM Size	RAM Size	Classification	Package
MN103SFL7G	128 KB	12 KB	Flash EEPROM version	TQFP048-P-0707F
MN103SFL7K	256 KB			

■ Features

- CPU core

  MN103S core
  4 GB of memory space (for instructions / data)
  LOAD/STORE architecture with 5-stage pipeline
  46 basic instructions + 23 extended arithmetic instructions
  6 addressing modes
  Instruction set of 1 byte in word length
  Extended arithmetic unit incorporated (high-speed multiply/divide instructions)
  Machine cycle: 16.7 ns (oscillation frequency: 10 MHz, 6 multiplying)
  Operation mode: NORMAL mode, SLEEP mode, HALT mode, STOP mode

- Oscillation Circuit

  External high-speed oscillation (crystal/ ceramic)
  Internal high-speed oscillation (10 MHz)
  Internal low-speed oscillation for Watchdog timer 2 (35 kHz)

- Clock Multiplication Circuit

  PLL output clock (IOCLK): High-speed oscillation is multiplied by 3 to 15

- Internal Memory

  ROM 128 KB (MN103SFL7G), ROM 256 KB (MN103SFL7K)
  RAM 12 KB

- DMA Controller

  Channel : 2 ch
  Transfer requests : 46 types
  (External interrupts: 8, Timer: 17, Serial: 6, IIC: 3, A/D converter: 4, CAN: 1, LIN: 1, PWM: 4, Power Voltage Detection: 1, Software: 1)
  Transfer mode : 3 modes (One word transfer / Burst transfer / Intermittent transfer)

■ Features (continued)

- Interrupts

Internal interrupts 48 interrupts

Watchdog timer overflow interrupts
System error interrupts
Fail safe function interrupts
(Watchdog timer 2 overflow, Clock error detection, Register protect)
Power voltage detection interrupts

<Timer Interrupts>
Timer 0 underflow interrupt
Timer 1 underflow interrupt
Timer 2 underflow interrupt
Timer 3 underflow interrupt
Timer 4 underflow interrupt
Timer 5 underflow interrupt
Timer 6 underflow interrupt
Timer 7 underflow interrupt
Timer 16 overflow/underflow interrupt
Timer 16 compare/capture A interrupt
Timer 16 compare/capture B interrupt
Timer 18 overflow/underflow interrupt
Timer 18 compare/capture A interrupt
Timer 18 compare/capture B interrupt
Timer 19 overflow/underflow interrupt
Timer 19 compare/capture A interrupt
Timer 19 compare/capture B interrupt

<Serial interface>
Serial 0 UART reception completion interrupt
Serial 0 clock synchronous communication completion /UART transmission completion interrupt
Serial 0 transmission data buffer empty interrupt
Serial 1 UART reception completion interrupt
Serial 1 clock synchronous communication completion /UART transmission completion interrupt
Serial 1 transmission data buffer empty interrupt
IIC stop condition detection interrupt
IIC communication end interrupt
IIC transmission data buffer empty interrupt
LIN interrupt
CAN interrupt

<PWM>
PWM0 overflow interrupt
PWM0 underflow interrupt
PWM0 synchronous A/D conversion start A interrupt
PWM0 synchronous A/D conversion start B interrupt

<A/D>
A /D 0 conversion end interrupt
A /D 0 conversion end B interrupt
A /D 1 conversion end interrupt
A /D 1 conversion end B interrupt

■ Features (continued)

- Interrupts (continued)

<DMA>
DMA0 transfer end interrupt
DMA0 request after DMA transfer end interrupt
DMA0 transfer request overflow interrupt
DMA1 transfer end interrupt
DMA1 request after DMA transfer end interrupt
DMA1 transfer request overflow interrupt

External interrupts : 8 interrupts
External interrupt pins : From IRQ00 to IRQ07
Interrupt detection condition : Each edge, both edges, high-level and low-level detection
Each interrupt detection condition is able to filtering with the noise filter

- Timer Counter

8-bit timer 8 sets
16-bit timer 3 sets

Timer 0 (8-bit timer)
Interval timer, Timer pulse output, Event count, Baud rate timer
Count clock source: IOCLK, IOCLK/8, IOCLK/32, IOCLK/128, TM0IO pin input, Timer 1 underflow, Timer 2 underflow

Timer 1 (8-bit timer)
Interval timer, Timer pulse output, Event count, Baud rate timer, Cascade connection
Count clock source: IOCLK, IOCLK/8, IOCLK/32, IOCLK/128, TM1IO pin input, Timer 0 underflow, Timer 2 underflow

Timer 2 (8-bit timer)
Interval timer, Baud rate timer, Cascade connection
Count clock source: IOCLK, IOCLK/8, IOCLK/32, IOCLK/128, Timer 0 underflow, Timer 1 underflow

Timer 3 (8-bit timer)
Interval timer, Baud rate timer, Cascade connection
Count clock source: IOCLK, IOCLK/8, IOCLK/32, IOCLK/128, Timer 0 underflow, Timer 1 underflow, Timer 2 underflow

Timer 4 (8-bit timer)
Interval timer, Timer pulse output, Event count
Count clock source: IOCLK, IOCLK/8, IOCLK/32, IOCLK/128, TM4IO pin input, Timer 5 underflow, Timer 6 underflow

Timer 5 (8-bit timer)
Interval timer, Timer pulse output, Event count, Cascade connection
Count clock source: IOCLK, IOCLK/8, IOCLK/32, IOCLK/128, TM5IO pin input, Timer 4 underflow, Timer 6 underflow

Timer 6 (8-bit timer)
Interval timer, Timer pulse output, Event count, Cascade connection
Count clock source: IOCLK, IOCLK/8, IOCLK/32, IOCLK/128, TM6IO pin input, Timer 4 underflow, Timer 5 underflow

Timer 7 (8-bit timer)
Interval timer, Timer pulse output, Event count, Cascade connection
Count clock source: IOCLK, IOCLK/8, IOCLK/32, IOCLK/128, TM7IO pin input, Timer 4 underflow,
Timer 5 underflow, Timer 6 underflow

■ Features (continued)

- Timer Counter (continued)

Timer 16 (16-bit timer)

Interval timer, Event count, Up/down count, Timer output,
PWM output, Input capture, one-shot output, External trigger start
Count clock source: IOCLK, IOCLK/8, Timer 4 underflow, Timer 5 underflow, TM16BIO pin input

Timer 18 (16-bit timer)

Interval timer, Event count, Up/down count, Timer output,
PWM output (output to 6 ports all at once is possible), Input capture, one-shot output, External trigger start
Count clock source: IOCLK, IOCLK/8, IOCLK/64, Timer 7 underflow, TM18BIO pin input

Timer 19 (16-bit timer)

Interval timer, Event count, Up/down count, External trigger start,
Start by PWM0 overflow/underflow interrupt, A/D conversion start trigger generation
Count clock source: IOCLK, IOCLK/8, Timer 6 underflow, Timer 7 underflow, TM19BIO pin input

- Watchdog Timer

Count clock Machine cycle
Detection time (External or internal) high-speed oscillation cycle $\times 2^{16}$ to 2^{24}
Generates non-maskable interrupt at detection
Generates hard-reset at second consecutive overflow

- Watchdog Timer 2

Count clock Internal low-speed oscillation
Detection time 457.14 µs to 936.23 ms
Generates non-maskable interrupt at detection
Generates hard-reset at second consecutive overflow

- A /D Converter

Minimum conversion time 0.6 µs
12 bit: 2 converters (8 channels, 7channels)
A/D conversion start trigger pin output
A/D conversion start trigger is in synchronization with complementary 3-phase PWM cycle and 16-bit timer
Input signal amplification functions, 2 sets of difference input amplification (4 pins)
Gain setting 2.03 to 19.45 times
Input range ± 1 V (Negative voltage input is enabled)
Offset cancel function (input short control, input chopping control)
Half value of power supply voltage input function
5 potentials between AVDD to AVSS.

- Complementary 3-phase PWM output

Min. resolution: 16.7 ns
Triangular and saw-tooth waves output
Incorporates a dead time insertion circuit
Can overwrite registers by double buffer during PWM operation
PWM output protection circuit supporting external interrupts and non-maskable interrupt
Output timing varying function
A/D conversion start trigger, 16-bit timer start trigger output

■ Features (continued)

- CAN Controller

Channels : 1 channel
CAN 2.0B specification basis
Communication method : NRZ (Non-Return to Zero)
Transmission line : Interactive 2-wire serial communication
Communication speed: Max 1 Mbps
Data length : 0 to 8 byte
Message frame : Standard frame and extended frame are supported
(Standard frame format ID: 11 bits, Extended frame format ID: 29 bits)
Buffer size : 32 messages (32 × 132 bit)
Interrupt: 1 interrupt
Interrupt requests:
Bus-off state, error active state
Error alert state (When the error counter is over 96.)
Release the error alert state (When the error counter is under 96.)
Transmission/Reception end
Transmission/Reception error (Ack/Form/Stuff/ Bit1/ Bit0/CRC error)

- Serial Interface 2 channels

Serial 0 (Hardware LIN/Full duplex UART / Synchronous serial interface)
Synchronous serial interface
Overrun error detection
Transfer clock source: 1/2, 1/4, 1/16 and 1/64 of timer 0 underflow,
1/2, 1/4, 1/16 and 1/64 of timer 1 underflow,
1/2, 1/4, 1/16 and 1/64 of timer 2 underflow,
1/2, 1/4, 1/16 and 1/64 of timer 3 underflow, IOCLK/2, IOCLK/4, SBT0 pin
Transfer clock division value selection : Divided by 8, 16
Can be selected as the first bit to be transferred, Any transfer size from 2 to 8 bits can be selected.
Can be continuously transmitted, received or transmitted and received.
Maximum transfer rate: 5.0 Mbps

Full duplex UART
Parity check, Overrun and framing error detection
Transfer clock source: 1/2, 1/4, 1/16, and 1/64 of timer 0 underflow,
1/2, 1/4, 1/16, and 1/64 of timer 1 underflow,
1/2, 1/4, 1/16, and 1/64 of timer 2 underflow,
1/2, 1/4, 1/16, and 1/64 of timer 3 underflow,
IOCLK/2, IOCLK/4
Transfer clock division value selection : Divided by 8, 16
Can be selected as the first bit to be transferred, Any transfer size from 7 to 8 bits can be selected.
Continuous transmission, reception, and transmission/reception
Maximum transfer rate: 300 kbps

Hardware LIN
Operate in conjunction with Timer 4, 5 and 16.
Master communication: Synch Break field transmission
Slave communication: Wake-up reception, Synch Break field reception, Synch field reception, Check sum arithmetic
Error detection: Check sum error, bit error

■ Features (continued)

- Serial Interface

Serial 1 (Multi master IIC / Full duplex UART / Synchronous serial interface)

Synchronous serial interface

Overrun error detection

Transfer clock source: 1/2, 1/4, 1/16 and 1/64 of timer 0 underflow,
1/2, 1/4, 1/16 and 1/64 of timer 1 underflow,
1/2, 1/4, 1/16 and 1/64 of timer 2 underflow,
1/2, 1/4, 1/16 and 1/64 of timer 3 underflow,
IOCLK/2, IOCLK/4, SBT1 pin

Transfer clock division value selection : Divided by 8, 16

Can be selected as the first bit to be transferred, Any transfer size from 2 to 8 bits can be selected.

Can be continuously transmitted, received or transmitted and received.

Maximum transfer rate: 5.0 Mbps

Full duplex UART

Parity check, Overrun and framing error detection

Transfer clock source: 1/2, 1/4, 1/16, and 1/64 of timer 0 underflow,
1/2, 1/4, 1/16, and 1/64 of timer 1 underflow,
1/2, 1/4, 1/16, and 1/64 of timer 2 underflow,
1/2, 1/4, 1/16, and 1/64 of timer 3 underflow,
IOCLK/2, IOCLK/4

Transfer clock division value selection : Divided by 8, 16

Can be selected as the first bit to be transferred, Any transfer size from 7 to 8 bits can be selected.

Continuous transmission, reception, and transmission/reception

Maximum transfer rate: 300 kbps

Multi master IIC

7, 10-bit slave address is settable

General call communication mode is supported

Transfer clock source: 1/2, 1/4, 1/16, and 1/32 of timer 0 underflow,
1/2, 1/4, 1/16, and 1/32 of timer 1 underflow,
1/2, 1/4, 1/16, and 1/32 of timer 2 underflow,
1/2, 1/4, 1/16, and 1/32 of timer 3 underflow,
IOCLK/2, IOCLK/4

Transfer clock division value selection : Divided by 8

- Power Supply Voltage Detection

Detection level 4.15 V ± 0.25 V (At falling voltage)
4.25 V ± 0.25 V (At rising voltage)

When power supply voltage become equal to detection level, interrupt is generated.

- Auto Reset Circuit

Detection level 3.50 V ± 0.20 V (At falling voltage)
3.65 V ± 0.35 V (At rising voltage)

When power supply voltage is under detection level, reset is generated.

- Clock Monitoring Function

Frequency error of the external high-speed oscillation (include PLL output) can detect.

When the error is detected, reset is generated.

■ Features (continued)

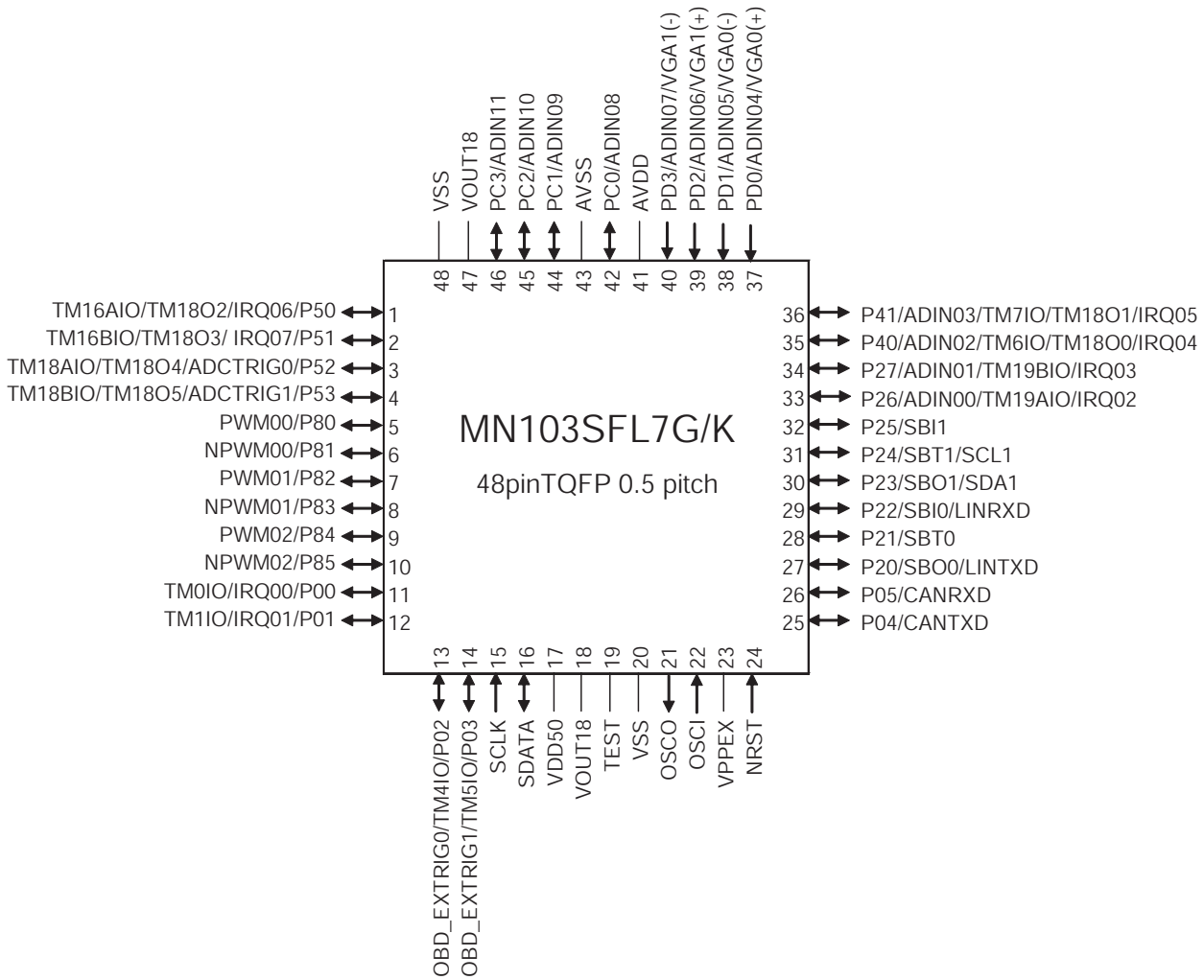
- Port / pins

I/O ports	30	pins
Motor control output	6	pins
External interrupt	8	pins
A/D input	8	pins
Input ports	4	pins
VGA, A/D input	4	pins
Special pins	14	pins
Reset input pin	1	pin
Oscillation pin	2	pins
Test mode input pin	2	pins
Power pin	7	pins
On-board debugger pin	2	pins

- Package Code name

  TQFP48 (7 mm square, 0.5 mm pitch, halogen free)
  TQFP048-P-0707F

■ Pin Description



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