UTC UNISONIC TECHNOLOGIES CO., LTD

4051

8-CHANNEL ANALOG MULTIPLEXERS/DEMULTIPLEXERS
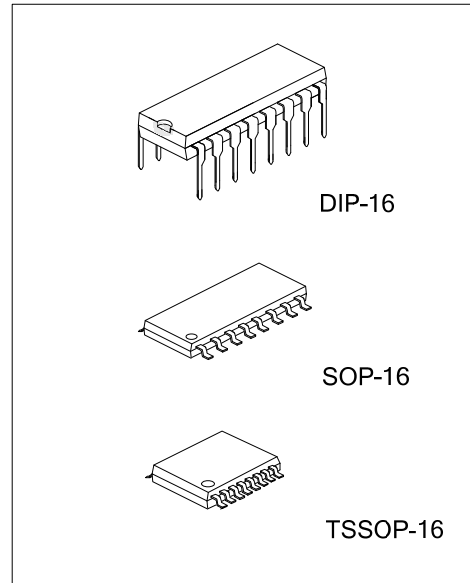

DIP-16

SOP-16

TSSOP-16

■ DESCRIPTION

UTC **4051** is single 8-channel analog multiplexers/demultiplexers for application as digitally–controlled analog switches.

The device has three binary control inputs and an inhibit input. It feature low ON impedance and very low OFF leakage current. Control of analog signals up to the complete supply voltage range can be achieved.

■ FEATURES

* Wide Analog Voltage Range: V_{DD}–V_{EE} = 3V~18V.
  (Note: V_{EE} must be $\leqq V_{SS}$)
* Break-Before-Make Switching Eliminates Channel Overlap.
* Linearized Transfer Characteristics
* Implement an SP8T solid state switch effectively.
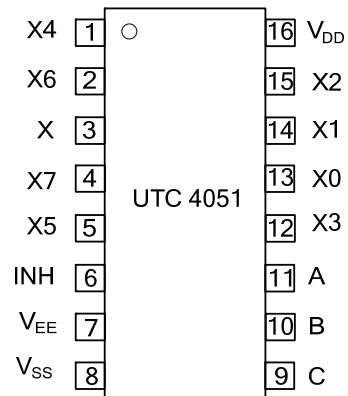* Pin–to–Pin Replacement for CD4051

■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
4051L-D16-T	4051G-D16-T	DIP-16	Tube
-	4051G-S16-R	SOP-16	Tape Reel
-	4051G-P16-R	TSSOP-16	Tape Reel

4051L-D16-T

— (1)Packing Type

— (2)Package Type

— (3)Green Package

(1) T: Tube, R: Tape Reel

(2) D16: DIP-16, S16: SOP-16, P16: TSSOP-16

(3) L: Lead Free, G: Halogen Free and Lead Free

■ MARKING

DIP-16	SOP-16 / TSSOP-16

DIP-16:
16 15 14 13 12 11 10 9
UTC □□□□ → Date Code
4051□ L: Lead Free
□□ → G: Halogen Free
□□ → Lot Code
1 2 3 4 5 6 7 8

SOP-16 / TSSOP-16:
16 15 14 13 12 11 10 9
UTC□□□□ → Date Code
4051G
□□ → Lot Code
1 2 3 4 5 6 7 8

■ **PIN CONFIGURATION**

```
         X4  [1]  ○        [16]  V_DD
         X6  [2]           [15]  X2
          X  [3]           [14]  X1
         X7  [4]  UTC 4051 [13]  X0
         X5  [5]           [12]  X3
        INH  [6]           [11]  A
       V_EE  [7]           [10]  B
       V_SS  [8]            [9]  C
```

■ **PIN DESCRIPTION**

PIN No.	SYMBAL	I/O	NAME AND FUNCTION
3	X	I/O	Common Input/Output
6	INH	I	Inhibit Inputs
7	V_{EE}		Supply Voltage
8	V_{SS}		Ground
11,10,9	A,B,C	I	Binary Control Inputs
13,14,15,12,1,5,2,4	X0~X7	I/O	Independent Inputs/Outputs
16	V_{DD}		Positive Supply Voltage

■ **ABSOLUTE MAXIMUM RATING**

PARAMETER	SYMBOL	RATINGS	UNIT
DC Supply Voltage (Referenced to V_{EE}, $V_{SS} \geqq V_{EE}$)	V_{DD}	-0.5 ~ +18	V
Input or Output Voltage (DC or Transient) (Referenced to V_{SS} for Control Inputs and V_{EE} for Switch I/O)	V_{IN}, V_{OUT}	-0.5 ~ V_{DD} +0.5	V
Input Current (DC or Transient), per Control Pin	I_{IN}	±10	mA
Switch Through Current	I_{SW}	±25	mA
Power Dissipation	P_D	500	mW
Derating above 65℃		7	mW/°C
Junction Temperature	T_J	125	°C
Operating Temperature	T_{OPR}	-40 ~ +125	°C
Storage Temperature	T_{STG}	-40 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ **ELECTRICAL CHARACTERISTICS** (T_A=25℃, unless otherwise specified.)

| PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY REQUIREMENTS (Voltages Referenced to V_{EE})							
Power Supply Voltage Range		V_{DD}	$V_{DD} - 3.0 \geqq V_{SS} \geqq V_{EE}$	3		18	V
Quiescent Current per Package	V_{DD}=5V	I_Q	Control Inputs: V_{IN} = V_{SS} or V_{DD} Switch I/O: $V_{EE} \leqq V_{I/O} \leqq V_{DD}$, $\Delta V_{SW} \leqq 500mV$(Note 2)		0.005	5	µA
	V_{DD}=10V				0.010	10	
	V_{DD}=15V				0.015	20	
Total Supply Current (Dynamic Plus Quiescent, Per Package)	V_{DD}=5V	$I_{D(AV)}$	T_A=25℃ only (The channel component, $(V_{IN}-V_{OUT})/Ron$, is not included.)		(0.07 µA/kHz) f + I_Q		µA
	V_{DD}=10V				(0.20 µA/kHz) f + I_Q		
	V_{DD}=15V				(0.36 µA/kHz) f + I_Q		
SWITCHES IN/OUT AND COMMONS OUT/IN -- X, Y, Z (Voltages Referenced to V_{EE})							
Recommended Peak–to–Peak Voltage Into or Out of the Switch		$V_{I/O}$	Channel On or Off	0		V_{DD}	V_{PP}
Recommended Static or Dynamic Voltage Across the Switch		ΔV_{SW}	Channel On	0		600	mV
Output Offset Voltage		$V_{O(OFF)}$	V_{IN} = 0V, No Load		10		µV
ON Resistance	V_{DD}=5V	R_{ON}	$\Delta V_{SW} \leqq 500mV$ V_{IN} = V_{IL} or V_{IH} (Control), V_{IN} = 0 to V_{DD} (Switch)		250	1050	Ω
	V_{DD}=10V				120	500	
	V_{DD}=15V				80	280	
ΔON Resistance Between Any Two Channels in the Same Package	V_{DD}=5V	ΔR_{ON}			25	70	Ω
	V_{DD}=10V				10	50	
	V_{DD}=15V				10	45	
Off–Channel Leakage Current		I_{OFF}	V_{IN} = V_{IL} or V_{IH} (Control) Channel to Channel or Any One Channel, V_{DD}=15V		±0.05	±100	nA
Capacitance, Switch I/O		$C_{I/O}$	Inhibit = V_{DD}		10		pF
Capacitance, Common O/I		$C_{O/I}$	Inhibit = V_{DD}		17		pF
Capacitance, Feedthrough (Channel Off)		$C_{I/O}$	Pins Not Adjacent		0.15		pF
			Pins Adjacent		0.47		

■ **ELECTRICAL CHARACTERISTICS(Cont.)**

PARAMETER•SYMBOL•TEST CONDITIONS•MIN•TYP•MAX•UNIT••**CONTROL INPUTS – INHIBIT A, B, C (Voltages Referenced to V$_{SS}$)••**Low Level Input Voltage•V$_{DD}$=5V•V$_{IL}$•R$_{ON}$= per spec,

SYMBOL•TEST CONDITIONS•MIN•TYP•MAX•UNIT••**CONTROL INPUTS – INHIBIT A, B, C (Voltages Referenced to V$_{SS}$)••**Low Level Input Voltage•V$_{DD}$=5V•V$_{IL}$•R$_{ON}$= per spec,

TEST CONDITIONS•MIN•TYP•MAX•UNIT••**CONTROL INPUTS – INHIBIT A, B, C (Voltages Referenced to V$_{SS}$)••**Low Level Input Voltage•V$_{DD}$=5V•V$_{IL}$•R$_{ON}$= per spec,

MIN•TYP•MAX•UNIT••**CONTROL INPUTS – INHIBIT A, B, C (Voltages Referenced to V$_{SS}$)••**Low Level Input Voltage•V$_{DD}$=5V•V$_{IL}$•R$_{ON}$= per spec,

TYP•MAX•UNIT••**CONTROL INPUTS – INHIBIT A, B, C (Voltages Referenced to V$_{SS}$)••**Low Level Input Voltage•V$_{DD}$=5V•V$_{IL}$•R$_{ON}$= per spec,

MAX•UNIT••**CONTROL INPUTS – INHIBIT A, B, C (Voltages Referenced to V$_{SS}$)••**Low Level Input Voltage•V$_{DD}$=5V•V$_{IL}$•R$_{ON}$= per spec,

UNIT••**CONTROL INPUTS – INHIBIT A, B, C (Voltages Referenced to V$_{SS}$)••**Low Level Input Voltage•V$_{DD}$=5V•V$_{IL}$•R$_{ON}$= per spec,

•**CONTROL INPUTS – INHIBIT A, B, C (Voltages Referenced to V$_{SS}$)••**Low Level Input Voltage•V$_{DD}$=5V•V$_{IL}$•R$_{ON}$= per spec,

CONTROL INPUTS – INHIBIT A, B, C (Voltages Referenced to V$_{SS}$)••Low Level Input Voltage•V$_{DD}$=5V•V$_{IL}$•R$_{ON}$= per spec,

Notes: 1. Data of "TYP" is intended as an indication of the IC's potential performance.

2. For voltage drops across the switch(ΔV_{SW})>600mV (>300mV at high temperature), excessive V_{DD} current may be drawn, i.e. the current out of the switch may contain both V_{DD} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.
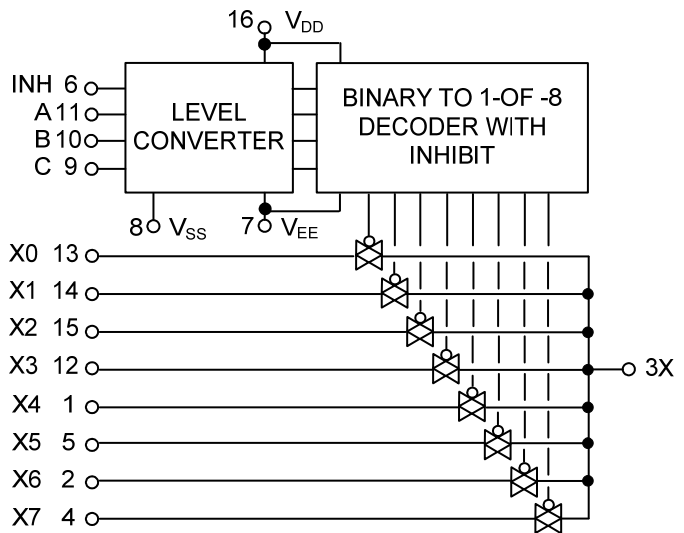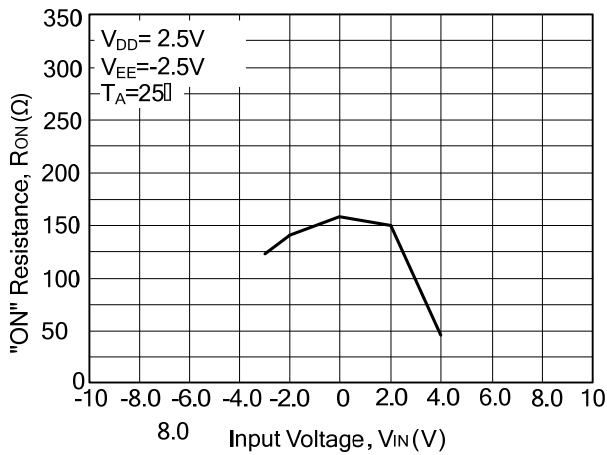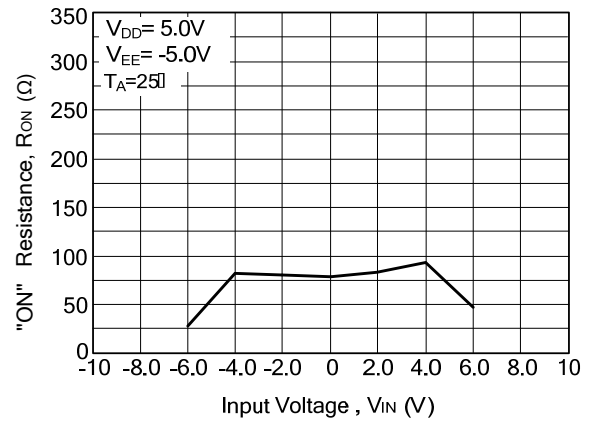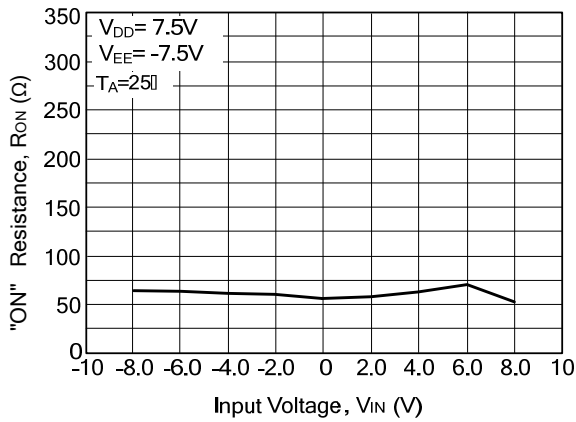
■ **TEST CIRCUIT**
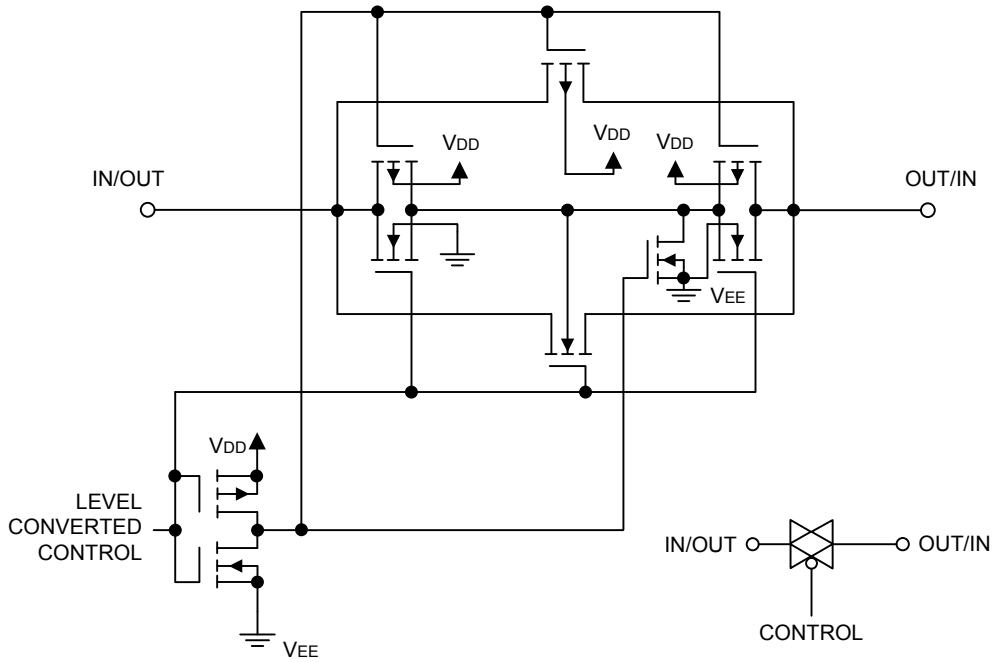
Switch Circuit Schematic

■ **TRUTH TABLE**

Control Inputs				ON Switches
INHIBIT	C	B	A	
0	0	0	0	X0
0	0	0	1	X1
0	0	1	0	X2
0	0	1	1	X3
0	1	0	0	X4
0	1	0	1	X5
0	1	1	0	X6
0	1	1	1	X7
1	x	x	x	None

x = Don't Care

UTC 4051 Functional Diagram

■ **TYPICAL CHARACTERISTICS**