NVMFS5833N, NVMFS5833NWF

Power MOSFET

40 V, 7.5 mΩ, 86 A, Single N−Channel, SO−8FL

Features

- Low $R_{DS(on)}$
- Low Capacitance
- Optimized Gate Charge
- AEC−Q101 Qualified and PPAP Capable
- NVMFS5833NWF − Wettable Franks Product
- These Devices are Pb−Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	40	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\Psi J-mb}$ (Notes 1, 2, 3 & 4)	Steady State	T_{mb} = 25°C	I_D	86	A
		T_{mb} = 100°C		61	
Power Dissipation $R_{\Psi J-mb}$ (Notes 1, 2, 3)		T_{mb} = 25°C	P_D	112	W
		T_{mb} = 100°C		56	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 3 & 4)	Steady State	T_A = 25°C	I_D	16	A
		T_A = 100°C		11	
Power Dissipation $R_{\theta JA}$ (Notes 1 & 3)		T_A = 25°C	P_D	3.7	W
		T_A = 100°C		1.8	
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		I_{DM}	324	A
Operating Junction and Storage Temperature			T_J, T_{stg}	−55 to 175	°C
Source Current (Body Diode)			I_S	86	A
Single Pulse Drain−to−Source Avalanche Energy (T_J = 25°C, $I_{L(pk)}$ = 36 A, L = 0.1 mH)			E_{AS}	65	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

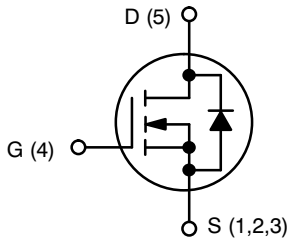
Parameter	Symbol	Value	Unit
Junction−to−Mounting Board (top) − Steady State (Notes 2, 3)	$R_{\Psi J-mb}$	1.3	°C/W
Junction−to−Ambient − Steady State (Note 3)	$R_{\theta JA}$	41	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Psi (Ψ) is used as required per JESD51−12 for packages in which substantially less than 100% of the heat flows to single case surface.
3. Surface−mounted on FR4 board using a 650 mm^2, 2 oz. Cu pad.
4. Continuous DC current rating. Maximum current for pulses as long as 1 second are higher but are dependent on pulse duration and duty cycle/

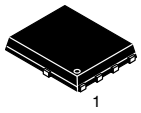
ON Semiconductor®

http://onsemi.com

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
40 V	7.5 mΩ @ 10 V	86 A

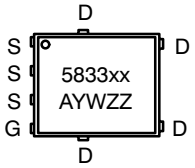


N−CHANNEL MOSFET



SO−8 FLAT LEAD CASE 488AA STYLE 1

MARKING DIAGRAM



5833	= Specific Device Code
xx	= N (NVMFS5833N) or WF (NVMFS5833NWF)
A	= Assembly Location
Y	= Year
W	= Work Week
ZZ	= Lot Traceability

ORDERING INFORMATION

Device	Package	Shipping†
NVMFS5833NT1G	SO−8FL (Pb−Free)	1500 / Tape & Reel
NVMFS5833NT3G	SO−8FL (Pb−Free)	5000 / Tape & Reel
NVMFS5833NWFT1G	SO−8FL (Pb−Free)	1500 / Tape & Reel
NVMFS5833NWFT3G	SO−8FL (Pb−Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		40			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				32.6		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 40 V	T_J = 25°C			1.0	μA
			T_J = 125°C			100	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA
ON CHARACTERISTICS (Note 5)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		2.0		3.5	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				−7.6		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 40 A			6.2	7.5	mΩ
Forward Transconductance	g_{FS}	V_{DS} = 5 V, I_D = 5 A			38		S
CHARGES AND CAPACITANCES							
Input Capacitance	C_{iss}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = 25 V			1714		pF
Output Capacitance	C_{oss}				210		
Reverse Transfer Capacitance	C_{rss}				144		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 32 V, I_D = 40 A			32.5		nC
Threshold Gate Charge	$Q_{G(TH)}$				2.77		
Gate−to−Source Charge	Q_{GS}				7.37		
Gate−to−Drain Charge	Q_{GD}				9		
SWITCHING CHARACTERISTICS (Note 6)							
Turn−On Delay Time	$t_{d(on)}$	V_{GS} = 10 V, V_{DS} = 20 V, I_D = 40 A, R_G = 2.5 Ω			10.23		ns
Rise Time	t_r				19.5		
Turn−Off Delay Time	$t_{d(off)}$				23.60		
Fall Time	t_f				3.00		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 40 A	T_J = 25°C		0.85	1.2	V
			T_J = 125°C		0.7		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, d_{IS}/d_t = 100 A/μs, I_S = 40 A			23.5		ns
Charge Time	t_a				13.5		
Discharge Time	t_b				10		
Reverse Recovery Charge	Q_{RR}				14		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: pulse width = 300 μs, duty cycle ≤ 2%.
6. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

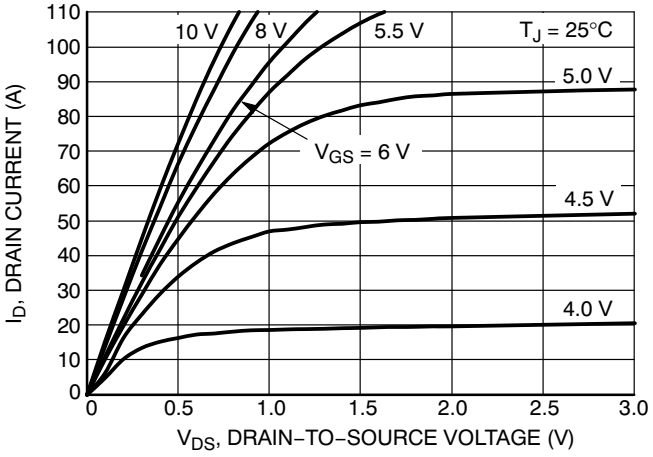


Figure 1. On−Region Characteristics

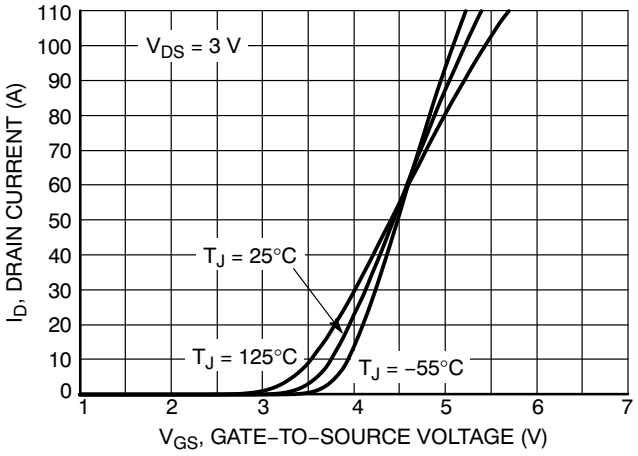


Figure 2. Transfer Characteristics

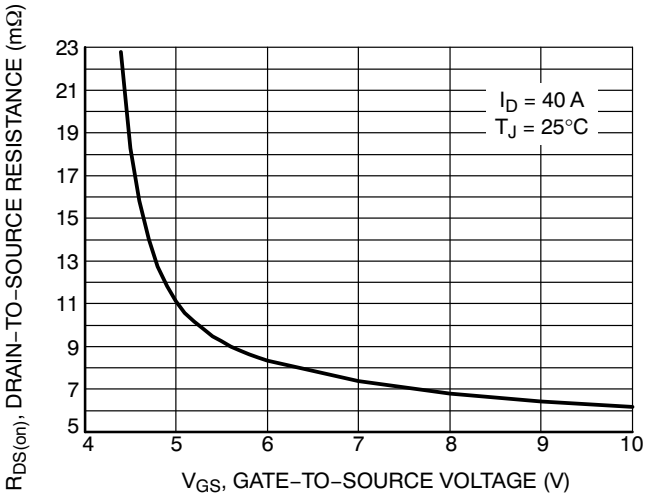


Figure 3. On−Resistance vs. Gate−to−Source Voltage

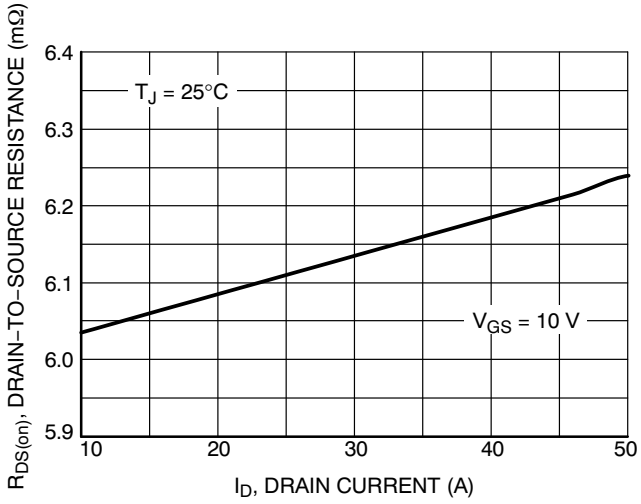


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

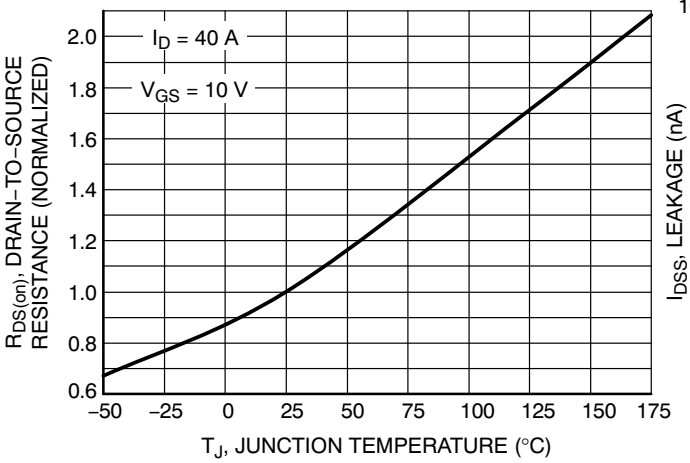


Figure 5. On−Resistance Variation with Temperature

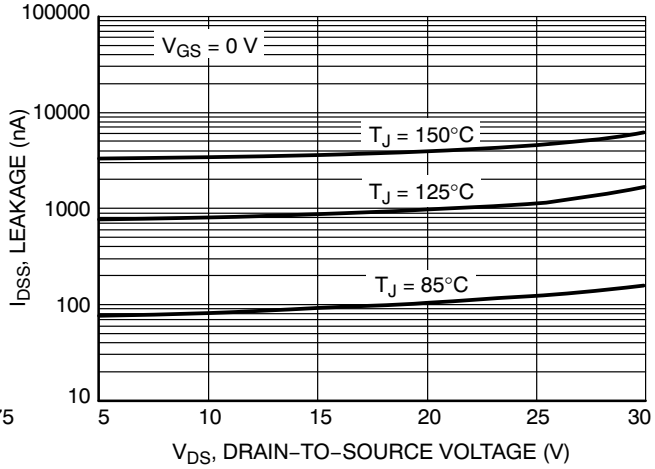


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

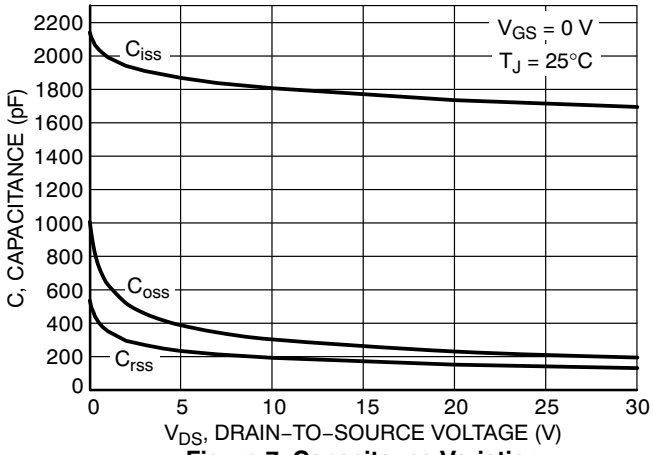


Figure 7. Capacitance Variation

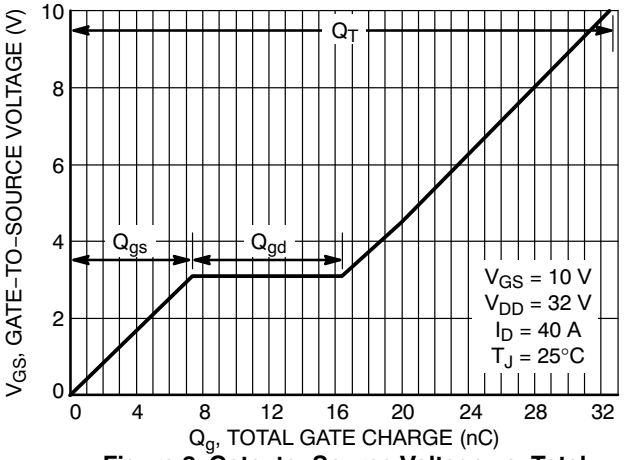


Figure 8. Gate−to−Source Voltage vs. Total Charge

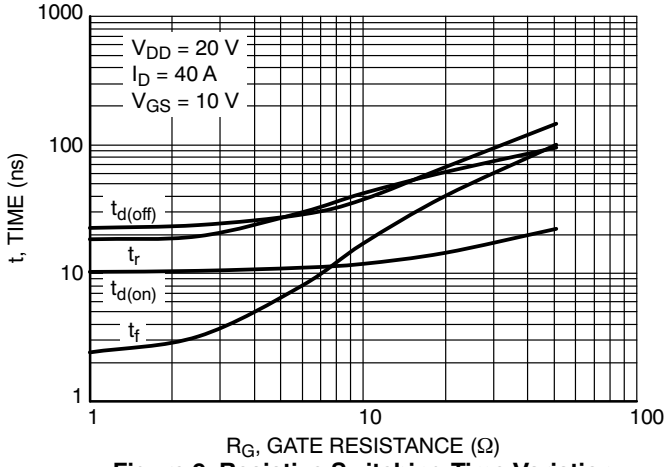


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

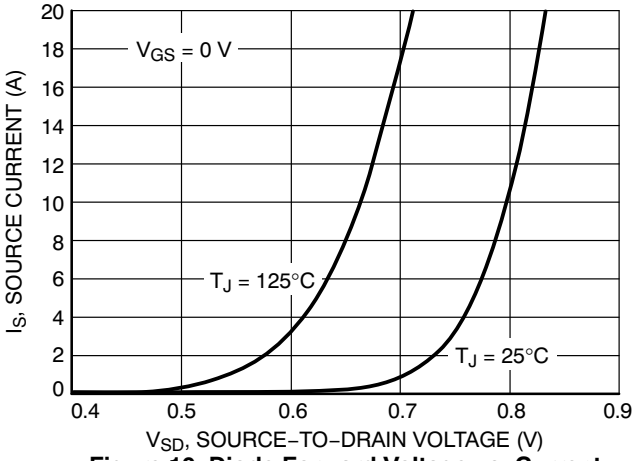


Figure 10. Diode Forward Voltage vs. Current

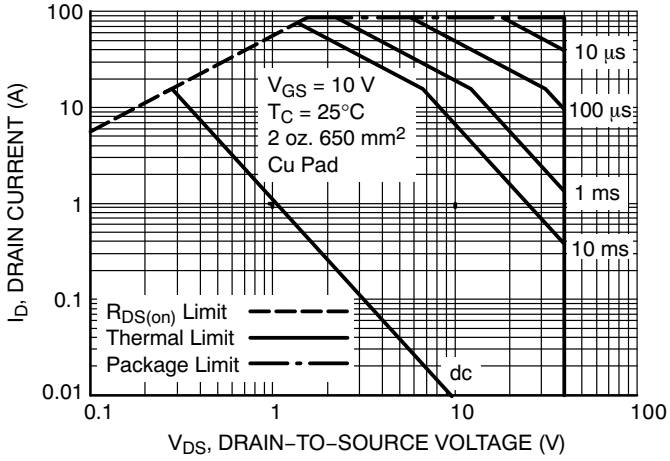


Figure 11. Maximum Rated Forward Biased Safe Operating Area

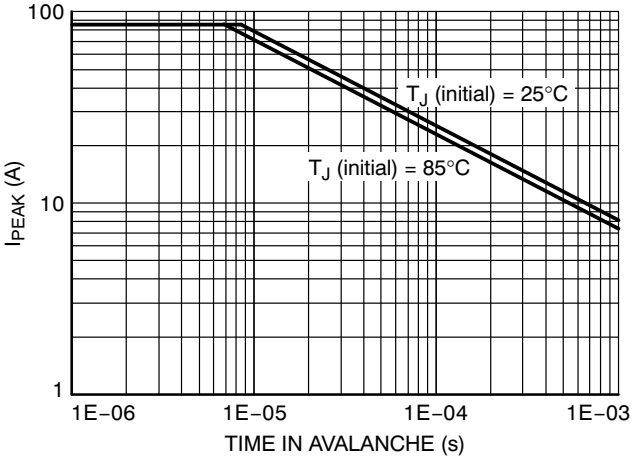


Figure 12. Avalanche Characteristics

TYPICAL CHARACTERISTICS

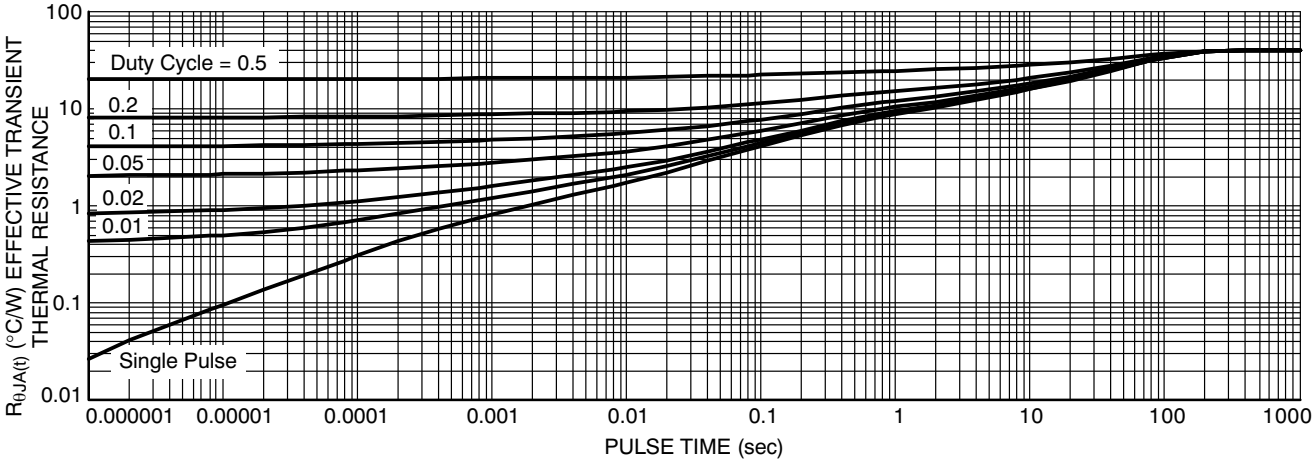
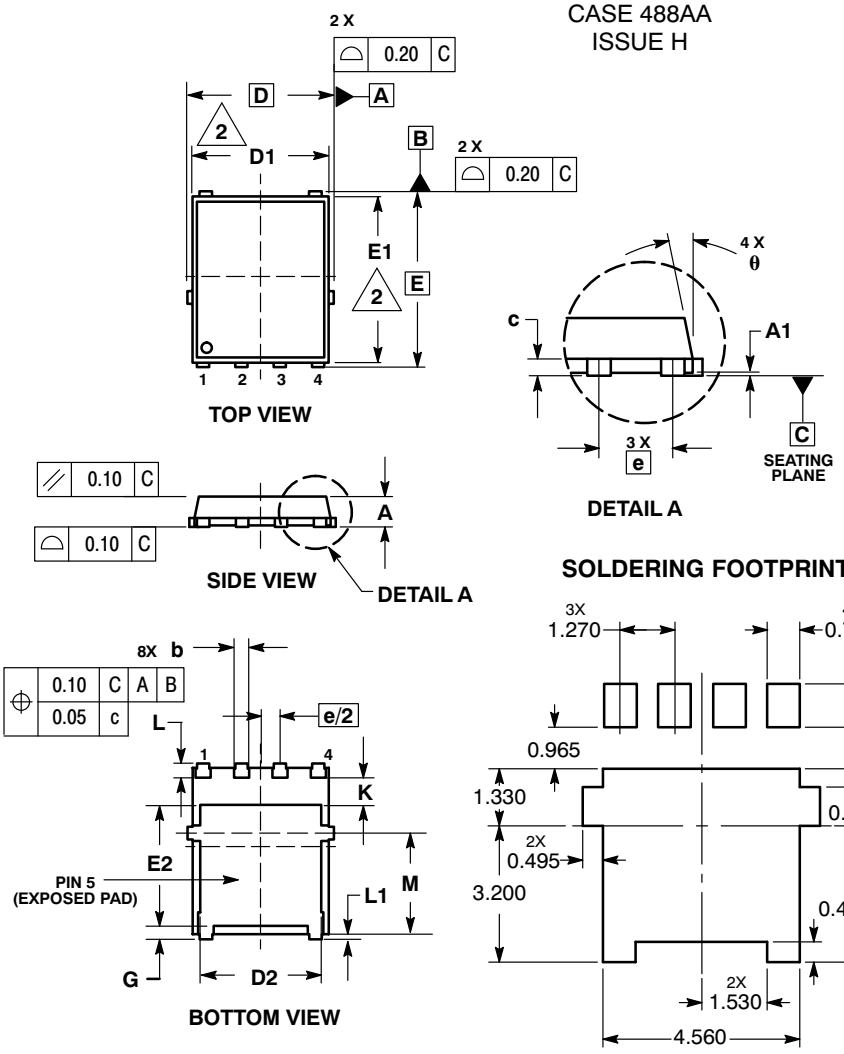


Figure 13. Thermal Response

PACKAGE DIMENSIONS

DFN5 5x6, 1.27P
(SO−8FL)
CASE 488AA
ISSUE H



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D		5.15 BSC	
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E		6.15 BSC	
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e		1.27 BSC	
G	0.51	0.61	0.71
K	1.20	1.35	1.50
L	0.51	0.61	0.71
L1	0.05	0.17	0.20
M	3.00	3.40	3.80
θ	0 °	---	12 °

STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative