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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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HD74CBT1G126

Single FET Bus Switch

RENESAS

ADE-205-661 (Z)

Rev. 0
Jan. 2002

Description

The HD74CBT1G126 features a single high-speed line switch. The switch is disabled when the output enable (OE) input is low.

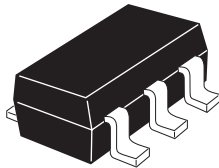
Features

- Minimal propagation delay through the switch.
- 5 Ω switch connection between two ports.
- TTL-compatible input levels.
- Ultra low quiescent power.
-Ideally suited for notebook applications.
- Package Type

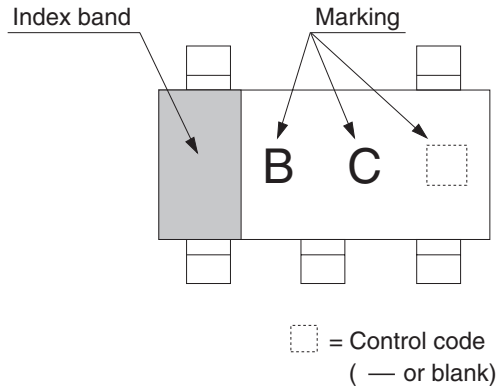
Package type	Package code	Package suffix	Taping code
CMPAK-5 pin	CMPAK-5	CM	E (3,000 pcs / Reel)

Outline and Article Indication

• HD74CBT1G126



CMTAK-5

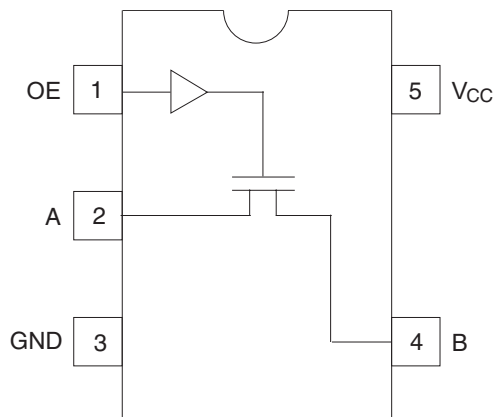


Function Table

Input OE	Function
H	A port = B port
L	Disconnect

H: High level
L: Low level

Pin Arrangement



(Top view)

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage range	V_{CC}	-0.5 to 7.0	V	
Input voltage range ¹	V_I	-0.5 to 7.0	V	
Input clamp current	I_{IK}	-50	mA	$V_I < 0$
Continuous output current	I_O	128	mA	$V_O = 0$ to V_{CC}
Continuous current through V_{CC} or GND	I_{CC} or I_{GND}	± 100	mA	
Maximum power dissipation at $T_a = 25^\circ\text{C}$ (in still air) ²	P_T	200	mW	
Storage temperature	T_{stg}	-65 to 150	$^\circ\text{C}$	

Notes: The absolute maximum ratings are values which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

1. The input and output voltage ratings may be exceeded even if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation was calculated using a junction temperature of 150°C .

Recommended Operating Conditions

Item	Symbol	Min	Max	Unit	Conditions
Supply voltage range	V_{CC}	4.0	5.5	V	
Input voltage range	V_I	0	5.5	V	
Output voltage range	V_{IO}	0	5.5	V	
Input transition rise or fall rate	$\Delta t / \Delta v$	0	5	ns / V	$V_{CC} = 4.5$ to 5.5 V
Operating free-air temperature	T_a	-40	85	$^\circ\text{C}$	

Note: Unused or floating inputs must be held high or low.

DC Electrical Characteristics

(Ta = -40 to 85°C)

Item	Symbol	V _{CC} (V)	Min	Typ ¹	Max	Unit	Test conditions
Clamp diode voltage	V _{IK}	4.5	—	—	-1.2	V	I _{IN} = -18 mA
Input voltage	V _{IH}	4.0 to 5.5	2.0	—	—	V	
	V _{IL}	4.0 to 5.5	—	—	0.8		
On-state switch resistance ²	R _{ON}	4.0	—	14	20	Ω	V _{IN} = 2.4 V, I _{IN} = 15 mA Typ at V _{CC} = 4.0 V
		4.5	—	5	7		V _{IN} = 0 V, I _{IN} = 64 mA
		4.5	—	5	7		V _{IN} = 0 V, I _{IN} = 30 mA
		4.5	—	10	15		V _{IN} = 2.4 V, I _{IN} = 15 mA
Input current	I _{IN}	0 to 5.5	—	—	±1.0	μA	V _{IN} = 5.5 V or GND
Off-state leakage current	I _{OZ}	5.5	—	—	±1.0	μA	0 ≤ A, B ≤ V _{CC}
Quiescent supply current	I _{CC}	5.5	—	—	1.0	μA	V _{IN} = V _{CC} or GND, I _O = 0 mA
Increase in I _{CC} per input ³	ΔI _{CC}	5.5	—	—	2.5	mA	One input at 3.4 V, other inputs at V _{CC} or GND

Notes: For condition shown as Min or Max use the appropriate values under recommended operating conditions.

1. All typical values are at V_{CC} = 5 V (unless otherwise noted), Ta = 25°C.
2. Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower voltage of the two (A or B) terminals.
3. This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

Capacitance

(Ta = 25°C)

Item	Symbol	V _{CC} (V)	Min	Typ	Max	Unit	Test conditions
Control input capacitance	C _{IN}	5.0	—	3	—	pF	V _{IN} = 0 or 3 V
Input / output capacitance	C _{I/O(OFF)}	5.0	—	5	—	pF	V _O = 0 or 3 V OE = GND

Note: This parameter is determined by device characterization is not production tested.

Switching Characteristics

($T_a = -40$ to 85°C)

- $V_{CC} = 4.0\text{ V}$

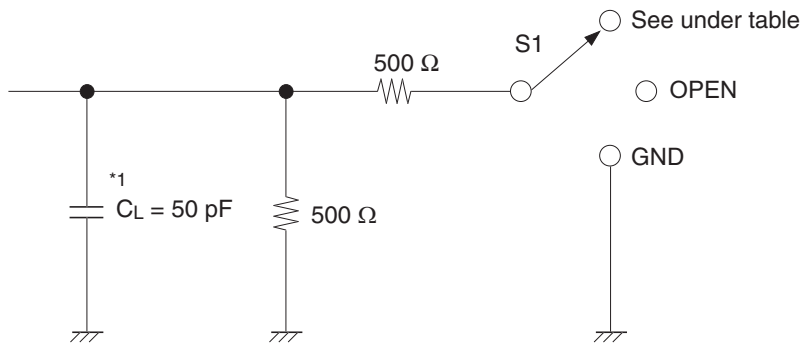
Item	Symbol	Min	Max	Unit	Test conditions	FROM (Input)	TO (Output)
Propagation delay time ¹⁾	t_{PLH} t_{PHL}	—	0.35	ns	$C_L = 50\text{ pF}$ $R_L = 500\ \Omega$	A or B	B or A
Enable time	t_{ZH} t_{ZL}	—	5.5	ns	$C_L = 50\text{ pF}$ $R_L = 500\ \Omega$	OE	A or B
Disable time	t_{HZ}	—	4.5	ns	$C_L = 50\text{ pF}$ $R_L = 500\ \Omega$	OE	A or B
	t_{LZ}	—	4.5				

- $V_{CC} = 5.0 \pm 0.5\text{ V}$

Item	Symbol	Min	Max	Unit	Test conditions	FROM (Input)	TO (Output)
Propagation delay time ¹⁾	t_{PLH} t_{PHL}	—	0.25	ns	$C_L = 50\text{ pF}$ $R_L = 500\ \Omega$	A or B	B or A
Enable time	t_{ZH} t_{ZL}	1.6	4.9	ns	$C_L = 50\text{ pF}$ $R_L = 500\ \Omega$	OE	A or B
Disable time	t_{HZ}	1.0	4.2	ns	$C_L = 50\text{ pF}$ $R_L = 500\ \Omega$	OE	A or B
	t_{LZ}	1.0	4.8				

Note: 1. The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

Test Circuit

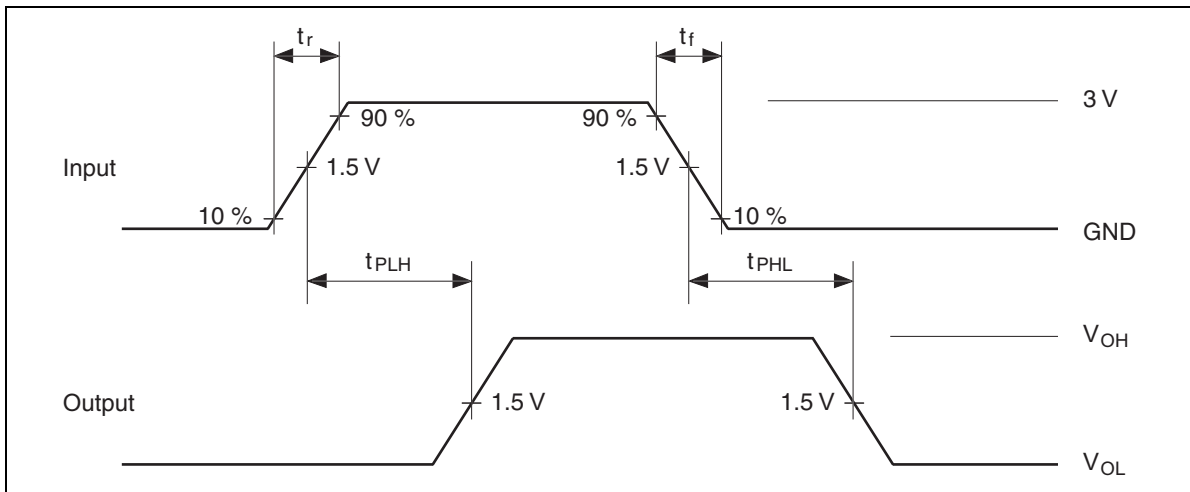


Load circuit for outputs

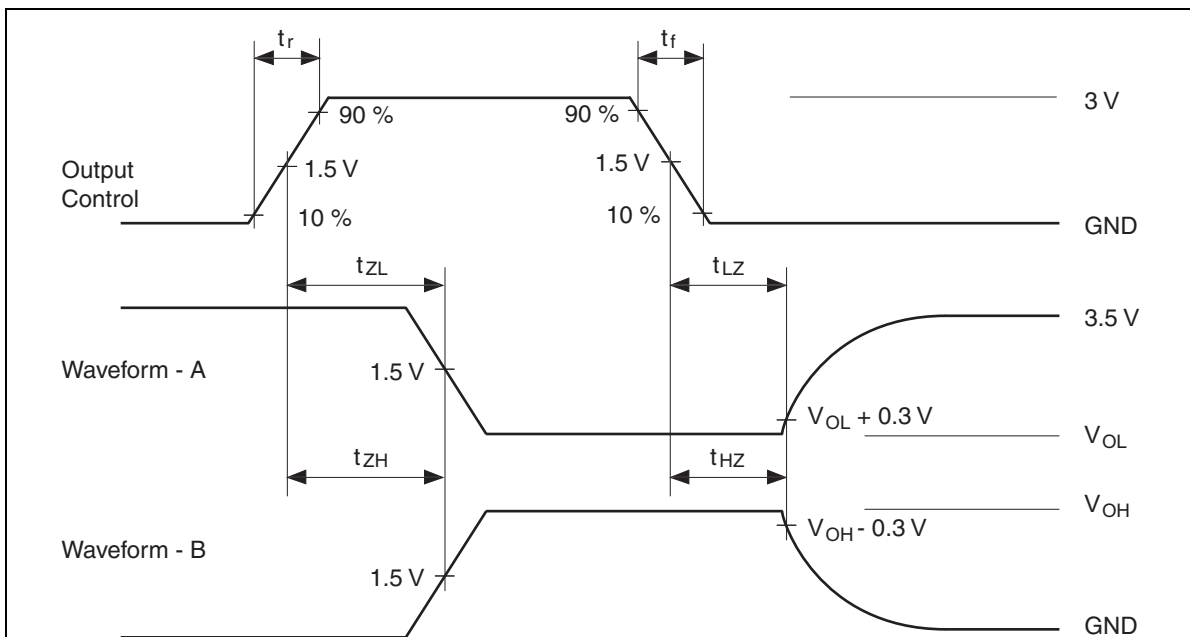
Symbol	S1
t_{PLH} / t_{PHL}	OPEN
t_{ZH} / t_{HZ}	OPEN
t_{ZL} / t_{LZ}	7 V

Note: 1. C_L includes probe and jig capacitance.

Waveforms – 1



Waveforms – 2

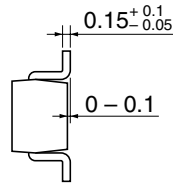
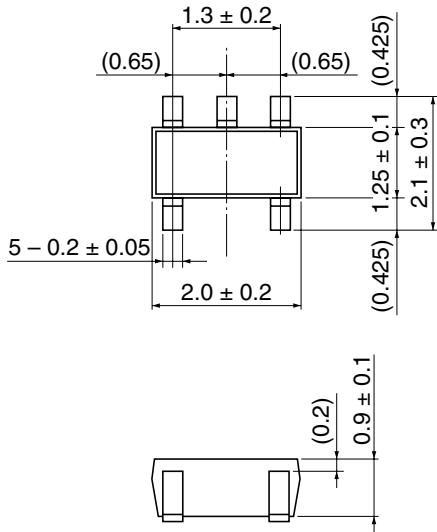


- Notes:
1. All input pulses are supplied by generators having the following characteristics :
 $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 2. Waveform - A is for an output with internal conditions such that the output is low except when disabled by the output control.
 3. Waveform - B is for an output with internal conditions such that the output is high except when disabled by the output control.
 4. The output are measured one at a time with one transition per measurement.

Package Dimensions

As of July, 2001

Unit: mm



Hitachi Code	CMPAK-5(T)
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.006 g

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Sales Offices

HITACHI

Hitachi, Ltd.

Semiconductor & Integrated Circuits
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: <1> (408) 433-1990 Fax: (03) 3270-5109

URL <http://www.hitachisemiconductor.com/>

For further information write to:

Hitachi Semiconductor
(America) Inc.
179 East Tasman Drive
San Jose, CA 95134
Tel: <1> (408) 433-1990
Fax: <1> (408) 433-0223

Hitachi Europe Ltd.
Electronic Components Group
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 585200

Hitachi Europe GmbH
Electronic Components Group
Dornacher Straße 3
D-85622 Feldkirchen
Postfach 201, D-85619 Feldkirchen
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Asia Ltd.
Hitachi Tower
16 Collyer Quay #20-00
Singapore 049318
Tel: <65>-538-6533/538-8577
Fax: <65>-538-6933/538-3877
URL: <http://semiconductor.hitachi.com.sg>

Hitachi Asia Ltd.
(Taipei Branch Office)
4/F, No. 167, Tun Hwa North Road
Hung-Kuo Building
Taipei (105), Taiwan
Tel: <886>-(2)-2718-3666
Fax: <886>-(2)-2718-8180
Telex: 23222 HAS-TP
URL: <http://www.hitachi.com.tw>

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower
World Finance Centre,
Harbour City, Canton Road
Tsim Sha Tsui, Kowloon Hong Kong
Tel: <852>-(2)-735-9218
Fax: <852>-(2)-730-0281
URL: <http://semiconductor.hitachi.com.hk>

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