215MHz, Rail-to-Rail Output, 1.1nV/√Hz, 3.5mA Op Amp Family

FEATURES

- **Low Noise Voltage: 1.1nV/√Hz**
- **Low Supply Current: 3.5mA/Amp Max**
- **Low Offset Voltage: 350μV Max**
- Gain Bandwidth Product:
  LT6230: 215MHz; $A_V \geq 1$
  LT6230-10: 1450MHz; $A_V \geq 10$
- Wide Supply Range: 3V to 12.6V
- Output Swings Rail-to-Rail
- Common Mode Rejection Ratio: 115dB Typ
- Output Current: 30mA
- Operating Temperature Range: –40°C to 85°C
- LT6230 Shutdown to 10μA Maximum
- LT6230/LT6230-10 in a Low Profile (1mm) ThinSOT™ Package
- Dual LT6231 in 8-Pin SO and Tiny DFN Packages
- LT6232 in a 16-Pin SSOP Package

APPLICATIONS

- Ultrasound Amplifiers
- Low Noise, Low Power Signal Processing
- Active Filters
- Driving A/D Converters
- Rail-to-Rail Buffer Amplifiers

DESCRIPTION

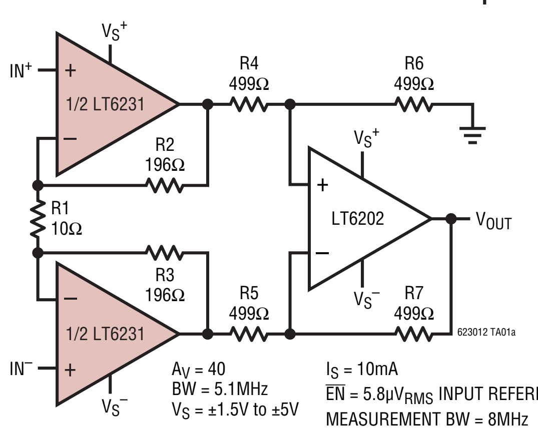
The LT®6230/LT6231/LT6232 are single/dual/quad low noise, rail-to-rail output unity-gain stable op amps that feature 1.1nV/√Hz noise voltage and draw only 3.5mA of supply current per amplifier. These amplifiers combine very low noise and supply current with a 215MHz gain-bandwidth product, a 70V/μs slew rate and are optimized for low supply voltage signal conditioning systems. The LT6230-10 is a single amplifier optimized for higher gain applications resulting in higher gain bandwidth and slew rate. The LT6230 and LT6230-10 include an enable pin that can be used to reduce the supply current to less than 10μA.

The amplifier family has an output that swings within 50mV of either supply rail to maximize the signal dynamic range in low supply applications and is specified on 3.3V, 5V and ±5V supplies. The $e_n \bullet \sqrt{I_{SUPPLY}}$ product of 1.9 per amplifier is among the most noise efficient of any op amp.

The LT6230/LT6230-10 are available in the 6-lead SOT-23 package and the LT6231 dual is available in the 8-pin SO package with standard pinouts. For compact layouts, the dual is also available in a tiny dual fine pitch leadless package (DFN). The LT6232 is available in the 16-pin SSOP package.

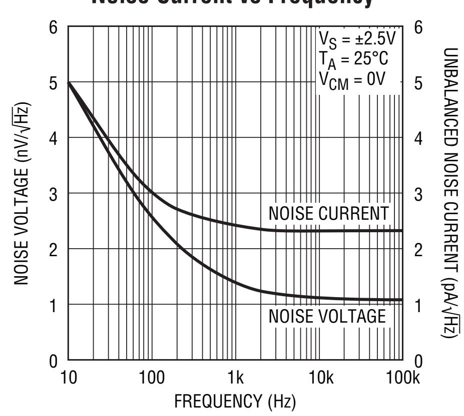
TYPICAL APPLICATION

Low Noise Low Power Instrumentation Amplifier



$A_V = 40$
BW = 5.1MHz
V_S = ±1.5V to ±5V
I_S = 10mA
$\overline{EN}$ = 5.8μV_{RMS} INPUT REFERRED,
MEASUREMENT BW = 8MHz

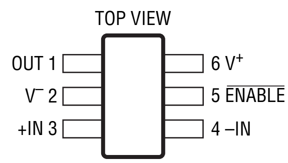
Noise Voltage and Unbalanced Noise Current vs Frequency



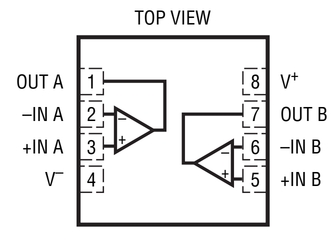
ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-) 12.6V
Input Current (Note 2) .... ±40mA
Output Short-Circuit Duration (Note 3) .... Indefinite
Operating Temperature Range (Note 4) .... –40°C to 85°C
Specified Temperature Range (Note 5) .... –40°C to 85°C
Junction Temperature .... 150°C
Junction Temperature (DD Package) .... 125°C
Storage Temperature Range .... –65°C to 150°C
Storage Temperature Range
(DD Package) .... –65°C to 125°C
Lead Temperature (Soldering, 10 sec) .... 300°C

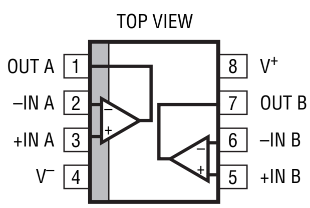
PIN CONFIGURATION



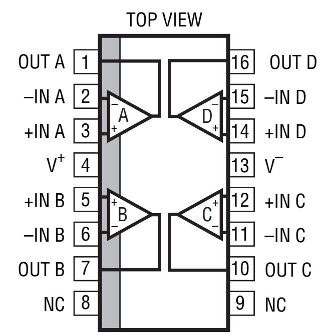
S6 PACKAGE
6-LEAD PLASTIC TSOT-23
T_{JMAX} = 150°C, θ_{JA} = 250°C/W



DD PACKAGE
8-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 160°C/W
UNDERSIDE METAL CONNECTED TO V^- (PCB CONNECTION OPTIONAL)



S8 PACKAGE
8-LEAD PLASTIC SO
T_{JMAX} = 150°C, θ_{JA} = 200°C/W



GN PACKAGE
16-LEAD NARROW PLASTIC SSOP
T_{JMAX} = 150°C, θ_{JA} = 135°C/W

623012fc

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LT6230CS6#PBF	LT6230CS6#TRPBF	LTAFJ	6-Lead Plastic TSOT-23	0°C to 70°C
LT6230IS6#PBF	LT6230IS6#TRPBF	LTAFJ	6-Lead Plastic TSOT-23	–40°C to 85°C
LT6230CS6-10#PBF	LT6230CS6-10#TRPBF	LTAFK	6-Lead Plastic TSOT-23	0°C to 70°C
LT6230IS6-10#PBF	LT6230IS6-10#TRPBF	LTAFK	6-Lead Plastic TSOT-23	–40°C to 85°C
LT6231CS8#PBF	LT6230CS8#TRPBF	6231	8-Lead Plastic SO	0°C to 70°C
LT6231IS8#PBF	LT6230IS8#TRPBF	6231I	8-Lead Plastic SO	–40°C to 85°C
LT6231CDD#PBF	LT6231CDD#TRPBF	LAEU	8-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LT6231IDD#PBF	LT6231IDD#TRPBF	LAEU	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LT6232CGN#PBF	LT6232CGN#TRPBF	6232	16-Lead Narrow Plastic SSOP	0°C to 70°C
LT6232IGN#PBF	LT6232IGN#TRPBF	6232I	16-Lead Narrow Plastic SSOP	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_S = 5V, 0V; V_S = 3.3V, 0V; V_{CM} = V_{OUT} = half supply, $\overline{ENABLE}$ = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	LT6230S6, LT6230S6-10 LT6231S8, LT6232GN LT6231DD		100 50 75	500 350 450	µV µV µV
	Input Offset Voltage Match (Channel-to-Channel) (Note 6)			100	600	µV
I_B	Input Bias Current			5	10	µA
	I_B Match (Channel-to-Channel) (Note 6)			0.1	0.9	µA
I_{OS}	Input Offset Current			0.1	0.6	µA
	Input Noise Voltage	0.1Hz to 10Hz		180		nV_{P-P}
e_n	Input Noise Voltage Density	f = 10kHz, V_S = 5V		1.1	1.7	$nV/\sqrt{Hz}$
in	Input Noise Current Density, Balanced Source Input Noise Current Density, Unbalanced Source	f = 10kHz, V_S = 5V, R_S = 10k f = 10kHz, V_S = 5V, R_S = 10k		1 2.4		$pA/\sqrt{Hz}$ $pA/\sqrt{Hz}$
	Input Resistance	Common Mode Differential Mode		6.5 7.5		MΩ kΩ
C_{IN}	Input Capacitance	Common Mode Differential Mode		2.9 7.7		pF pF
A_{VOL}	Large-Signal Gain	V_S = 5V, V_O = 0.5V to 4.5V, R_L = 10k to $V_S/2$ V_S = 5V, V_O = 0.5V to 4.5V, R_L = 1k to $V_S/2$ V_S = 5V, V_O = 1V to 4V, R_L = 100Ω to $V_S/2$	105 21 5.4	200 40 9		V/mV V/mV V/mV
		V_S = 3.3V, V_O = 0.65V to 2.65V, R_L = 10k to $V_S/2$ V_S = 3.3V, V_O = 0.65V to 2.65V, R_L = 1k to $V_S/2$	90 16.5	175 32		V/mV V/mV
V_{CM}	Input Voltage Range	Guaranteed by CMRR, V_S = 5V, 0V Guaranteed by CMRR, V_S = 3.3V, 0V	1.5 1.15		4 2.65	V V
CMRR	Common Mode Rejection Ratio	V_S = 5V, V_{CM} = 1.5V to 4V V_S = 3.3V, V_{CM} = 1.15V to 2.65V	90 90	115 115		dB dB
	CMRR Match (Channel-to-Channel) (Note 6)	V_S = 5V, V_{CM} = 1.5V to 4V	84	120		dB

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_S = 5V, 0V; V_S = 3.3V, 0V; V_{CM} = V_{OUT} = half supply, $\overline{ENABLE}$ = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
PSRR	Power Supply Rejection Ratio	V_S = 3V to 10V	90	115		dB
	PSRR Match (Channel-to-Channel) (Note 6)	V_S = 3V to 10V	84	115		dB
	Minimum Supply Voltage (Note 7)		3			V
V_{OL}	Output Voltage Swing Low (Note 8)	No Load I_{SINK} = 5mA V_S = 5V, I_{SINK} = 20mA V_S = 3.3V, I_{SINK} = 15mA		4 85 240 185	40 190 460 350	mV mV mV mV
V_{OH}	Output Voltage Swing High (Note 8)	No Load I_{SOURCE} = 5mA V_S = 5V, I_{SOURCE} = 20mA V_S = 3.3V, I_{SOURCE} = 15mA		5 90 325 250	50 200 600 400	mV mV mV mV
I_{SC}	Short-Circuit Current	V_S = 5V V_S = 3.3V	±30 ±25	±45 ±40		mA mA
I_S	Supply Current per Amplifier Disabled Supply Current per Amplifier	 $\overline{ENABLE}$ = V^+ – 0.35V		3.15 0.2	3.5 10	mA µA
$I_{\overline{ENABLE}}$	$\overline{ENABLE}$ Pin Current	$\overline{ENABLE}$ = 0.3V		–25	–75	µA
V_L	$\overline{ENABLE}$ Pin Input Voltage Low				0.3	V
V_H	$\overline{ENABLE}$ Pin Input Voltage High		V^+ – 0.35V			V
	Output Leakage Current	$\overline{ENABLE}$ = V^+ – 0.35V, V_O = 1.5V to 3.5V		0.2	10	µA
t_{ON}	Turn-On Time	$\overline{ENABLE}$ = 5V to 0V, R_L = 1k, V_S = 5V		300		ns
t_{OFF}	Turn-Off Time	$\overline{ENABLE}$ = 0V to 5V, R_L = 1k, V_S = 5V		41		µs
GBW	Gain-Bandwidth Product	Frequency = 1MHz, V_S = 5V LT6230-10		200 1300		MHz MHz
SR	Slew Rate	V_S = 5V, A_V = –1, R_L = 1k, V_O = 1.5V to 3.5V	42	60		V/µs
		LT6230-10, V_S = 5V, A_V = –10, R_L = 1k, V_O = 1.5V to 3.5V		250		V/µs
FPBW	Full-Power Bandwidth	V_S = 5V, V_{OUT} = $3V_{P-P}$ (Note 9)	4.8	6.3		MHz
		LT6230-10, HD2 = HD3 = ≤1%		11		MHz
t_S	Settling Time (LT6230, LT6231, LT6232)	0.1%, V_S = 5V, V_{STEP} = 2V, A_V = –1, R_L = 1k		55		ns

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the 0°C < T_A < 70°C temperature range. V_S = 5V, 0V; V_S = 3.3V, 0V; V_{CM} = V_{OUT} = half supply, $\overline{ENABLE}$ = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
V_{OS}	Input Offset Voltage	LT6230CS6, LT6230CS6-10 LT6231CS8, LT6232CGN LT6231CDD	● ● ●			600 450 550	µV µV µV
	Input Offset Voltage Match (Channel-to-Channel) (Note 6)		●			800	µV
V_{OS} TC	Input Offset Voltage Drift (Note 10)	V_{CM} = Half Supply	●		0.5	3	µV/°C
I_B	Input Bias Current		●			11	µA
	I_B Match (Channel-to-Channel) (Note 6)		●			1	µA
I_{OS}	Input Offset Current		●			0.7	µA
A_{VOL}	Large-Signal Gain	V_S = 5V, V_O = 0.5V to 4.5V, R_L = 10k to V_S/2 V_S = 5V, V_O = 0.5V to 4.5V, R_L = 1k to V_S/2 V_S = 5V, V_O = 1V to 4V, R_L = 100Ω to V_S/2	● ● ●	78 17 4.1			V/mV V/mV V/mV
		V_S = 3.3V, V_O = 0.65V to 2.65V, R_L = 10k to V_S/2 V_S = 3.3V, V_O = 0.65V to 2.65V, R_L = 1k to V_S/2	● ●	66 13			V/mV V/mV
V_{CM}	Input Voltage Range	Guaranteed by CMRR V_S = 5V, 0V Vs = 3.3V, 0V	 ● ●	 1.5 1.15		 4 2.65	 V V
CMRR	Common Mode Rejection Ratio	V_S = 5V, V_{CM} = 1.5V to 4V V_S = 3.3V, V_{CM} = 1.15V to 2.65V	● ●	90 85			dB dB
	CMRR Match (Channel-to-Channel) (Note 6)	V_S = 5V, V_{CM} = 1.5V to 4V	●	84			dB
PSRR	Power Supply Rejection Ratio	V_S = 3V to 10V	●	85			dB
	PSRR Match (Channel-to-Channel) (Note 6)	V_S = 3V to 10V	●	79			dB
	Minimum Supply Voltage (Note 7)		●	3			V
V_{OL}	Output Voltage Swing Low (Note 8)	No Load I_{SINK} = 5mA V_S = 5V, I_{SINK} = 20mA V_S = 3.3V, I_{SINK} = 15mA	● ● ● ●			50 200 500 380	mV mV mV mV
V_{OH}	Output Voltage Swing High (Note 8)	No Load I_{SOURCE} = 5mA V_S = 5V, I_{SOURCE} = 20mA V_S = 3.3V, I_{SOURCE} = 15mA	● ● ● ●			60 215 650 430	mV mV mV mV
I_{SC}	Short-Circuit Current	V_S = 5V V_S = 3.3V	● ●	±25 ±20			mA mA
I_S	Supply Current per Amplifier Disabled Supply Current per Amplifier	 $\overline{ENABLE}$ = V^+ – 0.25V	● ●		 1	4.2 	mA µA
$I_{\overline{ENABLE}}$	$\overline{ENABLE}$ Pin Current	$\overline{ENABLE}$ = 0.3V	●			–85	µA
V_L	ENABLE Pin Input Voltage Low		●			0.3	V
V_H	ENABLE Pin Input Voltage High		●	V^+ – 0.25V			V
	Output Leakage Current	$\overline{ENABLE}$ = V^+ – 0.25V, V_O = 1.5V to 3.5V	●		1		µA
t_{ON}	Turn-On Time	$\overline{ENABLE}$ = 5V to 0V, R_L = 1k, V_S = 5V	●		300		ns
t_{OFF}	Turn-Off Time	$\overline{ENABLE}$ = 0V to 5V, R_L = 1k, V_S = 5V	●		65		µs
SR	Slew Rate	V_S = 5V, A_V = –1, R_L = 1k, V_O = 1.5V to 3.5V	●	35			V/µs
		LT6230-10, A_V = –10, R_L = 1k, V_O = 1.5V to 3.5V	●		225		V/µs
FPBW	Full-Power Bandwidth (Note 9)	V_S = 5V, V_{OUT} = $3V_{P-P}$; LT6230C, LT6231C, LT6232C	●	3.7			MHz

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the –40°C < T_A < 85°C temperature range. V_S = 5V, 0V; V_S = 3.3V, 0V; V_{CM} = V_{OUT} = half supply, $\overline{ENABLE}$ = 0V, unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	LT6230IS6, LT6230IS6-10 LT6231IS8, LT6232IGN LT6231IDD	● ● ●			700 550 650	μV μV μV
	Input Offset Voltage Match (Channel-to-Channel) (Note 6)		●			1000	μV
V_{OS} TC	Input Offset Voltage Drift (Note 10)	V_{CM} = Half Supply	●		0.5	3	μV/°C
I_B	Input Bias Current		●			12	μA
	I_B Match (Channel-to-Channel) (Note 6)		●			1.1	μA
I_{OS}	Input Offset Current		●			0.8	μA
A_{VOL}	Large-Signal Gain	V_S = 5V, V_O = 0.5V to 4.5V, R_L = 10k to V_S/2 V_S = 5V, V_O = 0.5V to 4.5V, R_L = 1k to V_S/2 V_S = 5V, V_O = 1V to 4V, R_L = 100Ω to V_S/2	● ● ●	72 16 3.6			V/mV V/mV V/mV
		V_S = 3.3V, V_O = 0.65V to 2.65V, R_L = 10k to V_S/2 V_S = 3.3V, V_O = 0.65V to 2.65V, R_L = 1k to V_S/2	● ●	60 12			V/mV V/mV
V_{CM}	Input Voltage Range	Guaranteed by CMRR V_S = 5V, 0V V_S = 3.3V, 0V	 ● ●	 1.5 1.15		 4 2.65	 V V
CMRR	Common Mode Rejection Ratio	V_S = 5V, V_{CM} = 1.5V to 4V V_S = 3.3V, V_{CM} = 1.15V to 2.65V	● ●	90 85			dB dB
	CMRR Match (Channel-to-Channel) (Note 6)	V_S = 5V, V_{CM} = 1.5V to 4V	●	84			dB
PSRR	Power Supply Rejection Ratio	V_S = 3V to 10V	●	85			dB
	PSRR Match (Channel-to-Channel) (Note 6)	V_S = 3V to 10V	●	79			dB
	Minimum Supply Voltage (Note 7)		●	3			V
V_{OL}	Output Voltage Swing Low (Note 8)	No Load I_{SINK} = 5mA V_S = 5V, I_{SINK} = 15mA V_S = 3.3V, I_{SINK} = 15mA	● ● ● ●			60 210 510 390	mV mV mV mV
V_{OH}	Output Voltage Swing High (Note 6)	No Load I_{SOURCE} = 5mA V_S = 5V, I_{SOURCE} = 20mA V_S = 3.3V, I_{SOURCE} = 15mA	● ● ● ●			70 220 675 440	mV mV mV mV
I_{SC}	Short-Circuit Current	V_S = 5V V_S = 3.3V	● ●	±15 ±15			mA mA
I_S	Supply Current per Amplifier Disabled Supply Current per Amplifier	 $\overline{ENABLE}$ = V^+ – 0.2V	● ●		 1	4.4 	mA μA
$I_{\overline{ENABLE}}$	$\overline{ENABLE}$ Pin Current	$\overline{ENABLE}$ = 0.3V	●			–100	μA
V_L	$\overline{ENABLE}$ Pin Input Voltage Low		●			0.3	V
V_H	$\overline{ENABLE}$ Pin Input Voltage High		●	V^+ – 0.2V			V
	Output Leakage Current	$\overline{ENABLE}$ = V^+ – 0.2V, V_O = 1.5V to 3.5V	●		1		μA
t_{ON}	Turn-On Time	$\overline{ENABLE}$ = 5V to 0V, R_L = 1k, V_S = 5V	●		300		ns
t_{OFF}	Turn-Off Time	$\overline{ENABLE}$ = 0V to 5V, R_L = 1k, V_S = 5V	●		72		μs
SR	Slew Rate	V_S = 5V, A_V = –1, R_L = 1k, V_O = 1.5V to 3.5V	●	31			V/μs
		LT6230-10, A_V = –10, R_L = 1k, V_O = 1.5V to 3.5V	●		185		V/μs
FPBW	Full-Power Bandwidth (Note 9)	V_S = 5V, V_{OUT} = $3V_{P-P}$; LT6230I, LT6231I, LT6232I	●	3.3			MHz

ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_S = ±5V$, $V_{CM} = V_{OUT} = 0V$, $\overline{ENABLE} = 0V$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	LT6230, LT6230-10 LT6231S8, LT6232GN LT6231DD		100 50 75	500 350 450	µV µV µV
	Input Offset Voltage Match (Channel-to-Channel) (Note 6)			100	600	µV
I_B	Input Bias Current			5	10	µA
	I_B Match (Channel-to-Channel) (Note 6)			0.1	0.9	µA
I_{OS}	Input Offset Current			0.1	0.6	µA
	Input Noise Voltage	0.1Hz to 10Hz		180		nV_{P-P}
e_n	Input Noise Voltage Density	f = 10kHz		1.1	1.7	$nV/\sqrt{Hz}$
i_n	Input Noise Current Density, Balanced Source Input Noise Current Density, Unbalanced Source	f = 10kHz, R_S = 10k f = 10kHz, R_S = 10k		1 2.4		$pA/\sqrt{Hz}$ $pA/\sqrt{Hz}$
	Input Resistance	Common Mode Differential Mode		6.5 7.5		MΩ kΩ
C_{IN}	Input Capacitance	Common Mode Differential Mode		2.4 6.5		pF pF
A_{VOL}	Large-Signal Gain	V_O = ±4.5V, R_L = 10k V_O = ±4.5V, R_L = 1k V_O = ±2V, R_L = 100Ω	140 35 8.5	260 65 16		V/mV V/mV V/mV
V_{CM}	Input Voltage Range	Guaranteed by CMRR	–3		4	V
CMRR	Common Mode Rejection Ratio	V_{CM} = –3V to 4V	95	120		dB
	CMRR Match (Channel-to-Channel) (Note 6)	V_{CM} = –3V to 4V	89	125		dB
PSRR	Power Supply Rejection Ratio	V_S = ±1.5V to ±5V	90	115		dB
	PSRR Match (Channel-to-Channel) (Note 6)	V_S = ±1.5V to ±5V	84	115		dB
V_{OL}	Output Voltage Swing Low (Note 8)	No Load I_{SINK} = 5mA I_{SINK} = 20mA		4 85 240	40 190 460	mV mV mV
V_{OH}	Output Voltage Swing High (Note 8)	No Load I_{SOURCE} = 5mA I_{SOURCE} = 20mA		5 90 325	50 200 600	mV mV mV
I_{SC}	Short-Circuit Current		±30			mA
I_S	Supply Current per Amplifier Disabled Supply Current per Amplifier	 $\overline{ENABLE}$ = 4.65V		3.3 0.2	3.9	mA µA
$I_{\overline{ENABLE}}$	$\overline{ENABLE}$ Pin Current	$\overline{ENABLE}$ = 0.3V		–35	–85	µA
V_L	$\overline{ENABLE}$ Pin Input Voltage Low				0.3	V
V_H	$\overline{ENABLE}$ Pin Input Voltage High		4.65			V
	Output Leakage Current	$\overline{ENABLE}$ = V^+ – 4.65V, V_O = ±1V		0.2	10	µA
t_{ON}	Turn-On Time	$\overline{ENABLE}$ = 5V to 0V, R_L = 1k		300		ns
t_{OFF}	Turn-Off Time	$\overline{ENABLE}$ = 0V to 5V, R_L = 1k		62		µs
GBW	Gain-Bandwidth Product	Frequency = 1MHz LT6230-10	150 1000	215 1450		MHz MHz
SR	Slew Rate	A_V = –1, R_L = 1k, V_O = –2V to 2V	50	70		V/µs
		LT6230-10, A_V = –10, R_L = 1k, V_O = –2V to 2V		320		V/µs
FPBW	Full-Power Bandwidth	V_{OUT} = $3V_{P-P}$ (Note 9)	5.3	7.4		MHz
		LT6230-10, HD2 = HD3 ≤ 1%		11		MHz
t_S	Settling Time (LT6230, LT6231, LT6232)	0.1%, V_{STEP} = 2V, A_V = –1, R_L = 1k		50		ns

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the 0°C < T_A < 70°C temperature range. V_S = ±5V, V_{CM} = V_{OUT} = 0V, $\overline{ENABLE}$ = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	LT6230CS6, LT6230CS6-10 LT6231CS8, LT6232CGN LT6231CDD	● ● ●			600 450 550	µV µV µV
	Input Offset Voltage Match (Channel-to-Channel) (Note 6)		●			800	µV
V_{OS} TC	Input Offset Voltage Drift (Note 10)		●		0.5	3	µV/°C
I_B	Input Bias Current		●			11	µA
	I_B Match (Channel-to-Channel) (Note 6)		●			1	µA
I_{OS}	Input Offset Current		●			0.7	µA
A_{VOL}	Large-Signal Gain	V_O = ±4.5V, R_L = 10k V_O = ±4.5V, R_L = 1k V_O = ±2V, R_L = 100Ω	● ● ●	100 27 6			V/mV V/mV V/mV
V_{CM}	Input Voltage Range	Guaranteed by CMRR	●	–3		4	V
CMRR	Common Mode Rejection Ratio	V_{CM} = –3V to 4V	●	95			dB
	CMRR Match (Channel-to-Channel) (Note 6)	V_{CM} = –3V to 4V	●	89			dB
PSRR	Power Supply Rejection Ratio	V_S = ±1.5V to ±5V	●	85			dB
	PSRR Match (Channel-to-Channel) (Note 6)	V_S = ±1.5V to ±5V	●	79			dB
V_{OL}	Output Voltage Swing Low (Note 8)	No Load I_{SINK} = 5mA I_{SINK} = 20mA	● ● ●			50 200 500	mV mV mV
V_{OH}	Output Voltage Swing High (Note 8)	No Load I_{SOURCE} = 5mA I_{SOURCE} = 20mA	● ● ●			60 215 650	mV mV mV
I_{SC}	Short-Circuit Current		●	±25			mA
I_S	Supply Current per Amplifier Disabled Supply Current per Amplifier	 $\overline{ENABLE}$ = 4.75V	● ●		 1	4.6 	mA µA
$I_{\overline{ENABLE}}$	$\overline{ENABLE}$ Pin Current	$\overline{ENABLE}$ = 0.3V	●			–95	µA
V_L	$\overline{ENABLE}$ Pin Input Voltage Low		●			0.3	V
V_H	$\overline{ENABLE}$ Pin Input Voltage High		●	4.75			V
	Output Leakage Current	$\overline{ENABLE}$ = 4.75V, V_O = ±1V	●		1		µA
t_{ON}	Turn-On Time	$\overline{ENABLE}$ = 5V to 0V, R_L = 1k	●		300		ns
t_{OFF}	Turn-Off Time	$\overline{ENABLE}$ = 0V to 5V, R_L = 1k	●		85		µs
SR	Slew Rate	A_V = –1, R_L = 1k, V_O = –2V to 2V	●	44			V/µs
		LT6230-10, A_V = –10, R_L = 1k, V_O = –2V to 2V	●		315		V/µs
FPBW	Full-Power Bandwidth	V_{OUT} = $3V_{P-P}$ (Note 9) LT6230C, LT6231C, LT6232C	●	4.66			MHz

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the –40°C < T_A < 85°C temperature range. V_S = ±5V, V_{CM} = V_{OUT} = 0V, $\overline{ENABLE}$ = 0V, unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	LT6230I, LT6230I-10 LT6231IS8, LT6232IGN LT6231IDD	● ● ●			700 550 650	μV μV μV
	Input Offset Voltage Match (Channel-to-Channel) (Note 6)		●			1000	μV
V_{OS} TC	Input Offset Voltage Drift (Note 10)		●		0.5	3	μV/°C
I_B	Input Bias Current		●			12	μA
	I_B Match (Channel-to-Channel) (Note 6)		●			1.1	μA
I_{OS}	Input Offset Current		●			0.8	μA
A_{VOL}	Large-Signal Gain	V_O = ±4.5V, R_L = 10k V_O = ±4.5V, R_L = 1k V_O = ±1.5V, R_L = 100Ω	● ● ●	93 25 4.8			V/mV V/mV V/mV
V_{CM}	Input Voltage Range	Guaranteed by CMRR	●	–3		4	V
CMRR	Common Mode Rejection Ratio	V_{CM} = –3V to 4V	●	95			dB
	CMRR Match (Channel-to-Channel) (Note 6)	V_{CM} = –3V to 4V	●	89			dB
PSRR	Power Supply Rejection Ratio	V_S = ±1.5V to ±5V	●	85			dB
	PSRR Match (Channel-to-Channel) (Note 6)	V_S = ±1.5V to ±5V	●	79			dB
V_{OL}	Output Voltage Swing Low (Note 8)	No Load I_{SINK} = 5mA I_{SINK} = 15mA	● ● ●			60 210 510	mV mV mV
V_{OH}	Output Voltage Swing High (Note 8)	No Load I_{SOURCE} = 5mA I_{SOURCE} = 20mA	● ● ●			70 220 675	mV mV mV
I_{SC}	Short-Circuit Current		●	±15			mA
I_S	Supply Current per Amplifier Disabled Supply Current per Amplifier	 $\overline{ENABLE}$ = 4.8V	● ●		 1	4.85 	mA μA
$I_{\overline{ENABLE}}$	$\overline{ENABLE}$ Pin Current	$\overline{ENABLE}$ = 0.3V	●			–110	μA
V_L	$\overline{ENABLE}$ Pin Input Voltage Low		●			0.3	V
V_H	$\overline{ENABLE}$ Pin Input Voltage High		●	4.8			V
	Output Leakage Current	$\overline{ENABLE}$ = 4.8V, V_O = ±1V	●		1		μA
t_{ON}	Turn-On Time	$\overline{ENABLE}$ = 5V to 0V, R_L = 1k	●		300		ns
t_{OFF}	Turn-Off Time	$\overline{ENABLE}$ = 0V to 5V, R_L = 1k	●		72		μs
SR	Slew Rate	A_V = –1, R_L = 1k, V_O = –2V to 2V	●	37			V/μs
		LT6230-10, A_V = –10, R_L = 1k, V_O = –2V to 2V	●		260		V/μs
FPBW	Full-Power Bandwidth (Note 9)	V_{OUT} = $3V_{P-P}$; LT6230I, LT6231I, LT6232I	●	3.9			MHz

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Inputs are protected by back-to-back diodes. If the differential input voltage exceeds 0.7V, the input current must be limited to less than 40mA.

Note 3: A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output is shorted indefinitely.

Note 4: The LT6230C/LT6230I the LT6231C/LT6231I, and LT6232C/LT6232I are guaranteed functional over the temperature range of –40°C and 85°C.

Note 5: The LT6230C/LT6231C/LT6232C are guaranteed to meet specified performance from 0°C to 70°C. The LT6230C/LT6231C/LT6232C are designed, characterized and expected to meet specified performance from –40°C to 85°C, but are not tested or QA sampled at these temperatures. The LT6230I/LT6231I/LT6232I are guaranteed to meet specified performance from –40°C to 85°C.

ELECTRICAL CHARACTERISTICS

Note 6: Matching parameters are the difference between the two amplifiers A and D and between B and C of the LT6232; between the two amplifiers of the LT6231. CMRR and PSRR match are defined as follows: CMRR and PSRR are measured in µV/V on the matched amplifiers. The difference is calculated between the matching sides in µV/V. The result is converted to dB.

Note 7: Minimum supply voltage is guaranteed by power supply rejection ratio test.

Note 8: Output voltage swings are measured between the output and power supply rails.

Note 9: Full-power bandwidth is calculated from the slew rate:

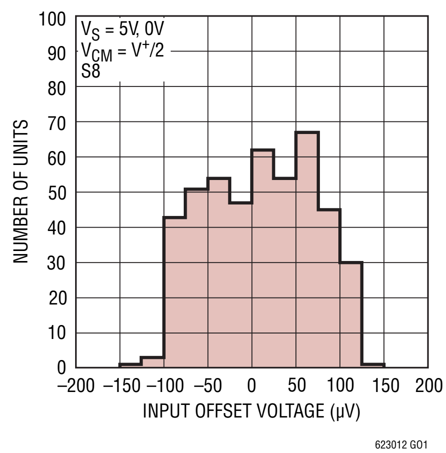
$FPBW = SR/2\pi V_P$

Note 10: This parameter is not 100% tested.

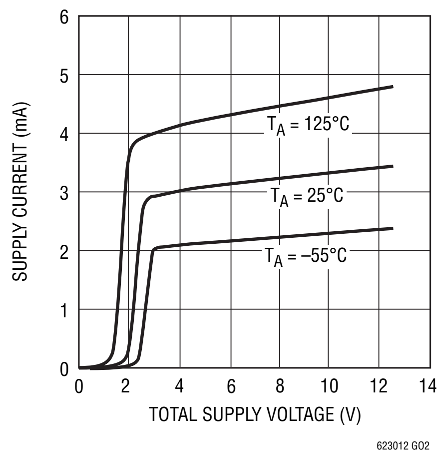
TYPICAL PERFORMANCE CHARACTERISTICS

(LT6230/LT6231/LT6232)

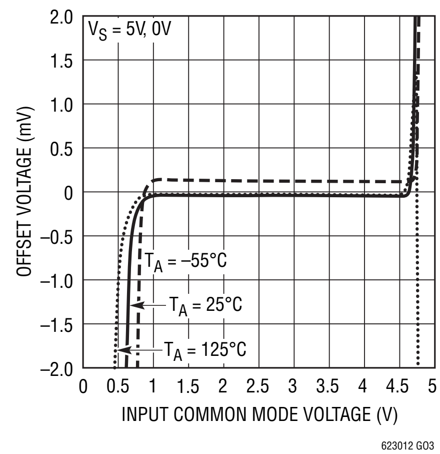
V_{OS} Distribution



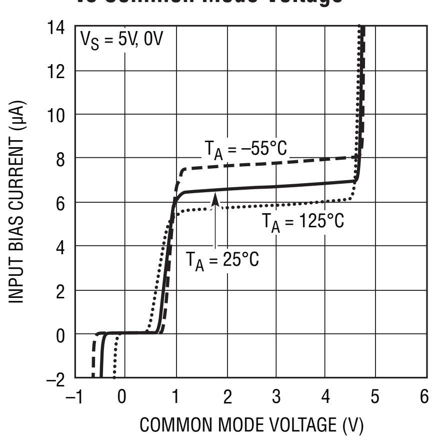
Supply Current vs Supply Voltage (Per Amplifier)



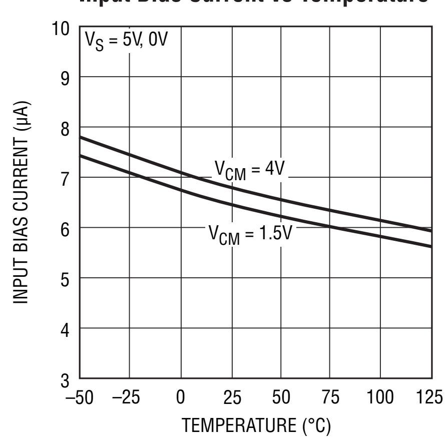
Offset Voltage vs Input Common Mode Voltage



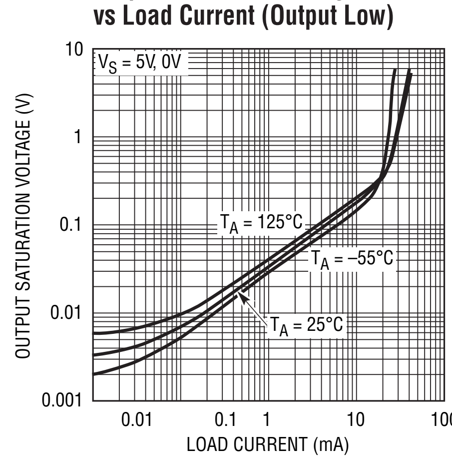
Input Bias Current vs Common Mode Voltage



Input Bias Current vs Temperature



Output Saturation Voltage vs Load Current (Output Low)

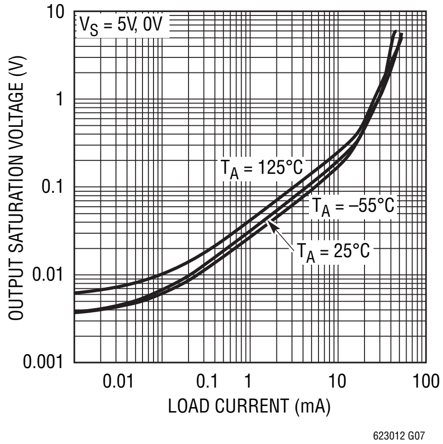


623012fc

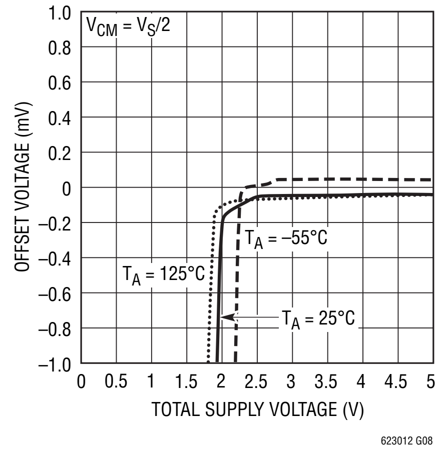
TYPICAL PERFORMANCE CHARACTERISTICS

(LT6230/LT6231/LT6232)

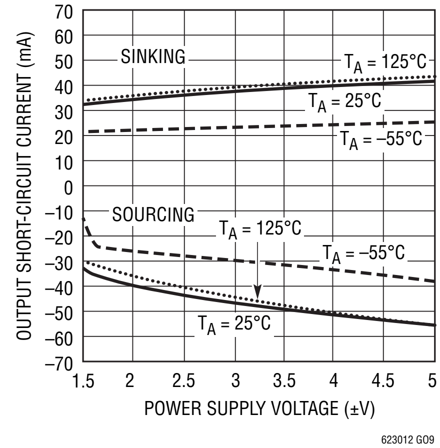
Output Saturation Voltage vs Load Current (Output High)



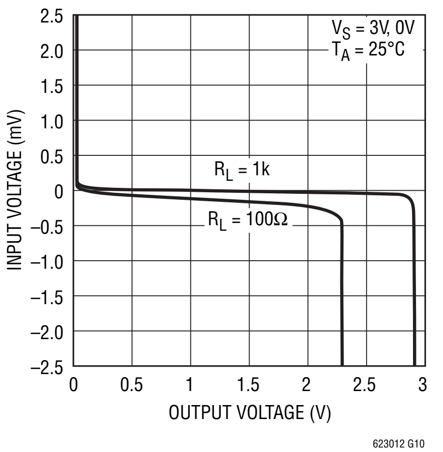
Minimum Supply Voltage



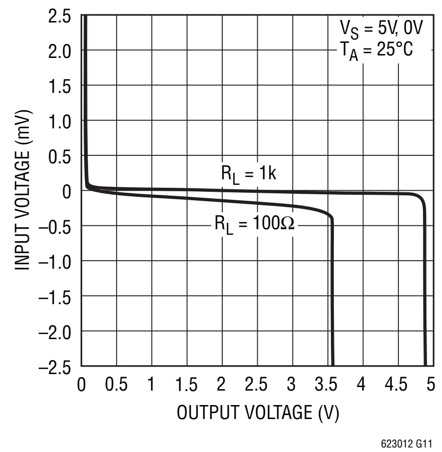
Output Short-Circuit Current vs Power Supply Voltage



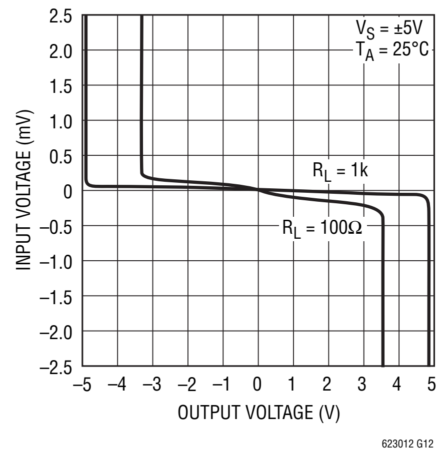
Open-Loop Gain



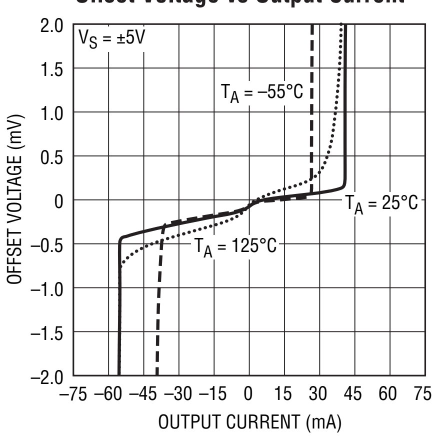
Open-Loop Gain



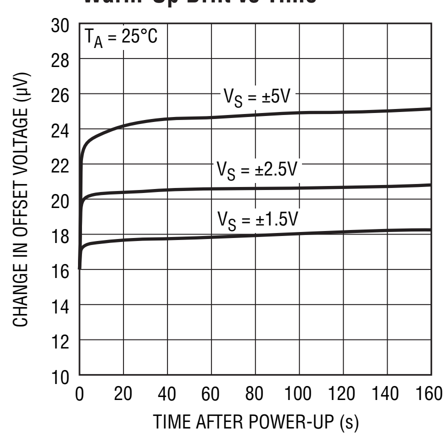
Open-Loop Gain



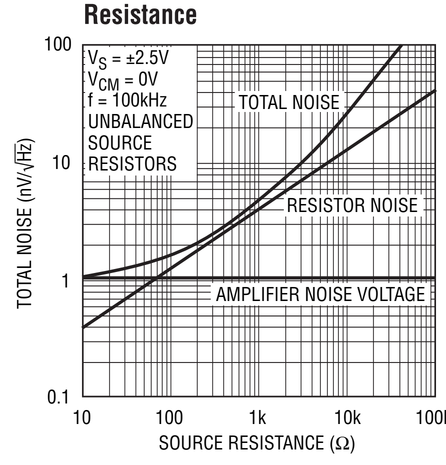
Offset Voltage vs Output Current



Warm-Up Drift vs Time



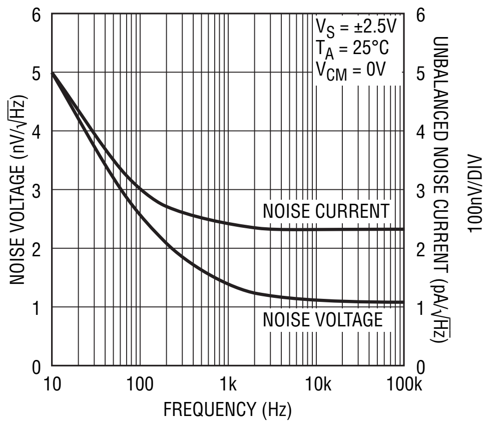
Total Noise vs Total Source Resistance



TYPICAL PERFORMANCE CHARACTERISTICS

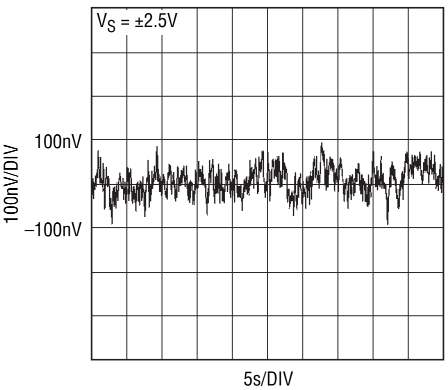
(LT6230/LT6231/LT6232)

Noise Voltage and Unbalanced Noise Current vs Frequency



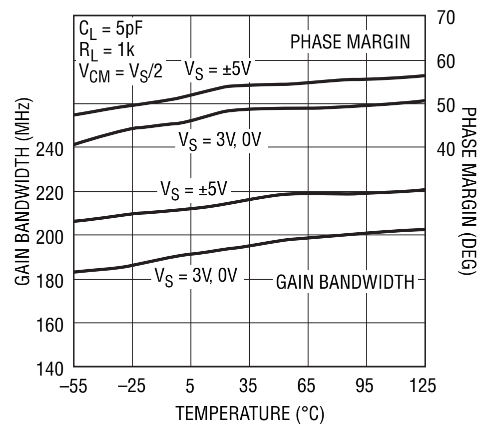
623012 G16

0.1Hz to 10Hz Output Voltage Noise



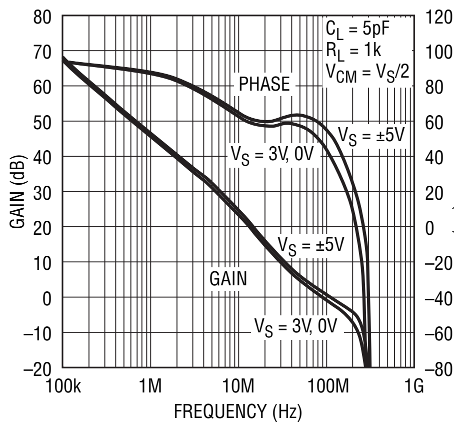
623012 G17

Gain Bandwidth and Phase Margin vs Temperature



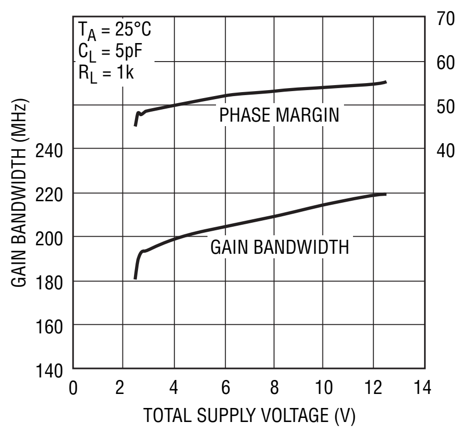
623012 G18

Open-Loop Gain vs Frequency



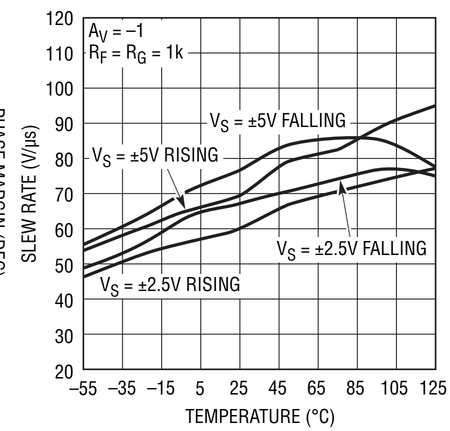
623012 G19

Gain Bandwidth and Phase Margin vs Supply Voltage



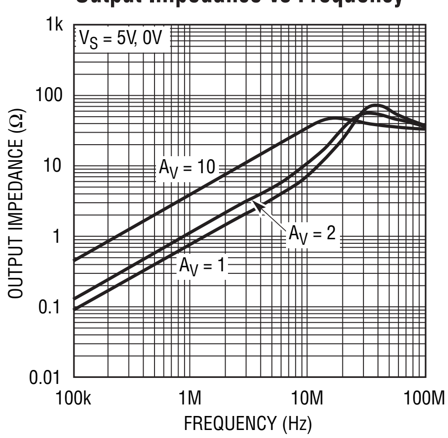
623012 G20

Slew Rate vs Temperature



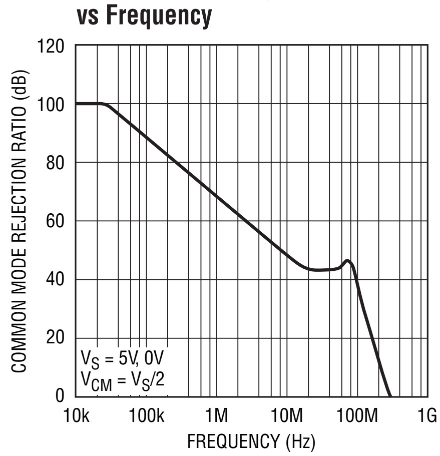
623012 G21

Output Impedance vs Frequency



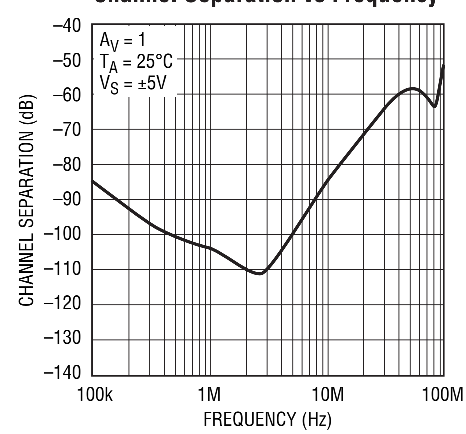
623012 G22

Common Mode Rejection Ratio vs Frequency



623012 G23

Channel Separation vs Frequency



623012 G24

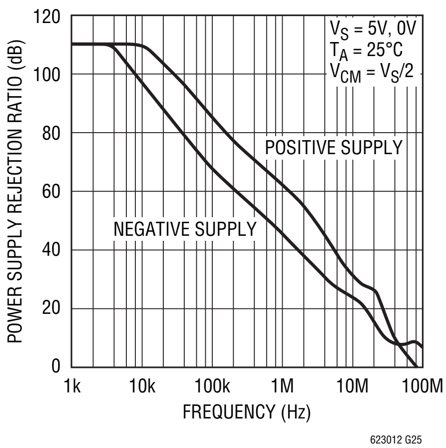
623012fc

LINEAR TECHNOLOGY

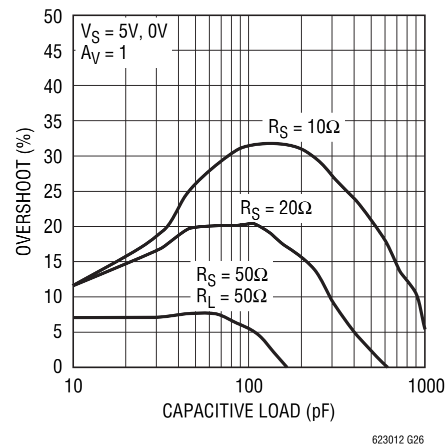
TYPICAL PERFORMANCE CHARACTERISTICS

(LT6230/LT6231/LT6232)

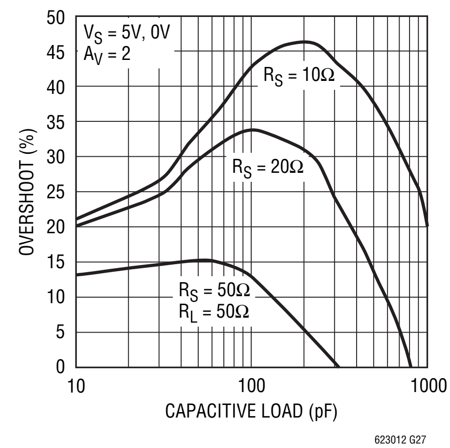
Power Supply Rejection Ratio vs Frequency



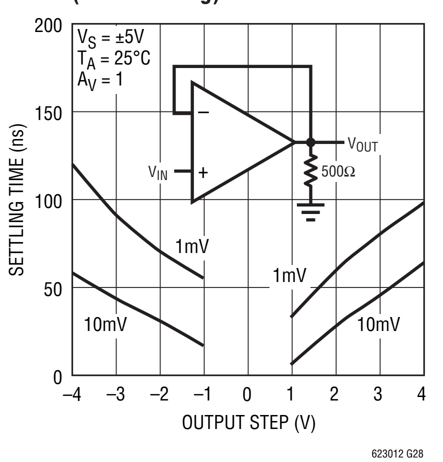
Series Output Resistance and Overshoot vs Capacitive Load



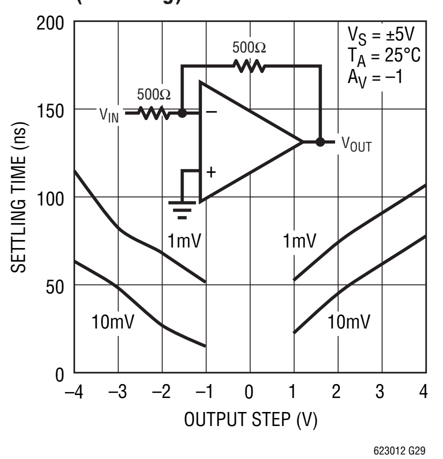
Series Output Resistance and Overshoot vs Capacitive Load



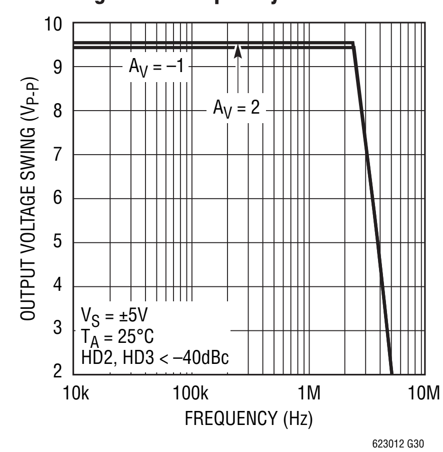
Settling Time vs Output Step (Noninverting)



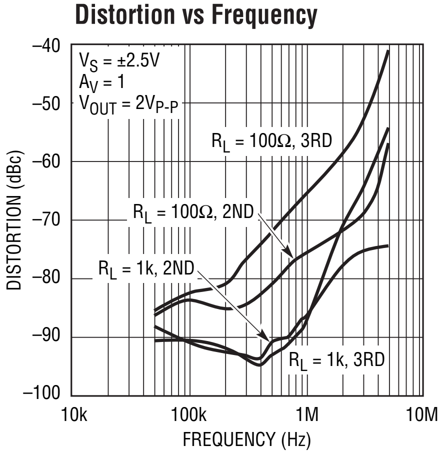
Settling Time vs Output Step (Inverting)



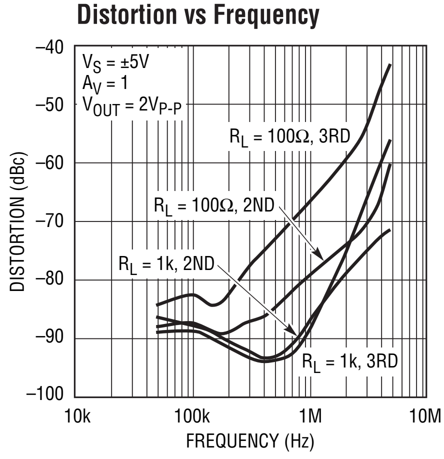
Maximum Undistorted Output Signal vs Frequency



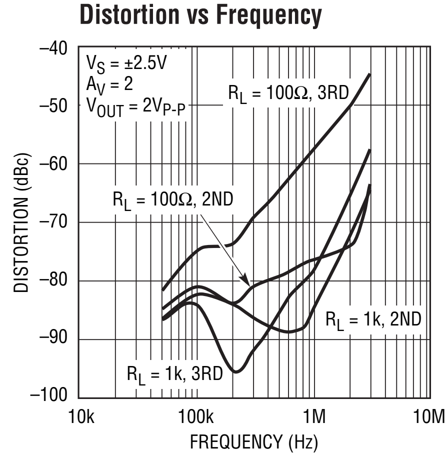
Distortion vs Frequency



Distortion vs Frequency



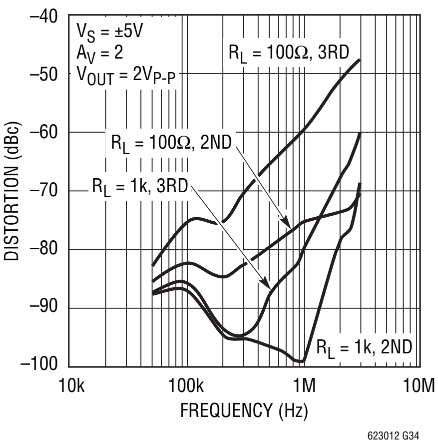
Distortion vs Frequency



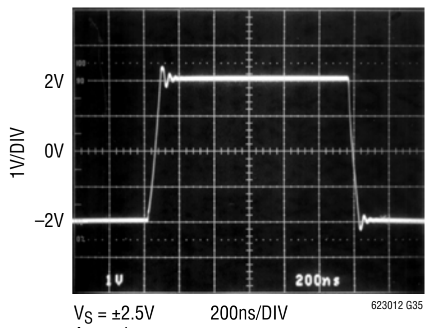
TYPICAL PERFORMANCE CHARACTERISTICS

(LT6230/LT6231/LT6232)

Distortion vs Frequency

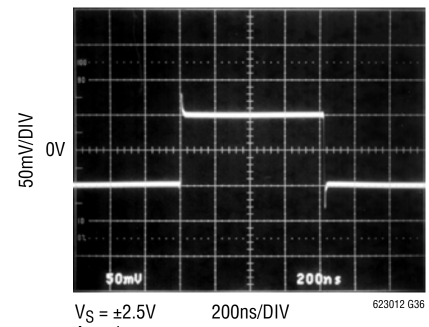


Large-Signal Response



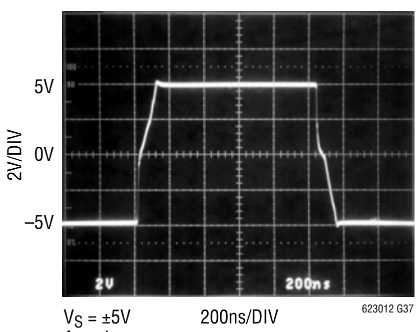
V_S = ±2.5V 200ns/DIV
A_V = –1
R_L = 1k

Small-Signal Response



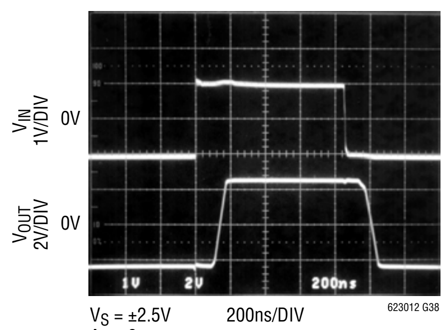
V_S = ±2.5V 200ns/DIV
A_V = 1
R_L = 1k

Large-Signal Response



V_S = ±5V 200ns/DIV
A_V = 1
R_L = 1k

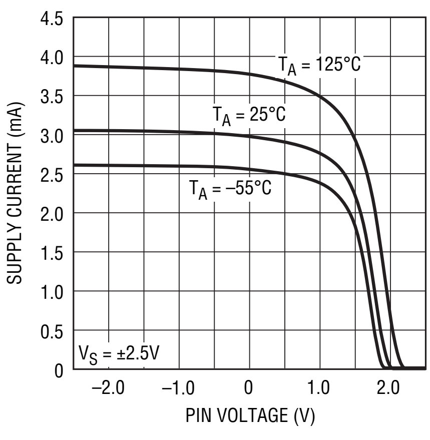
Output Overdrive Recovery



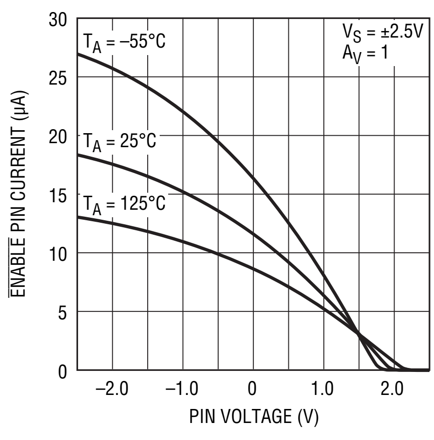
V_S = ±2.5V 200ns/DIV
A_V = 3

(LT6230) $\overline{\text{ENABLE}}$ Characteristics

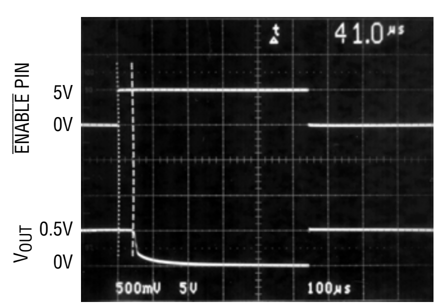
Supply Current vs $\overline{\text{ENABLE}}$ Pin Voltage



$\overline{\text{ENABLE}}$ Pin Current vs $\overline{\text{ENABLE}}$ Pin Voltage



$\overline{\text{ENABLE}}$ Pin Response Time

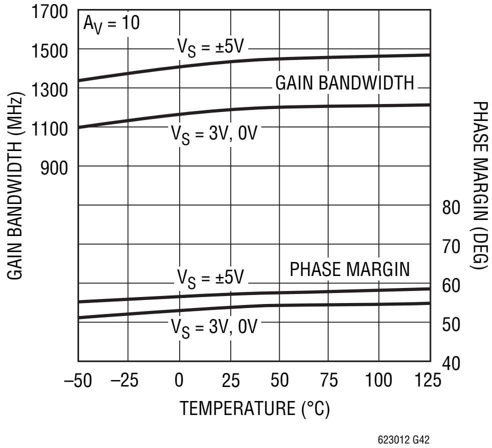


V_S = ±2.5V 100μs/DIV
V_{IN} = 0.5V
A_V = 1
R_L = 1k

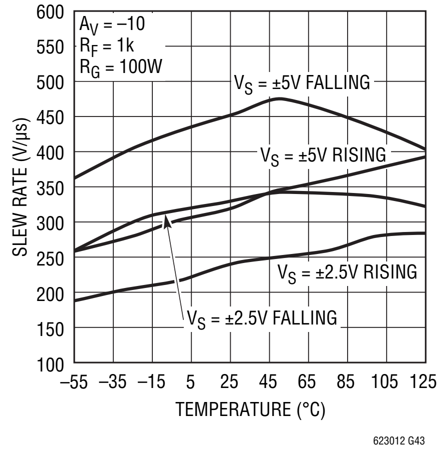
TYPICAL PERFORMANCE CHARACTERISTICS

(LT6230-10)

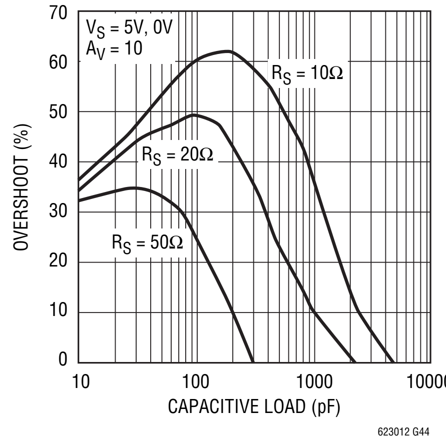
Gain Bandwidth and Phase Margin vs Temperature



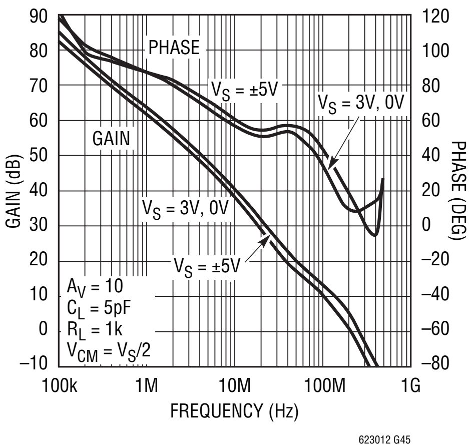
Slew Rate vs Temperature



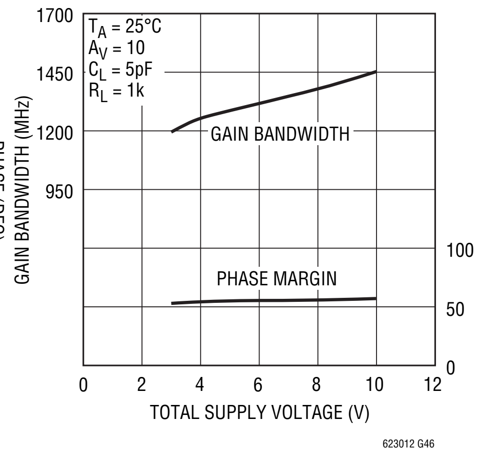
Series Output Resistor and Overshoot vs Capacitive Load



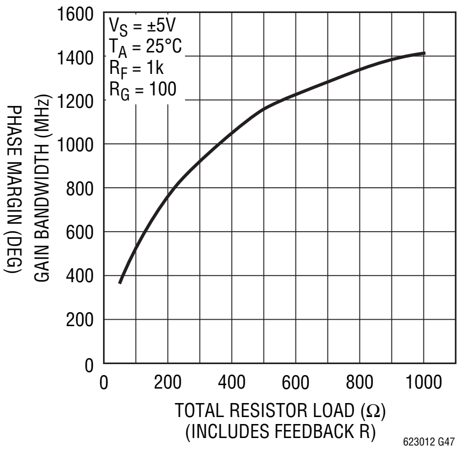
Open-Loop Gain and Phase vs Frequency



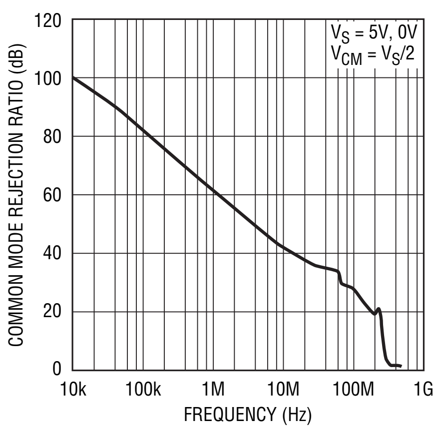
Gain Bandwidth and Phase Margin vs Supply Voltage



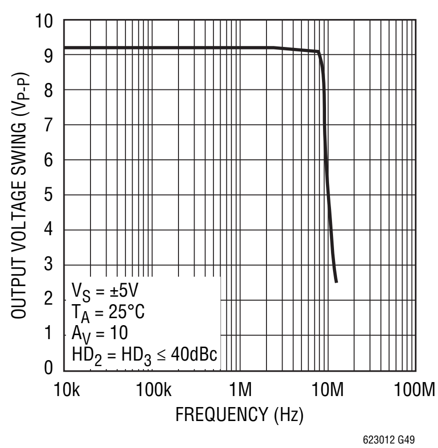
Gain Bandwidth vs Resistor Load



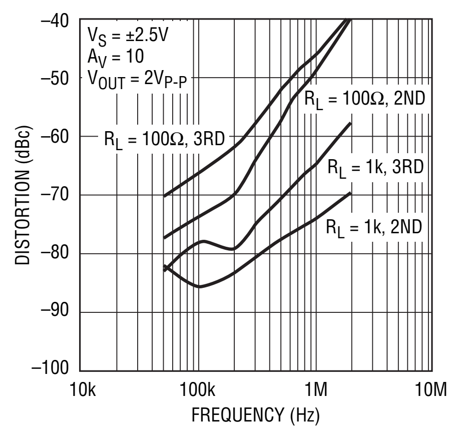
Common Mode Rejection Ratio vs Frequency



Maximum Undistorted Output Signal vs Frequency



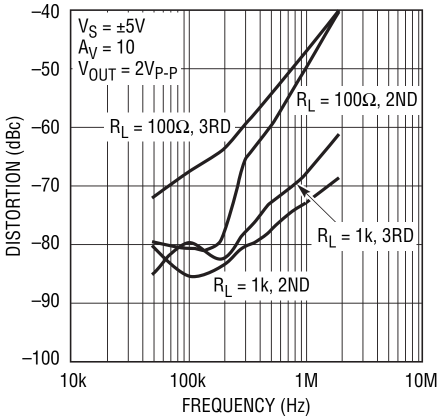
2nd and 3rd Harmonic Distortion vs Frequency



TYPICAL PERFORMANCE CHARACTERISTICS

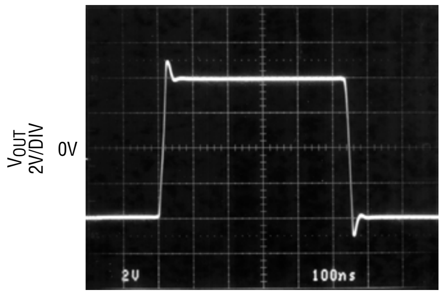
(LT6230-10)

2nd and 3rd Harmonic Distortion vs Frequency



623012 G51

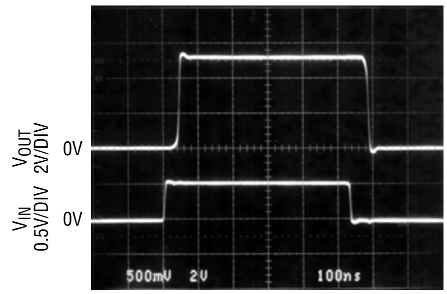
Large-Signal Response



V_S = ±5V 100ns/DIV
A_V = 10
R_F = 900Ω
R_G = 100Ω

623012 G52

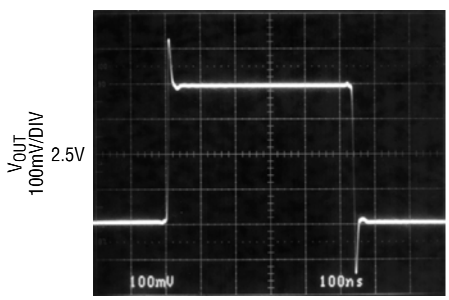
Output-Overload Recovery



V_S = 5V, 0V 100ns/DIV
A_V = 10
R_F = 900Ω
R_G = 100Ω

623012 G53

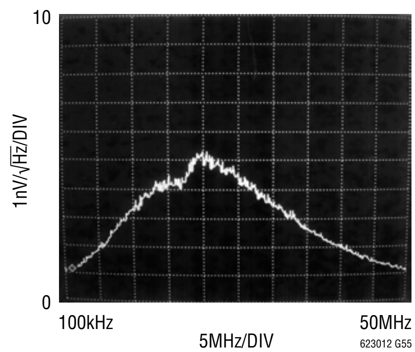
Small-Signal Response



V_S = 5V, 0V 100ns/DIV
A_V = 10
R_F = 900Ω
R_G = 100Ω

623012 G54

Input Referred High Frequency Noise Spectrum



623012 G55

APPLICATIONS INFORMATION

Amplifier Characteristics

Figure 1 is a simplified schematic of the LT6230/LT6231/LT6232, which has a pair of low noise input transistors Q1 and Q2. A simple current mirror, Q3/Q4, converts the differential signal to a single-ended output, and these transistors are degenerated to reduce their contribution to the overall noise.

Capacitor C1 reduces the unity-cross frequency and improves the frequency stability without degrading the gain bandwidth of the amplifier. Capacitor C_M sets the overall amplifier gain bandwidth. The differential drive generator supplies current to transistors Q5 and Q6 that swing the output from rail-to-rail.

Input Protection

There are back-to-back diodes, D1 and D2 across the + and – inputs of these amplifiers to limit the differential input voltage to ±0.7V. The inputs of the LT6230/LT6231/LT6232 do not have internal resistors in series with the input transistors. This technique is often used to protect the input devices from overvoltage that causes excessive current to flow. The addition of these resistors would significantly degrade the low noise voltage of these amplifiers. For instance, a 100Ω resistor in series with each input would generate 1.8nV/√Hz of noise, and the total amplifier noise voltage would rise from 1.1nV/√Hz to 2.1nV/√Hz. Once the input differential voltage exceeds ±0.7V, steady-state current conducted through the protection diodes should be limited to ±40mA. This implies 25Ω of protection resistance is necessary per volt of overdrive beyond ±0.7V. These input diodes are rugged enough to handle transient currents due to amplifier slew rate overdrive and clipping without protection resistors.

The photo of Figure 2 shows the output response to an input overdrive with the amplifier connected as a voltage follower. With the input signal low, current source I_1 saturates and the differential drive generator drives Q6 into saturation so the output voltage swings all the way to $V^–$. The input can swing positive until transistor Q2 saturates into current mirror Q3/Q4. When saturation occurs, the output tries to phase invert, but diode D2 conducts current from the signal source to the output through the feedback connection. The output is clamped a diode drop below the input. In this photo, the input signal generator is limiting at about 20mA.

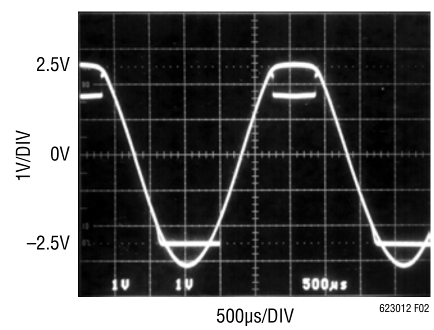


Figure 2. V_S = ±2.5V, A_V = 1 with Large Overdrive

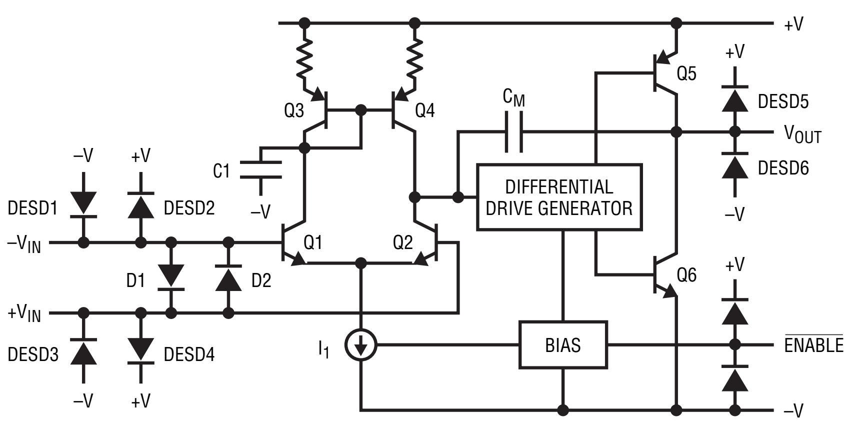


Figure 1. Simplified Schematic

APPLICATIONS INFORMATION

With the amplifier connected in a gain of $A_V \geq 2$, the output can invert with very heavy overdrive. To avoid this inversion, limit the input overdrive to 0.5V beyond the power supply rails.

ESD

The LT6230/LT6231/LT6232 have reverse-biased ESD protection diodes on all inputs and outputs as shown in Figure 1. If these pins are forced beyond either supply, unlimited current will flow through these diodes. If the current is transient and limited to one hundred milliamps or less, no damage to the device will occur.

Noise

The noise voltage of the LT6230/LT6231/LT6232 is equivalent to that of a 75Ω resistor, and for the lowest possible noise it is desirable to keep the source and feedback resistance at or below this value, i.e., $R_S + R_G||R_{FB} \leq 75\Omega$. With $R_S + R_G||R_{FB} = 75\Omega$ the total noise of the amplifier is:

$$e_N=\sqrt{(1.1nV)^2+(1.1nV)^2} = 1.55nV/\sqrt{Hz}$$

Below this resistance value, the amplifier dominates the noise, but in the region between 75Ω and about 3k, the noise is dominated by the resistor thermal noise. As the total resistance is further increased beyond 3k, the amplifier noise current multiplied by the total resistance eventually dominates the noise.

The product of $e_N \bullet \sqrt{I_{SUPPLY}}$ is an interesting way to gauge low noise amplifiers. Most low noise amplifiers with low eN have high I_{SUPPLY} current. In applications that require low noise voltage with the lowest possible supply current, this product can prove to be enlightening. The LT6230/LT6231/LT6232 have an $e_N \bullet \sqrt{I_{SUPPLY}}$ product of only 1.9 per amplifier, yet it is common to see amplifiers with similar noise specifications to have $e_N \bullet \sqrt{I_{SUPPLY}}$ as high as 13.5.

For a complete discussion of amplifier noise, see the LT1028 data sheet.

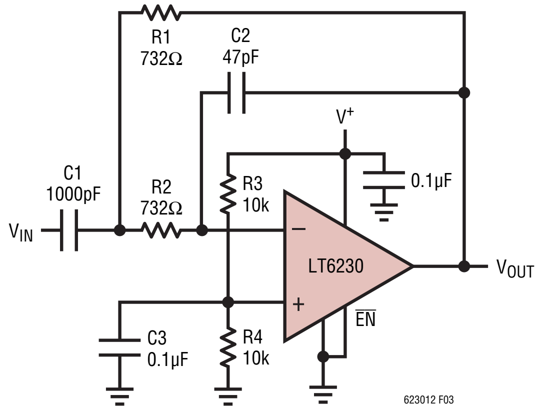
ENABLE Pin

The LT6230 includes an $\overline{\text{ENABLE}}$ pin that shuts down the amplifier to 10µA maximum supply current. The $\overline{\text{ENABLE}}$ pin must be driven low to operate the amplifier with normal supply current. The $\overline{\text{ENABLE}}$ pin must be driven high to within 0.35V of V^+ to shut down the supply current. This can be accomplished with simple gate logic; however care must be taken if the logic and the LT6230 operate from different supplies. If this is the case, then open-drain logic can be used with a pull-up resistor to ensure that the amplifier remains off. See the Typical Performance Characteristics.

The output leakage current when disabled is very low; however, current can flow into the input protection diodes D1 and D2 if the output voltage exceeds the input voltage by a diode drop.

TYPICAL APPLICATIONS

Single Supply, Low Noise, Low Power, Bandpass Filter with Gain = 10



$f_0 = \frac{1}{2\pi RC} = 1\text{MHz}$

$C = \sqrt{C1C2}$, R = R1 = R2

$f_0 = \left(\frac{732\Omega}{R}\right)$MHz, MAXIMUM f_0 = 1MHz

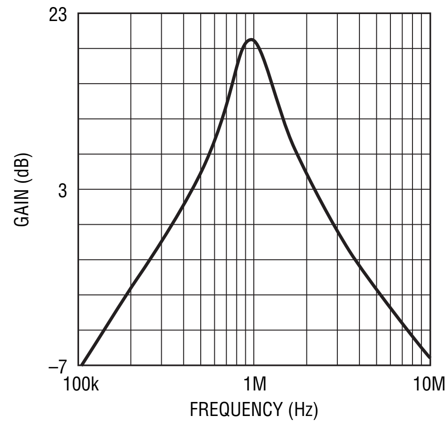
$f_{-3dB} = \frac{f_0}{2.5}$

A_V = 20dB at f_0

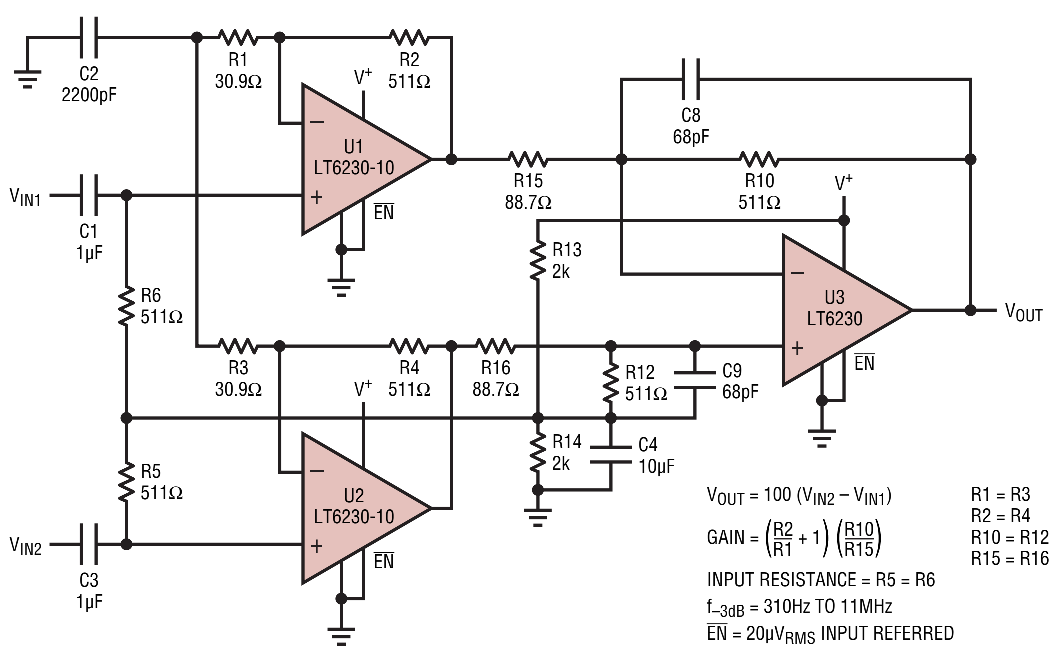
$\overline{EN}$ = 4µV_{RMS} INPUT REFERRED

I_S = 3.7mA FOR V^+ = 5V

Frequency Response Plot of Bandpass Filter



Low Noise, Low Power, Single Supply, Instrumentation Amplifier with Gain = 100



$V_{OUT} = 100\,(V_{IN2} - V_{IN1})$

$\text{GAIN} = \left(\frac{R2}{R1} + 1\right)\left(\frac{R10}{R15}\right)$

INPUT RESISTANCE = R5 = R6

f_{-3dB} = 310Hz TO 11MHz

$\overline{EN}$ = 20µV_{RMS} INPUT REFERRED

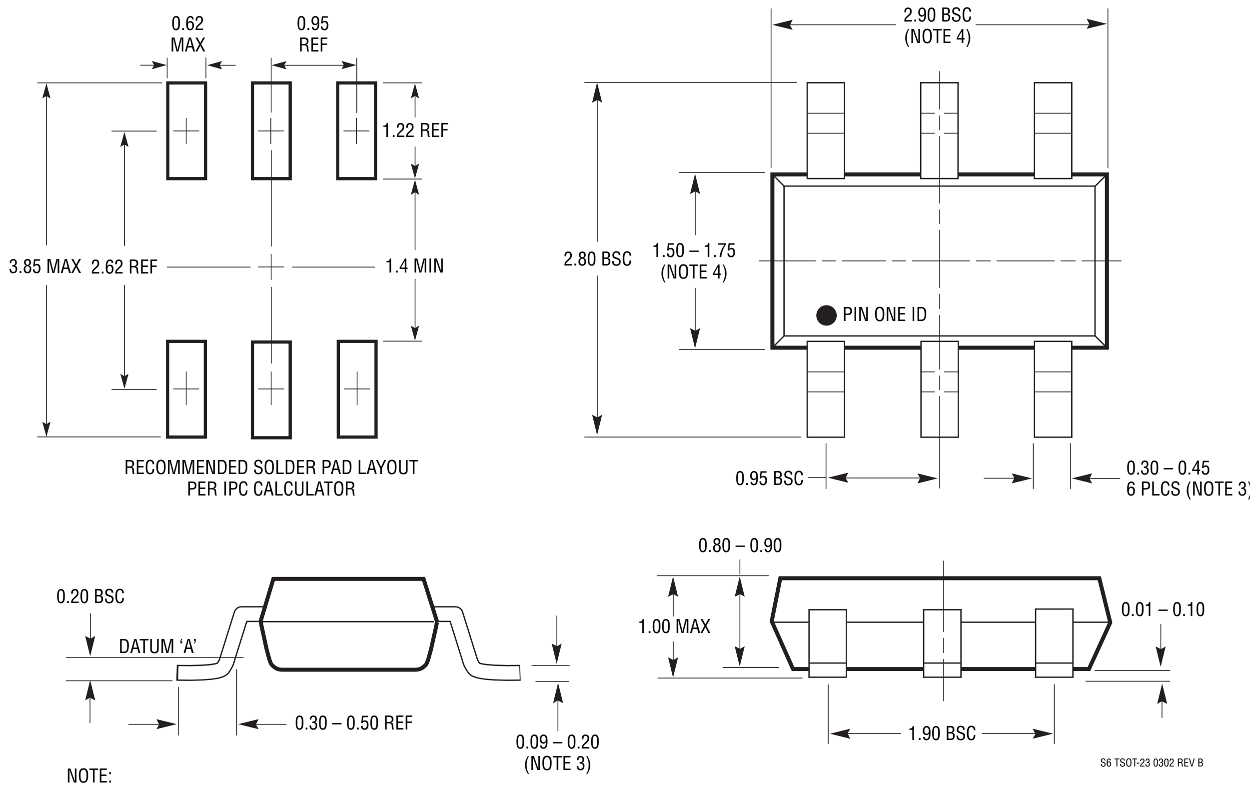
I_S = 10.5mA FOR V_S = 5V, 0V

R1 = R3
R2 = R4
R10 = R12
R15 = R16

623012 F05

PACKAGE DESCRIPTION

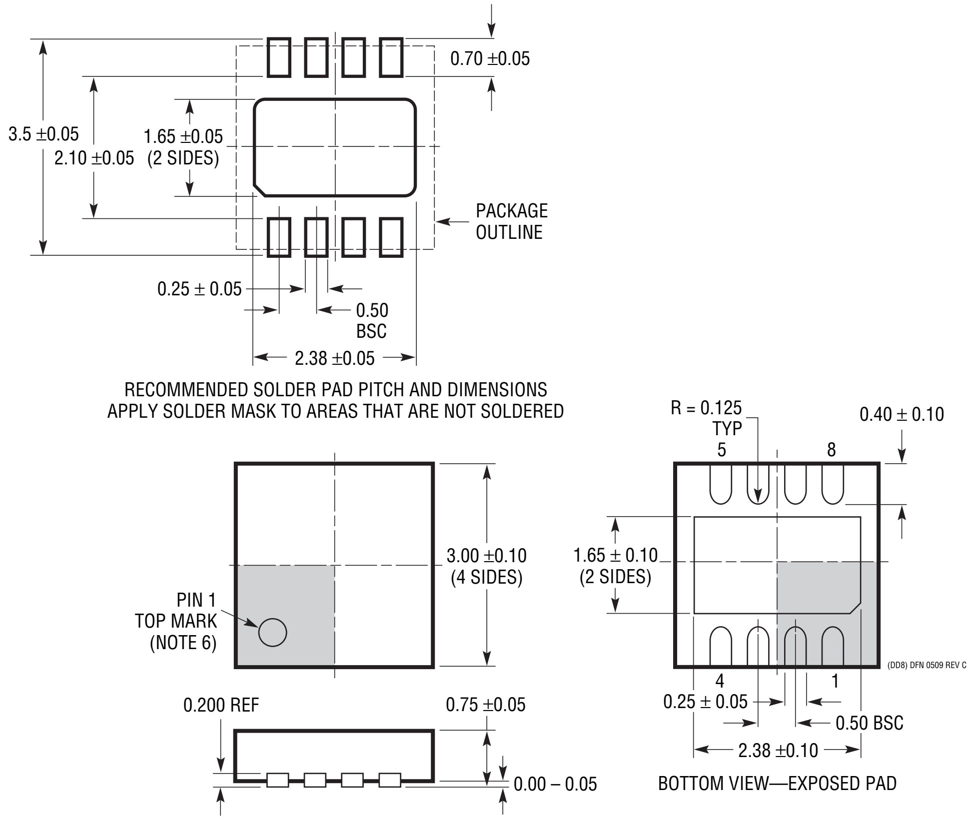
S6 Package
6-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1636)



NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

PACKAGE DESCRIPTION

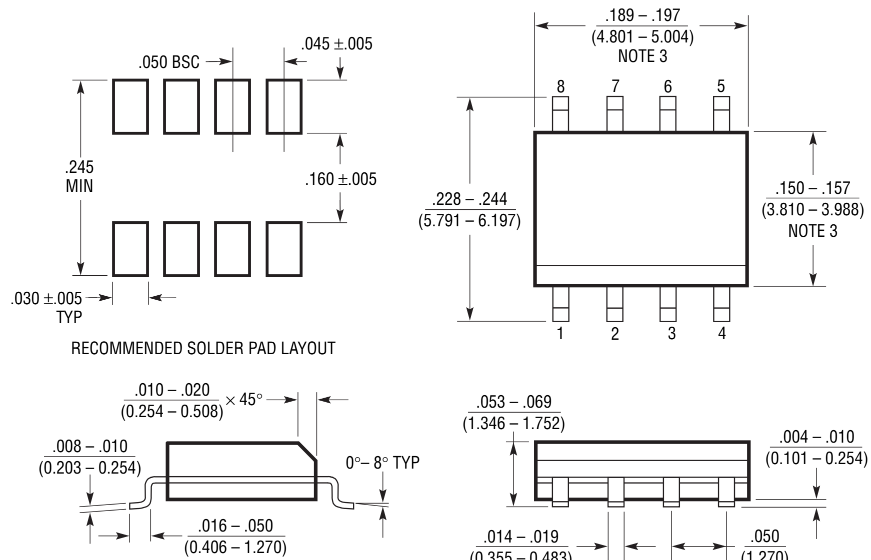
DD Package
8-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1698 Rev C)



NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

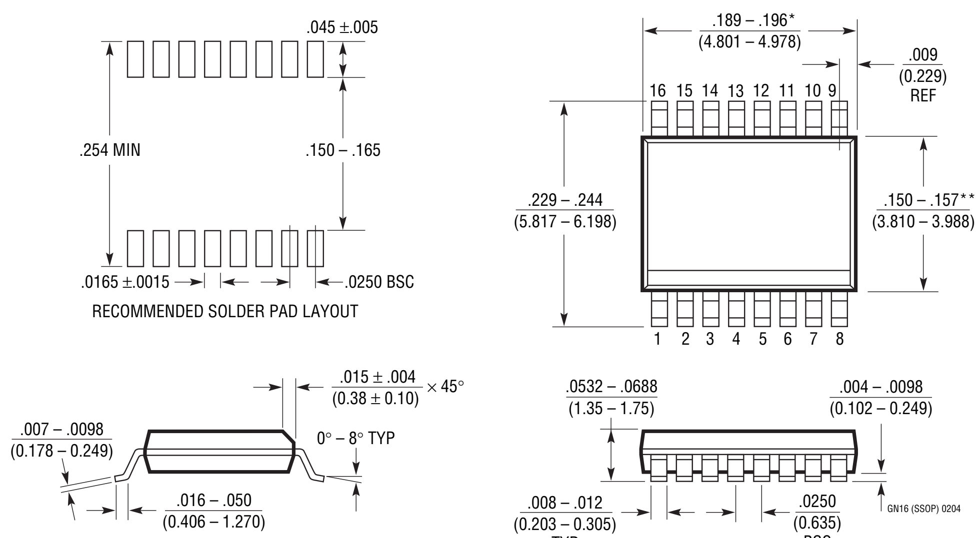
S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)



NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{\text{(MILLIMETERS)}}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

SO8 0303

GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{\text{(MILLIMETERS)}}$
3. DRAWING NOT TO SCALE
*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

REVISION HISTORY (Revision history begins at Rev C)

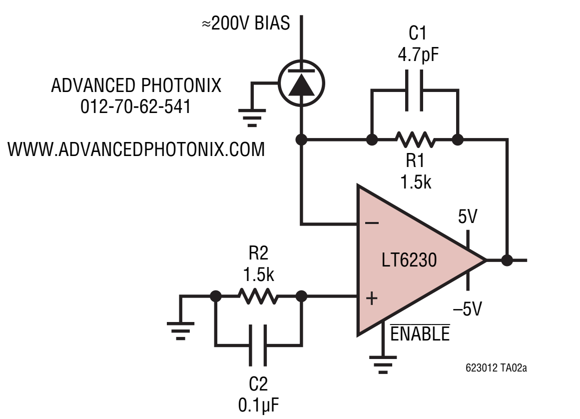
REV	DATE	DESCRIPTION	PAGE NUMBER
C	1/11	Updated ENABLE Pin section in Applications Information	18

TYPICAL APPLICATIONS

The LT6230 is applied as a transimpedance amplifier with an I-to-V conversion gain of 1.5kΩ set by R1. The LT6230 is ideally suited to this application because of its low input offset voltage and current, and its low noise. This is because the 1.5k resistor has an inherent thermal noise of 5nV/√Hz or 3.4pA/√Hz at room temperature, while the LT6230 contributes only 1.1nV and 2.4pA /√Hz. So, with respect to both voltage and current noises, the LT6230 is actually quieter than the gain resistor.

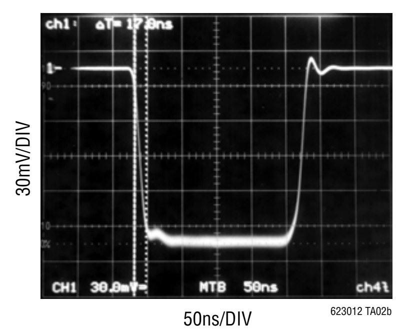
The circuit uses an avalanche photodiode with the cathode biased to approximately 200V. When light is incident on the photodiode, it induces a current I_{PD} which flows into the amplifier circuit. The amplifier output falls negative to maintain balance at its inputs. The transfer function is therefore $V_{OUT} = -I_{PD} \bullet 1.5k$. C1 ensures stability and good settling characteristics. Output offset was measured at 280µV, so low in part because R2 serves to cancel the DC effects of bias current. Output noise was measured at $1.1mV_{P-P}$ on a 100MHz measurement bandwidth, with C2 shunting R2's thermal noise. As shown in the scope photo, the rise time is 17ns, indicating a signal bandwidth of 20MHz.

Low Power Avalanche Photodiode Transimpedance Amplifier
I_S = 3.3mA



OUTPUT OFFSET = 500µV TYPICAL
BANDWIDTH = 20MHz
OUTPUT NOISE = $1.1mV_{P-P}$ (100MHz MEASUREMENT BW)

Photodiode Amplifier Time Domain Response



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1028	Single, Ultralow Noise 50MHz Op Amp	0.85nV/√Hz
LT1677	Single, Low Noise Rail-to-Rail Amplifier	3V Operation, 2.5mA, 4.5nV/√Hz, 60µV Max V_{OS}
LT1806/LT1807	Single/Dual, Low Noise 325MHz Rail-to-Rail Amplifier	2.5V Operation, 550µV Max V_{OS}, 3.5nV/√Hz
LT6200/LT6201	Single/Dual, Low Noise 165MHz	0.95nV√Hz, Rail-to-Rail Input and Output
LT6202/LT6203/LT6204	Single/Dual/Quad, Low Noise, Rail-to-Rail Amplifier	1.9nV/√Hz, 3mA Max, 100MHz Gain Bandwidth

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