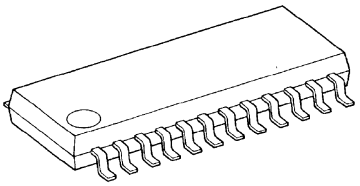
TOSHIBA Intelligent Power Device Silicon Monolithic Power MOS Integrated Circuit

TPD7210F

Power MOSFET Gate Driver for 3-Phase DC Motor

The TPD7210F is a power MOSFET gate driver for 3-phase full-bridge circuits that use a charge pump system. The inclusion of a charge pump circuit for high-side drive inside the IC makes it easy to configure a 3-phase full-bridge circuit.



SSOP24-P-300-1.00C

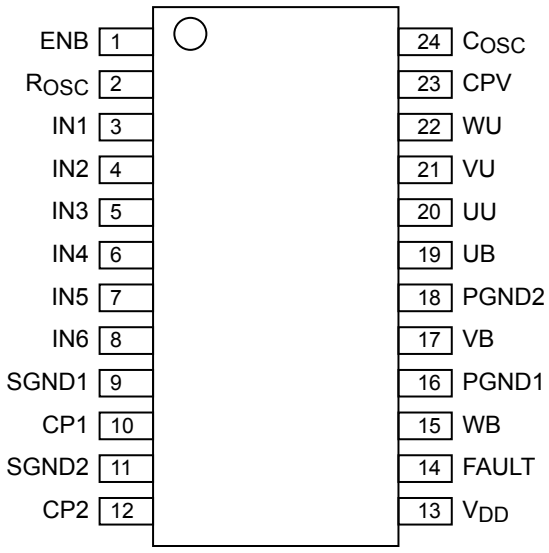
Weight: 0.29 g (typ.)

Features

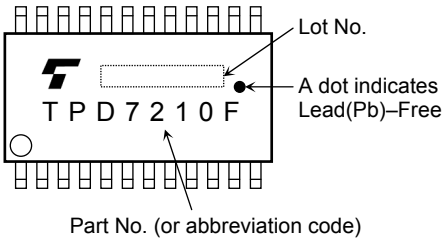
- Power MOSFET gate driver for 3-phase DC motor
- Built-in diagnosis function: under-voltage detection
- Built-in charge pump circuit
- Package: SSOP-24 (300 mil) with embossed-tape packing

Pin Assignment

(TOP VIEW)

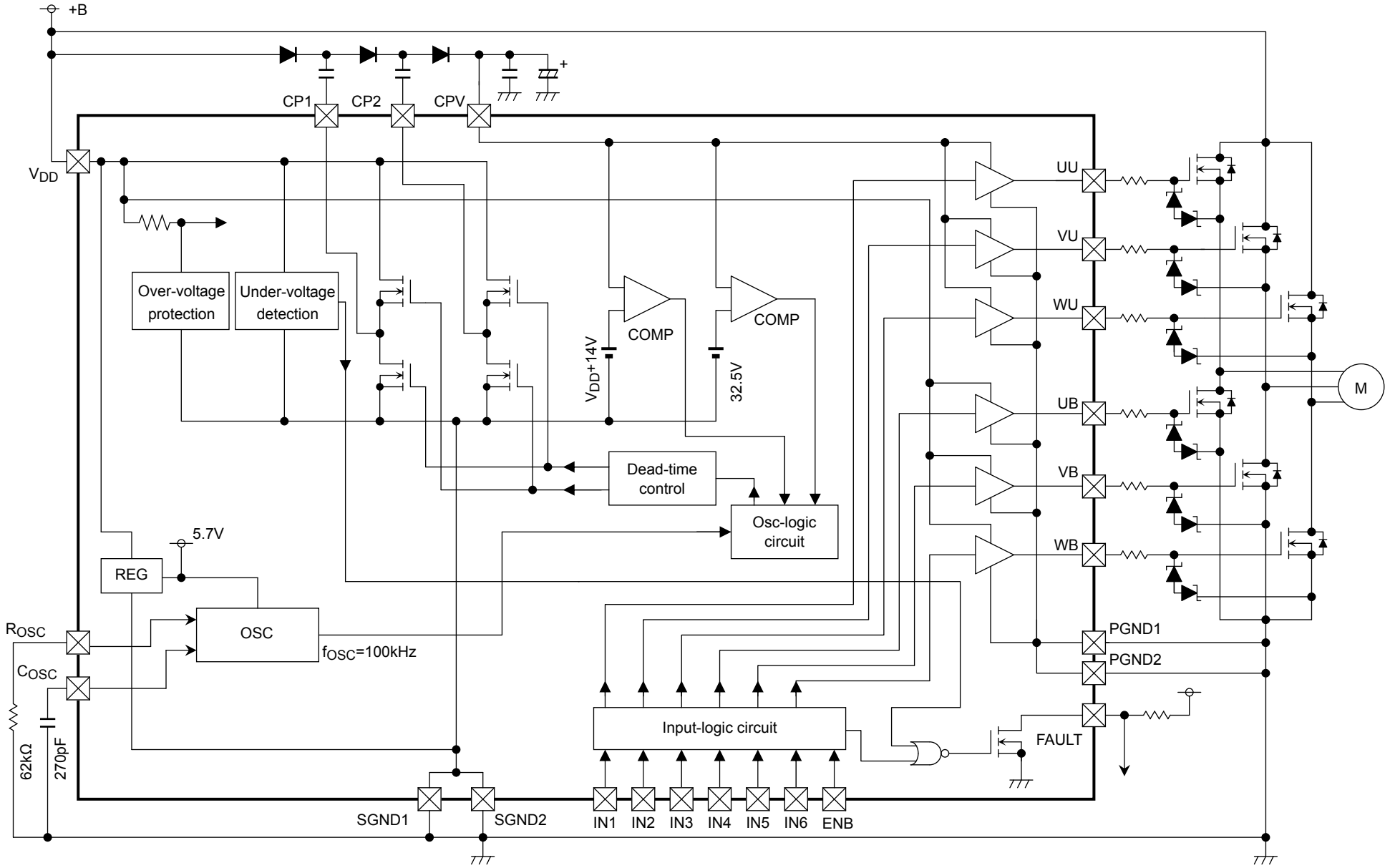


Marking



This product has a MOS structure and is sensitive to electrostatic discharge.

Block Diagram / Application Circuit



Pin Description

Pin No.	Symbol	Pin Description
1	ENB	Inhibit pin (high active): By driving this pin low, all outputs can be turned off regardless of input signals. Built-in pull-down resistor (100 kΩ typ.).
2	R_{OSC}	This pin sets the oscillation frequency for the charge pump drive. Connect a 62 kΩ (typ.) resistor.
3	IN1	Input pin: it controls the power MOSFET connected to UU. Built-in pull-down resistor (100 kΩ typ.).
4	IN2	Input pin: it controls the power MOSFET connected to VU. Built-in pull-down resistor (100 kΩ typ.).
5	IN3	Input pin: it controls the power MOSFET connected to WU. Built-in pull-down resistor (100 kΩ typ.).
6	IN4	Input pin: it controls the power MOSFET connected to UB. Built-in pull-down resistor (100 kΩ typ.).
7	IN5	Input pin: it controls the power MOSFET connected to VB. Built-in pull-down resistor (100 kΩ typ.).
8	IN6	Input pin: it controls the power MOSFET connected to WB. Built-in pull-down resistor (100 kΩ typ.).
9	SGND1	Signal block GND pin: shared internally with pin 11.
10	CP1	Capacitor pin for charge pump.
11	SGND2	Signal block GND pin: shared internally with pin 9.
12	CP2	Capacitor pin for charge pump.
13	V_{DD}	Power supply pin: when under-voltage (5.5 V typ.) is detected, FAULT output goes high. On this occasion, all outputs are switching normally, and charge pump circuit does not come to a stop.
14	FAULT	Diagnosis output pin: when under-voltage (5.5 V typ.) is detected, FAULT output goes high. High-side/low-side arm shorting mode, FAULT output goes high and all outputs are shut down. Circuit configuration is N-ch open drain.
15	WB	Drives the power MOSFET connected to the low side of the W phase.
16	PGND1	Power block GND pin: shared internally with pin 18.
17	VB	Drives the power MOSFET connected to the low side of the V phase.
18	PGND2	Power block GND pin: shared internally with pin 16.
19	UB	Drives the power MOSFET connected to the low side of the U phase.
20	UU	Drives the power MOSFET connected to the high side of the U phase.
21	VU	Drives the power MOSFET connected to the high side of the V phase.
22	WU	Drives the power MOSFET connected to the high side of the W phase.
23	CPV	Final stage capacitor pin for the charge pump.
24	C_{OSC}	This pin sets the oscillation frequency for the charge pump drive. Connect a 270pF (typ.) capacitor.

Truth Table
(All outputs go to low for input in high-side/low-side arm shorting mode)

Mode No.	Input						Output						Remarks
	IN1 (UU)	IN2 (VU)	IN3 (WU)	IN4 (UB)	IN5 (VB)	IN6 (WB)	OUT UU	OUT VU	OUT WU	OUT UB	OUT VB	OUT WB	
01	L	L	L	L	L	L	L	L	L	L	L	L	
02	H	L	L	L	L	L	H	L	L	L	L	L	
03	L	H	L	L	L	L	L	H	L	L	L	L	
04	L	L	H	L	L	L	L	L	H	L	L	L	
05	L	L	L	H	L	L	L	L	L	H	L	L	
06	L	L	L	L	H	L	L	L	L	L	H	L	
07	L	L	L	L	L	H	L	L	L	L	L	H	
08	H	L	L	H	L	L	L	L	L	L	L	L	High-side/low-side arm shorting mode *
09	H	L	L	L	H	L	H	L	L	L	H	L	120° square wave conducting normal mode
10	H	L	L	L	L	H	H	L	L	L	L	H	120° square wave conducting normal mode
11	L	H	L	H	L	L	L	H	L	H	L	L	120° square wave conducting normal mode
12	L	H	L	L	H	L	L	L	L	L	L	L	High-side/low-side arm shorting mode *
13	L	H	L	L	L	H	L	H	L	L	L	H	120° square wave conducting normal mode
14	L	L	H	H	L	L	L	L	H	H	L	L	120° square wave conducting normal mode
15	L	L	H	L	H	L	L	L	H	L	H	L	120° square wave conducting normal mode
16	L	L	H	L	L	H	L	L	L	L	L	L	High-side/low-side arm shorting mode *
17	H	H	L	L	L	L	H	H	L	L	L	L	
18	L	H	H	L	L	L	L	H	H	L	L	L	
19	H	L	H	L	L	L	H	L	H	L	L	L	
20	L	L	L	H	H	L	L	L	L	H	H	L	
21	L	L	L	L	H	H	L	L	L	L	H	H	
22	L	L	L	H	L	H	L	L	L	H	L	H	
23	H	H	L	H	L	L	L	L	L	L	L	L	High-side/low-side arm shorting mode *
24	H	H	L	L	H	L	L	L	L	L	L	L	High-side/low-side arm shorting mode *
25	H	H	L	L	L	H	H	H	L	L	L	H	
26	L	H	H	H	L	L	L	H	H	H	L	L	
27	L	H	H	L	H	L	L	L	L	L	L	L	High-side/low-side arm shorting mode *
28	L	H	H	L	L	H	L	L	L	L	L	L	High-side/low-side arm shorting mode *
29	H	L	H	H	L	L	L	L	L	L	L	L	High-side/low-side arm shorting mode *
30	H	L	H	L	H	L	H	L	H	L	H	L	

*: High-side/low-side arm shorting mode is disabled by the internal logic. FAULT output goes high (open-drain, high-impedance)

*: By driving ENB pin low, all outputs can be turned off regardless of input signals. By driving ENB pin high, all outputs are switching normally.

Mode No.	Input						Output						Remarks
	IN1 (UU)	IN2 (VU)	IN3 (WU)	IN4 (UB)	IN5 (VB)	IN6 (WB)	OUT UU	OUT VU	OUT WU	OUT UB	OUT VB	OUT WB	
31	H	L	H	L	L	H	L	L	L	L	L	L	High-side/low-side arm shorting mode *
32	H	L	L	H	H	L	L	L	L	L	L	L	High-side/low-side arm shorting mode *
33	H	L	L	L	H	H	H	L	L	L	H	H	
34	H	L	L	H	L	H	L	L	L	L	L	L	High-side/low-side arm shorting mode *
35	L	H	L	H	H	L	L	L	L	L	L	L	High-side/low-side arm shorting mode *
36	L	H	L	L	H	H	L	L	L	L	L	L	High-side/low-side arm shorting mode *
37	L	H	L	H	L	H	L	H	L	H	L	H	
38	L	L	H	H	H	L	L	L	H	H	H	L	
39	L	L	H	L	H	H	L	L	L	L	L	L	High-side/low-side arm shorting mode *
40	L	L	H	H	L	H	L	L	L	L	L	L	High-side/low-side arm shorting mode *
41	H	H	H	L	L	L	H	H	H	L	L	L	
42	L	L	L	H	H	H	L	L	L	H	H	H	
43	H	H	L	H	H	L	L	L	L	L	L	L	High-side/low-side arm shorting mode *
44	H	H	L	L	H	H	L	L	L	L	L	L	High-side/low-side arm shorting mode *
45	H	H	L	H	L	H	L	L	L	L	L	L	High-side/low-side arm shorting mode *
46	L	H	H	H	H	L	L	L	L	L	L	L	High-side/low-side arm shorting mode *
47	L	H	H	L	H	H	L	L	L	L	L	L	High-side/low-side arm shorting mode *
48	L	H	H	H	L	H	L	L	L	L	L	L	High-side/low-side arm shorting mode *
49	H	L	H	H	H	L	L	L	L	L	L	L	High-side/low-side arm shorting mode *
50	H	L	H	L	H	H	L	L	L	L	L	L	High-side/low-side arm shorting mode *
51	H	L	H	H	L	H	L	L	L	L	L	L	High-side/low-side arm shorting mode *
52	H	H	H	H	L	L	L	L	L	L	L	L	High-side/low-side arm shorting mode *
53	H	H	H	L	H	L	L	L	L	L	L	L	High-side/low-side arm shorting mode *
54	H	H	H	L	L	H	L	L	L	L	L	L	High-side/low-side arm shorting mode *
55	H	L	L	H	H	H	L	L	L	L	L	L	High-side/low-side arm shorting mode *
56	L	H	L	H	H	H	L	L	L	L	L	L	High-side/low-side arm shorting mode *
57	L	L	H	H	H	H	L	L	L	L	L	L	High-side/low-side arm shorting mode *
58	H	H	H	H	H	L	L	L	L	L	L	L	High-side/low-side arm shorting mode *
59	H	H	H	L	H	H	L	L	L	L	L	L	High-side/low-side arm shorting mode *
60	H	H	H	H	L	H	L	L	L	L	L	L	High-side/low-side arm shorting mode *
61	H	H	L	H	H	H	L	L	L	L	L	L	High-side/low-side arm shorting mode *
62	L	H	H	H	H	H	L	L	L	L	L	L	High-side/low-side arm shorting mode *
63	H	L	H	H	H	H	L	L	L	L	L	L	High-side/low-side arm shorting mode *
64	H	H	H	H	H	H	L	L	L	L	L	L	High-side/low-side arm shorting mode *

*: High-side/low-side arm shorting mode is disabled by the internal logic. FAULT output goes high (open-drain, high-impedance)

*: By driving ENB pin low, all outputs can be turned off regardless of input signals. By driving ENB pin high, all outputs are switching normally.

Absolute Maximum Ratings (T_a = 25°C)

Characteristic	Symbol	Rating	Unit	Remarks
Power supply voltage	$V_{DD(1)}$	−0.5 to 30	V	
Power supply voltage	$V_{DD(2)}$	45	V	Pulse width ≤ 200ms
Output current	I_{SOURCE}	1	A	Pulse width ≤ 10μs
	I_{SINK}	1		
Input voltage	V_{IN} , V_{ENB}	−0.5 to 7.0	V	
FAULT pin voltage	V_{FAULT}	30	V	
PGND pin negative voltage	$P_{GND}(-)$	−0.5	V	Negative voltage that can be applied to PGND pin (reference to SGND pin)
Output pin negative voltage	$V_{OUT(-)}$	−0.5	V	Negative voltage that can be applied to UU, VU,WU,UB,VB and WB pins (Reference to SGND pin)
FAULT pin current	I_{FAULT}	5	mA	
Power dissipation	P_D	0.8	W	
		1.2 (Note2)		
Operating temperature	T_{opr}	−40 to 125	°C	
Junction temperature	T_j	150	°C	
Storage temperature	T_{stg}	−40 to 150	°C	

Note1 : Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/”Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Thermal Resistance

Characteristic	Symbol	Rating	Unit
Junction to ambient thermal resistance	$R_{th\ (j-a)}$	156.3	°C / W
		104.2 (Note2)	

Note2: When the device is mounted on a 60 mm × 60 mm × 1.6 mm glass epoxy PCB

Electrical Characteristics

(Unless otherwise specified, T_a = −40 to 125°C, CP1, 2 = 0.1μF, R_{OSC} = 62kΩ, C_{OSC} = 270pF)

Characteristic	Symbol	Test Circuit	Condition	Min	Typ.	Max	Unit	Remarks
Operating supply voltage (Note3)	$V_{DD(opr)}$	−	−	4.5	13.5	18	V	
Supply current	$I_{DD(1)}$	−	V_{DD} = 13.5 V	−	−	7	mA	Oscillation circuit stops
	$I_{DD(2)}$	−	V_{DD} = 13.5 V, V_{IN1} to V_{IN6} = 0 V, CP1,2 = 0.1μF	−	−	9		When oscillation circuit is operating f = 100 kHz, mean current
Input voltage	V_{IH}	−	V_{DD} = 7 to 18 V, I_O = 0 A	3.5	−	−	V	IN1 to IN6 and ENB High-level input voltage
	V_{IL}			−	−	1.5		IIN1 to IN6 and ENB low-level input voltage
Input current	I_{IH}	−	V_{DD} = 7 to 18V, V_{IN} = 5 V	−	−	200	μA	IN1 to IN6, ENB input current (per one input)
	I_{IL}		V_{DD} = 7 to 18 V, V_{IN} = 0 V	− 10	−	10	μA	
Charge pump voltage (Note4)(Note5)	V_{CPV}	−	V_{DD} = 7 V, V_{IN1} to V_{IN6} = 0 V	V_{DD} +10.9	V_{DD} +11.9	−	V	$V_{CPV} \approx 3 \times (V_{DD} - V_F)$ V_{CPV} denotes CPV pin voltage. (reference to SGND pin)
			V_{DD} = 13.5 V, V_{IN1} to V_{IN6} = 0 V	V_{DD} +12	V_{DD} +14	V_{DD} +16	V	V_{CPV} denotes CPV pin voltage. (reference to SGND pin)
			V_{DD} = 18 V, V_{IN1} to V_{IN6}= 0 V	V_{DD} +12	V_{DD} +14	V_{DD} +16	V	
High-side high-level output voltage	$V_{OH(H1)}$	−	V_{DD} = 7V, V_{IN} = 5V, I_O = −10mA	−	V_{DD} + 9.9	−	V	UU, VU and WU pin voltage (reference to SGND pin) *Measuring single pulse
	$V_{OH(H2)}$		V_{DD} = 13.5 V, V_{IN} = 5 V, I_O = −10 mA	−	V_{DD} + 12	−		
	$V_{OH(H3)}$		V_{DD} = 18 V, V_{IN} = 5 V, I_O = −10 mA	−	V_{DD} + 12	−		
High-side high-level output voltage drop	V_{DROP}		V_{IN} = 5 V, I_O = −10 mA, $V_{DROP} = V_{CPV} - V_{OH}$	−	2	3		
High-side low-level output voltage	$V_{OL(H)}$	−	V_{DD} = 7 to 18 V, V_{IN} = 0 V, I_O = 0 A	−	−	0.1		
Low-side high-level output voltage	$V_{OH(L)}$	−	V_{DD} = 7 to 18V, V_{IN} = 5V, I_O = −10mA	V_{DD}- 0.1	V_{DD}	−		UB, VB and WB pin voltage (reference to SGND pin)
Low-side low-level output voltage	$V_{OL(L)}$	−	V_{DD} = 7 to 18 V, V_{IN} = 0 V, I_O = 0 A	−	−	0.1		
Output ON resistance	R_{SOURCE}	−	V_{DD} = 13.5 V, V_{IN} = 5 V, I_O = −0.5 A	−	7	10	Ω	UU, VU, WU, UB, VB and WB output resistance pulse width ≤ 10 μs
	R_{SINK}		V_{DD} = 13.5 V, V_{IN} = 0 V, I_O = 0.5 A	−	4.5	10		

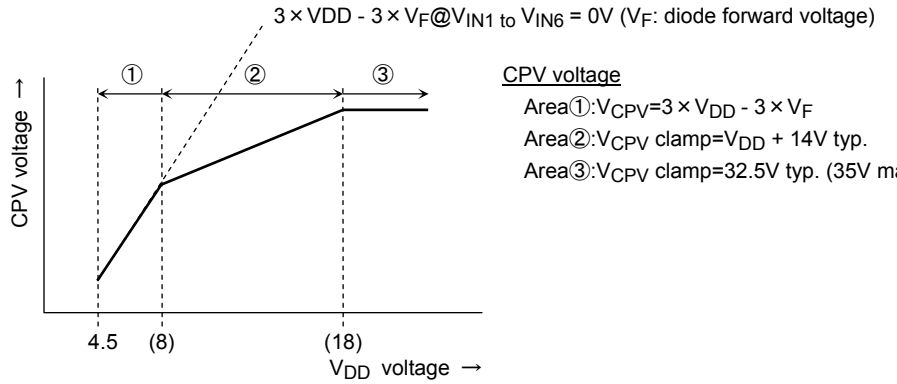
Characteristic		Symbol	Test Circuit	Condition	Min	Typ.	Max	Unit	Remarks
Under-voltage detection	Detection	V_{DDUV}	–	–	5.0	5.5	6.0	V	Under voltage detection voltage and hysteresis (V_{DD} voltage detected)
	Hysteresis	ΔV_{DDUV}			–	0.5	–		
Switching times	Turn-on delay time	$t_{d\ (ON)}$	1	V_{DD} = 13.5 V, V_{CPV} = 13.5 V, C_{OUT} = 12400 pF, R_G = 47 Ω	–	0.25	1	μs	UU, VU, WU, UB, VB and WB switching times
	Turn-on time	t_{ON}			–	0.5	2		
	Turn-off delay time	$t_{d\ (OFF)}$			–	0.25	1		
	Turn-off time	t_{OFF}			–	0.5	2		
Dead time (Note 6)		t_{dead}	–	V_{DD} = 13.5 V, $t_{dead} = t_{OFF} - t_{d(ON)}$	–	0.25	1	μs	
Oscillating frequency		f_{OSC}	–	V_{DD} = 7 to 18V, R_{OSC} = 62 kΩ, C_{OSC} = 270 pF	80	100	120	kHz	
FAULT output voltage		V_{FAULT}	–	V_{DD} = 7 to 18 V, I_{FAULT} = 1 mA	–	–	0.8	V	FAULT pin low−level voltage (open−drain)
FAULT output leakage current		I_{FAULT}	–	V_{DD} = 7 to 18 V, V_{FAULT} = 18 V	–	–	10	μA	
FAULT output delay time		$t_{d(FAULT)}$	–	–	–	–	1	μs	

Note3 : On-off output control, FAULT output and charge pump circuit operate from $V_{DD} \geq 4.5V$. However, charge pump voltage (CPV voltage) decreases by there are a lot of output currents in the condition with a low power supply voltage (V_{DD}). It may be not enough voltage (V_{GS}) to drive external power MOSFET. Be careful enough when using it .

Note4 : When converting foward voltage of the charge pump circuit diode by 0.7V. Please use the diode of high-speed type (trr ≤ 100ns).

Note5 : About the charge pump voltage

So as not to apply over-voltage to the gate-source voltage(V_{GS}) of external power MOSFET, and so as to become the best driving voltage,the clamping circuit is built into. When the CPV voltage reaches the value, so as not to apply over-voltage, the oscillation logic circuit of the charge pump is stopped.



CPV voltage

Area①:$V_{CPV} = 3 \times V_{DD} - 3 \times V_F$

Area②:V_{CPV} clamp=V_{DD} + 14V typ.

Area③:V_{CPV} clamp=32.5V typ. (35V max)

Note6 : About the dead time

High-side/low-side arm shorting mode is disabled by the internal logic. All outputs can be turned off. The deadtime of this product is 1μs. That doesn't contain deadtime of external power MOSFET. Please set the deadtime of the input signal after considering the switching time of external power MOSFET.

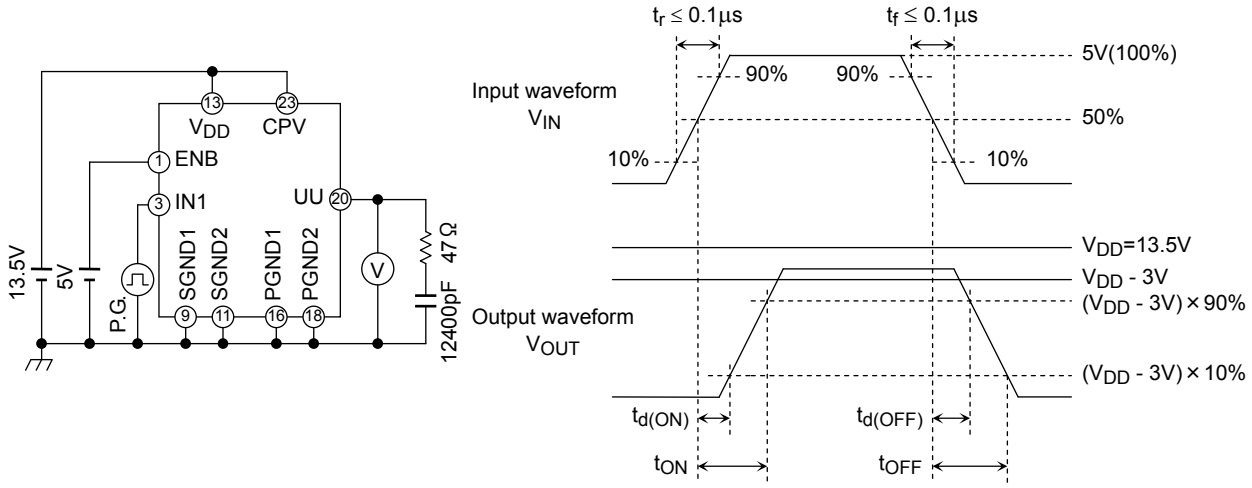
Note7 : About the direct input method of the charge pump oscillation frequency

By the oscillation signal from the outside to C_{OSC} it is possible to set up the charge pump oscillation. As this method, please input the signal to C_{OSC} after V_{DD} becomes over 9V. ($V_{COSC} \leq 5.5V$) Moreover, please use the terminal R_{OSC} by the resistance unconnection (open). When the CPV voltage reaches up to the clamping voltage, though the signal is input to C_{OSC}, the movement of the charge pump (oscillation) stops.

Test Circuit 1

Switching times

Example of measuring UU output



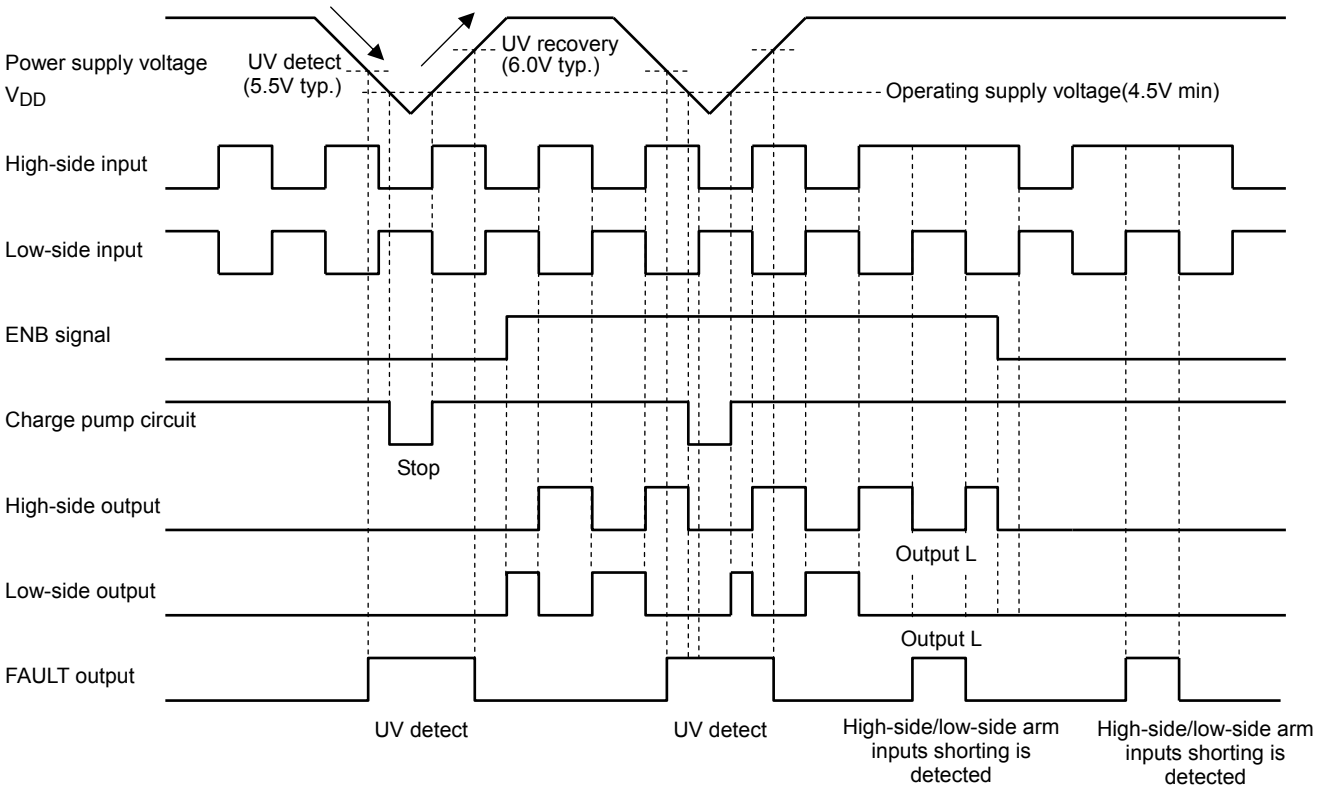
Truth Table

IN	ENB	VOUT	FAULT	STATE
L	L	L	L	Normal
H	L	L	L	
L	H	L	L	
H	H	H	L	
L	L	L	H	V_{DD} under-voltage detection
H	L	L	H	
L	H	L	H	
H	H	H	H	
High-side H	L	L	H	Upper and lower short-circuit input detection
Low-side H	H	L	H	

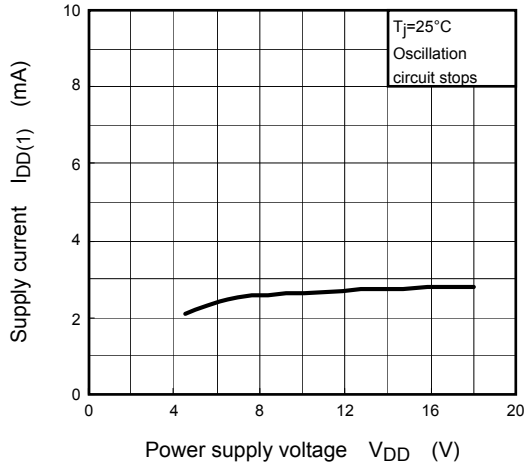
・When under-voltage (5.5V typ.) is detected, only FAULT outputs “H".
Neither the output nor the operation of the charge pump circuit stops(off).

・When a in-phase high side and the low side input are the “H" levels, all the outputs be made “L" level, and the “H" level is output to FAULT.

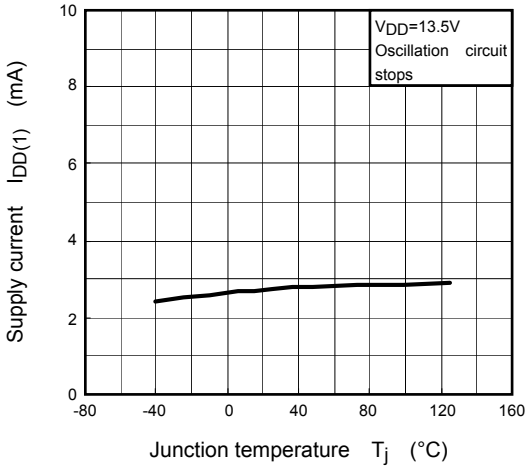
Timing chart



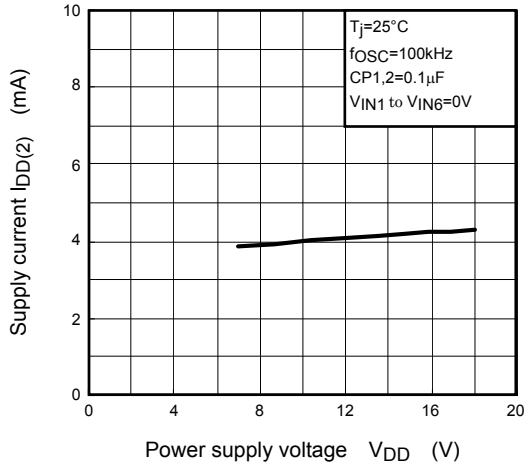
$I_{DD(1)}$ - V_{DD}



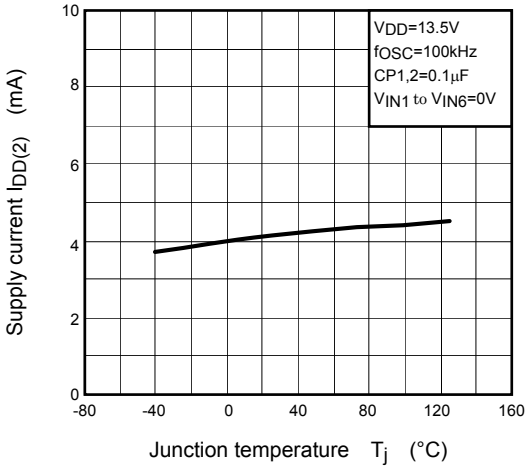
$I_{DD(1)}$ - T_j



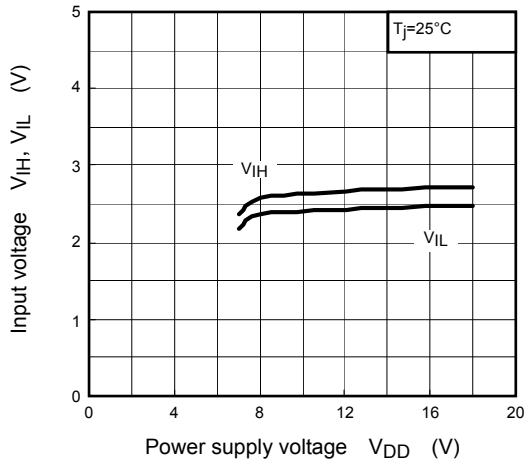
$I_{DD(2)}$ - V_{DD}



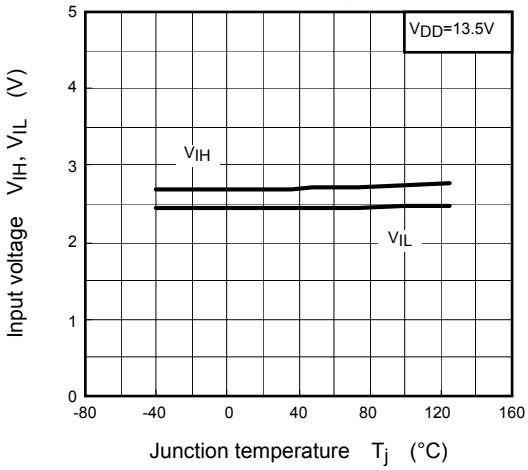
$I_{DD(2)}$ - T_j



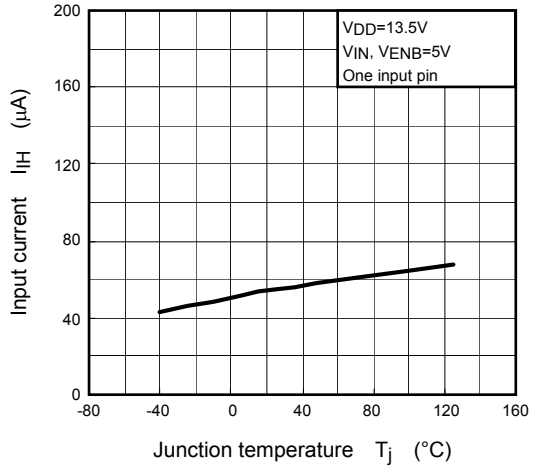
V_{IH}, V_{IL}- V_{DD}



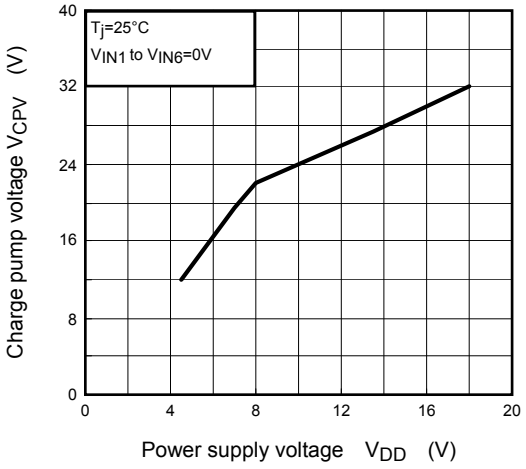
V_{IH}, V_{IL}- T_j



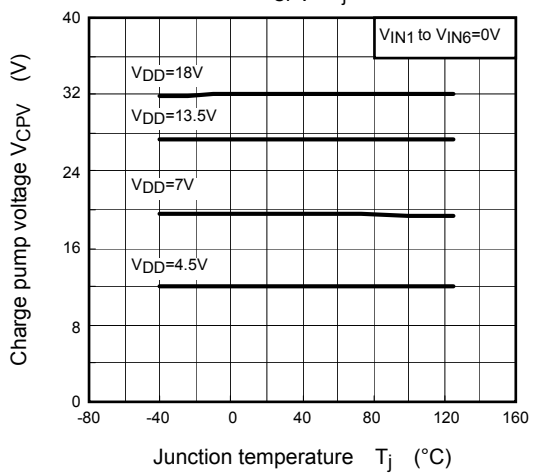
I_{IH} - T_j



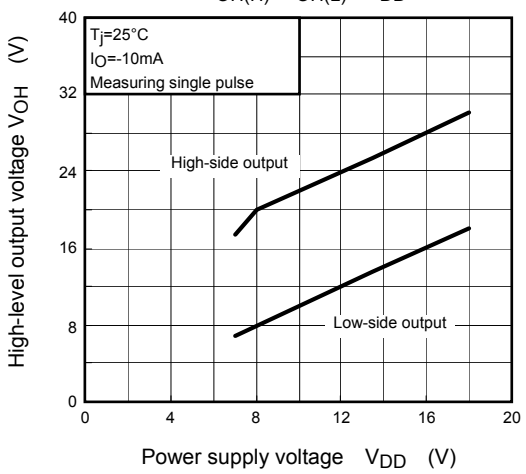
V_{CPV} - V_{DD}



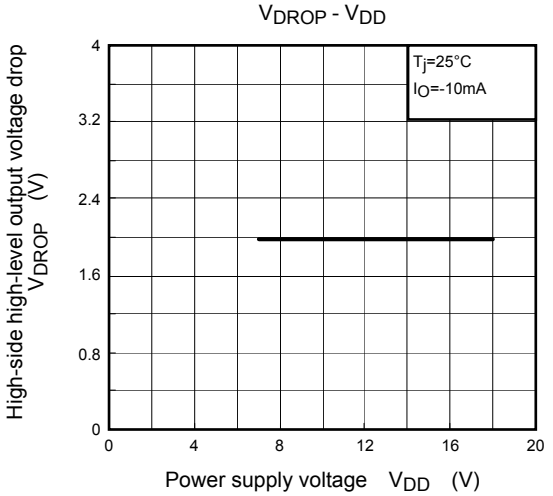
V_{CPV} - T_j



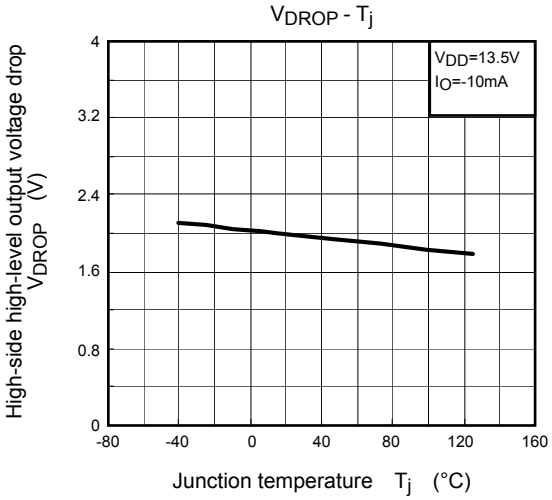
$V_{OH(H)}$, $V_{OH(L)}$ - V_{DD}



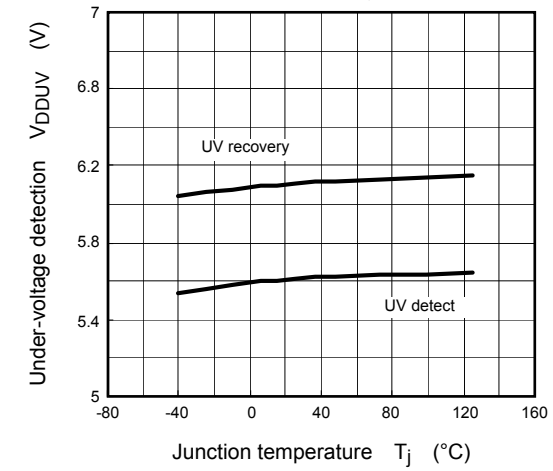
V_{DROP} - V_{DD}



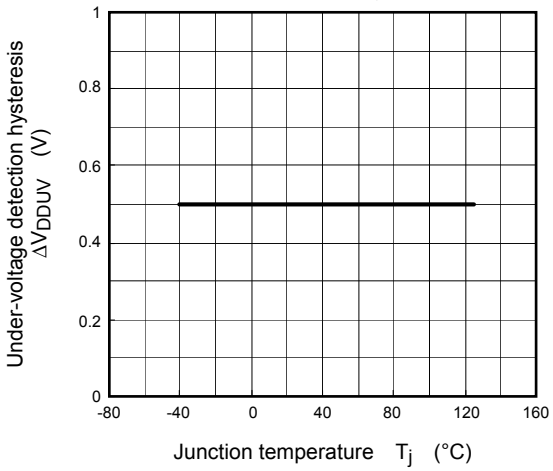
V_{DROP} - T_j



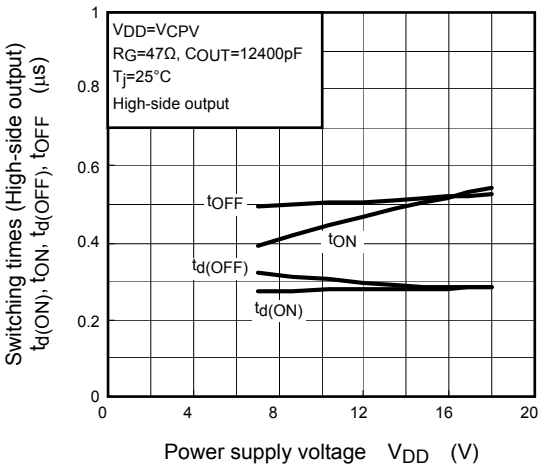
V_{DDUV} - T_j



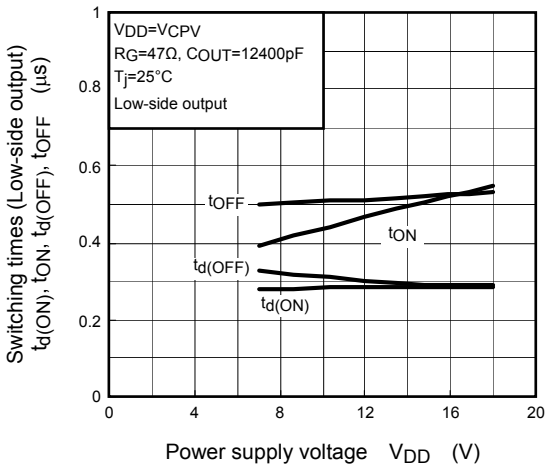
ΔV_{DDUV} - T_j



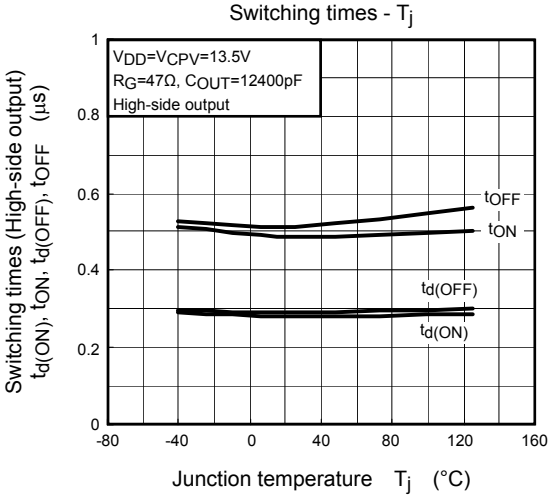
Switching times - V_{DD}



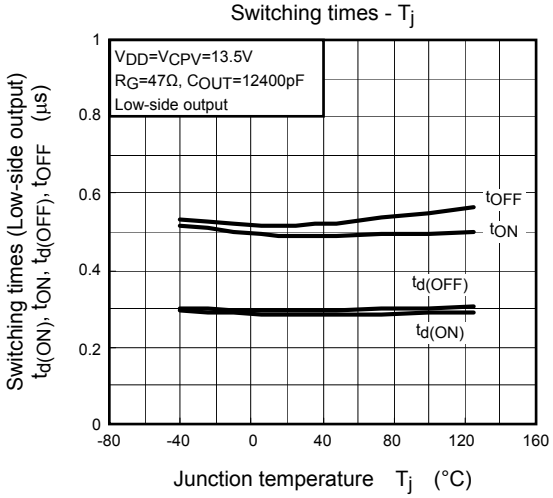
Switching times - V_{DD}



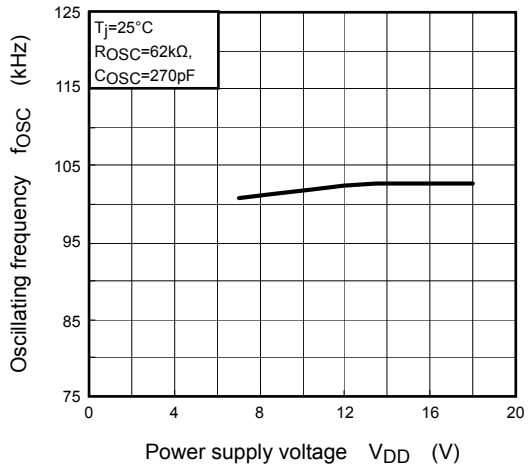
Switching times - T_j



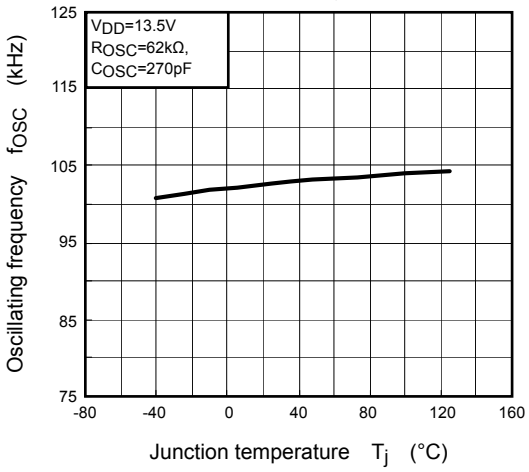
Switching times - T_j



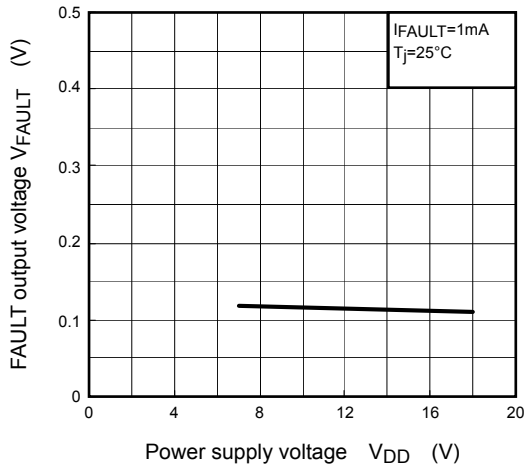
f_{OSC} - V_{DD}



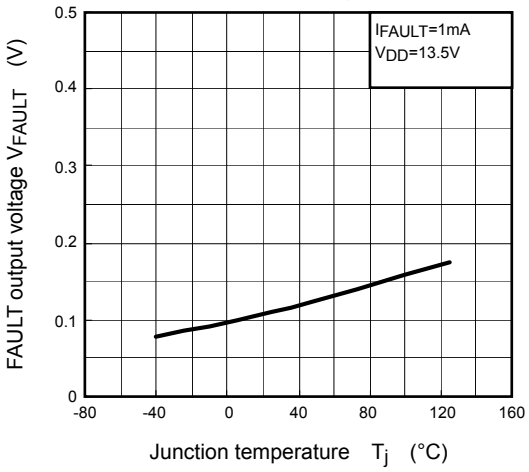
f_{OSC} - T_j



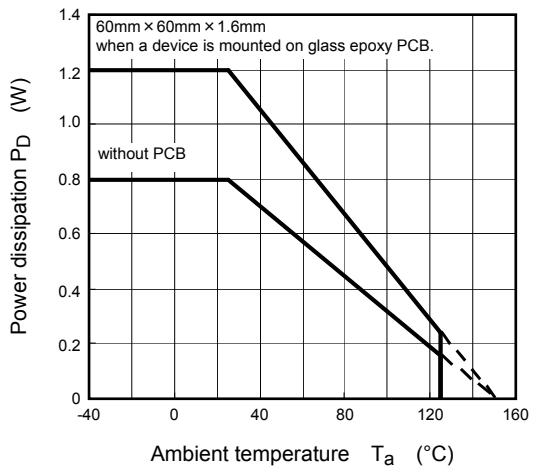
V_{FAULT} - V_{DD}



V_{FAULT} - T_j



P_D - T_a



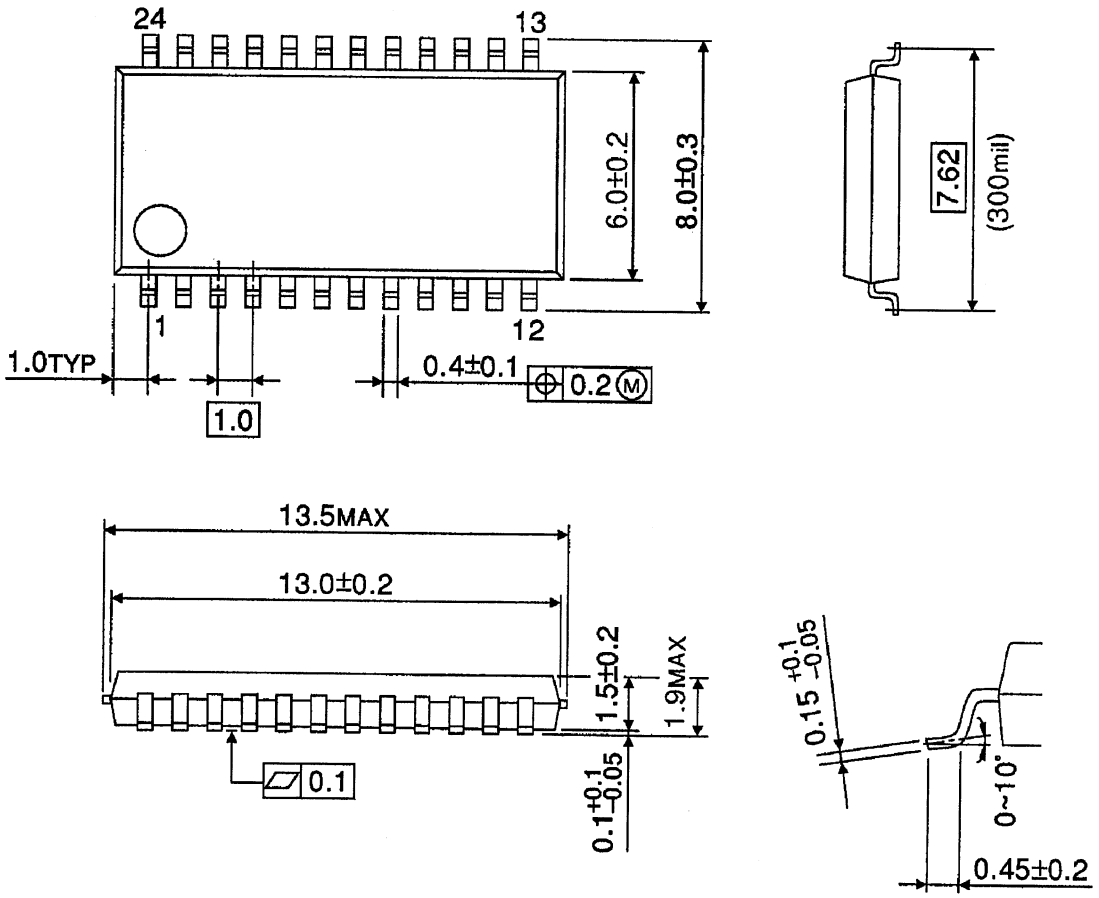
Usage Precautions

Precautions on dry packing

After unpacking dry or moisture-proof packing, make sure the device is mounted in place within 48 hours at a temperature and humidity of 30°C and 60% RH or less. Because the device is emboss-taped and cannot be processed by baking, always be sure to use it within the said allowable time after unpacking.
Standard tape packing quantity: 2000 devices / reel (EL1).

Package Dimensions

SSOP24-P-300-1.00C Unit: mm



Weight: 0.29 g (typ.)

RESTRICTIONS ON PRODUCT USE

20070701-EN GENERAL

- The information contained herein is subject to change without notice.
- TOSHIBA is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such TOSHIBA products could cause loss of human life, bodily injury or damage to property.
  In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent TOSHIBA products specifications. Also, please keep in mind the precautions and conditions set forth in the “Handling Guide for Semiconductor Devices,” or “TOSHIBA Semiconductor Reliability Handbook” etc.
- The TOSHIBA products listed in this document are intended for usage in general electronics applications (computer, personal equipment, office equipment, measuring equipment, industrial robotics, domestic appliances, etc.).These TOSHIBA products are neither intended nor warranted for usage in equipment that requires extraordinarily high quality and/or reliability or a malfunction or failure of which may cause loss of human life or bodily injury (“Unintended Usage”). Unintended Usage include atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, medical instruments, all types of safety devices, etc.. Unintended Usage of TOSHIBA products listed in his document shall be made at the customer’s own risk.
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