# 74LVC244A

# Low-Voltage CMOS Octal Buffer

## With 5 V−Tolerant Inputs and Outputs (3−State, Non−Inverting)

The 74LVC244A is a high performance, non−inverting octal buffer operating from a 1.2 to 3.6 V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A $V_I$ specification of 5.5 V allows 74LVC244A inputs to be safely driven from 5 V devices. The 74LVC244A is suitable for memory address driving and all TTL level bus oriented transceiver applications.

Current drive capability is 24 mA at the outputs. The Output Enable ($\overline{OE}$) input, when HIGH, disables the output by placing them in a HIGH Z condition.

### Features

- Designed for 1.2 V to 3.6 V $V_{CC}$ Operation
- 5 V Tolerant − Interface Capability With 5 V TTL Logic
- Supports Live Insertion and Withdrawal
- $I_{OFF}$ Specification Guarantees High Impedance When $V_{CC}$ = 0 V
- 24 mA Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (10 μA) Substantially Reduces System Power Requirements
- ESD Performance:
  - Human Body Model >2000 V
  - Machine Model >200 V
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

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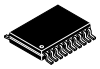
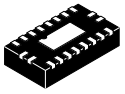
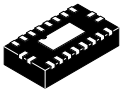


**TSSOP−20**
**DT SUFFIX**
**CASE 948E**

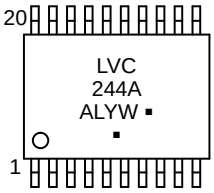


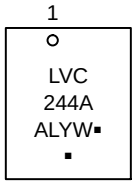
**QFN20**
**MN SUFFIX**
**CASE 485AA**



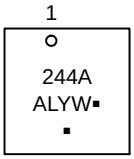
**QFN20**
**MN SUFFIX**
**CASE 485CB**

### MARKING DIAGRAMS




**QFN20 − 485AA**




**QFN20 − 485CB**

| | |
|---|---|
| A | = Assembly Location |
| L | = Wafer Lot |
| Y | = Year |
| W | = Work Week |
| ▪ | = Pb−Free Package |

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

This document contains information on some products that are still under development. ON Semiconductor reserves the right to change or discontinue these products without notice.

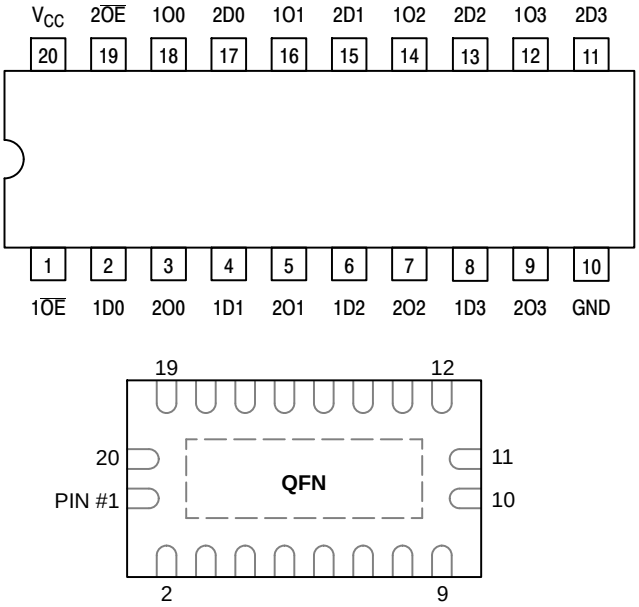



**Figure 1. Pinout: 20−Lead** (Top View)

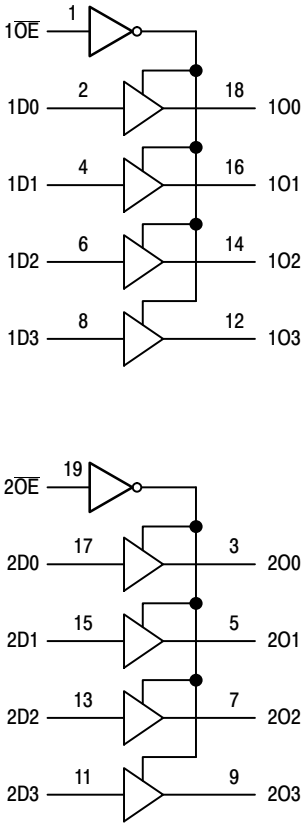



**Figure 2. Logic Diagram**

**PIN NAMES**

| PINS | FUNCTION |
|---|---|
| n$\overline{OE}$ | Output Enable Inputs |
| 1Dn, 2Dn | Data Inputs |
| 1On, 2On | 3−State Outputs |

**TRUTH TABLE**

| INPUTS | | OUTPUTS |
|---|---|---|
| **1$\overline{OE}$<br>2$\overline{OE}$** | **1Dn<br>2Dn** | **1On, 2On** |
| L | L | L |
| L | H | H |
| H | X | Z |

H = High Voltage Level
L = Low Voltage Level
Z = High Impedance State
X = High or Low Voltage Level and Transitions are Acceptable
For $I_{CC}$ reasons, DO NOT FLOAT Inputs

## MAXIMUM RATINGS

| Symbol | Parameter | Condition | Value | Unit |
|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage | | −0.5 to +6.5 | V |
| $V_I$ | DC Input Voltage | | $-0.5 \le V_I \le +6.5$ | V |
| $V_O$ | DC Output Voltage | Output in 3−State | $-0.5 \le V_O \le +6.5$ | V |
| | | Output in HIGH or LOW State (Note 1) | $-0.5 \le V_O \le V_{CC} + 0.5$ | V |
| $I_{IK}$ | DC Input Diode Current | $V_I < GND$ | −50 | mA |
| $I_{OK}$ | DC Output Diode Current | $V_O < GND$ | −50 | mA |
| | | $V_O > V_{CC}$ | +50 | mA |
| $I_O$ | DC Output Source/Sink Current | | ±50 | mA |
| $I_{CC}$ | DC Supply Current Per Supply Pin | | ±100 | mA |
| $I_{GND}$ | DC Ground Current Per Ground Pin | | ±100 | mA |
| $T_{STG}$ | Storage Temperature Range | | −65 to +150 | °C |
| $T_L$ | Lead Temperature, 1 mm from Case for 10 Seconds | | $T_L$ = 260 | °C |
| $T_J$ | Junction Temperature Under Bias | | $T_J$ = 135 | °C |
| $\theta_{JA}$ | Thermal Resistance (Note 2) | | 110.7 | °C/W |
| MSL | Moisture Sensitivity | Level 1 | | |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. $I_O$ absolute maximum rating must be observed.
2. Measured with minimum pad spacing on an FR4 board, using 10 mm−by−1 inch, 2 ounce copper trace no air flow.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage<br>Operating<br>Functional | <br>1.65<br>1.2 | | <br>3.6<br>3.6 | V |
| $V_I$ | Input Voltage | 0 | | 5.5 | V |
| $V_O$ | Output Voltage<br>HIGH or LOW State<br>3−State | <br>0<br>0 | | <br>$V_{CC}$<br>5.5 | V |
| $I_{OH}$ | HIGH Level Output Current<br>$V_{CC}$ = 3.0 V − 3.6 V<br>$V_{CC}$ = 2.7 V − 3.0 V | | | <br>−24<br>−12 | mA |
| $I_{OL}$ | LOW Level Output Current<br>$V_{CC}$ = 3.0 V − 3.6 V<br>$V_{CC}$ = 2.7 V − 3.0 V | | | <br>24<br>12 | mA |
| $T_A$ | Operating Free−Air Temperature | −40 | | +125 | °C |
| $\Delta t/\Delta V$ | Input Transition Rise or Fall Rate<br>$V_{CC}$ = 1.65 V to 2.7 V<br>$V_{CC}$ = 2.7 V to 3.6 V | <br>0<br>0 | | <br>20<br>10 | ns/V |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Conditions | −40°C to +85°C | | | −40°C to +125°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ (Note 3) | Max | Min | Typ (Note 3) | Max | |
| $V_{IH}$ | HIGH−level input voltage | $V_{CC}$ = 1.2 V | 1.08 | − | − | 1.08 | − | − | V |
| | | $V_{CC}$ = 1.65 V to 1.95 V | 0.65 x $V_{CC}$ | − | − | 0.65 x $V_{CC}$ | − | − | |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.7 | − | − | 1.7 | − | − | |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 2.0 | − | − | 2.0 | − | − | |
| $V_{IL}$ | LOW−level input voltage | $V_{CC}$ = 1.2 V | − | − | 0.12 | − | − | 0.12 | V |
| | | $V_{CC}$ = 1.65 V to 1.95 V | − | − | 0.35 x $V_{CC}$ | − | − | 0.35 x $V_{CC}$ | |
| | | $V_{CC}$ = 2.3 V to 2.7 V | − | − | 0.7 | − | − | 0.7 | |
| | | $V_{CC}$ = 2.7 V to 3.6 V | − | − | 0.8 | − | − | 0.8 | |
| $V_{OH}$ | HIGH−level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | | | | V |
| | | $I_O$ = −100 μA; $V_{CC}$ = 1.65 V to 3.6 V | $V_{CC}$ − 0.2 | − | − | $V_{CC}$ − 0.3 | − | − | |
| | | $I_O$ = −4 mA; $V_{CC}$ = 1.65 V | 1.2 | − | − | 1.05 | − | − | |
| | | $I_O$ = −8 mA; $V_{CC}$ = 2.3 V | 1.8 | − | − | 1.65 | − | − | |
| | | $I_O$ = −12 mA; $V_{CC}$ = 2.7 V | 2.2 | − | − | 2.05 | − | − | |
| | | $I_O$ = −18 mA; $V_{CC}$ = 3.0 V | 2.4 | − | − | 2.25 | − | − | |
| | | $I_O$ = −24 mA; $V_{CC}$ = 3.0 V | 2.2 | − | − | 2.0 | − | − | |
| $V_{OL}$ | LOW−level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | | | | V |
| | | $I_O$ = 100 μA; $V_{CC}$ = 1.65 V to 3.6 V | − | − | 0.2 | − | − | 0.3 | |
| | | $I_O$ = 4 mA; $V_{CC}$ = 1.65 V | − | − | 0.45 | − | − | 0.65 | |
| | | $I_O$ = 8 mA; $V_{CC}$ = 2.3 V | − | − | 0.6 | − | − | 0.8 | |
| | | $I_O$ = 12 mA; $V_{CC}$ = 2.7 V | − | − | 0.4 | − | − | 0.6 | |
| | | $I_O$ = 24 mA; $V_{CC}$ = 3.0 V | − | − | 0.55 | − | − | 0.8 | |
| $I_I$ | Input leakage current | $V_I$ = 5.5V or GND $V_{CC}$ = 3.6 V | − | ±0.1 | ±5 | − | ±0.1 | ±20 | μA |
| $I_{OZ}$ | OFF−state output current | VI = VIH or VIL; $V_O$ = 5.5 V or GND; $V_{CC}$ = 3.6 V | − | ±0.1 | ±5 | − | ±0.1 | ±20 | μA |
| $I_{OFF}$ | Power−off leakage current | $V_I$ or $V_O$ = 5.5 V; $V_{CC}$ = 0.0 V | − | ±0.1 | ±10 | − | ±0.1 | ±20 | μA |
| $I_{CC}$ | Supply current | $V_I$ = $V_{CC}$ or GND; $I_O$ = 0 A; $V_{CC}$ = 3.6 V | − | 0.1 | 10 | − | 0.1 | 40 | μA |
| $\Delta I_{CC}$ | Additional supply current | per input pin; $V_I$ = $V_{CC}$ − 0.6 V; $I_O$ = 0 A; $V_{CC}$ = 2.7 V to 3.6 V | − | 5 | 500 | − | 5 | 5000 | μA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. All typical values are measured at $T_A$ = 25°C and $V_{CC}$ = 3.3 V, unless stated otherwise.

**AC ELECTRICAL CHARACTERISTICS** ($t_R = t_F$ = 2.5 ns)

| Symbol | Parameter | Conditions | −40°C to +85°C | | | −40°C to +125°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ[1] | Max | Min | Typ[1] | Max | |
| $t_{pd}$ | Propagation Delay (Note 5) nDn to nOn | $V_{CC}$ = 1.2 V | − | 17.0 | − | − | − | − | ns |
| | | $V_{CC}$ = 1.65 V to 1.95 V | 1.5 | 6.4 | 13.7 | 1.5 | − | 15.8 | |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.0 | 3.4 | 7.1 | 1.0 | − | 8.2 | |
| | | $V_{CC}$ = 2.7 V | 1.5 | 3.4 | 6.9 | 1.5 | − | 9.0 | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 1.5 | 2.9 | 5.9 | 1.5 | − | 7.5 | |
| $t_{en}$ | Enable Time (Note 6) $n\overline{OE}$ to nOn | $V_{CC}$ = 1.2 V | − | 24.0 | − | − | − | − | ns |
| | | $V_{CC}$ = 1.65 V to 1.95 V | 1.5 | 7.0 | 17.3 | 1.5 | − | 20.0 | |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.5 | 3.9 | 9.5 | 1.5 | − | 11.0 | |
| | | $V_{CC}$ = 2.7 V | 1.5 | 4.1 | 8.6 | 1.5 | − | 11.0 | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 1.0 | 3.2 | 7.6 | 1.0 | − | 9.5 | |
| $t_{dis}$ | Disable Time (Note 7) $n\overline{OE}$ to nOn | $V_{CC}$ = 1.2 V | − | 9.0 | − | − | − | − | ns |
| | | $V_{CC}$ = 1.65 V to 1.95 V | 2.2 | 4.5 | 9.8 | 2.2 | − | 11.3 | |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 0.5 | 3.6 | 5.5 | 0.5 | − | 6.4 | |
| | | $V_{CC}$ = 2.7 V | 1.5 | 3.3 | 6.8 | 1.5 | − | 8.5 | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 1.5 | 3.1 | 5.8 | 1.5 | − | 7.5 | |
| $t_{sk(0)}$ | Output Skew Time (Note 8) | | − | − | 1 | − | − | 1.5 | ns |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Typical values are measured at $T_A$ = 25°C and $V_{CC}$ = 3.3 V, unless stated otherwise.
5. $t_{pd}$ is the same as $t_{PLH}$ and $t_{PHL}$.
6. $t_{en}$ is the same as $t_{PZL}$ and $t_{PZH}$.
7. $t_{dis}$ is the same as $t_{PLZ}$ and $t_{PHZ}$.
8. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

**DYNAMIC SWITCHING CHARACTERISTICS**

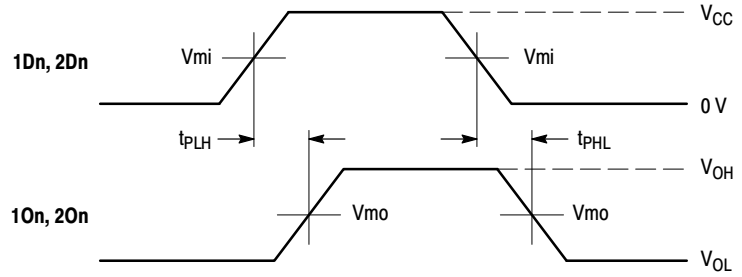
| Symbol | Characteristic | Condition | $T_A$ = +25°C | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $V_{OLP}$ | Dynamic LOW Peak Voltage (Note 9) | $V_{CC}$ = 3.3 V, $C_L$ = 50 pF, $V_{IH}$ = 3.3 V, $V_{IL}$ = 0 V<br>$V_{CC}$ = 2.5 V, $C_L$ = 30 pF, $V_{IH}$ = 2.5 V, $V_{IL}$ = 0 V | | 0.8<br>0.6 | | V |
| $V_{OLV}$ | Dynamic LOW Valley Voltage (Note 9) | $V_{CC}$ = 3.3 V, $C_L$ = 50 pF, $V_{IH}$ = 3.3 V, $V_{IL}$ = 0 V<br>$V_{CC}$ = 2.5 V, $C_L$ = 30 pF, $V_{IH}$ = 2.5 V, $V_{IL}$ = 0 V | | −0.8<br>−0.6 | | V |

9. Number of outputs defined as “n”. Measured with “n−1” outputs switching from HIGH−to−LOW or LOW−to−HIGH. The remaining output is measured in the LOW state.

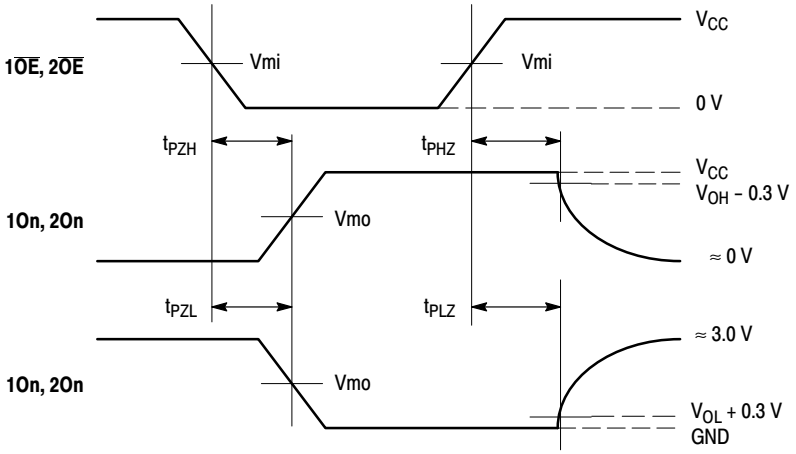
**CAPACITIVE CHARACTERISTICS**

| Symbol | Parameter | Condition | Typical | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{CC}$ = 3.3 V, $V_I$ = 0 V or $V_{CC}$ | 4 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{CC}$ = 3.3 V, $V_I$ = 0 V or $V_{CC}$ | 5 | pF |
| $C_{PD}$ | Power Dissipation Capacitance (Note 10) | Per input; $V_I$ = GND or $V_{CC}$ | | pF |
| | | $V_{CC}$ = 1.65 V to 1.95 V | 6.4 | |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 9.6 | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 12.5 | |

10. $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in μW).
$P_D = C_{PD} \times V_{CC}^2 \times fi \times N + \Sigma (C_L \times V_{CC}^2 \times fo)$ where:
fi = input frequency in MHz; fo = output frequency in MHz
$C_L$ = output load capacitance in pF $V_{CC}$ = supply voltage in Volts
N = number of outputs switching
$\Sigma(C_L \times V_{CC}^2 \times fo)$ = sum of the outputs.



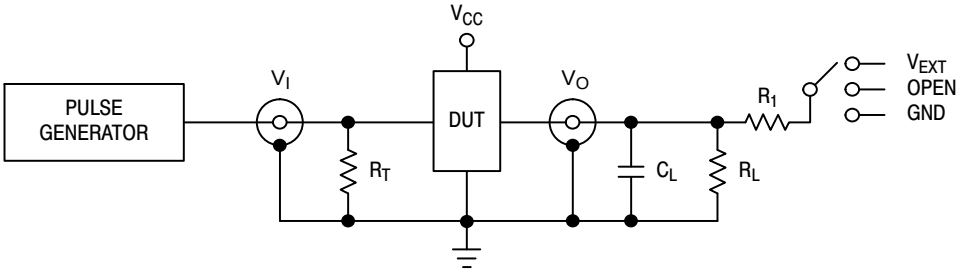

**WAVEFORM 1 − PROPAGATION DELAYS**
$t_R = t_F$ = 2.5 ns, 10% to 90%; f = 1 MHz; $t_W$ = 500 ns




**WAVEFORM 2 − OUTPUT ENABLE AND DISABLE TIMES**
$t_R = t_F$ = 2.5 ns, 10% to 90%; f = 1 MHz; $t_W$ = 500 ns

**Figure 3. AC Waveforms**

| | $V_{CC}$ | | |
|---|---|---|---|
| **Symbol** | **3.3 V ± 0.3 V** | **2.7 V** | **$V_{CC}$ < 2.7 V** |
| Vmi | 1.5 V | 1.5 V | $V_{CC}/2$ |
| Vmo | 1.5 V | 1.5 V | $V_{CC}/2$ |
| $V_{HZ}$ | $V_{OL}$ + 0.3 V | $V_{OL}$ + 0.3 V | $V_{OL}$ + 0.15 V |
| $V_{LZ}$ | $V_{OH}$ − 0.3 V | $V_{OH}$ − 0.3 V | $V_{OH}$ − 015 V |




$C_L$ includes jig and probe capacitance
$R_T = Z_{OUT}$ of pulse generator (typically 50 Ω)
$R_1 = R_L$

| Supply Voltage | Input | | Load | | $V_{EXT}$ | | |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ (V) | $V_I$ | $t_r$, $t_f$ | $C_L$ | $R_L$ | $t_{PLH}$, $t_{PHL}$ | $t_{PLZ}$, $t_{PZL}$ | $t_{PHZ}$, $t_{PZH}$ |
| 1.2 | $V_{CC}$ | ≤ 2 ns | 30 pF | 1 kΩ | Open | 2 x $V_{CC}$ | GND |
| 1.65 − 1.95 | $V_{CC}$ | ≤ 2 ns | 30 pF | 1 kΩ | Open | 2 x $V_{CC}$ | GND |
| 2.3 − 2.7 | $V_{CC}$ | ≤ 2 ns | 30 pF | 500 Ω | Open | 2 x $V_{CC}$ | GND |
| 2.7 | 2.7 V | ≤ 2.5 ns | 50 pF | 500 Ω | Open | 2 x $V_{CC}$ | GND |
| 3 − 3.6 | 2.7 V | ≤ 2.5 ns | 50 pF | 500 Ω | Open | 2 x $V_{CC}$ | GND |

**Figure 4. Test Circuit**

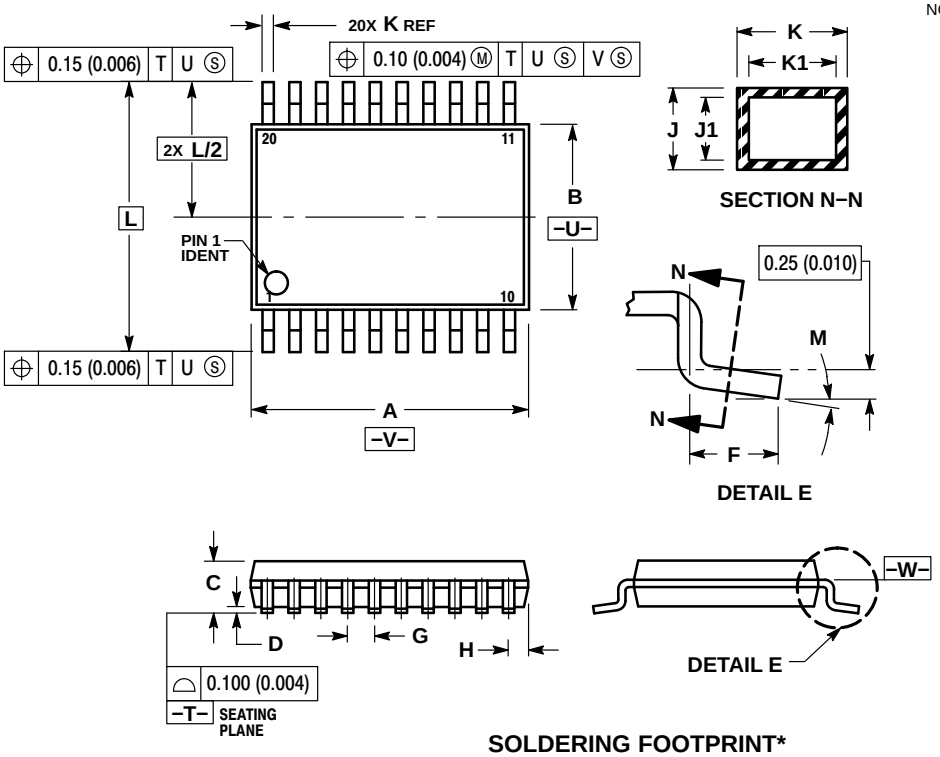
## ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| 74LVC244ADTR2G | TSSOP−20 (Pb−Free) | 2500 / Tape & Reel |
| 74LVC244AMN2TWG (In Development) | QFN20, 2.5x3.5 (Pb−Free) | 3000 / Tape & Reel |
| 74LVC244AMNTWG (In Development) | QFN20, 2.5x4.5 (Pb−Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## PACKAGE DIMENSIONS

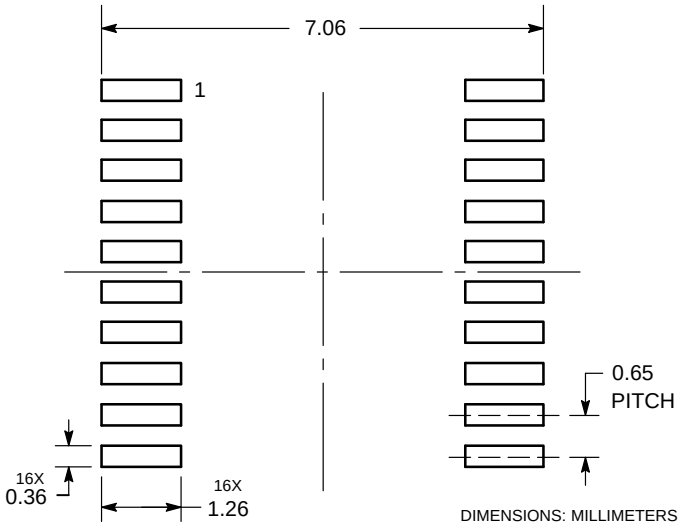
**TSSOP−20**
CASE 948E−02
ISSUE C




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 6.40 | 6.60 | 0.252 | 0.260 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.27 | 0.37 | 0.011 | 0.015 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

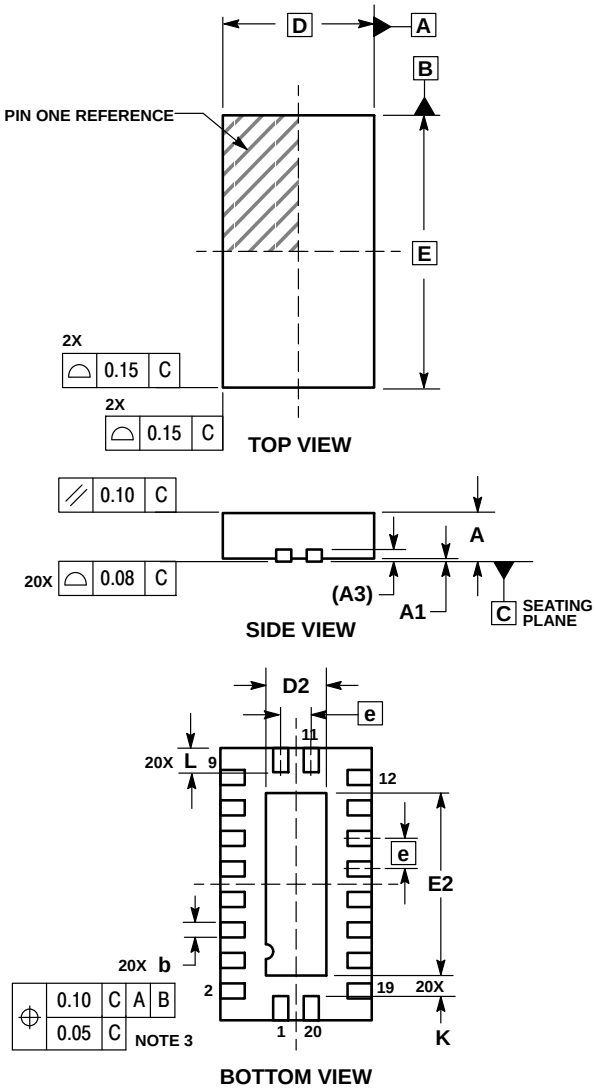
### SOLDERING FOOTPRINT*




*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## PACKAGE DIMENSIONS

**QFN20, 2.5x4.5 MM**
CASE 485AA
ISSUE B

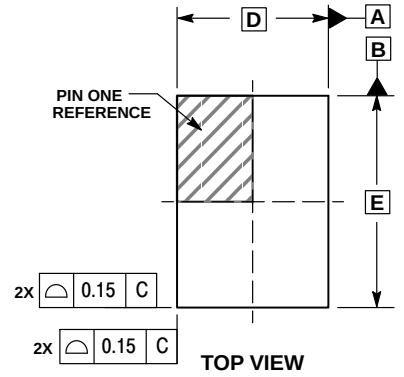



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

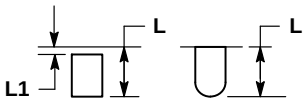
| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 REF | |
| b | 0.20 | 0.30 |
| D | 2.50 BSC | |
| D2 | 0.85 | 1.15 |
| E | 4.50 BSC | |
| E2 | 2.85 | 3.15 |
| e | 0.50 BSC | |
| K | 0.20 | --- |
| L | 0.35 | 0.45 |

## PACKAGE DIMENSIONS

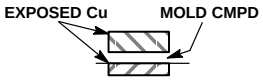
**QFN20, 2.5x3.5, 0.4P**
CASE 485CB
ISSUE O




TOP VIEW



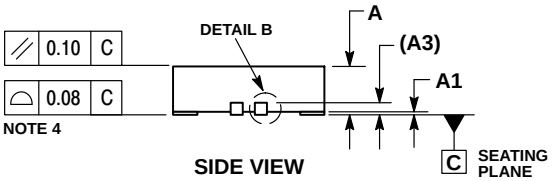

DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS



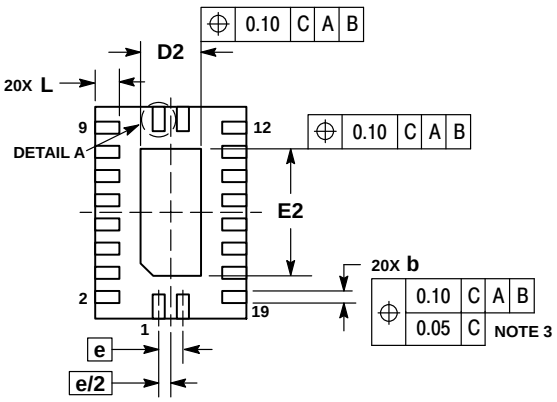

DETAIL B
ALTERNATE CONSTRUCTIONS

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 REF | |
| b | 0.15 | 0.25 |
| D | 2.50 BSC | |
| D2 | 0.90 | 1.10 |
| E | 3.50 BSC | |
| E2 | 2.00 | 2.20 |
| e | 0.40 BSC | |
| L | 0.35 | 0.45 |
| L1 | --- | 0.15 |

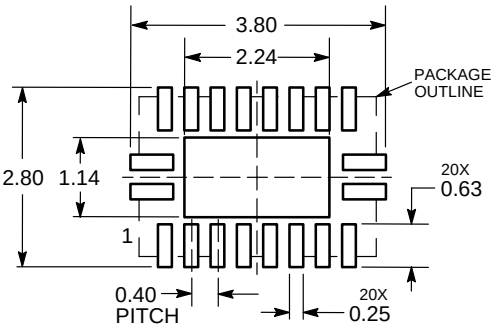



SIDE VIEW




BOTTOM VIEW

SOLDERING FOOTPRINT*




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



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