

Description

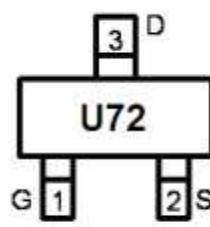
It utilizes the latest processing techniques to achieve the high cell density and reduces the on-resistance with high repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in power switching application and a wide variety of other applications.

Features

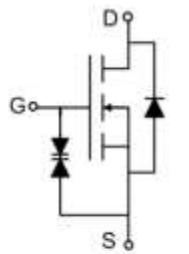
- Advanced MOSFET process technology
- Special designed for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- ESD Rating : 2000V HBM
- 150°C operating temperature



SOT-23



Marking and pin
Assignment



Schematic diagram

Main Product Characteristics

| | |
|--------------|----------|
| V_{DSS} | 60V |
| $R_{DS(on)}$ | 3Ω(max.) |
| I_D | 0.3A |

Absolute Maximum Ratings

| Symbol | Parameter | Max. | Units |
|----------------------------------|---|-------------|-------|
| I_D @ $T_C = 25^\circ\text{C}$ | Continuous Drain Current, $V_{GS} @ 10\text{V}$ ① | 0.3 | A |
| I_{DM} | Pulsed Drain Current② | 1.2 | A |
| P_D @ $T_C = 25^\circ\text{C}$ | Power Dissipation③ | 0.63 | W |
| V_{DS} | Drain-Source Voltage | 60 | V |
| V_{GS} | Gate-to-Source Voltage | ± 20 | V |
| T_J T _{STG} | Operating Junction and Storage Temperature Range | -55 to +150 | °C |

Thermal Characteristics

| Symbol | Symbol | Typ. | Max. | Units |
|---------------|--|------|------|-------|
| θ_{JA} | Junction-to-ambient ($t \leq 10\text{ S}$) ④ | | 200 | °C/W |

Electrical Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

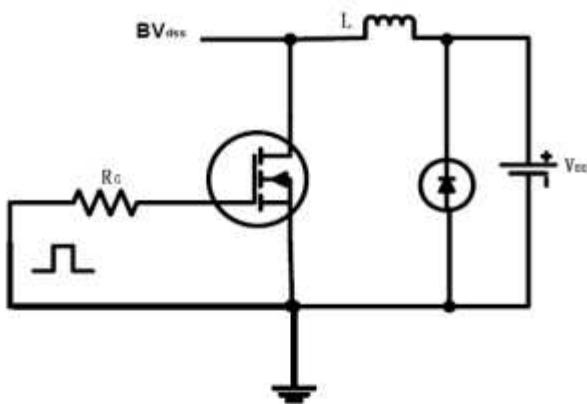
| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|--------------------------------------|---------------------|--|-----|------|-----------|---------------|
| Drain-to-Source breakdown voltage | V(BR)DSS | $V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$ | 60 | | | V |
| Static Drain-to-Source on-resistance | RDS(on) | $V_{GS}=10\text{V}, I_D=0.5\text{A}$ | | 1.6 | 3 | Ω |
| | | $V_{GS}=5\text{V}, I_D=0.05\text{A}$ | | | 3.5 | |
| Gate threshold voltage | $V_{GS(\text{th})}$ | $V_{DS} = V_{GS}, I_D = 250\mu\text{A}$ | 1 | | 2.5 | V |
| Drain-to-Source leakage current | I_{DSS} | $V_{DS} = 60\text{V}, V_{GS} = 0\text{V}$ | | | 1 | μA |
| Gate-to-Source forward leakage | I_{GSS} | $V_{GS}=\pm 5\text{V}, V_{DS}=0\text{V}$ | | | ± 100 | nA |
| | | $V_{GS}=\pm 20\text{V}, V_{DS}=0\text{V}$ | | | ± 10 | μA |
| Turn-on delay time | $t_{d(\text{on})}$ | $V_{GS}=10\text{V}, V_{DS}=30\text{V}, I_D=0.2\text{A}, R_{\text{GEN}}=10\Omega$ | | | 25 | ns |
| Turn-Off delay time | $t_{d(\text{off})}$ | | | | 45 | |
| Input capacitance | C_{iss} | $V_{GS} = 0\text{V}$ $V_{DS} = 25\text{V}$ $f = 1\text{MHz}$ | | 40 | | pF |
| Output capacitance | C_{oss} | | | 16.6 | | |
| Reverse transfer capacitance | C_{rss} | | | 9.5 | | |

Source-Drain Ratings and Characteristics

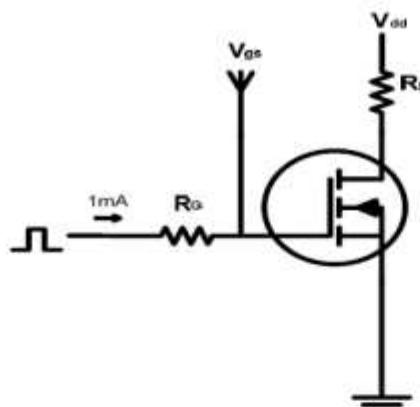
| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|----------|---|-----|-----|-----|------|
| Continuous Source Current (Body Diode) | I_S | MOSFET symbol showing the integral reverse p-n junction diode | | | 0.3 | A |
| Pulsed Source Current (Body Diode) | I_{SM} | | | | 1.2 | A |
| Diode Forward Voltage | V_{SD} | $I_S=0.2\text{A}, V_{GS}=0\text{V}$ | | | 1.3 | V |

Test circuits and Waveforms

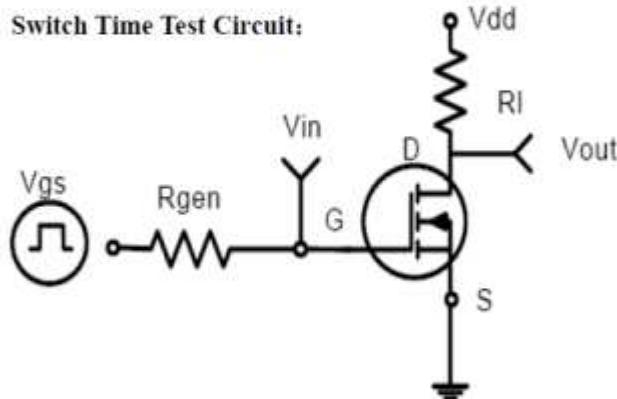
EAS test circuits:



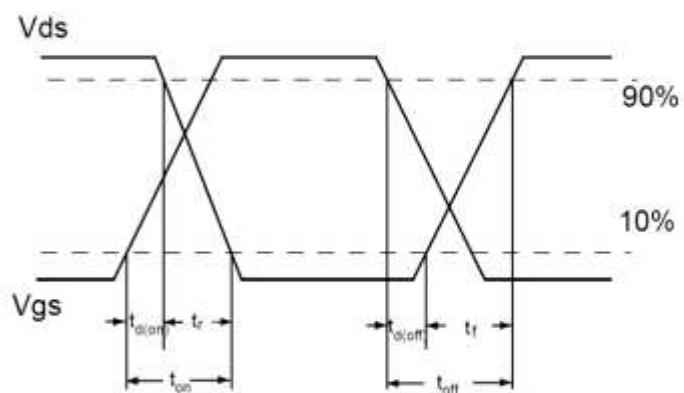
Gate charge test circuit:



Switch Time Test Circuit:



Switch Waveforms:



Notes:

- ① The maximum current rating is limited by bond-wires.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ The power dissipation PD is based on max. junction temperature, using junction-to-case thermal resistance.
- ④ The value of $R_{DS(on)}$ is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with $TA = 25^\circ C$
- ⑤ These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)} = 150^\circ C$.

Typical electrical and thermal characteristics

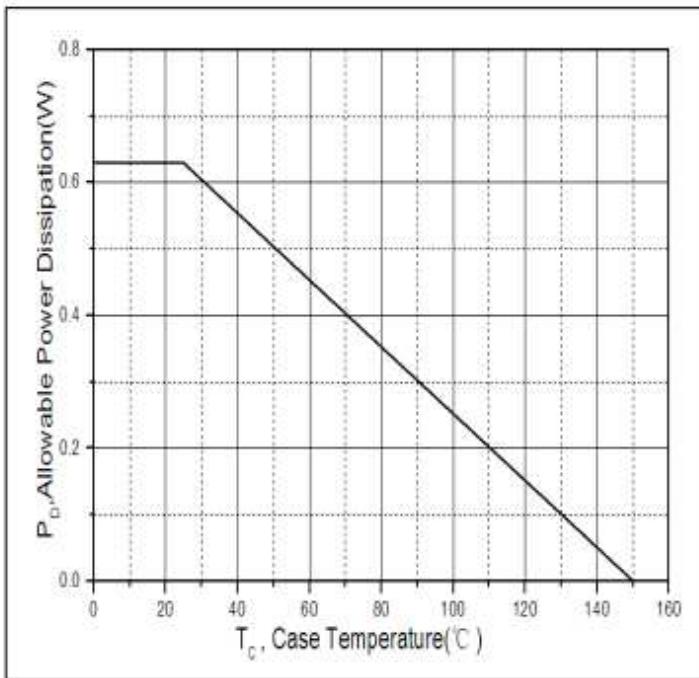


Figure 1. Power Dissipation Vs. Case Temperature

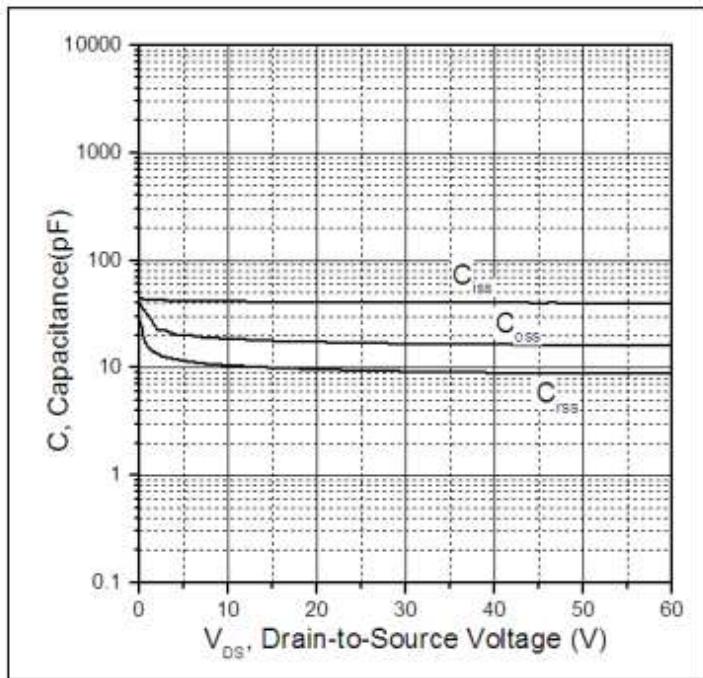


Figure 2.Typical Capacitance Vs. Drain-to-Source Voltage

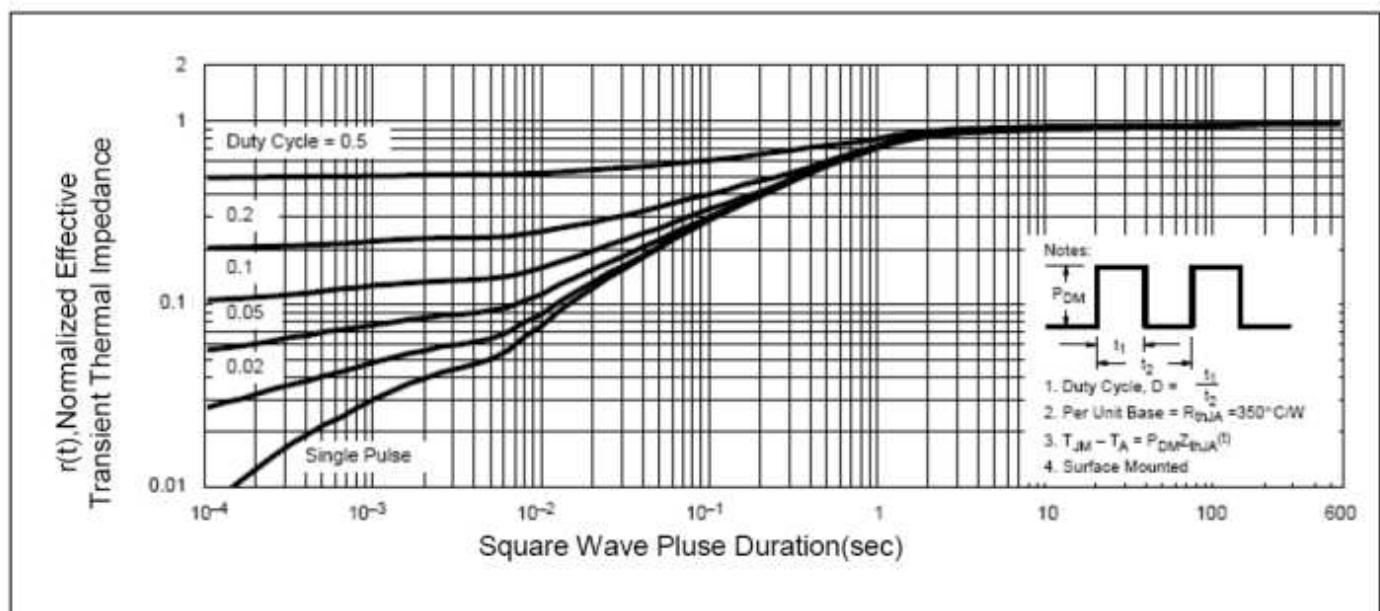


Figure3. Maximum Effective Transient Thermal Impedance, Junction-to-Case



60V、0.3A N-Channel MOSFET

EC732N7002KU

Ordering and Marking Information

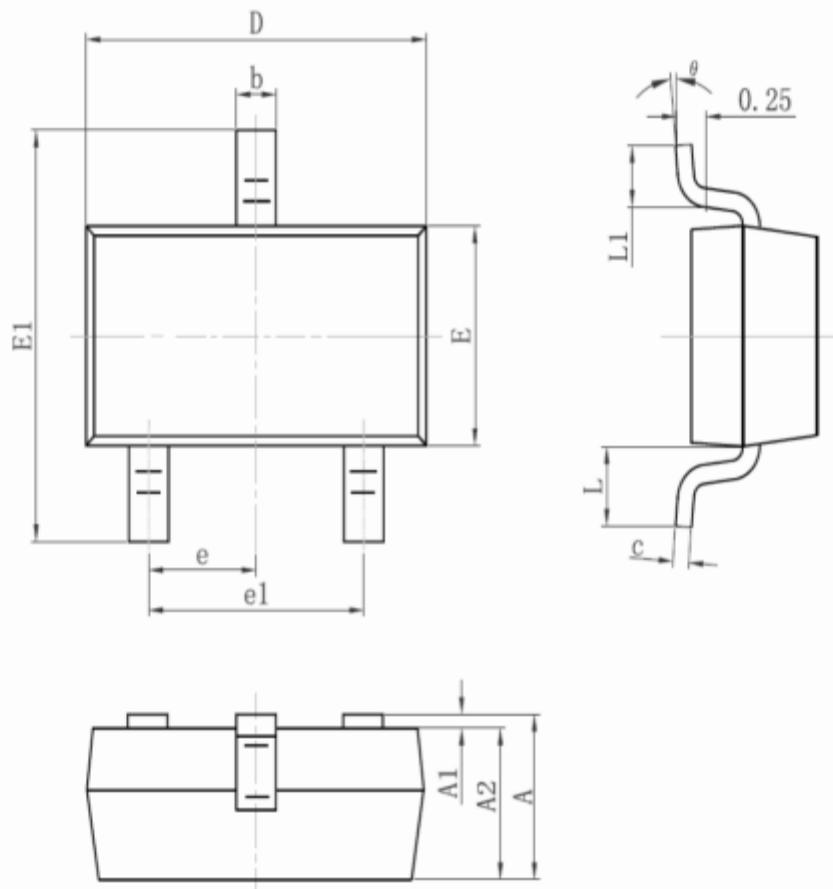
EC732N7002KU XX X

B1:SOT23-3L

R : Tape & Reel

| Part Number | Package | Marking |
|-----------------|----------|---------|
| EC732N7002KUB1R | SOT23-3L | U72 |

SOT23 Package Outline Dimension



| Symbol | Dimension In Millimeters | | Dimension In Inches | |
|--------|--------------------------|-------|---------------------|-------|
| | Min | Max | Min | Max |
| A | 0.900 | 1.150 | 0.035 | 0.045 |
| A1 | 0.000 | 0.100 | 0.000 | 0.004 |
| A2 | 0.900 | 1.050 | 0.035 | 0.041 |
| b | 0.300 | 0.500 | 0.012 | 0.020 |
| c | 0.080 | 0.150 | 0.003 | 0.006 |
| D | 2.800 | 3.000 | 0.110 | 0.118 |
| E | 1.200 | 1.400 | 0.047 | 0.055 |
| E1 | 2.250 | 2.550 | 0.089 | 0.100 |
| e | 0.95TYP | | 0.037TYP | |
| e1 | 1.800 | 2.000 | 0.071 | 0.079 |
| L | 0.55REF | | 0.022REF | |
| L1 | 0.300 | 0.500 | 0.012 | 0.020 |
| θ | 0° | 8° | 0° | 8° |