CMOS 16-Bit Microcontrollers

TMP91CW12F

1. Outline and Features

TMP91CW12 is a high-speed 16-bit microcontroller designed for the control of various mid- to large-scale equipment.
TMP91CW12 comes in a 100-pin flat package.
Listed below are the features.

(1) High-speed 16-bit CPU (900/L1 CPU)
- Instruction mnemonics are upward-compatible with TLCS-90/900
- 16 Mbytes of linear address space
- General-purpose registers and register banks
- 16-bit multiplication and division instructions; bit transfer and arithmetic instructions
- Micro DMA : Four-channels (1.0μs/2 bytes at 16MHz)

(2) Minimum instruction execution time : 250ns (at 16MHz)

(3) Built-in RAM : 4 Kbytes
Built-in ROM : 128 Kbytes

(4) External memory expansion
- Expandable up to 16 Mbytes (shared program/data area)
- Can simultaneously support 8-/16-bit width external data bus
  ··· Dynamic data bus sizing

(5) 8-bit timers: 8 channels

(6) 16-bit timer/event counter : 2 channels

(7) General-purpose serial interface : 2 channels

(8) Serial Bus Interface : 1 channel

(9) 10-bit AD converter : 8 channels

(10) Watchdog timer

(11) Timer for real-time clock (RTC)

(12) Chip select/wait controller : 4 blocks

(13) Interrupts : 45 interrupts
- 9 CPU interrupts : Software interrupt instruction and illegal instruction
- 26 internal interrupts :] Seven selectable priority levels
- 10 external interrupts :]

(14) Input/output ports : 81 pins

(15) Standby mode
- Three Halt modes : Programmable-Idle2, Idle1, Stop

(16) Triple clock controller

(17) Operating voltage
- V_{CC} = 2.7 to 5.5V (fc max = 16 MHz)
- V_{CC} = 4.5 to 5.5V (fc max = 25 MHz)

(18) Package
- 100-pin QFP : P-LQFP100-1414-0.50C

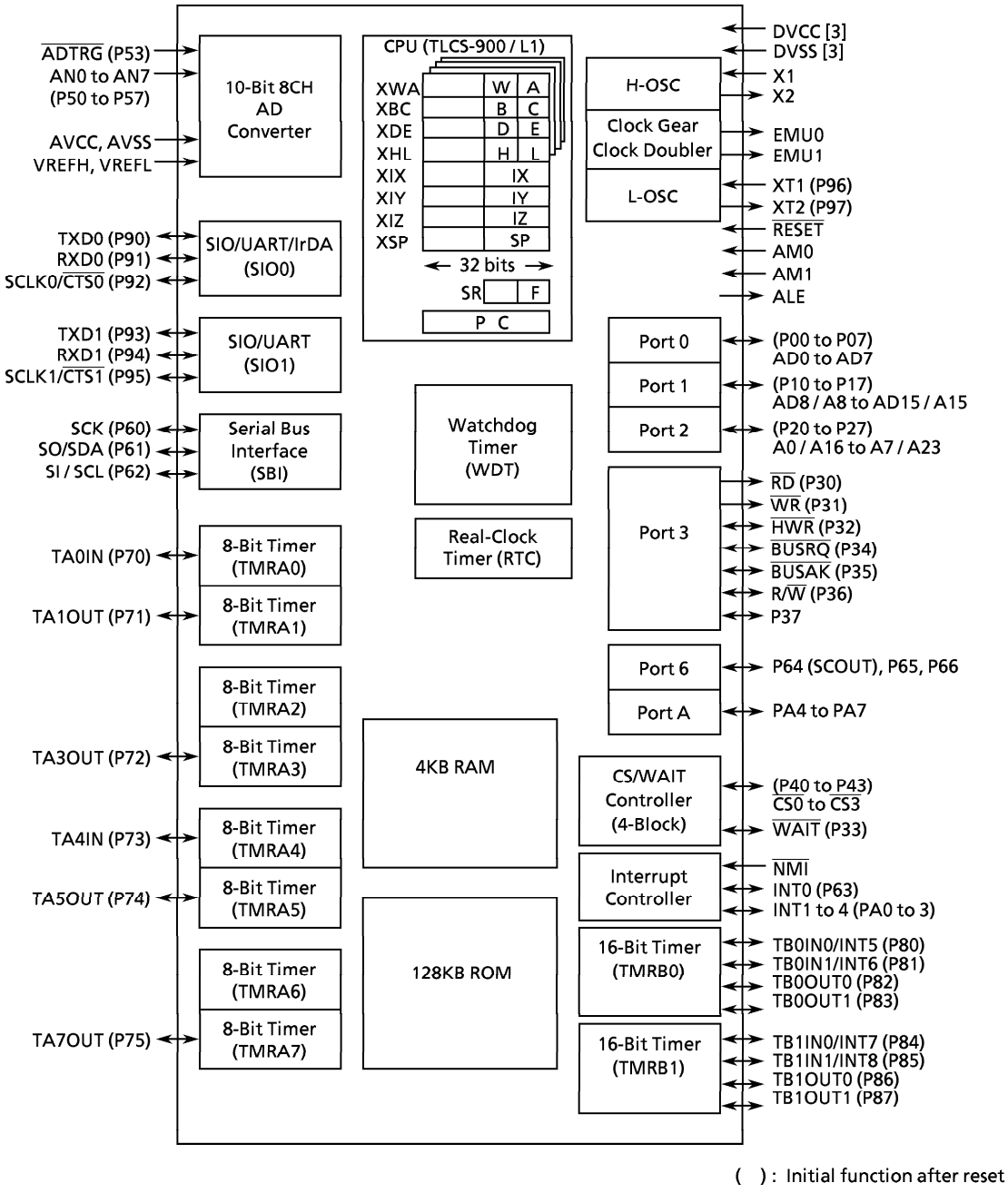


Figure 1.1 TMP91CW12 Block Diagram

2. Pin Assignment and Pin Functions

This section shows the TMP91CW12F pin assignment, and the names and an outline of the functions of the input/output pins.

2.1 Pin Assignment Diagram

Figure 2.1.1 is a pin assignment diagram for TMP91CW12F.

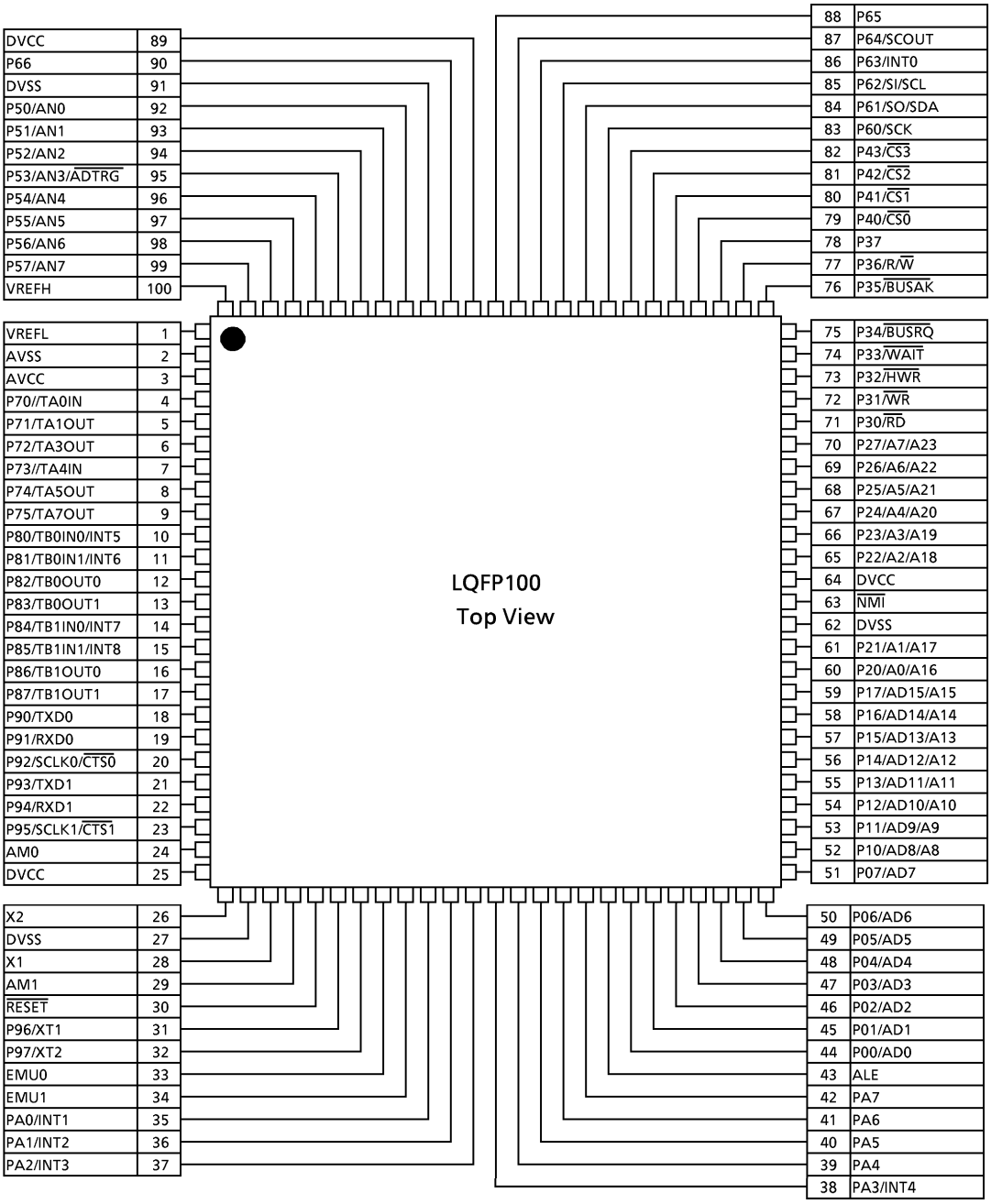


Figure 2.1.1 Pin Assignment Diagram (100-Pin LQFP)

2.2 Pin Names and Functions

The names of the input / output pins and their functions are described below.
Table 2.2.1 Pin Names and Functions.

Table 2.2.1 Pin Names and Functions (1/4)

Pin name	Number of pins	I/O	Functions
P00 to P07 AD0 to AD7	8	I/O Tri-state	Port 0: I/O port that allows I/O to be selected at the bit level Address and data (lower): Bits 0 to 7 for address and data bus
P10 to P17 AD8 to AD15 A8 to A15	8	I/O Tri-state Output	Port 1: I/O port that allows I/O to be selected at the bit level Address and data (upper): Bits 8 to 15 for address and data bus Address: Bits 8 to 15 for address bus
P20 to P27 A0 to A7 A16 to A23	8	I/O Output Output	Port 2: I/O port that allows to be selected at the bit level Address: Bits 0 to 7 for address bus Address: Bits 16 to 23 for address bus
P30 $\overline{RD}$	1	Output Output	Port 30: Output port Read: Strobe signal for reading external memory
P31 $\overline{WR}$	1	Output Output	Port 31: Output port Write: Strobe signal for writing data on pins AD0 to 7
P32 $\overline{HWR}$	1	I/O Output	Port 32: I/O port (with pull-up resistor) High write: Strobe signal for writing data on pins AD8 to 15
P33 $\overline{WAIT}$	1	I/O Input	Port 33: I/O port (with pull-up resistor) Wait: Pin used to request CPU bus wait
P34 $\overline{BUSRQ}$	1	I/O Input	Port 34: I/O port (with pull-up resistor) Bus request: Signal used to request bus release.
P35 $\overline{BUSAK}$	1	I/O Output	Port 35: I/O port (with pull-up resistor) Bus acknowledge: Signal used to acknowledge bus release.
P36 R/$\overline{W}$	1	I/O Output	Port 36: I/O port (with pull-up resistor) Read/write: 1 represents read or dummy cycle; 0 represents write cycle.
P37	1	I/O	Port 37: I/O port (with pull-up resistor)
P40 $\overline{CS0}$	1	I/O Output	Port 40: I/O port (with pull-up resistor) Chip select 0: Outputs 0 when address is within specified address area.
P41 $\overline{CS1}$	1	I/O Output	Port 41: I/O port (with pull-up resistor) Chip select 1: Outputs 0 if address is within specified address area.
P42 $\overline{CS2}$	1	I/O Output	Port 42: I/O port (with pull-up resistor) Chip select 2: Outputs 0 if address is within specified address area.
P43 $\overline{CS3}$	1	I/O Output	Port 43: I/O port (with pull-up resistor) Chip select 3: Outputs 0 if address is within specified address area.
P50 to P57 AN0 to AN7 $\overline{ADTRG}$	8	Input Input Input	Port 5: Pin used to input port Analog input: Pin used to input to AD converter AD trigger: Signal used to request AD start.

Note : This device's built-in memory or built-in I/O cannot be accessed by an external DMA controller, using the $\overline{BUSRQ}$ and $\overline{BUSAK}$ signals.

Table 2.2.1 Pin Names and Functions (2/4)

Pin name	Number of pins	I/O	Functions
P60 SCK	1	I/O I/O	Port 60: I/O Port Serial Bus Interface Clock at SIO mode.
P61 SO SDA	1	I/O Output I/O	Port 61: I/O Port Serial Bus Interface Output data at SIO mode. Serial Bus Interface Data at I^2C bus mode.
P62 SI SCL	1	I/O Input I/O	Port 62: I/O Port Serial Bus Interface Input data at SIO mode. Serial Bus Interface Clock at I^2C bus mode.
P63 INT0	1	I/O Input	Port 63: I/O Port Interrupt request pin 0: Interrupt request pin with programmable level / rising edge / falling edge
P64 SCOUT	1	I/O Output	Port 64: I/O Port System Clock Output: Output f_{FPH} or fs clock
P65	1	I/O	Port 65: I/O Port
P66	1	I/O	Port 66: I/O Port
P70 TA0IN	1	I/O Input	Port 70: I/O Port Timer A0 input
P71 TA1OUT	1	I/O Output	Port 71: I/O Port Timer A1 output
P72 TA3OUT	1	I/O Output	Port 72: I/O Port Timer A3 output
P73 TA4IN	1	I/O Input	Port 73: I/O Port Timer A4 input
P74 TA5OUT	1	I/O Output	Port 74: I/O Port Timer A5 output
P75 TA7OUT	1	I/O Output	Port 75: I/O Port Timer A7 output
P80 TB0IN0 INT5	1	I/O Input Input	Port 80: I/O Port Timer B0 input 0 Interrupt request pin 5: Interrupt request pin with programmable rising edge / falling edge
P81 TB0IN1 INT6	1	I/O Input Input	Port 81: I/O Port Timer B0 input 1 Interrupt request pin 6: Interrupt request pin with rising edge
P82 TB0OUT0	1	I/O Output	Port 82: I/O Port Timer B0 output 0
P83 TB0OUT1	1	I/O Output	Port 83: I/O Port Timer B0 output 1

Table 2.2.1 Pin Names and Functions (3/4)

Pin name	Number of pins	I/O	Functions
P84 TB1IN0 INT7	1	I/O Input Input	Port 84: I/O Port Timer B1 input 0 Interrupt request pin 7: Interrupt request pin with programmable rising edge / falling edge
P85 TB1IN1 INT8	1	I/O Input Input	Port 85: I/O Port Timer B1 input 1 Interrupt request pin 8: Interrupt request pin with rising edge
P86 TB1OUT0	1	I/O Output	Port 86: I/O Port Timer B1 output 0
P87 TB1OUT1	1	I/O Output	Port 87: I/O Port Timer B1 output 1
P90 TXD0	1	I/O Output	Port 90: I/O Port Serial send data 0
P91 RXD0	1	I/O Input	Port 91: I/O Port Serial receive data 0
P92 SCLK0 $\overline{CTS0}$	1	I/O I/O Input	Port 92: I/O Port Serial clock I/O 0 Serial data send enable 0 (Clear to Send)
P93 TXD1	1	I/O Output	Port 93: I/O Port Serial send data 1
P94 RXD1	1	I/O Input	Port 94: I/O Port (with pull-up resistor) Serial receive data 1
P95 SCLK1 $\overline{CTS1}$	1	I/O I/O Input	Port 95: I/O Port (with pull-up resistor) Serial clock I/O 1 Serial data send enable 1 (Clear to Send)
P96 XT1	1	I/O Input	Port 96: I/O port (Open Drain Output) Low Frequency Oscillator connecting pin
P97 XT2	1	I/O Output	Port 97: I/O port (Open Drain Output) Low Frequency Oscillator connecting pin
PA0 to PA3 INT1 to INT4	4	I/O Input	Port A0 to A3: I/O Port Interrupt request pin 1 to 4: Interrupt request pin with programmable rising edge / falling edge
PA4 to PA7	4	I/O	Port A4 to A7: I/O Port
ALE	1	Output	Address Latch Enable Can be disabled for reducing noise.
$\overline{NMI}$	1	Input	Non-maskable interrupt request pin: Interrupt request pin with programmable falling edge or both edges.
AM0/AM1	2	Input	Address mode: The Vcc pin should be connected.
EMU0/EMU1	2	Output	Test pin: Open pins.
$\overline{RESET}$	1	Input	Reset: Initializes TMP91CW12. (With pull-up resistor)

Table 2.2.1 Pin Names and Functions (4/4)

Pin name	Number of pins	I/O	Functions
VREFH	1	Input	Pin for reference voltage input to AD converter (H)
VREFL	1	Input	Pin for reference voltage input to AD converter (L)
X1/X2	2	I/O	High Frequency Oscillator connecting pin
AVCC	1		Power supply pin for AD converter
AVSS	1		GND pin for AD converter (0 V)
DVCC	3		Power supply pin (All VCC pins should be connected with the power supply pin.)
DVSS	3		GND pin (0 V) (All VSS pins should be connected with GND (0 V).)

Note : All pins that have built-in pull-up resistors (other than the $\overline{\text{RESET}}$ pin) can be disconnected from the built-in pull-up resistor by software.

3. OPERATION

The following describes block by block the functions and basic operation of TMP91CW12.
Notes and restrictions for each block are outlined in "7, Use Precautions and Restrictions" at the end of this manual.

3.1 CPU

TMP91CW12 incorporates a high-performance 16-bit CPU (900/L1-CPU). For CPU operation, see the "TLCS-900/L1 CPU".
The following describes the unique functions of the CPU used in TMP91CW12; these functions are not covered in the TLCS-900/L1 CPU section.

3.1.1 Reset

When resetting the TMP91CW12 microcontroller, ensure that the power supply voltage is within the operating voltage range, and that the internal high-frequency oscillator has stabilized. Then hold the $\overline{\text{RESET}}$ input to low level for at least 10 system clocks (ten states: 80μs at 4MHz).
When the reset is accepted, the CPU:

- Sets as follows the program counter (PC) in accordance with the reset vector stored at address FFFF00H - FFFF02H:
  PC (7 : 0) ← value at FFFF00H address
  PC (15 : 8) ← value at FFFF01H address
  PC (23 : 16) ← value at FFFF02H address
- Sets the stack pointer (XSP) to 100H.
- Sets bits <IFF2 to 0> of the status register (SR) to 111 (sets the interrupt level mask register to level 7).
- Sets the <MAX> bit of the status register to 1 (MAX mode).
  (Note: As this product does not support a MIN mode, don't write 0 to <MAX>.)
- Clears bits <RFP2 to 0> of the status register to 000 (sets the register bank to 0).

When reset is released, the CPU starts executing instructions in accordance with the program counter settings. CPU internal registers not mentioned above do not change when the reset is released.
When the reset is accepted, the CPU sets internal I/O, ports, and other pins as follows.

- Initializes the internal I/O registers.
- Sets the port pins, including the pins that also act as internal I/O, to general-purpose input or output port mode.
- Sets the ALE pin to High-Z.
  Figure 3.1.1 is a reset timing of the TMP91CW12.

3.2 Memory Map

Figure 3.2.1 is a memory map of the TMP91CW12.

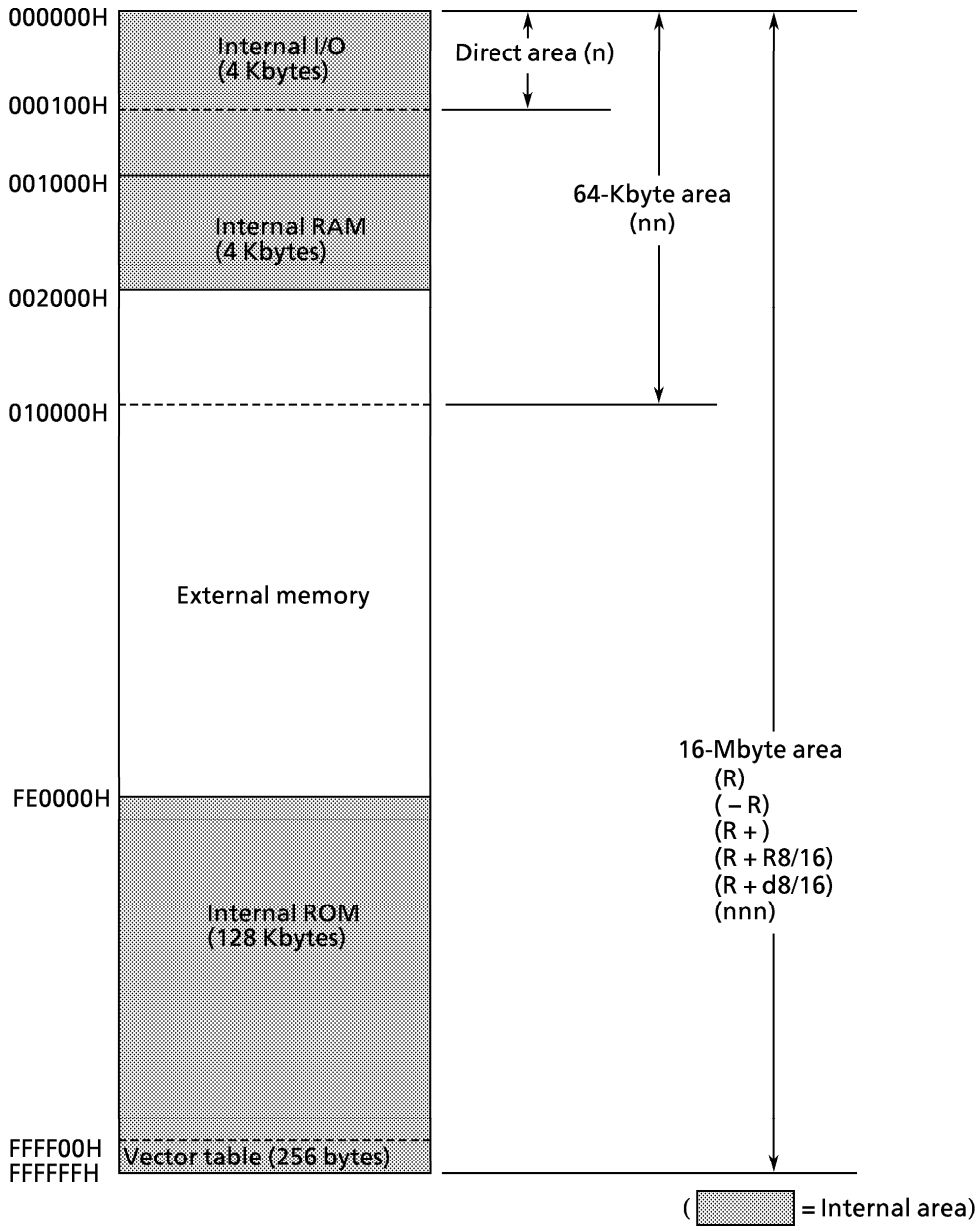


Figure 3.2.1 Memory Map

4. ELECTRICAL CHARACTERISTICS

4.1 Absolute Maximum

Parameter	Symbol	Rating	Unit
Power Supply Voltage	Vcc	– 0.5 to 6.5	V
Input Voltage	V_{IN}	– 0.5 to Vcc + 0.5	V
Output Current	I_{OL}	2	mA
Output Current	I_{OH}	– 2	mA
Output Current (total)	ΣI_{OL}	80	mA
Output Current (total)	ΣI_{OH}	– 80	mA
Power Dissipation (Ta = 85 °C)	P_D	600	mW
Soldering Temperature (10 s)	T_{SOLDER}	260	°C
Storage Temperature	T_{STG}	– 65 to 150	°C
Operating Temperature	T_{OPR}	– 40 to 85	°C

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

4.2 DC Characteristics (1/2)

Parameter		Symbol	Condition	Min	Typ. (Note)	Max	Unit
Power Supply Voltage (AVCC = DVcc) (AVss = DVss = 0 V)		Vcc	fc = 2 to 16 MHz, fs = 30 to 34 kHz	2.7		5.5	V
			fc = 4 to 25 MHz	4.5			
Input Low Voltage	P00 to P17 (AD0 to 15)	V_{IL}	Vcc < 4.5V	– 0.3		0.6	V
			Vcc ≧ 4.5V			0.8	
	P20 to PA7 (except P63)	V_{IL1}	Vcc = 2.7 to 5.5V			0.3Vcc	
	RESET, NMI, P63 (INT0)	V_{IL2}				0.25Vcc	
	AM0, 1	V_{IL3}				0.3	
	X1	V_{IL4}				0.2Vcc	
Input High Voltage	P00 to P17 (AD0 to 15)	V_{IH}	Vcc<4.5V	2.0		Vcc + 0.3	
			Vcc≧4.5V	2.2			
	P20 to PA7 (except P63)	V_{IH1}	Vcc = 2.7 to 5.5V	0.7Vcc			
	RESET, NMI, P63 (INT0)	V_{IH2}		0.75Vcc			
	AM0, 1	V_{IH3}		Vcc – 0.3			
	X1	V_{IH4}		0.8Vcc			
Output Low Voltage		V_{OL}	I_{OL} = 1.6 mA (Vcc = 2.7 to 5.5V)			0.45	V
Output High Voltage		V_{OH}	I_{OH} = – 400 μA (Vcc = 3.0V ± 10%)	2.4			
			I_{OH} = – 400 μA (Vcc = 5.0V ± 10%)	4.2			

Note : Typical values are for Ta = 25 °C and V_{CC} = 3.0 V unless otherwise noted.

4.2 DC Characteristics (2/2)

Parameter	Symbol	Condition		Min	Typ. (Note1)	Max	Unit
Input Leakage Current	I_{LI}	$0.0 \leqq V_{IN} \leqq Vcc$			0.02	± 5	μA
Output Leakage Current	I_{LO}	$0.2 \leqq V_{IN} \leqq Vcc - 0.2$			0.05	± 10	
Power Down Voltage (at STOP, RAM Back up)	V_{STOP}	$V_{IL2} = 0.2$ Vcc, $V_{IH2} = 0.8$ Vcc		2.0		6.0	V
$\overline{RESET}$ Pull Up Resister	R_{RST}	Vcc = 3 V ± 10 %		100		400	kΩ
		Vcc = 5 V ± 10 %		50		230	
Pin Capacitance	C_{IO}	fc = 1 MHz				10	pF
Schmitt Width $\overline{RESET}$, $\overline{NMI}$, INT0	V_{TH}			0.4	1.0		V
Programmable Pull Up Resister	P_{KH}	Vcc = 3 V ± 10 %		100		400	kΩ
		Vcc = 5 V ± 10 %		50		230	
NORMAL (Note2)	Icc	Vcc = 3 V ± 10 % fc = 16 MHz			6.7	10.0	mA
IDLE2					2.4	4.0	
IDLE1					0.8	1.6	
NORMAL (Note2)		Vcc = 5 V ± 10 % fc = 25 MHz (Typ. : Vcc = 5.0 V)			20.5	35.0	mA
IDLE2					8.6	13.0	
IDLE1					3.5	7.0	
SLOW (Note2)		Vcc = 3 V ± 10 % fs = 32.768 kHz			16.0	35.0	μA
IDLE2					5.4	12.0	
IDLE1					3.0	8.0	
STOP		Ta ≦ 50 °C	Vcc = 2.7 to 5.5 V		0.2	10	μA
		Ta ≦ 70 °C				20	
		Ta ≦ 85 °C				50	

Note 1: Typical values are for Ta = 25 °C and V_{CC} = 3.0 V unless otherwise noted.
Note 2: I_{CC} measurement condition (NORMAL, SLOW):
All functions are operational; output pins are open and input pins are fixed.

4.3 AC Characteristics

(1) Vcc = 3.0 V ± 10 %

No.	Symbol	Parameter	Variable		16 MHz		Unit
			Min	Max	Min	Max	
1	t_{FPH}	f_{FPH} Period (= x)	62.5	31250	62.5		ns
2	t_{AL}	A0 to 15 Valid → ALE Fall	0.5x – 26		5		ns
3	t_{LA}	ALE Fall → A0 to 15 Hold	0.5x – 26		5		ns
4	t_{LL}	ALE High Width	x – 52		10		ns
5	t_{LC}	ALE Fall → $\overline{RD}$/$\overline{WR}$ Fall	0.5x – 28		3		ns
6	t_{CLR}	$\overline{RD}$ Rise → ALE Rise	0.5x – 26		5		
7	t_{CLW}	$\overline{WR}$ Rise → ALE Rise	x – 26		36		ns
8	t_{ACL}	A0 to 15 Valid → $\overline{RD}$/$\overline{WR}$ Fall	x – 41		21		ns
9	t_{ACH}	A0 to 23 Valid → $\overline{RD}$/$\overline{WR}$ Fall	1.5x – 50		43		ns
10	t_{CAR}	$\overline{RD}$ Rise→ A0 to 23 Hold	0.5x – 31		0		
11	t_{CAW}	$\overline{WR}$ Rise→ A0 to 23 Hold	x – 31		31		ns
12	t_{ADL}	A0 to 15 Valid→ D0 to 15 Input		3.0x – 87		100	ns
13	t_{ADH}	A0 to 23 Valid→ D0 to 15 Input		3.5x – 98		120	ns
14	t_{RD}	$\overline{RD}$ Fall → D0 to 15 Input		2.0x – 75		50	ns
15	t_{RR}	$\overline{RD}$ Low Width	2.0x – 40		85		ns
16	t_{HR}	$\overline{RD}$ Rise → D0 to 15 Hold	0		0		ns
17	t_{RAE}	$\overline{RD}$ Rise → A0 to 15 Output	x – 25		37		ns
18	t_{WW}	$\overline{WR}$ Low Width	1.5x – 55		39		ns
19	t_{DW}	D0 to 15 Valid → $\overline{WR}$ Rise	1.5x – 78		15		ns
20	t_{WD}	$\overline{WR}$ Rise →D0 to 15 Hold	x – 49		13		ns
21	t_{AWH}	A0 to 23 Valid → $\overline{WAIT}$ Input $\left(\begin{smallmatrix}1WAIT\\+n\ mode\end{smallmatrix}\right)$		3.5x – 118		100	ns
22	t_{AWL}	A0 to 15 Valid → $\overline{WAIT}$ Input $\left(\begin{smallmatrix}1WAIT\\+n\ mode\end{smallmatrix}\right)$		3.0x – 117		70	ns
23	t_{CW}	$\overline{RD}$/$\overline{WR}$ Fall →$\overline{WAIT}$ Hold $\left(\begin{smallmatrix}1WAIT\\+n\ mode\end{smallmatrix}\right)$	2.0x + 0		125		ns
24	t_{APH}	A0 to 23 Valid → PORT Input		3.5x – 168		50	ns
25	t_{APH2}	A0 to 23 Valid → PORT Hold	3.5x		218		ns
26	t_{AP}	A0 to 23 Valid → PORT Valid		3.5x + 100		319	ns

AC Measuring Conditions

- Output Level : High 0.7 Vcc / Low 0.3 Vcc, CL = 50 pF
- Input Level : High 0.9 Vcc / Low 0.1 Vcc

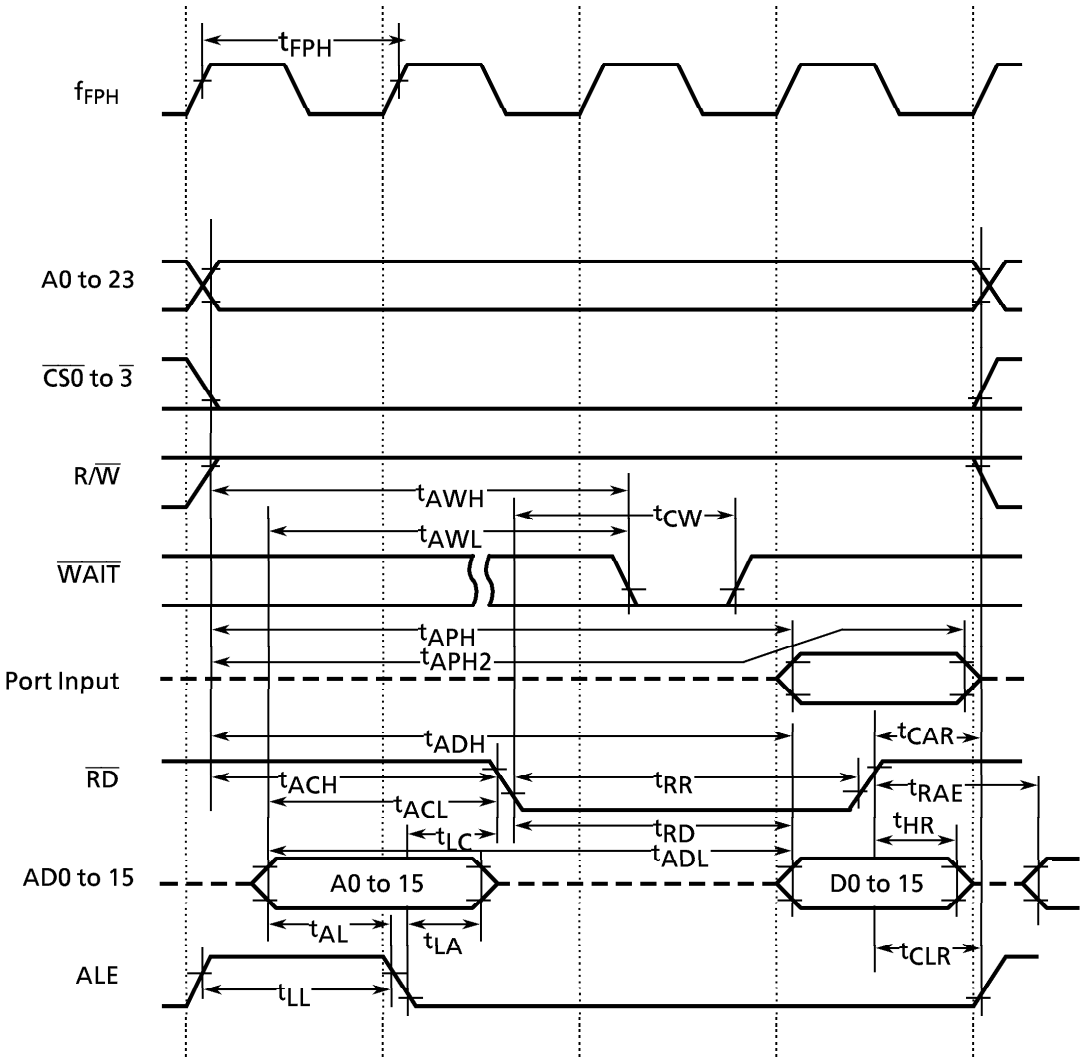
(2) Vcc = 5.0 V ± 10 %

No.	Symbol	Parameter	Variable		25 MHz		Unit
			Min	Max	Min	Max	
1	t_{FPH}	f_{FPH} Period (= x)	40	31250	40		ns
2	t_{AL}	A0 to 15 Valid → ALE Fall	0.5x – 15		5		ns
3	t_{LA}	ALE Fall → A0 to 15 Hold	0.5x – 15		5		ns
4	t_{LL}	ALE High Width	x – 20		20		ns
5	t_{LC}	ALE Fall → $\overline{RD}/\overline{WR}$ Fall	0.5x – 20		0		ns
6	t_{CLR}	$\overline{RD}$ Rise → ALE Rise	0.5x – 15		5		
7	t_{CLW}	$\overline{WR}$ Rise → ALE Rise	x – 15		25		ns
8	t_{ACL}	A0 to 15 Valid → $\overline{RD}/\overline{WR}$ Fall	x – 25		15		ns
9	t_{ACH}	A0 to 23 Valid → $\overline{RD}/\overline{WR}$ Fall	1.5x – 50		10		ns
10	t_{CAR}	$\overline{RD}$ Rise→ A0 to 23 Hold	0.5x – 20		0		
11	t_{CAW}	$\overline{WR}$ Rise→ A0 to 23 Hold	x – 20		20		ns
12	t_{ADL}	A0 to 15 Valid→ D0 to 15 Input		3.0x – 45		75	ns
13	t_{ADH}	A0 to 23 Valid→ D0 to 15 Input		3.5x – 35		105	ns
14	t_{RD}	$\overline{RD}$ Fall → D0 to 15 Input		2.0x – 40		40	ns
15	t_{RR}	$\overline{RD}$ Low Width	2.0x – 20		60		ns
16	t_{HR}	$\overline{RD}$ Rise → D0 to 15 Hold	0		0		ns
17	t_{RAE}	$\overline{RD}$ Rise → A0 to 15 Output	x – 15		25		ns
18	t_{WW}	$\overline{WR}$ Low Width	1.5x – 20		40		ns
19	t_{DW}	D0 to 15 Valid → $\overline{WR}$ Rise	1.5x – 50		10		ns
20	t_{WD}	$\overline{WR}$ Rise →D0 to 15 Hold	x – 15		25		ns
21	t_{AWH}	A0 to 23 Valid → $\overline{WAIT}$ Input $\left(^{1WAIT}_{+n\ mode}\right)$		3.5x – 90		50	ns
22	t_{AWL}	A0 to 15 Valid → $\overline{WAIT}$ Input $\left(^{1WAIT}_{+n\ mode}\right)$		3.0x – 80		40	ns
23	t_{CW}	$\overline{RD}/\overline{WR}$ Fall →$\overline{WAIT}$ Hold $\left(^{1WAIT}_{+n\ mode}\right)$	2.0x + 0		80		ns
24	t_{APH}	A0 to 23 Valid → Port Input		3.5x – 120		20	ns
25	t_{APH2}	A0 to 23 Valid → Port Hold	3.5x		140		ns
26	t_{AP}	A0 to 23 Valid → Port Valid		3.5x + 100		319	ns

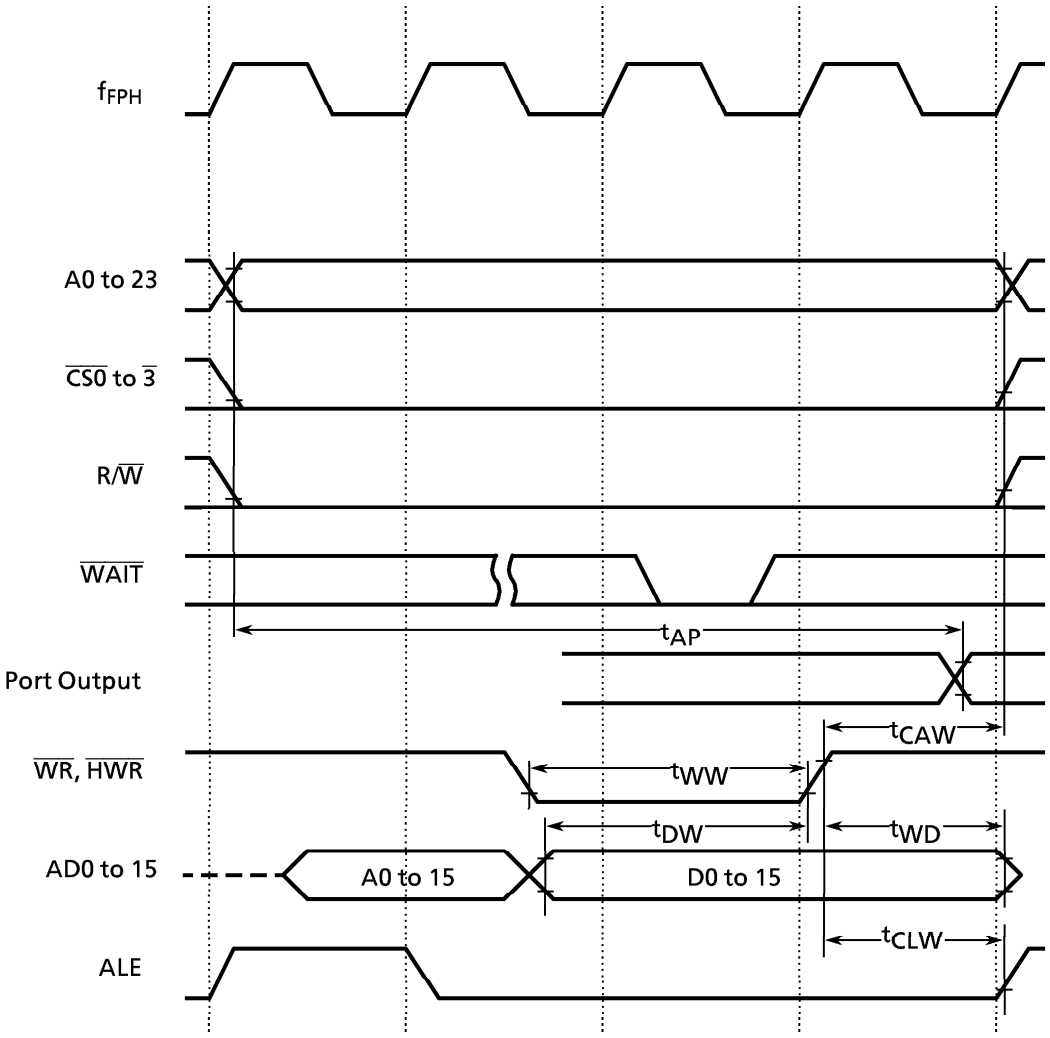
AC Measuring Conditions

- Output Level : High 2.2 V / Low 0.8 V , CL = 50 pF
- Input Level : High 2.4 V / Low 0.45 V (AD0 to AD15)
  High 0.8 Vcc / Low 0.2 Vcc (except AD0 to AD15)

(1) Read Cycle


tFPH
fFPH
A0 to 23
CS0 to 3
R/W
tAWH
tCW
tAWL
WAIT
tAPH
tAPH2
Port Input
tADH
tCAR
RD
tACH
tRR
tRAE
tACL
tHR
tRD
tLC
tADL
AD0 to 15
A0 to 15
D0 to 15
tAL
tLA
tCLR
ALE
tLL

(2) Write Cycle



4.4 AD Conversion Characteristics

$AV_{CC} = V_{CC}$, $AV_{SS} = V_{SS}$

Symbol	Parameter	Condition	Min	Typ.	Max	Unit
VREFH	Analog Reference Voltage (+)	V_{CC} = 3V ± 10 %	V_{CC} – 0.2 V	V_{CC}	V_{CC}	V
		V_{CC} = 5V ± 10 %	V_{CC} – 1.5 V	V_{CC}	V_{CC}	
VREFL	Analog Reference Voltage (–)	V_{CC} = 3V ± 10 %	V_{SS}	V_{SS}	V_{SS} + 0.2 V	
		V_{CC} = 5V ± 10 %	V_{SS}	V_{SS}	V_{SS} + 0.2 V	
VAIN	Analog Input Voltage Range		VREFL		VREFH	
IREF (VREFL = 0 V)	Analog Current for Analog Reference Voltage <VREFON> = 1	V_{CC} = 3V ± 10 %		0.85	1.20	mA
		V_{CC} = 5V ± 10 %		1.44	2.00	
	<VREFON> = 0	V_{CC} = 2.7 to 5.5V		0.02	5.0	μA
–	Error (not including quantizing errors)	V_{CC} = 3V ± 10 %		± 1.0	± 4.0	LSB
		V_{CC} = 5V ± 10 %		± 1.0	± 4.0	

Note 1: 1LSB = (VREFH – VREFL) / 1024 [V]
Note 2: The operation above is guaranteed for $f_{FPH} \geqq 4$ MHz.
Note 3: The value I_{CC} includes the current which flows through the AVCC pin.

4.5 Serial Channel Timing (I/O Internal Mode)

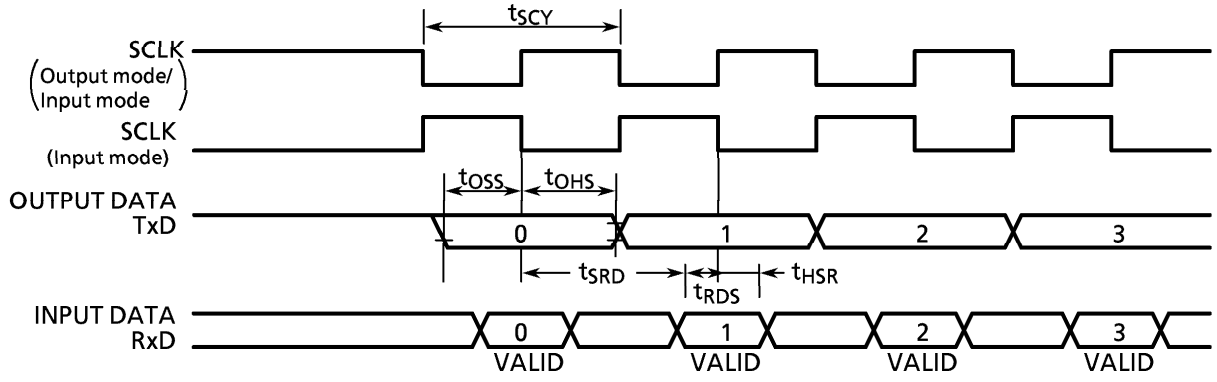
(1) SCLK Input Mode

Symbol	Parameter	Variable		25 MHz		16 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t_{SCY}	SCLK Period	16X		0.64		1.0		μs
t_{OSS}	Output Data → SCLK Rising/Falling Edge *	$t_{SCY}/2 - 4X - 85$ (V_{CC} = 5 V ± 10%)		75		165		ns
		$t_{SCY}/2 - 4X - 130$ (V_{CC} = 3 V ± 10%)		—		120		
t_{OHS}	SCLK Rising/Falling Edge * → Output Data Hold	$t_{SCY}/2 + 2X + 0$		400		625		ns
t_{HSR}	SCLK Rising/Falling Edge * → Input Data Hold	3X + 10		130		198		ns
t_{SRD}	SCLK Rising/Falling Edge * → Valid Data Input		$t_{SCY} - 0$		640		1000	ns
t_{RDS}	Valid Data Input → SCLK Rising/Falling edge	0		0		0		ns

*) SCLK Rising/Falling Edge : The rising edge is used in SCLK rising mode.
The falling edge is used in SCLK falling mode.

(2) SCLK Output Mode

Symbol	Parameter	Variable		25 MHz		16 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t_{SCY}	SCLK Period (Programable)	16X	8192X	0.64	327	1.0	512	μs
t_{OSS}	Output Data → SCLK Rising/Falling Edge	$t_{SCY}/2 - 40$		280		460		ns
t_{OHS}	SCLK Rising/Falling Edge → Output Data Hold	$t_{SCY}/2 - 40$		280		460		ns
t_{HSR}	SCLK Rising/Falling Edge → Input Data Hold	0		0		0		ns
t_{SRD}	SCLK Rising/Falling Edge → Valid Data Input		$t_{SCY} - 1X - 90$		510		847	ns
t_{RDS}	Valid Data Input → SCLK Rising/Falling edge	1X + 90		130		153		ns



4.6 Event Counter (TA0IN, TA4IN, TB0IN0, TB0IN1, TB1IN0, TB1IN1)

Symbol	Parameter	Variable		25 MHz		16 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t_{VCK}	Clock Period	8X + 100		420		600		ns
t_{VCKL}	Clock Low Level width	4X + 40		200		290		ns
t_{VCKH}	Clock High Level width	4X + 40		200		290		ns

4.7 Interrupt, Capture

(1) $\overline{NMI}$, INT0 to 4 Interrupts

Symbol	Parameter	Variable		25 MHz		16 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t_{INTAL}	$\overline{NMI}$, INT0 to 4 Low level width	4X + 40		200		290		ns
t_{INTAH}	$\overline{NMI}$, INT0 to 4 High level width	4X + 40		200		290		ns

(2) INT5 to 8 Interrupt, Capture

The INT5 to 8 input width depends on the system clock select mode, prescaler clock mode.

System Clock selected <SYSCK>	Prescaler Clock selected <PRCK1, 0>	t_{INTBL} (INT5 to 8 Low Level Width)		t_{INTBH} (INT5 to 8 High Level Width)		Unit
		Variable	25 MHz	Variable	25 MHz	
		Min	Min	Min	Min	
0 (fc)	00 (f_{FPH})	8X + 100	420	8X + 100	420	ns
	10 (fc/16)	128Xc + 0.1	5.22	128Xc + 0.1	5.22	μs
1 (fs)	00 (f_{FPH})	8X + 0.1	244.3	8X + 0.1	244.3	

Note : Xc = Period of Clock fc

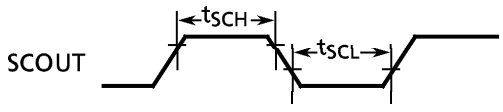
4.8 SCOUT pin AC characteristics

Symbol	Parameter	Variable		25 MHz		16 MHz		Condition	Unit
		Min	Max	Min	Max	Min	Max		
t_{SCH}	Low Level width	0.5T – 20		–		11		V_{CC} = 3 V ± 10%	ns
		0.5T – 15		5		16		V_{CC} = 5 V ± 10%	
t_{SCL}	High level width	0.5T – 20		–		11		V_{CC} = 3 V ± 10%	ns
		0.5T – 15		5		16		V_{CC} = 5 V ± 10%	

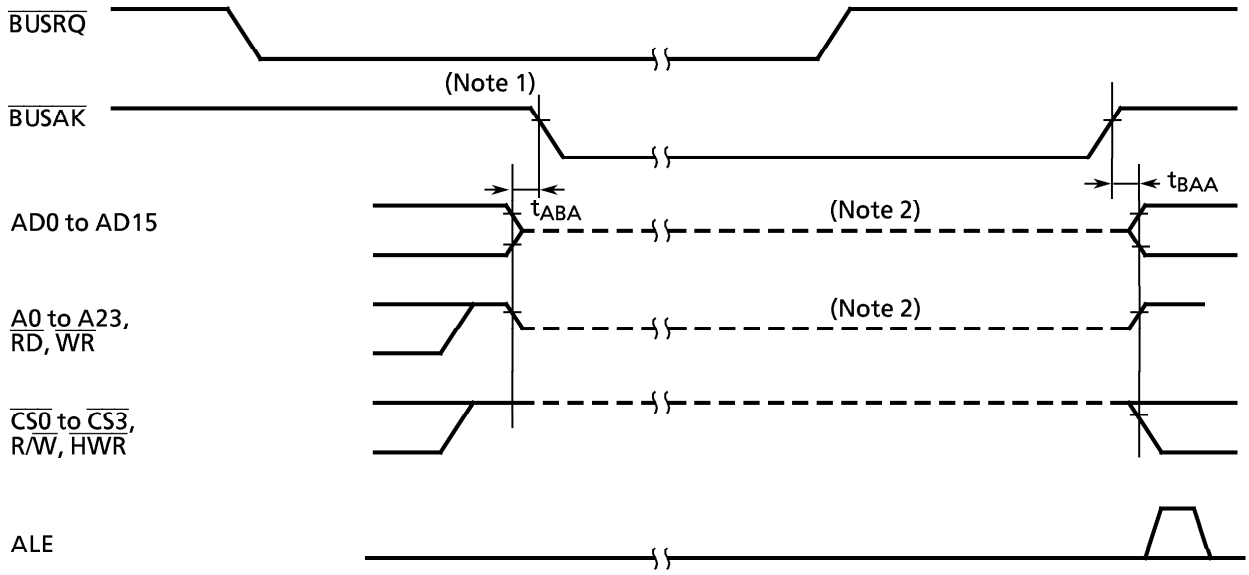
Note : T = Period of SCOUT

Measrement Condition

- Output Level : High 0.7 V_{CC} / Low 0.3 V_{CC}, CL = 10 pF



4.9 Bus Request / Bus Acknowledge



Symbol	Parameter	Variable		25 MHz		16 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t_{ABA}	Output Buffer off to $\overline{BUSAK}$ Low	0	80	0	80	0	80	ns
t_{BAA}	$\overline{BUSAK}$ High to Output Buffer on	0	80	0	80	0	80	ns

Note1 : Even if the $\overline{BUSRQ}$ signal goes low, the bus will not be released while the $\overline{WAIT}$ signal is low. The bus will only be released when $\overline{BUSRQ}$ goes low while $\overline{WAIT}$ is high.

Note2 : This line shows only that the output buffer is in the off state.
It does not indicate that the signal level is fixed.
Just after the bus is released, the signal level set before the bus was released is maintained dynamically by the external capacitance. Therefor, to fix the signal level using an external resistor during bus release, careful design is necessary, as fixing of the level is delayed.
The internal programmable pull-up/pull-down resistor is switched between the active and non-active states by the internal signal.

4.10 Recommended Oscillation Circuit

The TMP91CW12F/TMP91PW12F have been evaluated by the following resonator manufacturer. The evaluation results are shown below for your information.

Note: The load capacitance of the oscillation terminal is the sum of the load capacitances of C1 and C2 to be connected and the stray capacitance on the board. Even if the ratings of C1 and C2 are used, the load capacitance varies with each board and the oscillator may malfunction. Therefore, when designing a board, make the pattern around the oscillation circuit shortest. It is recommended that final evaluation of the resonator be performed on the board.

(1) Examples of resonator connection

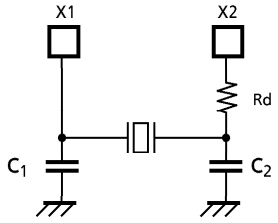


Figure 1 High-frequency Oscillator Connection

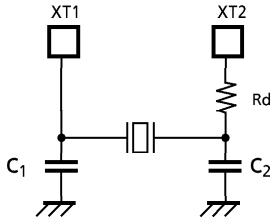


Figure 2 Low-frequency Oscillator Connection

(2) Recommended ceramic resonators for the TMP91CW12F/PW12F: Murata Manufacturing Co., Ltd.

Item	Oscillation frequency	Recommended resonator	Recommended rating			VCC[V]	Remarks
			C1[pF]	C2[pF]	Rd[kΩ]		
High-frequency Oscillator	2.0	CSA2.00MG	30	30	0	2.7 to 3.3	–
		CST2.00MG	(30)	(30)			
	4.0	CSA4.00MG	30	30		2.7 to 5.5	
		CST4.00MGW	(30)	(30)			
	10.0	CSA10.0MTZ	30	30		4.5 to 5.5	
		CST10.0MTW	(30)	(30)			
		CSA10.0MTZ	30	30		2.7 to 3.3	TMP91CW12F Only
		CST10.0MTW	(30)	(30)			
		CSA10.0MTZ093	30	30		2.7 to 3.3	TMP91PW12F Only
		CST10.0MTW093	(30)	(30)			
	12.5	CSA12.5MTZ	30	30		4.5 to 5.5	–
		CST12.5MTW	(30)	(30)			
		CSA12.5MTZ	30	30		2.7 to 3.3	TMP91CW12F Only
		CST12.5MTW	(30)	(30)			
		CSA12.5MTZ093	30	30		2.7 to 3.3	TMP91PW12F Only
		CST12.5MTW093	(30)	(30)			
	16.0	CSA16.00MXZ040	5	5		4.5 to 5.5	–
		CST16.00MXW0C1	(5)	(5)			
		CSA16.00MXZ040	Open	Open		2.7 to 3.3	TMP91CW12F Only
		CSA16.00MXZ046	Open	Open		2.7 to 3.3	TMP91PW12F Only
	20.0	CSA20.00MXZ040	3	3		4.5 to 5.5	–
	25.0	CSA25.00MXZ040	Open	Open			

- The values enclosed in brackets in the C1 and C2 columns apply to the condenser built-in type.
- MURATA MFG. CO., LTD. (JAPAN)
  The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change. For up-to-date information, please refer to the following URL;

  http://www.murata.co.jp/search/index.html