# International Rectifier

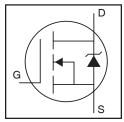
#### **AUTOMOTIVE GRADE**

## AUIRF1324S AUIRF1324L

HEXFET® Power MOSFET

### Features

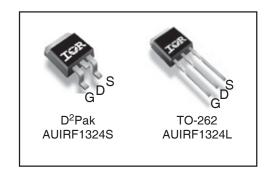
- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dV/dT Rating
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free, RoHS Compliant
- Automotive Qualified \*



V <sub>DSS</sub>	24V
R <sub>DS(on)</sub> typ.	1.3m $\Omega$
I <sub>D (Silicon Limited)</sub>	340A①
I <sub>D (Package Limited)</sub>	195A

### Description Specifically des

Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating . These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.



G	D	S
Gate	Drain	Source

#### **Absolute Maximum Ratings**

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature  $(T_A)$  is 25°C, unless otherwise specified.

Symbol	Parameter	Max.	Units
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, VGS @ 10V (Silicon Limited)	340	
I <sub>D</sub> @ T <sub>C</sub> = 100°C	Continuous Drain Current, V <sub>GS</sub> @ 10V (Silicon Limited)	240	┐ ,
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V (Package Limited)	195	A
I <sub>DM</sub>	Pulsed Drain Current ②	1420	
P <sub>D</sub> @T <sub>C</sub> = 25°C	Maximum Power Dissipation	300	W
	Linear Derating Factor	2.0	W/°C
$V_{GS}$	Gate-to-Source Voltage	± 20	V
E <sub>AS</sub>	Single Pulse Avalanche Energy (Thermally Limited) 3	270	mJ
I <sub>AR</sub>	Avalanche Current ②	See Fig. 14, 15, 22a, 22b	Α
E <sub>AR</sub>	Repetitive Avalanche Energy ②		mJ
dv/dt	Peak Diode Recovery @	0.46	V/ns
T <sub>J</sub>	Operating Junction and	-55 to + 175	
T <sub>STG</sub>	Storage Temperature Range		_l ∘c
	Soldering Temperature, for 10 seconds	300	
	(1.6mm from case)		

#### **Thermal Resistance**

Symbol	Parameter	Тур.	Max.	Units
$R_{\theta JC}$	Junction-to-Case 9		0.50	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mounted, steady-state) ®		40	

HEXFET® is a registered trademark of International Rectifier.

<sup>\*</sup>Qualification standards can be found at http://www.irf.com/



#### Static Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Тур.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	24			٧	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_{J}$	Breakdown Voltage Temp. Coefficient		22		mV/°C	Reference to 25°C, I <sub>D</sub> = 5.0mA <sup>②</sup>
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance		1.3	1.65	mΩ	$V_{GS} = 10V, I_D = 195A $ ⑤
$V_{GS(th)}$	Gate Threshold Voltage	2.0		4.0	٧	$V_{DS} = V_{GS}$ , $I_D = 250\mu A$
gfs	Forward Transconductance	180			S	$V_{DS} = 10V, I_{D} = 195A$
$R_{G}$	Internal Gate Resistance		2.3		Ω	
I <sub>DSS</sub>	Drain-to-Source Leakage Current		_	20	μΑ	$V_{DS} = 24V$ , $V_{GS} = 0V$
			_	250		$V_{DS} = 24V, V_{GS} = 0V, T_{J} = 125^{\circ}C$
I <sub>GSS</sub>	Gate-to-Source Forward Leakage			200	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage			-200		V <sub>GS</sub> = -20V

### Dynamic Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Тур.	Max.	Units	Conditions
$Q_g$	Total Gate Charge		160	240	nC	I <sub>D</sub> = 195A
$Q_{gs}$	Gate-to-Source Charge		84			$V_{DS} = 12V$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge		49			V <sub>GS</sub> = 10V ⑤
Q <sub>sync</sub>	Total Gate Charge Sync. (Q <sub>g</sub> - Q <sub>gd</sub> )		76	_		$I_D = 195A, V_{DS} = 0V, V_{GS} = 10V$
$t_{d(on)}$	Turn-On Delay Time		17		ns	$V_{DD} = 16V$
t <sub>r</sub>	Rise Time		190			I <sub>D</sub> = 195A
$t_{d(off)}$	Turn-Off Delay Time		83			$R_G = 2.7\Omega$
t <sub>f</sub>	Fall Time		120			V <sub>GS</sub> = 10V ⑤
C <sub>iss</sub>	Input Capacitance		7590		pF	$V_{GS} = 0V$
C <sub>oss</sub>	Output Capacitance		3440			$V_{DS} = 24V$
C <sub>rss</sub>	Reverse Transfer Capacitance		1960	_		f = 1.0  MHz,  See Fig. 5
C <sub>oss</sub> eff. (ER)	Effective Output Capacitance (Energy Related)		4700			$V_{GS} = 0V$ , $V_{DS} = 0V$ to 19V $\odot$ , See Fig. 11
C <sub>oss</sub> eff. (TR)	Effective Output Capacitance (Time Related)		4490			$V_{GS} = 0V, V_{DS} = 0V \text{ to } 19V $

#### **Diode Characteristics**

Symbol	Parameter	Min.	Тур.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current			350 <sup>①</sup>	Α	MOSFET symbol
	(Body Diode)					showing the
I <sub>SM</sub>	Pulsed Source Current			1420	Α	integral reverse
	(Body Diode) ②					p-n junction diode.
$V_{SD}$	Diode Forward Voltage			1.3	V	$T_J = 25^{\circ}C, I_S = 195A, V_{GS} = 0V $ ⑤
t <sub>rr</sub>	Reverse Recovery Time		46		ns	$T_J = 25^{\circ}C$ $V_R = 20V$ ,
			71			$T_J = 125^{\circ}C$ $I_F = 195A$
Q <sub>rr</sub>	Reverse Recovery Charge		160	_	nC	$T_J = 25^{\circ}C$ di/dt = 100A/ $\mu$ s $\odot$
			430			$T_J = 125$ °C
I <sub>RRM</sub>	Reverse Recovery Current		7.7		Α	$T_J = 25^{\circ}C$
t <sub>on</sub>	Forward Turn-On Time	Intrins	ic turn-	on time	is negl	ligible (turn-on is dominated by LS+LD)

#### Notes:

- ① Calculated continuous current based on maximum allowable junction ④  $I_{SD} \le 195A$ ,  $di/dt \le 450A/\mu s$ ,  $V_{DD} \le V_{(BR)DSS}$ ,  $T_{J} \le 175^{\circ}C$ . temperature. Bond wire current limit is 195A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements. (Refer to AN-1140).
- ② Repetitive rating; pulse width limited by max. junction temperature.
- $R_G = 25\Omega$ ,  $I_{AS} = 195A$ ,  $V_{GS} = 10V$ . Part not recommended for use above this value.
- ⑤ Pulse width  $\leq 400 \mu s$ ; duty cycle  $\leq 2\%$ .
- © Coss eff. (TR) is a fixed capacitance that gives the same charging time as  $C_{\text{oss}}$  while  $V_{\text{DS}}$  is rising from 0 to 80%  $V_{\text{DSS}}.$
- $\ensuremath{\mathfrak{D}}$  Coss eff. (ER) is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ® When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- $\mathfrak{G}$   $R_{\theta}$  is measured at  $T_J$  approximately 90°C.

### Qualification Information<sup>†</sup>

		Automotive			
		(per AEC-Q101) <sup>††</sup>			
Qualification Level  Comments: This part number(s) passed Automotive qualification level is greatension of the higher Automotive level.			al and Consumer qualification level is granted by		
Moisture Sensitivity Level		D2Pak MSL1			
		TO-262 N/A			
	Machine Model	Class M4			
		AEC-Q101-002			
505	Human Body Model	Class H3A			
ESD	ESD		AEC-Q101-001		
Charged Device Model		Class C5			
		AEC-Q101-005			
RoHS Compl	iant		Yes		

<sup>†</sup> Qualification standards can be found at International Rectifier's web site: http://www.irf.com/

<sup>††</sup> Exceptions to AEC-Q101 requirements are noted in the qualification report.

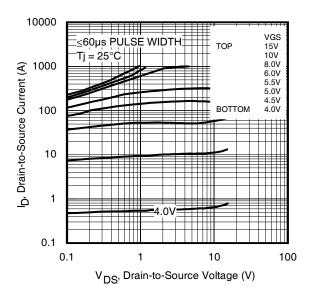


Fig 1. Typical Output Characteristics

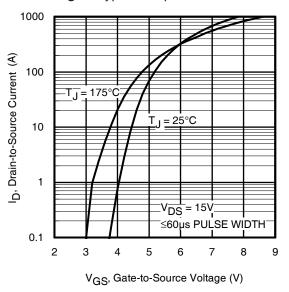
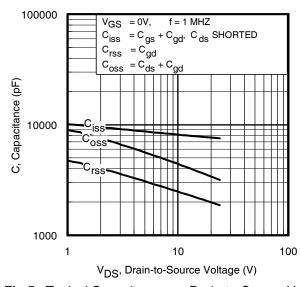


Fig 3. Typical Transfer Characteristics



**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage 4

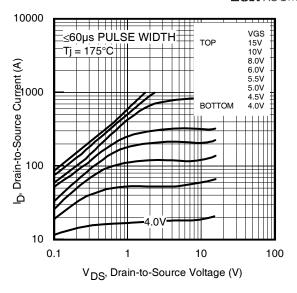


Fig 2. Typical Output Characteristics

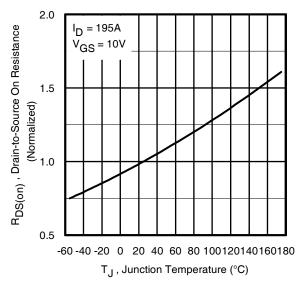
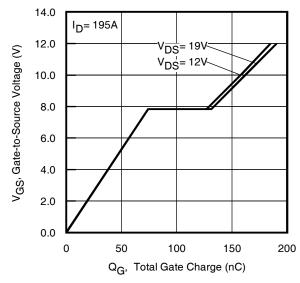


Fig 4. Normalized On-Resistance vs. Temperature



**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage www.irf.com

International AUIRF1324S/L

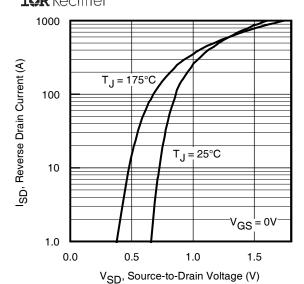
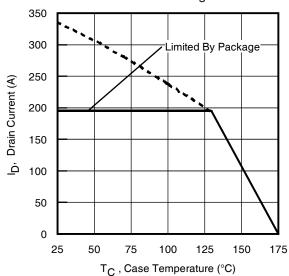
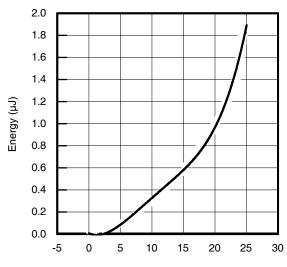


Fig 7. Typical Source-Drain Diode Forward Voltage



**Fig 9.** Maximum Drain Current vs. Case Temperature



 $\label{eq:VDS} $V_{DS}$, Drain-to-Source Voltage (V) $$ Fig 11. Typical $C_{OSS}$ Stored Energy $$ www.irf.com$ 

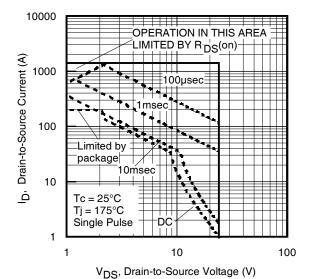


Fig 8. Maximum Safe Operating Area

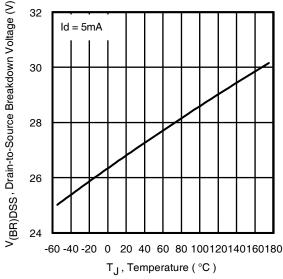


Fig 10. Drain-to-Source Breakdown Voltage

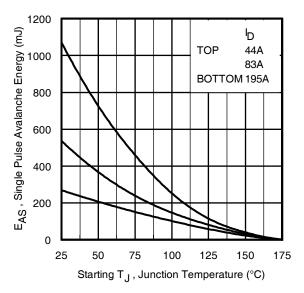


Fig 12. Maximum Avalanche Energy vs. DrainCurrent

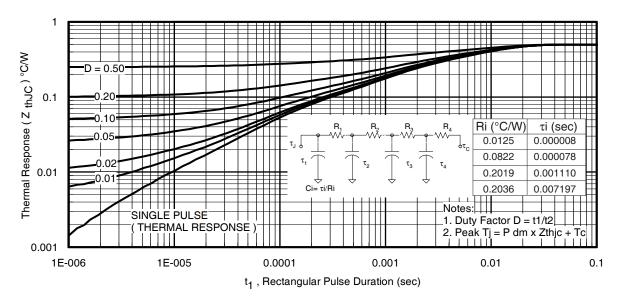


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

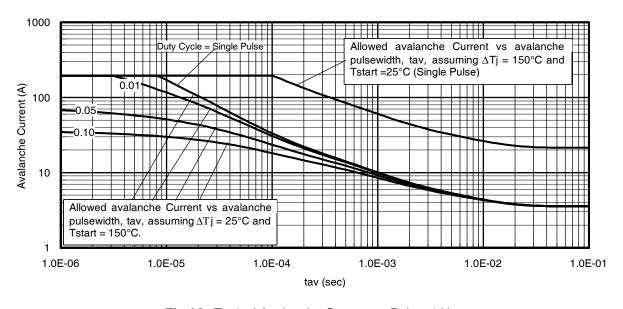


Fig 14. Typical Avalanche Current vs. Pulsewidth

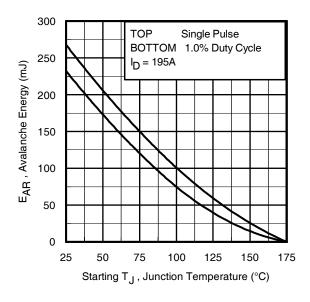


Fig 15. Maximum Avalanche Energy vs. Temperature

### Notes on Repetitive Avalanche Curves, Figures 14, 15: (For further info, see AN-1005 at www.irf.com)

- 1. Avalanche failures assumption:
- Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{imax}$ . This is validated for every part type.
- 2. Safe operation in Avalanche is allowed as long asT<sub>imax</sub> is not exceeded.
- 3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
- 4.  $P_{D (ave)}$  = Average power dissipation per single avalanche pulse.
- BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
- 6. I<sub>av</sub> = Allowable avalanche current.
- 7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 14, 15).

 $t_{av}$  = Average time in avalanche.

 $D = Duty cycle in avalanche = t_{av} \cdot f$ 

 $Z_{th,JC}(D, t_{av})$  = Transient thermal resistance, see Figures 13)

$$\begin{split} P_{D \; (ave)} &= 1/2 \; (\; 1.3 \cdot BV \cdot I_{av}) = \triangle T / \; Z_{thJC} \\ I_{av} &= 2\triangle T / \; [1.3 \cdot BV \cdot Z_{th}] \\ E_{AS \; (AR)} &= P_{D \; (ave)} \cdot t_{av} \end{split}$$

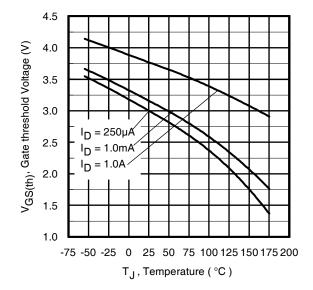


Fig 16. Threshold Voltage vs. Temperature

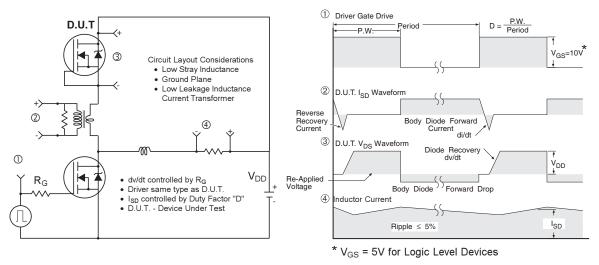


Fig 21. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

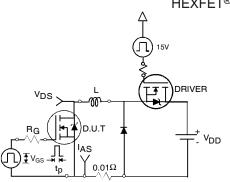


Fig 22a. Unclamped Inductive Test Circuit

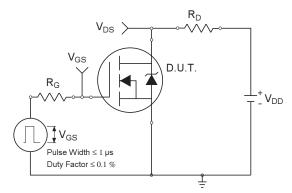


Fig 23a. Switching Time Test Circuit

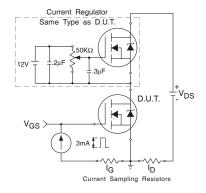


Fig 24a. Gate Charge Test Circuit

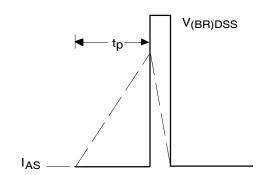


Fig 22b. Unclamped Inductive Waveforms

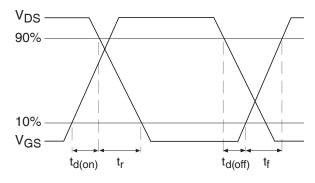


Fig 23b. Switching Time Waveforms

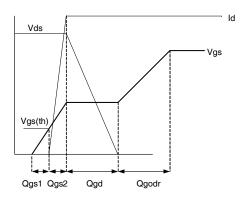
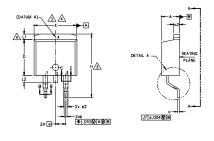


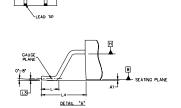
Fig 24b. Gate Charge Waveform

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### D<sup>2</sup>Pak (TO-263AB) Package Outline

Dimensions are shown in millimeters (inches)



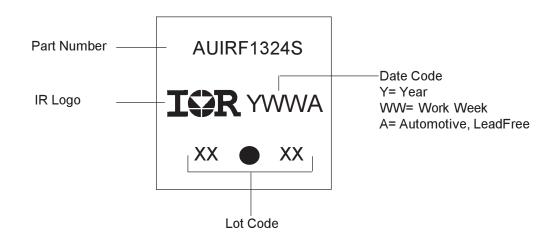


SCALE	8:1	
(E)	PLATING  BASE METAL  (c)  (c)  (b, b2)  SCRITCH IS-1 & C-G  SCALE: HONE	LEAD ASSIGNMENTS DIODES 1.— ANODE (T 2. 4.— CATHODE 3.— ANODE HEXTEI 1.— GATE 2. 4.— DRAIN 3.— SOURCE

M B O L	DIMENSIONS				
B	MILLIM	ETERS	INC	HES	O T E S
L	MIN.	MAX.	MIN.	MAX.	S
Α	4.06	4.83	.160	.190	
A1	0.00	0.254	.000	.010	
ь	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1,14	1.78	.045	.070	
ь3	1,14	1.73	.045	.068	5
С	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1,14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	-	.270		4
E	9.65	10.67	.380	.420	3,4
E1	6.22	-	.245		4
e	2.54	BSC	.100	BSC	
Н	14.61	15.88	.575	.625	
L	1,78	2.79	.070	.110	
L1	-	1.65	-	.066	4
L2	-	1.78	-	.070	
L3	0.25	BSC	.010	BSC	
L4	4.78	5.28	.188	.208	

- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
- 2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- \(\frac{\begin{small}
  \sigma\) DIMENSION D & E DO NOT INCLUDE MOLD FLASH, MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE, THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
- 1 THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
- 5. DIMENSION 61 AND c1 APPLY TO BASE METAL ONLY.
- 6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
- 7. CONTROLLING DIMENSION: INCH.
- 8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.

### D<sup>2</sup>Pak (TO-263AB) Part Marking Information



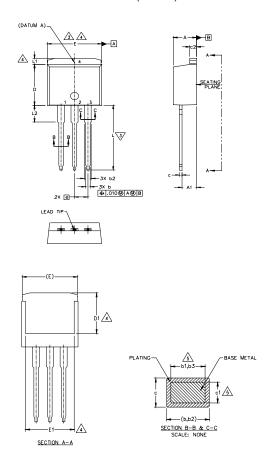
1.- Anode (TWO DIE) / OPEN (ONE DIE) 4.- CATHODE 3.- ANODE

IGBTs, CoPACK

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

#### TO-262 Package Outline

Dimensions are shown in millimeters (inches)



S Y M			Z		
M B O L	MILLIM	ETERS	INC	HES	ZOTES
L	MIN.	MAX.	MIN.	MAX.	S
Α	4.06	4.83	.160	.190	
A1	2.03	3.02	.080	.119	
ь	0.51	0.99	.020	.039	
ь1	0.51	0.89	.020	.035	5
ь2	1.14	1.78	.045	.070	
ь3	1.14	1.73	.045	.068	5
С	0.38	0.74	.015	.029	
с1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	_	.270	_	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	-	.245		4
е	2.54	BSC	.100	BSC	
∟	13.46	14.10	.530	.555	
<b>∟</b> 1	_	1.65	_	.065	4
L2	3.56	3.71	.140	.146	

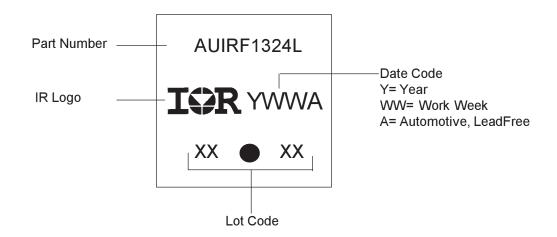
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OUTLINE CONFORM TO JEDEC TD-262 EXCEPT A1(max.), b(min.) AND D1(min.)
WHERE DIMENSIONS DERIVED THE ACTUAL PACKAGE OUTLINE.

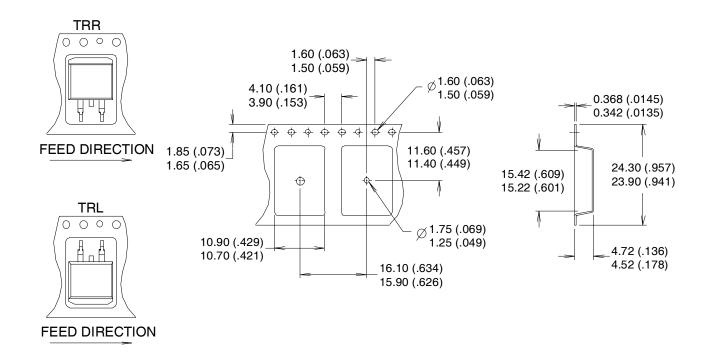
### TO-262 Part Marking Information

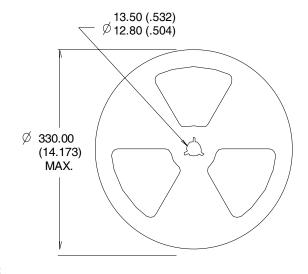


Note: For the most current drawing please refer to IR website at <a href="http://www.irf.com/package/">http://www.irf.com/package/</a>

### D<sup>2</sup>Pak (TO-263AB) Tape & Reel Information

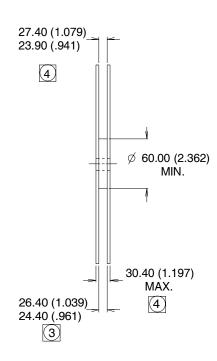
Dimensions are shown in millimeters (inches)







- 1. COMFORMS TO EIA-418.
- 2. CONTROLLING DIMENSION: MILLIMETER.
- 3 DIMENSION MEASURED @ HUB.
- 4 INCLUDES FLANGE DISTORTION @ OUTER EDGE.



### **Ordering Information**

Base part	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
AUIRF1324S	D2Pak	Tube	50	AUIRF1324S
		Tape and Reel Left	800	AUIRF1324STRL
		Tape and Reel Right	800	AUIRF1324STRR
AUIRF1324L	TO-262	Tube	50	AUIRF1324L



#### IMPORTANT NOTICE

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For technical support, please contact IR's Technical Assistance Center

http://www.irf.com/technical-info/

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